

LM49101 Boomer® Audio Power Amplifier Series Mono Class AB Audio Subsystem with a True Ground Headphone Amplifier and Earpiece Switch

Check for Samples: [LM49101](#), [LM49101TMEVAL](#)

FEATURES

- Differential Mono Input and Stereo Single-Ended Input
- Separate Earpiece (Receiver) Differential Input
- Analog Switch for a Separate Earpiece Path
- 32-Step Digital Volume Control (-80 to +18dB)
- Three Independent Volume Channels (Left, Right, Mono)
- Separate Headphone Volume Control
- Flexible Output for Speaker and Headphone Output
- True Ground Headphone Amplifier Eliminates Large DC Blocking Capacitors Reducing PCB Space and Cost
- Hardware Reset Function
- RF Immunity Topology
- “Click and Pop” Suppression Circuitry
- Thermal Shutdown Protection
- Micro-Power Shutdown
- I²C Control Interface
- Available in Space-Saving DSBGA Package

KEY SPECIFICATIONS

- Supply Voltage (V_{DDLS}): $2.7V \leq V_{DDLS} \leq 5.5V$
- Supply Voltage (V_{DDHP}): $1.8V \leq V_{DDHP} \leq 2.9V$
- I²C Supply Voltage: $1.7V \leq I^2CV_{DD} \leq 5.5V$
- Output Power, $V_{DDLS} = 5V$, $V_{DDHP} = 2.75V$, 1% THD+N
 - $R_L = 8\Omega$ Speaker 1.3W (Typ)
 - $R_L = 32\Omega$ Headphone 45mW (Typ)
- Output Power $V_{DDLS} = 3.3V$, $V_{DDHP} = 2.75V$, 1% THD+N
 - $R_L = 8\Omega$ Speaker 540W (Typ)
 - $R_L = 32\Omega$ Headphone 40mW (Typ)
- PSRR: $V_{DD} = 3.3V$, 217Hz Ripple, Mono In: 90dB (Typ)
- Shutdown Power Supply Current: 0.01µA (Typ)

APPLICATIONS

- Portable Electronic Devices
- Mobile Phones
- PDAs

DESCRIPTION

The LM49101 is a fully integrated audio subsystem with a mono power amplifier capable of delivering 540mW of continuous average power into an 8Ω BTL speaker load with 1% THD+N using a 3.3V supply. The LM49101 includes a separate stereo headphone amplifier that can deliver 44mW per channel into 32Ω loads using a 2.75V supply.

The LM49101 has four input channels. A pair of single-ended inputs and a fully differential input channel with volume control and amplification stages. Additionally, a bypass differential input is available that connects directly to the mono speaker outputs through an analog switch without any amplification or volume control stages. The LM49101 features a 32-step digital volume control on the input stage and an 8-step digital volume control on the headphone output stage.

The digital volume control and output modes, programmed through a two-wire I²C compatible interface, allows flexibility in routing and mixing audio channels.

The LM49101 is designed for cellular phones, PDAs, and other portable handheld applications. The high level of integration minimizes external components. The True Ground headphone amplifier eliminates the physically large DC blocking output capacitors reducing required board space and reducing cost.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Application

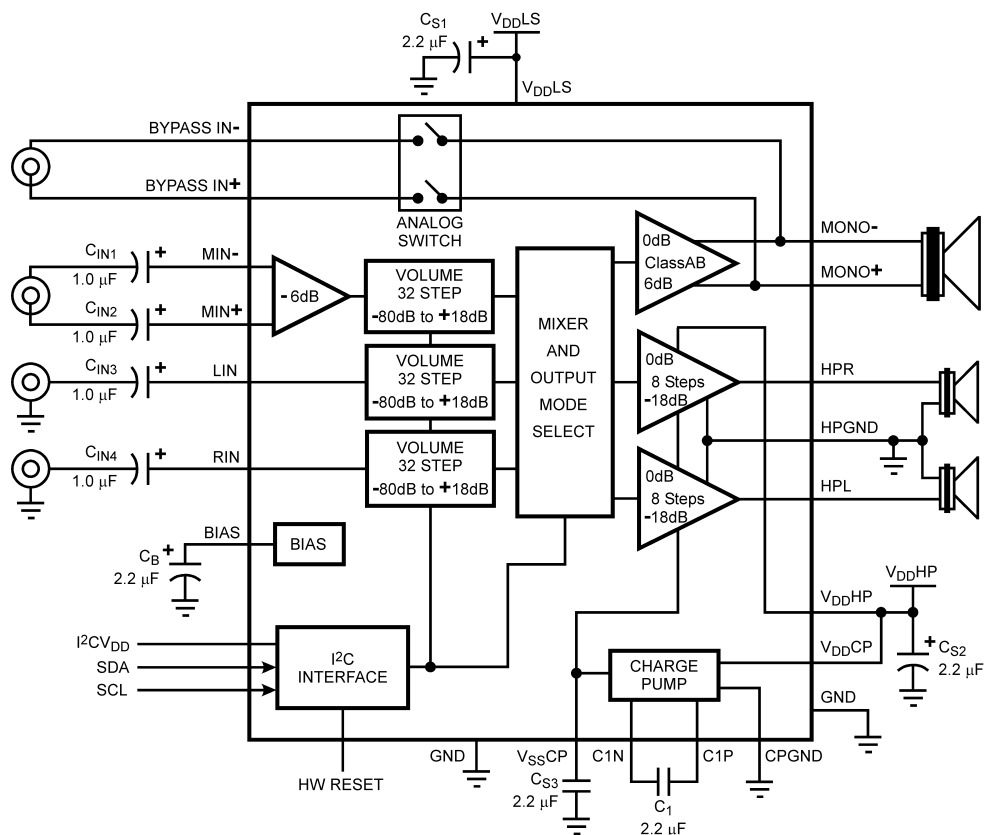


Figure 1. Typical Audio Application Circuit

Connection Diagram

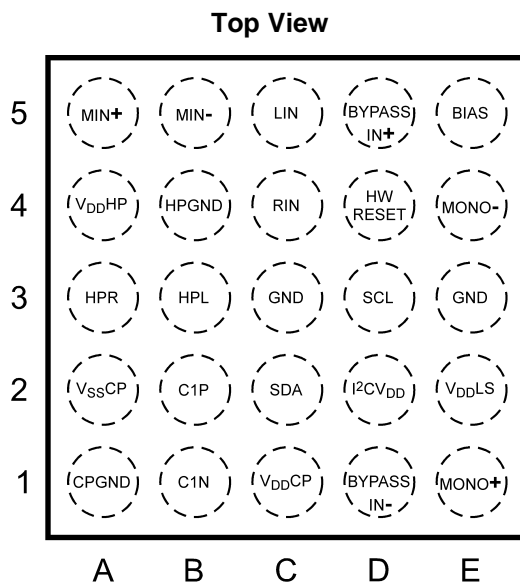


Figure 2. 25 Bump DSBGA Package
See Package Number YFQ0025BCA

Table 1. Bump Descriptions

Bump	Name	Pin Function	Type
A1	CPGND	Charge pump ground terminal	Ground
A2	V _{SS} CP	Negative charge pump power supply	Power Output
A3	HPR	Right headphone output	Analog Output
A4	V _{DD} HP	Headphone amplifier power supply	Power Input
A5	MIN+	Positive input pin for the mono, differential input	Analog Input
B1	C1N	Negative terminal of the charge pump flying capacitor	Analog Output
B2	C1P	Positive terminal of the charge pump flying capacitor	Analog Output
B3	HPL	Left headphone output	Analog Output
B4	HPGND	Headphone signal ground	Ground
B5	MIN-	Negative input pin for the mono, differential input	Analog Input
C1	V _{DD} CP	Charge pump power supply	Power Input
C2	SDA	I ² C data	Digital Input
C3	GND	Ground	Ground
C4	RIN	Single-ended input for the right channel	Analog Input
C5	LIN	Single-ended input for the left channel	Analog Input
D1	BYPASS_IN-	Earpiece negative input, bypass volume control and amplifier	Analog Input
D2	I ² CV _{DD}	I ² C power supply	Power Input
D3	SCL	I ² C clock	Digital Input
D4	HW RESET	Hardware reset function, active low. When pin is low (<0.6V) the LM49101 goes into shutdown mode and will remain in shutdown mode until pin goes to logic high (>1.6V) and is activated by I ² C control. When reset all registers are set to the default value of 0.	Digital Input
D5	BYPASS_IN+	Earpiece positive input, bypass volume control and amplifier	Analog Input
E1	MONO+	Positive loudspeaker output	Analog Output
E2	V _{DD} LS	Main power supply	Power Input
E3	GND	Ground	Ground
E4	MONO-	Negative loudspeaker output	Analog Output
E5	BIAS	Half-supply bias, capacitor bypassed	Analog Output



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

Supply Voltage (Loudspeaker, V_{DDLS})		6.0V
Supply Voltage (Headphone, V_{DDHP})		3.0V
Storage Temperature		-65°C to +150°C
Voltage at Any Input Pin		GND – 0.3 to $V_{DDLS} + 0.3$
Power Dissipation ⁽⁵⁾		Internally Limited
ESD Rating ⁽⁶⁾		2000V
ESD Rating ⁽⁷⁾		200V
Junction Temperature (T_{JMAX})		150°C
Soldering Information	Vapor Phase (60sec.)	215°C
	Infrared (15sec.)	220°C
Thermal Resistance	θ_{JA} ⁽⁸⁾	51°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The Electrical Characteristics tables list specified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) See AN-1112 "Micro SMD Wafer Level Chip Scale Package" ().
- (4) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature, T_A . The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever.
- (6) Human body model, applicable std. JESD22-A114C.
- (7) Machine model, applicable std. JESD22-A115-A.
- (8) The given θ_{JA} is for an LM49101 mounted on a demonstration board.

Operating Ratings

Temperature Range ($T_{MIN} \leq T_A \leq T_{MAX}$)	$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$
Supply Voltage (V_{DDLS})	$2.7\text{V} \leq V_{DDLS} \leq 5.5\text{V}$
Supply Voltage (V_{DDHP})	$1.8\text{V} \leq V_{DDHP} \leq 2.9\text{V}$ $V_{DDHP} \leq V_{DDLS}$
Supply Voltage (V_{DDCP})	$V_{DDCP} = V_{DDHP}$
Supply Voltage (I^2CV_{DD})	$1.7\text{V} \leq I^2CV_{DD} \leq 5.5\text{V}$
	$I^2CV_{DD} \leq V_{DDLS}$

Electrical Characteristics $V_{DDLS} = 3.3V$, $V_{DDHP} = 2.75V^{(1)(2)}$

The following specifications apply for $V_{DDLS} = 3.3V$, $V_{DDHP} = 2.75V$, $T_A = 25^\circ C$, all volume controls set to 0dB, unless otherwise specified. LS = Loudspeaker, HP = Headphone, EP = Earpiece.

Parameter		Test Conditions	LM49101		Units (Limits)
			Typ ⁽³⁾	Limits ⁽⁴⁾	
I_{DD}	Quiescent Power Supply Current	$V_{IN} = 0$, No Load			
		EP Receiver (Output Mode Bit EP Bypass = 1)	0.03	0.045	mA (max)
		LS only (Mode 1), GAMP_SD = 0 VDDL VDDHP	2.5 0	4.2	mA (max) mA
		LS only (Mode 1), GAMP_SD = 1 VDDL VDDHP	2 0		mA mA
		HP only (Mode 8), GAMP_SD = 0 VDDL VDDHP VDDL + VDDHP	1.6 3.1	2.0 4.5 6.45	mA (max) mA (max) mA (max)
		HP only (Mode 8), GAMP_SD = 1 VDDL VDDHP	2.8 3.3		mA mA
		LS+HP (Mode 10), GAMP_SD = 0 VDDL VDDHP VDDL + VDDHP	2.8 3.1	3.8 4.5 8	mA (max) mA (max) mA (max)
I_{SD}	Shutdown Current	Power_On = 0	0.01	2	μA (max)
V_{OS}	Output Offset Voltage	$V_{IN} = 0V$, Mode 10 LS output, $R_L = 8\Omega$ BTL HP output, $R_L = 32\Omega$ SE	2.5 0.5	22 5	mV (max) mV (max)
P_O	Output Power	LS output, Mode 1, $R_L = 8\Omega$ BTL THD+N = 1%, $f = 1kHz$, LS_Gain = 6dB	540	480	mW (min)
		HP output, Mode 8, $R_L = 32\Omega$ SE THD+N = 1%, $f = 1kHz$	44	40	mW (min)
THD+N	Total Harmonic Distortion + Noise	LS output, $f = 1kHz$, $R_L = 8\Omega$ BTL $P_O = 250mW$, Mode 1, LS_Gain = 6dB	0.065		%
		HP output, $f = 1kHz$, $R_L = 32\Omega$ SE $P_O = 20mW$, Mode 8	0.015		%
SNR	Signal-to-Noise Ratio	LS output, $f = 1kHz$, Mode 1 $V_{REF} = V_{OUT}$ (1%THD+N) Vol. Gain & LS_GAIN = 0dB A-Wtg, LIN & RIN AC terminated	105		dB
		HP output, $f = 1kHz$, Mode 8 $V_{REF} = V_{OUT}$ (1%THD+N) Vol. Gain = 0dB, A-weighted LIN & RIN AC terminated	100		dB

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The Electrical Characteristics tables list specified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Typical values represent most likely parametric norms at $T_A = +25^\circ C$, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
- (4) Datasheet min/max specification limits are specified by test or statistical analysis.

Electrical Characteristics $V_{DDLS} = 3.3V$, $V_{DDHP} = 2.75V^{(1)(2)}$ (continued)

The following specifications apply for $V_{DDLS} = 3.3V$, $V_{DDHP} = 2.75V$, $T_A = 25^\circ C$, all volume controls set to 0dB, unless otherwise specified. LS = Loudspeaker, HP = Headphone, EP = Earpiece.

Parameter		Test Conditions	LM49101		Units (Limits)
			Typ ⁽³⁾	Limits ⁽⁴⁾	
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} on $V_{DDLS} = 200mV_{PP}$, $f_{RIPPLE} = 217Hz$, $C_B = 2.2\mu F$ All inputs AC terminated to GND, output referred			
		LS: Mode 1, 5, 9, 13, $R_L = 8\Omega$ BTL	90		dB (max)
		LS: Mode 2, 6, 10, 14, $R_L = 8\Omega$ BTL	75		dB (max)
		HP: Mode 4, 5, 6, 7, $R_L = 32\Omega$ SE	85		dB (max)
		HP: Mode 8, 9, 10, 11, $R_L = 32\Omega$ SE	81		dB (max)
CMRR	Common-Mode Rejection Ratio	$f = 217Hz$, $V_{CM} = 1V_{P-P}$ LS: $R_L = 8\Omega$ BTL, Mode 1 HP: $R_L = 32\Omega$ SE, Mode 4	60 60		dB dB
X_{TALK}	Crosstalk	HP $P_O = 20mW$ $f = 1kHz$, Mode 8	72		dB
Z_{IN}	MIN, LIN, and RIN Input Impedance	Maximum Gain setting	12.5	10 15	K Ω (min) K Ω (max)
		Maximum Attenuation setting	110	90 130	K Ω (min) K Ω (max)
R_{ON}	On Resistance	Analog Switch On	3.4		Ω
VOL	Digital Volume Control Range	Maximum Gain	18		dB
		Maximum Attenuation	–80		dB
VOL	Volume Control Step Size Error		± 0.02		dB
T_{WU}	Wake-Up Time from Shutdown	$C_B = 2.2\mu F$, HP, Normal Turn-On Mode	30		ms
		$C_B = 2.2\mu F$, HP, Fast Turn-On Mode	15		ms

Electrical Characteristics $V_{DDLS} = 5.0V$, $V_{DDHP} = 2.75V^{(1)(2)}$

The following specifications apply for $V_{DDLS} = 5.0V$, $V_{DDHP} = 2.75V$, $T_A = 25^\circ C$, all volume controls set to 0dB, unless otherwise specified. LS = Loudspeaker, HP = Headphone, EP = Earpiece.

Parameter		Test Conditions	LM49101		Units (Limits)
			Typ ⁽³⁾	Limits ⁽⁴⁾	
I_{DD}	Quiescent Power Supply Current	$V_{IN} = 0$, No Load			
		EP Receiver (Output Mode Bit EP Bypass = 1)	0.05	0.07	mA (max)
		LS only (Mode 1), GAMP_SD = 0 VDDL VDDHP	2.9 0	4.4	mA (max) mA
		LS only (Mode 1), GAMP_SD = 1 VDDL VDDHP	2.1 0		mA mA
		HP only (Mode 8), GAMP_SD = 0 VDDL VDDHP VDDL+VDDHP	1.8 3.1	2.15 4.5 6.6	mA (max) mA (max) mA (max)
		HP only (Mode 8), GAMP_SD = 1 VDDL VDDHP	1.3 3.1		mA mA
		LS+HP only (Mode 10), GAMP_SD = 0 VDDL VDDHP VDDL+VDDHP	3 3.1	4.1 4.5 8.35	mA (max) mA (max) mA (max)
I_{SD}	Shutdown Current	Power_On = 0	0.01	2	μA (max)
V_{OS}	Output Offset Voltage	$V_{IN} = 0V$, Mode 10 LS output, $R_L = 8\Omega$ BTL HP output, $R_L = 32\Omega$ SE	2.5 0.5	22 5	mV (max) mV (max)
P_O	Output Power	LS output, Mode 1, $R_L = 8\Omega$ BTL THD+N = 1%, $f = 1kHz$, LS_Gain = 6dB	1.3		W
		HP output, Mode 8, $R_L = 32\Omega$ SE THD+N = 1%, $f = 1kHz$	45		mW
THD+N	Total Harmonic Distortion + Noise	LS output, $f = 1kHz$, $R_L = 8\Omega$ BTL $P_O = 600mW$, Mode 1, LS_Gain = 6dB	0.055		%
		HP output, $f = 1kHz$, $R_L = 32\Omega$ SE $P_O = 20mW$, Mode 8	0.015		%
SNR	Signal-to-Noise Ratio	LS output, $f = 1kHz$, Mode 1 $V_{REF} = V_{OUT}$ (1%THD+N) Vol. Gain & LS_GAIN = 0dB A-Wtg, LIN & RIN AC terminated	108		dB
		HP output, $f = 1kHz$, Mode 8 $V_{REF} = V_{OUT}$ (1%THD+N) Vol. Gain = 0dB, A-weighted LIN & RIN AC terminated	100		dB

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The Electrical Characteristics tables list specified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Typical values represent most likely parametric norms at $T_A = +25^\circ C$, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
- (4) Datasheet min/max specification limits are specified by test or statistical analysis.

Electrical Characteristics $V_{DDLS} = 5.0V$, $V_{DDHP} = 2.75V^{(1)(2)}$ (continued)

The following specifications apply for $V_{DDLS} = 5.0V$, $V_{DDHP} = 2.75V$, $T_A = 25^\circ C$, all volume controls set to 0dB, unless otherwise specified. LS = Loudspeaker, HP = Headphone, EP = Earpiece.

Parameter		Test Conditions	LM49101		Units (Limits)
			Typ ⁽³⁾	Limits ⁽⁴⁾	
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} on $V_{DDLS} = 200mV_{PP}$, $f_{RIPPLE} = 217Hz$, $C_B = 2.2\mu F$ All inputs AC terminated to GND, output referred			
		LS: Mode 1, 5, 9, 13, $R_L = 8\Omega$ BTL	90		dB
		LS: Mode 2, 6, 10, 14, $R_L = 8\Omega$ BTL	74		dB
		HP: Mode 4, 5, 6, 7, $R_L = 32\Omega$ SE	84		dB
		HP: Mode 8, 9, 10, 11, $R_L = 32\Omega$ SE	79		dB
CMRR	Common-Mode Rejection Ratio	$f = 217Hz$, $V_{CM} = 1V_{P-P}$ LS: $R_L = 8\Omega$ BTL, Mode 1 HP: $R_L = 32\Omega$ SE, Mode 4	60 60		dB dB
X_{TALK}	Crosstalk	HP $P_O = 20mW$, $f = 1kHz$, Mode 8	72		dB
Z_{IN}	MIN, LIN, and RIN Input Impedance	Maximum Gain setting	12.5	10 15	K Ω (min) K Ω (max)
		Maximum Attenuation setting	110	90 130	K Ω (min) K Ω (max)
R_{ON}	On Resistance	Analog Switch On	2		Ω
VOL	Digital Volume Control Range	Maximum Gain	18		dB
		Maximum Attenuation	–80		dB
VOL	Volume Control Step Size Error		± 0.02		dB
T_{WU}	Wake-Up Time from Shutdown	$C_B = 2.2\mu F$, HP, Normal Turn-On Mode	30		ms
		$C_B = 2.2\mu F$, HP, Fast Turn-On Mode	15		ms

I²C Interface 2.2V ≤ I²C_V_{DD} ≤ 5.5V⁽¹⁾⁽²⁾

The following specifications apply for V_{DD}LS = 5.0V and 3.3V, 2.2V ≤ I²C_V_{DD} ≤ 5.5V, T_A = 25°C, unless otherwise specified.

Parameter		Test Conditions	LM49101		Units (Limits)
			Typ ⁽³⁾	Limits ⁽⁴⁾⁽⁵⁾	
t ₁	I ² C Clock Period			2.5	μs (min)
t ₂	I ² C Data Setup Time			100	ns (min)
t ₃	I ² C Data Stable Time			0	ns (min)
t ₄	Start Condition Time			100	ns (min)
t ₅	Stop Condition Time			100	ns (min)
t ₆	I ² C Data Hold Time			100	ns (min)
V _{IH}	I ² C Input Voltage High			0.7xI ² CV _{DD}	V (min)
V _{IL}	I ² C Input Voltage Low			0.3xI ² CV _{DD}	V (max)

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified
- (2) The Electrical Characteristics tables list specified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Human body model, applicable std. JESD22-A114C.
- (4) Datasheet min/max specification limits are specified by test or statistical analysis.
- (5) Refer to the I²C timing diagram, [Figure 39](#).

I²C Interface 1.7V ≤ I²C_V_{DD} ≤ 2.2V⁽¹⁾⁽²⁾

The following specifications apply for V_{DD}LS = 5.0V and 3.3V, T_A = 25°C, 1.7V ≤ I²C_V_{DD} ≤ 2.2V, unless otherwise specified.

Parameter		Test Conditions	LM49101		Units (Limits)
			Typ ⁽³⁾	Limits ⁽⁴⁾⁽⁵⁾	
t ₁	I ² C Clock Period			2.5	μs (min)
t ₂	I ² C Data Setup Time			250	ns (min)
t ₃	I ² C Data Stable Time			0	ns (min)
t ₄	Start Condition Time			250	ns (min)
t ₅	Stop Condition Time			250	ns (min)
t ₆	I ² C Data Hold Time			250	ns (min)
V _{IH}	I ² C Input Voltage High			0.7xI ² CV _{DD}	V (min)
V _{IL}	I ² C Input Voltage Low			0.3xI ² CV _{DD}	V (max)

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified
- (2) The Electrical Characteristics tables list specified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Typical values represent most likely parametric norms at T_A = +25°C, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
- (4) Datasheet min/max specification limits are specified by test or statistical analysis.
- (5) Refer to the I²C timing diagram, [Figure 39](#).

Typical Performance Characteristics

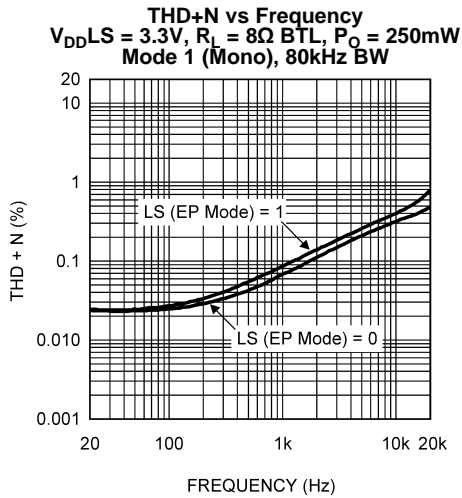


Figure 3.

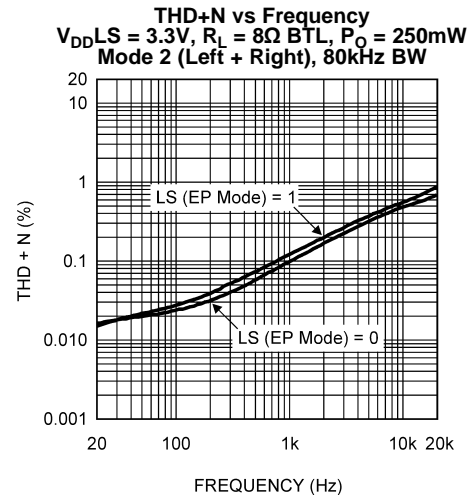


Figure 4.

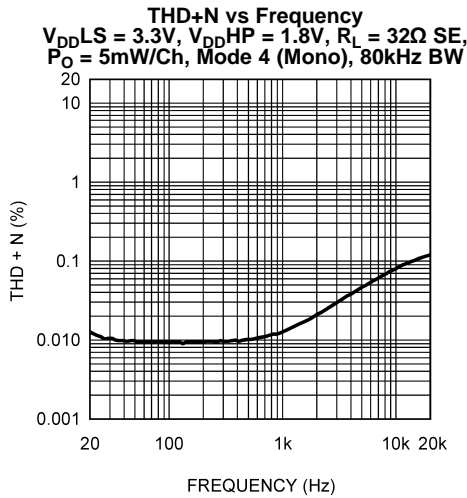


Figure 5.

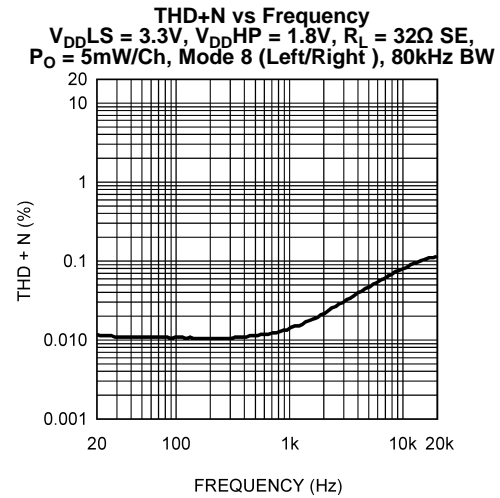


Figure 6.

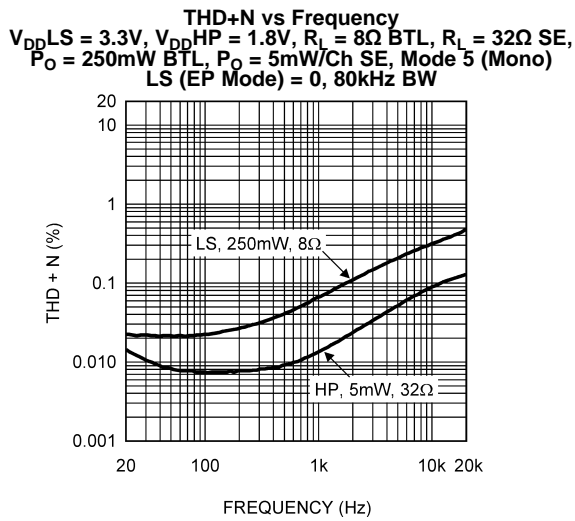


Figure 7.

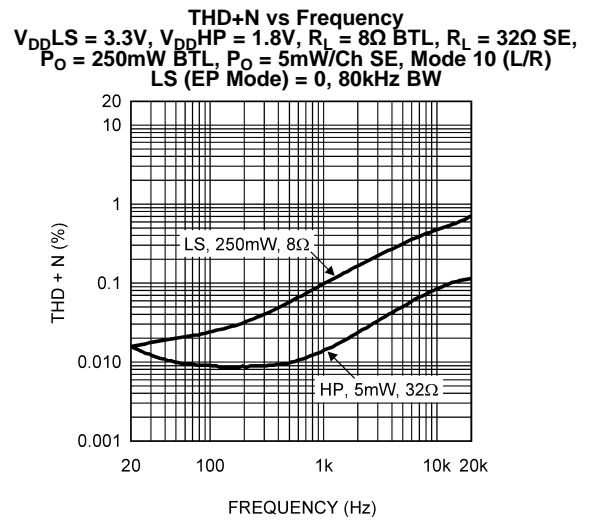


Figure 8.

Typical Performance Characteristics (continued)

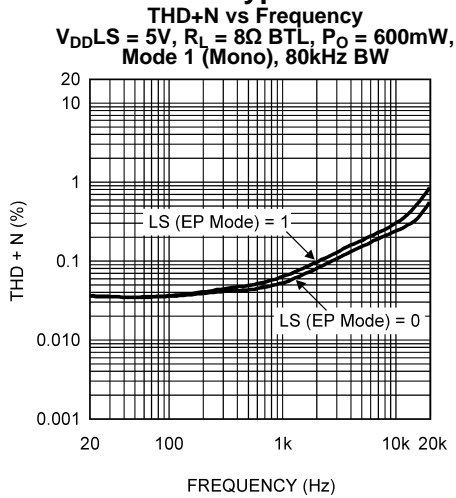


Figure 9.

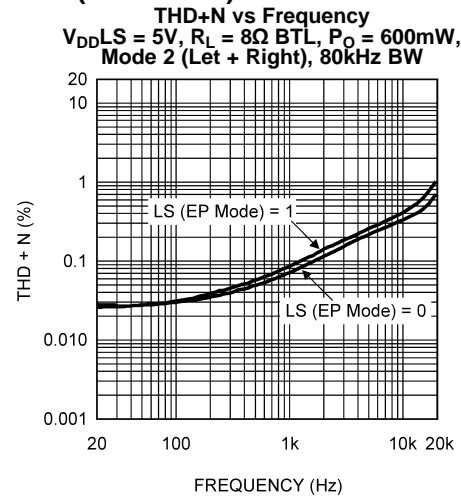


Figure 10.

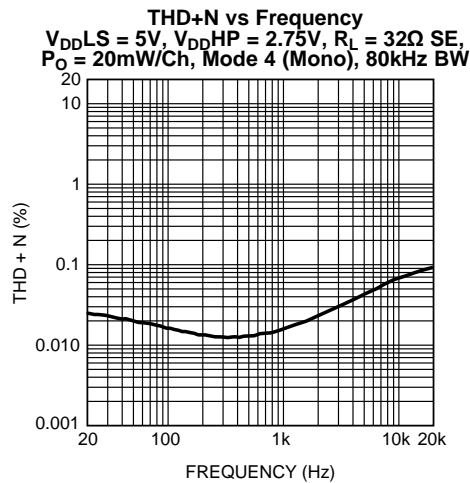


Figure 11.

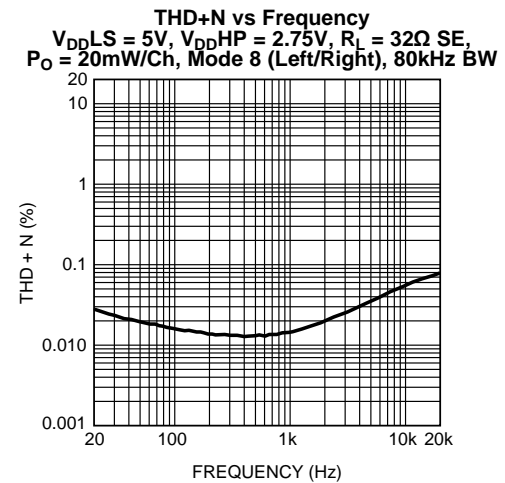


Figure 12.

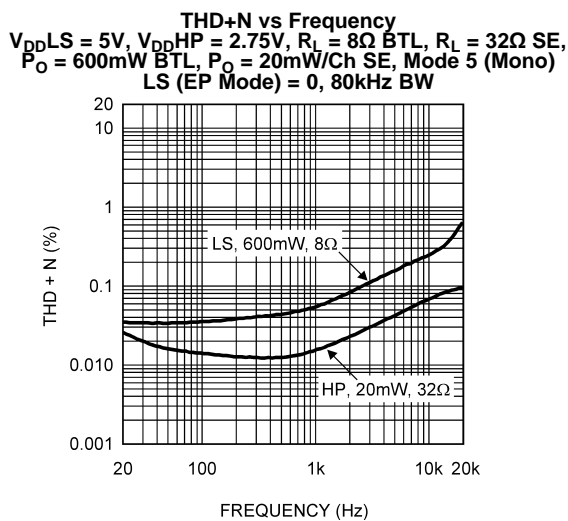


Figure 13.

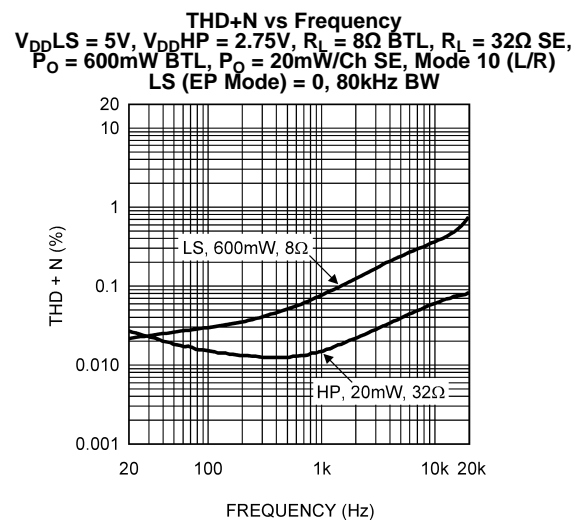


Figure 14.

Typical Performance Characteristics (continued)

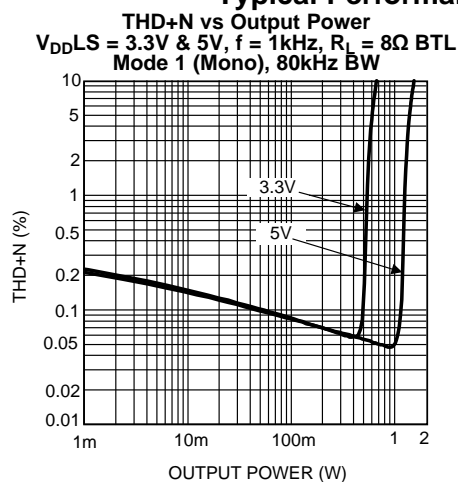


Figure 15.

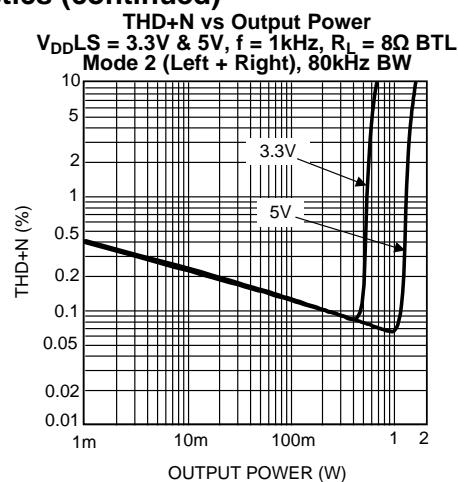


Figure 16.

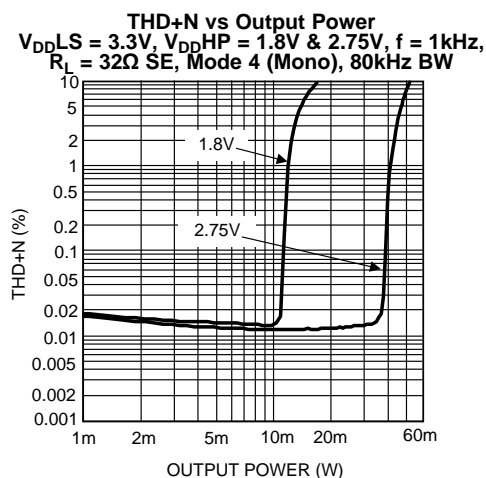


Figure 17.

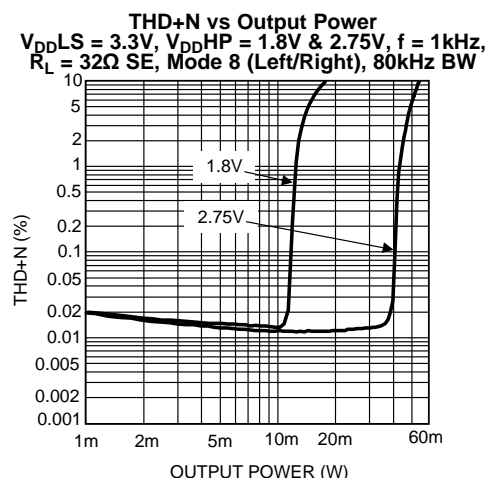


Figure 18.

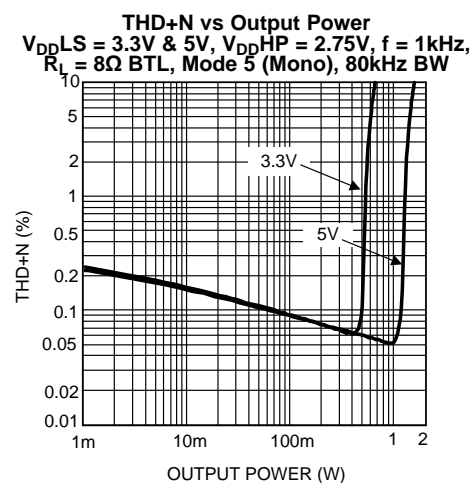


Figure 19.

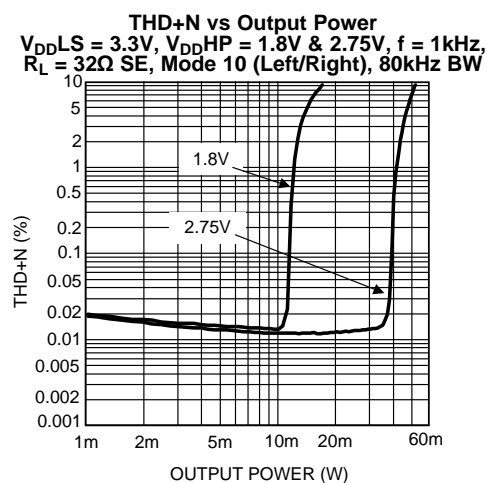


Figure 20.

Typical Performance Characteristics (continued)

PSRR vs Frequency
 $V_{DDLS} = 3.3V$, $V_{RIPPLELS} = 200mV_{PP}$, $R_L = 8\Omega$ BTL,
Mode 1 (Mono), 80kHz BW

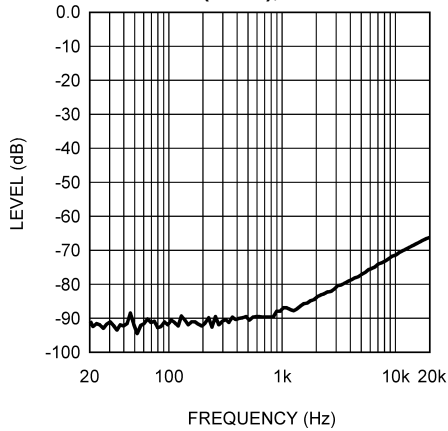


Figure 21.

PSRR vs Frequency
 $V_{DDLS} = 3.3V$, $V_{RIPPLELS} = 200mV_{PP}$, $R_L = 8\Omega$ BTL,
Mode 2 (Left + Right), 80kHz BW

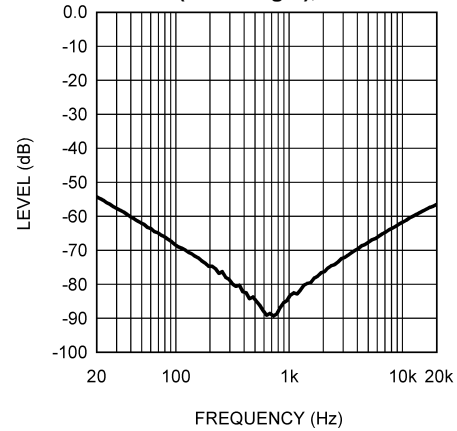


Figure 22.

PSRR vs Frequency
 $V_{DDLS} = 5V$, $V_{RIPPLELS} = 200mV_{PP}$, $R_L = 8\Omega$ BTL,
Mode 1 (Mono), 80kHz BW

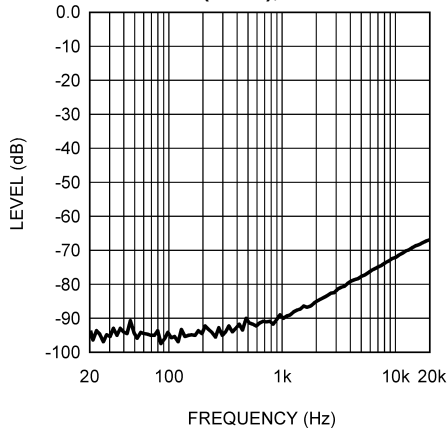


Figure 23.

PSRR vs Frequency
 $V_{DDLS} = 5V$, $V_{RIPPLELS} = 200mV_{PP}$, $R_L = 8\Omega$ BTL,
Mode 2 (Left + Right), 80kHz BW

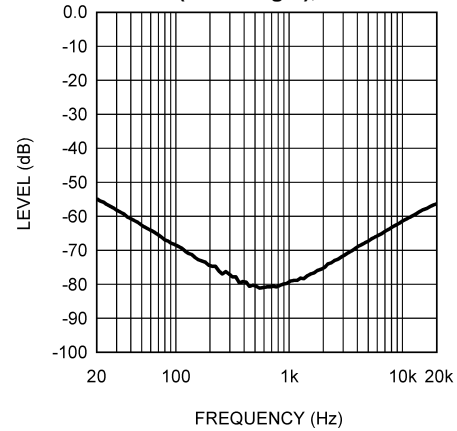


Figure 24.

PSRR vs Frequency
 $V_{DDLS} = 3.3V$, $V_{DDHP} = 1.8V$, $V_{RIPPLEHP} = 200mV_{PP}$,
 $R_L = 32\Omega$ SE, Mode 4 (Mono), 80kHz BW

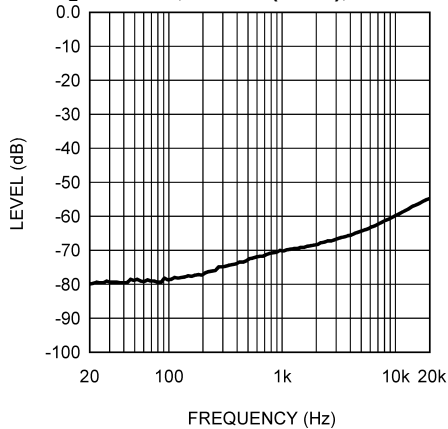


Figure 25.

PSRR vs Frequency
 $V_{DDLS} = 3.3V$, $V_{DDHP} = 1.8V$, $V_{RIPPLEHP} = 200mV_{PP}$,
 $R_L = 32\Omega$ SE, Mode 8 (Left/Right), 80kHz BW

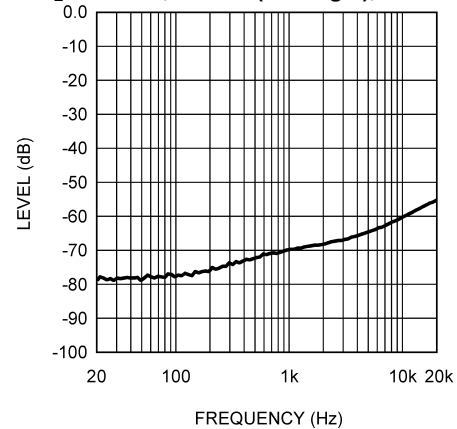


Figure 26.

Typical Performance Characteristics (continued)

PSRR vs Frequency
 $V_{DDLS} = 3.3V$, $V_{DDHP} = 2.75V$, $V_{RIPPLEHP} = 200mV_{PP}$,
 $R_L = 32\Omega$ SE, Mode 4 (Mono), 80kHz BW

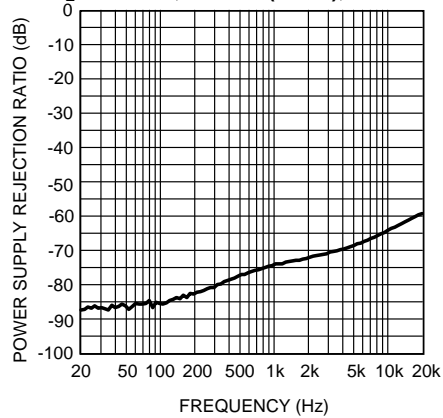


Figure 27.

PSRR vs Frequency
 $V_{DDLS} = 3.3V$, $V_{DDHP} = 2.75V$, $V_{RIPPLEHP} = 200mV_{PP}$,
 $R_L = 32\Omega$ SE, Mode 8 (Left/Right), 80kHz BW

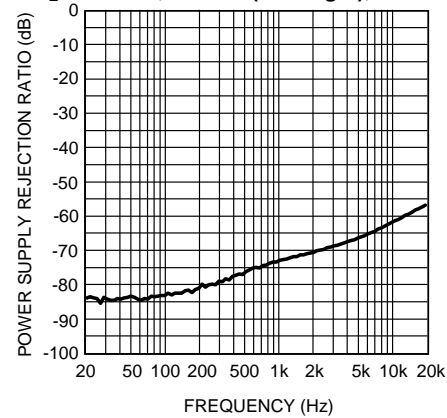


Figure 28.

Power Dissipation vs Output Power
 $V_{DDLS} = 3.3V$ & $5V$, $V_{DDHP} = 2.75V$, $R_L = 8\Omega$ BTL,
Mode 3 (Mono + Left + Right), 80kHz BW

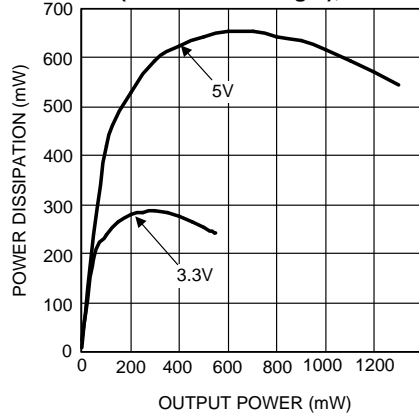


Figure 29.

Power Dissipation vs Output Power
 $V_{DDLS} = 5V$, $V_{DDHP} = 1.8V$ & $2.75V$, $R_L = 32\Omega$ SE,
Mode 12 (Mono + Left/ Right), 80kHz BW

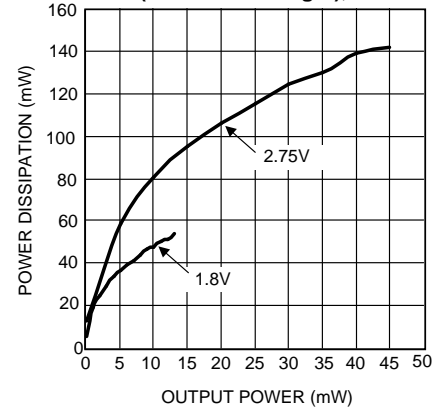


Figure 30.

Crosstalk vs Frequency
 $V_{DDLS} = 3.3V$, $V_{DDHP} = 1.8V$, $V_{IN} = 1V_{PP}$,
 $R_L = 32\Omega$ SE, Mode 8 (Left/Right), 80kHz BW

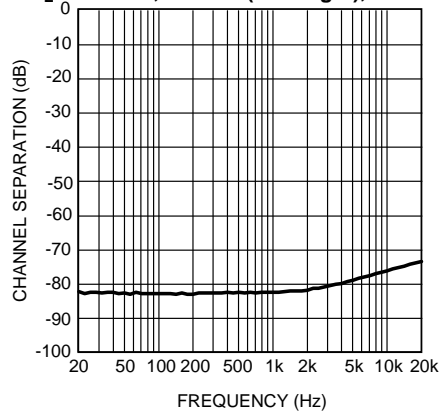


Figure 31.

Crosstalk vs Frequency
 $V_{DDLS} = 3.3V$, $V_{DDHP} = 2.75V$, $V_{IN} = 1V_{PP}$,
 $R_L = 32\Omega$ SE, Mode 8 (Left/Right), 80kHz BW

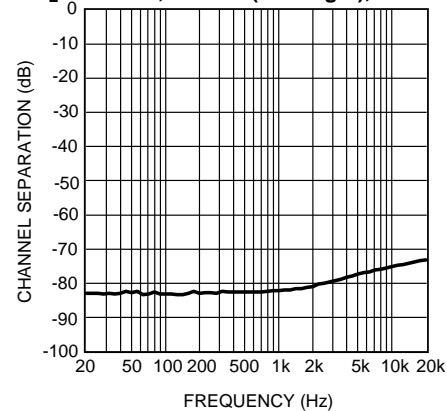


Figure 32.

Typical Performance Characteristics (continued)

Supply Current vs Supply Voltage (V_{DDLS})
 $V_{DDHP} = 2.75V$, No Load, Gain_SD = 0 & 1
LS (EP_Mode) = 0 & 1, Mode 1

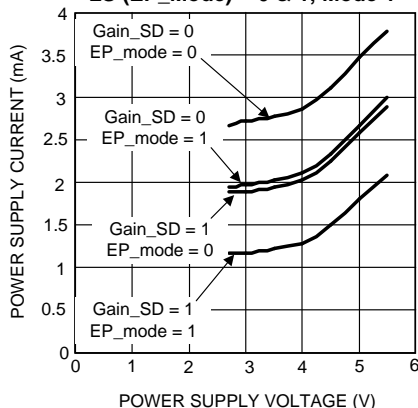


Figure 33.

Supply Current vs Supply Voltage (V_{DDLS})
 $V_{DDHP} = 2.75V$, No Load, Gain_SD = 0 & 1
LS (EP_Mode) = 0 & 1, Mode 2

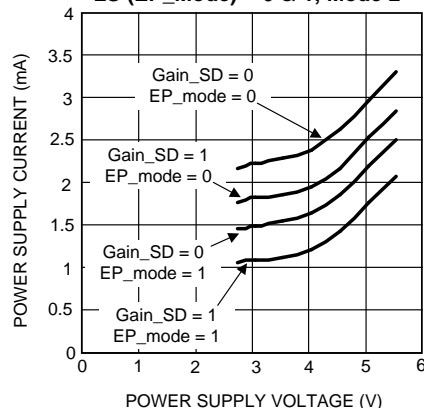


Figure 34.

Supply Current vs Supply Voltage (V_{DDHP})
 $V_{DDLS} = 3.3V$, No Load, Gain_SD = 0 or 1
HPR_SD = 0 & 1, Modes 4, 8, 15

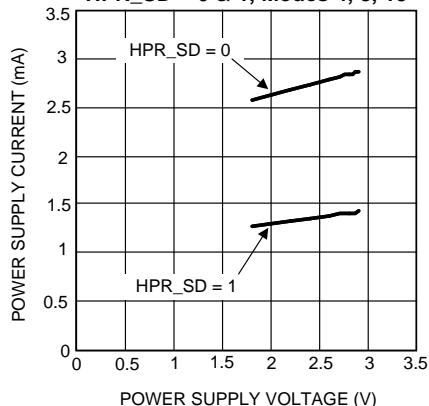


Figure 35.

Supply Current vs Supply Voltage (V_{DDHP})
 $V_{DDLS} = 2.75V$, No Load, Gain_SD = 0 or 1
LS (EP_Mode) = 0 & 1, Mode 15

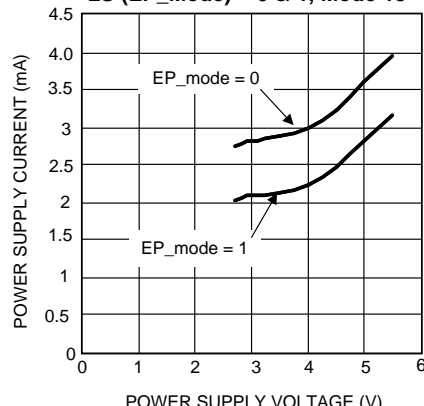


Figure 36.

Output Power vs Supply Voltage (V_{DDLS})
 $V_{DDHP} = 2.75V$, $R_L = 8\Omega$ BTL, Mode 1

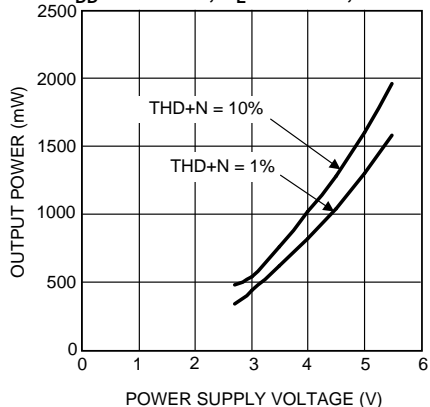


Figure 37.

Output Power vs Supply Voltage (V_{DDHP})
 $V_{DDLS} = 3.3V$, $R_L = 32\Omega$ SE, Mode 4

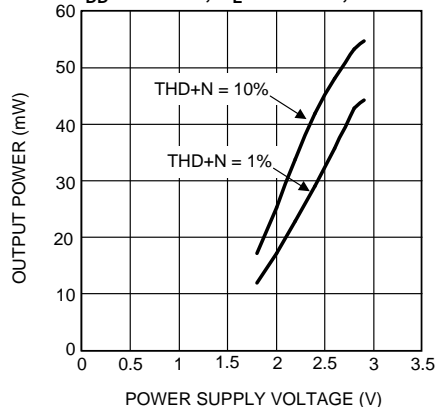


Figure 38.

APPLICATION INFORMATION

I²C COMPATIBLE INTERFACE

The LM49101 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM49101 and the master can communicate at clock rates up to 400kHz. Figure 39 shows the I²C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM49101 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 40). Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse (Figure 41). The LM49101 device address is 11111000.

I²C INTERFACE POWER SUPPLY PIN (I²CV_{DD})

The LM49101's I²C interface is powered up through the I²CV_{DD} pin. The LM49101's I²C interface operates at a voltage level set by the I²CV_{DD} pin which can be set independent to that of the main power supply pin V_{DD}LS. This is ideal whenever logic levels for the I²C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the V_{DD}LS voltage.

I²C BUS FORMAT

The I²C bus format is shown in Figure 41. The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH, is generated, alerting all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/W bit. R/W = 0 indicates the master is writing to the slave device, R/W = 1 indicates the master wants to read data from the slave device. Set R/W = 0; the LM49101 is a WRITE-ONLY device and will not respond to the R/W = 1. The data is latched in on the rising edge of the clock. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM49101 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data word is sent, the LM49101 sends another ACK bit. Following the acknowledgement of the register data word, the master issues a STOP bit, allowing SDA to go high while SCL is high.

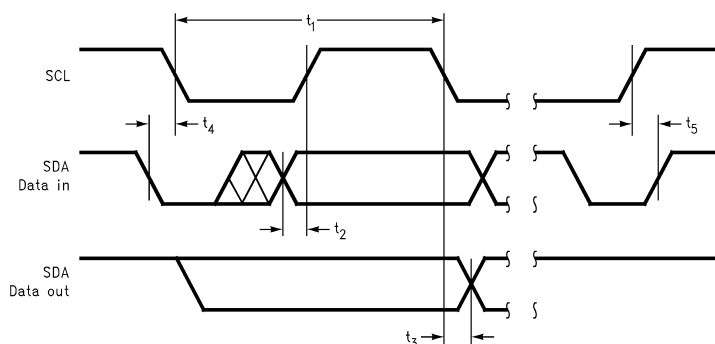


Figure 39. I²C Timing Diagram

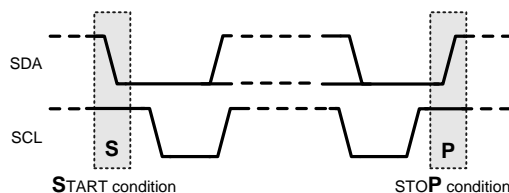
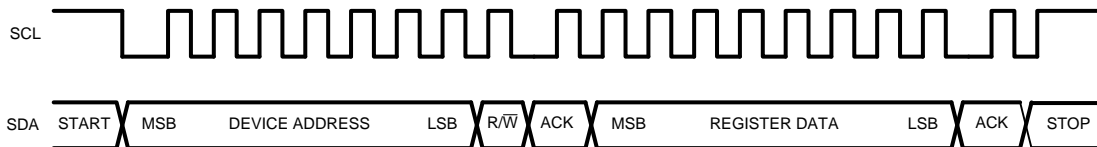


Figure 40. Start and Stop Diagram


Figure 41. Start and Stop Diagram
Table 2. Chip Address

	A7	A6	A5	A4	A3	A2	A1	A0
Chip Address	1	1	1	1	1	0	0	0

Table 3. Control Registers⁽¹⁾

Register	D7	D6	D5	D4	D3	D2	D1	D0
General Control	0	0	1	GAMP_SD ⁽²⁾	LS (EP_Mode) ⁽³⁾	0	Turn_On_Time ⁽⁴⁾	Power_On ⁽⁵⁾
Output Mode Control	0	1	EP Bypass ⁽⁶⁾	HPR_SD ⁽⁶⁾	Mode_Control ⁽⁷⁾			
Output Gain Control	1	0	0	Input_Mute ⁽⁸⁾	LS_Gain ⁽⁹⁾	HP_Gain ⁽¹⁰⁾		
Mono Input Volume Control	1	0	1	Mono_Vol ⁽¹¹⁾				
Left Input Volume Control	1	1	0	Left_Vol ⁽¹¹⁾				
Right Input Volume Control	1	1	1	Right_Vol ⁽¹¹⁾				

(1) All registers default to 0 on initial power-up.

(2) GAMP_SD: Is used to shut down gain amplifiers not in use and reduce current consumption. See [Table 4](#).

(3) LS (EP_Mode): Loudspeaker power amplifier bias current reduction. See [Table 4](#).

(4) Turn_On_Time: Reduces the turn on time for faster activation. See [Table 4](#).

(5) Power_On: Master Power on bit. See [Table 4](#).

(6) EP Bypass: Earpiece bypass mode to allow BYPASS inputs to drive speaker outputs. See [Table 5](#).

(7) Mode_Control: Sets the output mode. See [Table 5](#).

(8) Input Mute: Controls muting of the inputs except the BYPASS inputs. See [Table 6](#).

(9) LS_Gain: Sets the gain of the loudspeaker amplifier to 0dB or 6dB. See [Table 6](#).

(10) HP_Gain: Sets the headphone amplifier output gain. See [Table 6](#).

(11) Mono_Vol/Left_Vol/Right_Vol: Sets the input volume for Mono, Left and Right inputs. See [Table 7](#).

Table 4. General Control Register

Bit	Name	Value	Description
0	Power_On	This bit is a master shutdown control bit and sets the device to be on or off.	
		Value	Status
		0	Master power off, device disable.
		1	Master power on, device enable.
1	Turn_On_Time	This bit sets the turn on time of the device.	
		Value	Status
		0	Normal Turn-on time
		1	Fast Turn-on time
3	LS (EP Mode)	This bit enables EP Mode reducing loudspeaker output stage bias current by 500μA.	
		Value	Status
		0	Normal loudspeaker power amplifier operation.
		1	Enables EP Mode reducing loudspeaker output stage bias current by 500μA.

Table 4. General Control Register (continued)

Bit	Name	Value	Description
4	GAMP_SD		This bit is used to reduce I_{DD} by shutting down gain amplifiers not in use.
		0	Normal operation of all gain amplifiers.
		1	Disables the input gain amplifiers that are not in use to reduce current from V_{DDLS} . Recommended for Output Modes 1, 2, 4, 5, 8, 10.

Table 5. Output Mode Control Register⁽¹⁾

Bits	Field	Description					
3:0	Mode_Control	These bits determine how the input signals are mixed and routed to the outputs.					
				D3	D2	D1	D0
				Headphone		Loudspeaker	
		D ₃ D ₂ D ₁ D ₀	Mode	Left Headphone	Right Headphone		
		0000	0	SD	SD	SD	
		0001	1	SD	SD	G _M x M	
		0010	2	SD	SD	2 x (G _L x L + G _R x R)	
		0011	3	SD	SD	2 x (G _L x L + G _R x R) + G _M x M	
		0100	4	G _M x M/2	G _M x M/2	SD	
		0101	5	G _M x M/2	G _M x M/2	G _M x M	
		0110	6	G _M x M/2	G _M x M/2	2 x (G _L x L + G _R x R)	
		0111	7	G _M x M/2	G _M x M/2	2 x (G _L x L + G _R x R) + G _M x M	
		1000	8	G _L x L	G _R x R	SD	
		1001	9	G _L x L	G _R x R	G _M x M	
		1010	10	G _L x L	G _R x R	2 x (G _L x L + G _R x R)	
		1011	11	G _L x L	G _R x R	2 x (G _L x L + G _R x R) + G _M x M	
		1100	12	G _L x L + G _M x M/2	G _R x R + G _M x M/2	SD	
		1101	13	G _L x L + G _M x M/2	G _R x R + G _M x M/2	G _M x M	
		1110	14	G _L x L + G _M x M/2	G _R x R + G _M x M/2	2 x (G _L x L + G _R x R)	
		1111	15	G _L x L + G _M x M/2	G _R x R + G _M x M/2	2 x (G _L x L + G _R x R) + G _M x M	
4	HPR_SD	This bit sets the headphone amplifiers to normal mode or mono mode.					
		Value	Status				
		0	Normal stereo headphone operation.				
		1	Disable right headphone output.				
5	EP Bypass	This bit is used to control the analog switch to have the BYPASS inputs drive the loudspeaker outputs.					
		Value	Status				
		0	Normal output mode operation with analog switch off.				
		1	Loudspeaker and headphone amplifiers go into shutdown mode and Bypass (Receiver) path enable with the analog switch on.				

- (1) M : MIN, Mono differential input
 L : LIN, Left single-ended input
 R : RIN, Right single-ended input
 SD : Shutdown
 G_M : Mono_Vol setting determined by the Mono Input Volume Control register, See [Table 7](#).
 G_L : Left_Vol setting determined by the Left Input Volume Control register, See [Table 7](#).
 G_R : Right_Vol setting determined by the Right Input Volume Control register, See [Table 7](#).

Table 6. Output Gain Control Register

Bits	Field	Description	
2:0	HP_GAIN	These bits set the gain of the headphone output amplifiers.	
		Value	Gain (dB)
		000	0
		001	–1.2
		010	–2.5
		011	–4.0
		100	–6.0
		101	–8.5
		110	–12
		111	–18
3	LS_GAIN	This bit sets the loudspeaker output amplifier gain.	
		Value	Status
		0	Loudspeaker output amplifier gain is set to 0dB.
		1	Loudspeaker output amplifier gain is set to 6dB.
4	INPUT MUTE	This bit will set all the inputs except the BYPASS inputs to be in Mute mode.	
		Value	Status
		0	Normal operation of all inputs.
		1	Mutes all inputs except BYPASS with over 80dB of attenuation with out adjusting the volume settings. This bit can be used to mute the inputs to eliminate noise or transients from other systems and ICs. See INPUT MUTE BIT for a detailed explanation.

Table 7. Input Volume Control Registers

Bits	Fields	Description		
4:0	Mono_Vol Right_Vol Left_Vol	These bits set the input volume for each input volume register listed.		
		Volume Step	Value	Gain (dB)
		1	00000	–80.0
		2	00001	–46.5
		3	00010	–40.5
		4	00011	–34.5
		5	00100	–30.0
		6	00101	–27.0
		7	00110	–24.0
		8	00111	–21.0
		9	01000	–18.0
		10	01001	–15.0
		11	01010	–13.5
		12	01011	–12.0
		13	01100	–10.5
		14	01101	–9.0
		15	01110	–7.5
		16	01111	–6.0
		17	10000	–4.5
		18	10001	–3.0
		19	10010	–1.5
		20	10011	0.0
		21	10100	1.5
		22	10101	3.0
		23	10110	4.5
		24	10111	6.0
		25	11000	7.5
		26	11001	9.0
		27	11010	10.5
		28	11011	12.0
		29	11100	13.5
		30	11101	15.0
		31	11110	16.5
		32	11111	18.0

HW RESET FUNCTION

The LM49101 can be globally reset without using the I²C controls. When the HW RESET pin is set to a logic low the LM49101 will enter into shutdown, the mode control bits of the Output Mode Control register, volume control registers and Power_On bits will be set to the default value of zero. The other bits will retain their values. The LM49101 cannot be activated until the HW RESET pin is set to a logic high voltage. When the HW RESET is set to a logic high then the I²C controls can activate and set the register control bits.

GAMP_SD BIT

The GAMP_SD bit allows for reduced power consumption. When set to '1' the gain amplifiers on unused inputs will be shutdown saving approximately 0.4mA per input in shutdown. For example, in Mode 1 only the mono inputs are in use. Setting GAMP_SD to '1' will shut down the gain amplifiers for the left and right inputs reducing current draw from the V_{DD}LS supply by approximately 0.8mA. The GAMP_SD bit does not need to be set each time when changing modes as the LM49101 will automatically activate and deactivate the needed inputs based on the mode selected.

When operating with GAMP_SD set to '1', a transient may be observed on the outputs when changing modes. During power up, the LM49101 uses a start up sequence to eliminate any pops and clicks on the outputs. The volume control circuitry is powered up first followed by the other internal circuitry with the output amplifiers being powered up last. If a mode change requires a gain amplifier to turn on then a potential transient may be created that is amplified on the already active outputs. To eliminate unwanted noise on the outputs the Power_On bit should be used to turn off the LM49101 before changing modes, perform a mode change, then turn the LM49101 back on. This procedure will cause the LM49101 to follow the start up sequence.

LS (EP_MODE) BIT

The LS (EP_Mode) bit selects the amount of bias current in the loudspeaker amplifier. Setting the LS (EP_Mode) bit to a '1' will reduce the amount of current from the V_{DD}LS supply by approximately 0.5mA. The THD performance of the loudspeaker amplifier will be reduced as a result of lower bias current. See the performance graphs in [Typical Performance Characteristics](#).

TURN_ON_TIME BIT

The Turn_On_Time bit determines the delay time from the Power_On bit set to '1' and the internal circuits ready. For input capacitor values up to 0.47μF the Turn_On_Time bit can be set to fast mode by setting the bit to a '1'. When the input capacitor values are larger than 0.47μF then the Turn_On_Time bit should be set to '0' for normal turn-on time and higher delay. This allows sufficient time to charge the input capacitors to the ½ V_{DD}LS bias voltage.

POWER_ON BIT

The Power_On bit is the master control bit to activate or deactivate the LM49101. All registers can be loaded independent of the Power_On bit setting as long as the IC is powered correctly. Cycling the Power_On bit does not change the values of any registers nor return all bits to the default power on value of zero. The Power_On bit only determines whether the IC is on or off.

EP BYPASS BIT

The EP Bypass bit is used to set the LM49101 to earpiece mode. When this bit is set the analog switch is activated and the rest of the IC blocks except for the I²C circuitry will go into shutdown for minimal current consumption.

HPR_SD BIT

The HPR_SD bit will deactivate the right headphone output amplifier. This bit is provided to reduce power consumption when only one headphone output is needed.

MODE_CONTROL BITS

The LM49101 includes a comprehensive mixer multiplexer controlled through the I²C interface. The mixer/multiplexer allows any input combination to appear on any output of LM49101. Multiple input paths can be selected simultaneously. Under these conditions, the selected inputs are mixed together and output on the selected channel. [Table 5](#) shows how the input signals are mixed together for each possible input selection.

INPUT MUTE BIT

The Input Mute bit will mute all inputs except the Bypass inputs when set to a '1'. This allows complete and quick mute of the Mono, Left, and Right inputs without changing the Volume Control registers or HP_Gain bits. The volume and HP_Gain bits retain their values when the Input Mute is enabled or disabled.

The Input Mute bit can be used to mute all the inputs when other chips in a system, such as the baseband IC, create transients causing unwanted noise on the outputs of the LM49101. This added feature eliminates the need for power cycling the LM49101.

LS_GAIN BIT

The loudspeaker amplifier can have an additional gain of 0dB or 6dB by using the LS_Gain bit. The Mono input has 6dB of attenuation before the volume control (see [Figure 1](#)) while the Left and Right inputs do not. The LS_Gain bit is used to account for the different attenuation levels for each input and to achieve maximum output power. To obtain maximum output power on the loudspeaker outputs, the LS_Gain bit should be set to '1' for Modes 1, 5, 9, 13.

HP_GAIN BITS

The headphone outputs have an additional, single volume control set by the three HP_Gain bits in the Output Gain Control register. The HP_Gain volume setting controls the output level for both the left and the right headphone outputs.

VOLUME CONTROL BITS

The LM49101 has three independent 32-step volume controls, one for each of the inputs. The five bits of the Volume Control registers sets the volume for the specified input channel.

SHUTDOWN FUNCTION

The LM49101 features the following shutdown controls.

Bit D4 (GAMP_SD) of the GENERAL CONTROL register controls the gain amplifiers. When GAMP_SD = 1, it disables the gain amplifiers that are not in use. For example, in Modes 1, 4 and 5, the Mono inputs are in use, so the Left and Right input gain amplifiers are disabled, causing the I_{DD} to be minimized.

Bit D0 (Power_On) of the GENERAL CONTROL register is the global shutdown control for the entire device. Set Power_On = 0 for normal operation. Power_On = 1 overrides any other shutdown control bit.

DIFFERENTIAL AMPLIFIER EXPLANATION

The LM49101 features a differential input stage, which offers improved noise rejection compared to a single-ended input amplifier. Because a differential input amplifier amplifies the difference between the two input signals, any component common to both signals is cancelled. An additional benefit of the differential input structure is the possible elimination of the DC input blocking capacitors. Since the DC component is common to both inputs, and thus cancelled by the amplifier, the LM49101 can be used without input coupling capacitors when configured with a differential input signal.

BRIDGE CONFIGURATION EXPLAINED

By driving the load differentially through the MONO outputs, an amplifier configuration commonly referred to as “bridged mode” is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped.

A bridge configuration, such as the one used in LM49101, also creates a second advantage over single-ended amplifiers. Since the differential outputs are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. The power dissipation of the LM49101 varies with the mode selected. The maximum power dissipation occurs in modes where all inputs and outputs are active (Modes 6, 7, 8, 9, 10, 11, 13, 14, 15). The power dissipation is dominated by the Class AB amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from [Equation 1](#).

$$P_{\text{DMAX}} = 4 \cdot (V_{\text{DD}})^2 / (2\pi^2 R_L) \quad (1)$$

It is critical that the maximum junction temperature (T_{JMAX}) of 150°C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced from the free air value, resulting in higher P_{DMAX} . Additional copper foil can be added to any of the leads connected to the LM49101. It is especially effective when connected to V_{DD} , GND, and the output pins. Refer to [Demonstration Board](#) for an example of good heat sinking. If T_{JMAX} still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the [Typical Performance Characteristics](#) curves for power dissipation information for different output powers and output loading.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM49101. The selection of a bypass capacitor, especially C_B , is dependent upon PSRR requirements, click and pop performance, system cost, and size constraints.

GROUND REFERENCED HEADPHONE AMPLIFIER

The LM49101 features a low noise inverting charge pump that generates an internal negative supply voltage. This allows the headphone outputs to be biased about GND instead of a nominal DC voltage, like traditional headphone amplifiers. Because there is no DC component, the large DC blocking capacitors (typically 220µF) are not necessary. The coupling capacitors are replaced by two small ceramic charge pump capacitors, saving board space and cost. Eliminating the output coupling capacitors also improves low frequency response. In traditional headphone amplifiers, the headphone impedance and the output capacitor from a high-pass filter that not only blocks the DC component of the output, but also attenuates low frequencies, impacting the bass response. Because the LM49101 does not require the output coupling capacitors, the low frequency response of the device is not degraded by external components. In addition to eliminating the output coupling capacitors, the ground referenced output nearly doubles the available dynamic range of the LM49101 headphone amplifiers when compared to a traditional headphone amplifier operating from the same supply voltage.

HEADPHONE & CHARGE PUMP SUPPLY VOLTAGE (V_{DDHP} & V_{DDCP})

The headphone outputs are centered at ground by using dual supply voltages for the headphone amplifier. The positive power supply is set by the voltage on the V_{DDHP} pin while the negative supply is created with an internal charge pump. The negative supply voltage is equal in magnitude but opposite in voltage to the voltage on the V_{DDCP} pin.

INPUT CAPACITOR SELECTION

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM49101. The input capacitors create a high-pass filter with the input resistors R_{IN} . The -3dB point of the high-pass filter is found using [Equation 2](#) below.

$$f = 1 / 2\pi R_{IN} C_{IN} \text{ (Hz)} \quad (2)$$

Where the value of R_{IN} is given in [Electrical Characteristics VDDL5 = 3.3V, VDDHP = 2.75V](#) and [Electrical Characteristics VDDL5 = 5.0V, VDDHP = 2.75V](#) as Z_{IN} .

When the LM49101 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

CHARGE PUMP FLYING CAPACITOR (C_1)

The flying capacitor (C_1), see [Figure 1](#), affects the load regulation and output impedance of the charge pump. A C_1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C_1 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2 μ F, the $R_{DS(ON)}$ of the charge pump switches and the ESR of C_1 and C_{S3} dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

CHARGE PUMP HOLD CAPACITOR (C_{S3})

The value and ESR of the hold capacitor C_{S3} directly affects the ripple on V_{SSCP} . Increasing the value of C_{S3} reduces output ripple. Decreasing the ESR of C_{S3} reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

SELECTION OF INPUT RESISTORS

The Bypass_In inputs connect to the loudspeaker output through an FET switch when EP Bypass is active (see [Figure 42](#)). Because THD through this path is mainly dominated by the switch impedance variation, adding input resistors (R_3 and R_4 in [Figure 42](#)) will help reduce impedance effects resulting in improved THD. For example, a change in the switch impedance from 2 Ω to 3 Ω is a 67% change in impedance. If 10 Ω input resistors are used then the impedance change is from 12 Ω to 13 Ω , only 7.7% impedance variation. The analog switch impedance is typically 2 Ω to 3.4 Ω . The switch impedance change is a result of heating and the increase in $R_{DS(ON)}$ of the FETs.

The value of the input resistors must be balanced against the amount of output current and the load impedance on the loudspeaker outputs. A higher value input resistor reduces the effects of switch impedance variation but also causes voltage drop and reduced power to the load on the loudspeaker outputs.

The current through the FET switch should not exceed 500mA or die heating may cause thermal shut down activation and potential IC damage.

MINIMUM POWER OPERATION

The LM49101 has several options to reduce power consumption and is designed to conserve power when possible. When a speaker only mode is selected the headphone sections are shutdown and the current drawn from the V_{DDHP}/V_{DDCP} power supply will be zero. When a headphone mode is selected the current drawn from the V_{DDL5} supply is also reduced by shutting down unused circuitry. See the various Supply Current vs Supply Voltage graphs in [Typical Performance Characteristics](#).

To reduce power consumption further, the additional control bits GAMP_SD, LS (EP Mode), and HPR_SD are provided. When low power consumption is more important than the THD performance of the loudspeaker the LS (EP_mode) bit should be set to '1' saving approximately 0.5mA from the V_{DDL5} supply. The GAMP_SD bit should be set on to save approximately 0.4mA for each input shut down. For modes where only the mono input is used, up to 0.8mA can be saved from the V_{DDL5} supply. Also, the HPR_SD bit can be used to shut down the right headphone channel reducing power consumption when only one amplifier headphone output is needed.

Additionally, the supply voltages for the different V_{DD} pins (V_{DDL5} , V_{DDHP} , and V_{DDCP}) can be set to the minimum needed values to obtain the output power levels required by the design. By reducing the supply voltage the total power consumption will be reduced.

For best system efficiency, a DC-DC converter (buck) can be used to power the V_{DDHP} and V_{DDCP} voltages from the V_{DDL5} supply instead of a linear regulator. DC-DC converters achieve much higher efficiency (> 90%) than even a low dropout regulator (LDO).

Demo Board Circuit

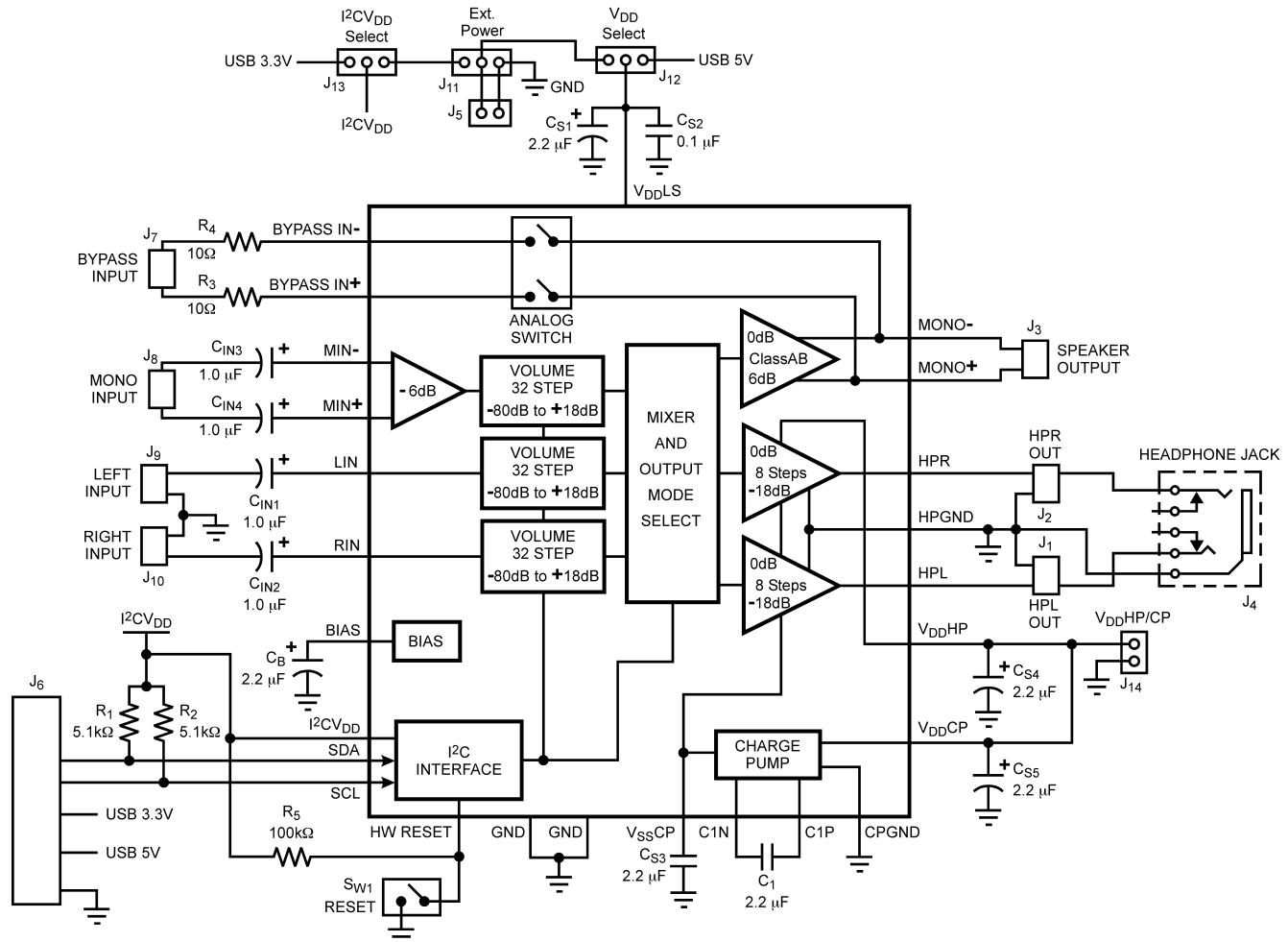


Figure 42. Demo Board Circuit

Demonstration Board

The demonstration board (see [Figure 42](#)) has connection and jumper options to be powered partially from the USB bus or from external power supplies. Additional options are to power the I²C logic and loudspeaker amplifier (V_{DDLS}) from a single power supply or separate power supplies. The headphone amplifier and charge pump can also be powered from the same supply as long as the voltage limits for each power supply are not exceeded, although the option is not built into the board. See [Operating Ratings](#) for each supply's range limit. When powered from the USB bus the I²CV_{DD} will be set to 3.3V and the V_{DDLS} will be set to 5V. Jumper headers J₁₃ and J₁₂ must be set accordingly. If a single power supply for I²CV_{DD} and V_{DDLS} is desired then header J₅ should be used with a jumper added to header J₁₁ to connect I²CV_{DD} to the external supply voltage connected to J₅ (see [Figure 42](#)).

Connection headers J₁ and J₂ are provided along with the stereo headphone jack J₄ for easily connection and monitoring of the headphone outputs.

INPUTS

MONO + -

RIGHT + -

SPEAKER OUTPUT

J2 GND HPR OUT

J8 J9

J3

J1 HPL OUT GND

J4 J5

J6 J7

J10 J11

J12

J13 J14

J15 J16

J17 J18

J19 J20

J21 J22

J23 J24

J25 J26

J27 J28

J29 J30

J31 J32

J33 J34

J35 J36

J37 J38

J39 J40

J41 J42

J43 J44

J45 J46

J47 J48

J49 J50

J51 J52

J53 J54

J55 J56

J57 J58

J59 J60

J61 J62

J63 J64

J65 J66

J67 J68

J69 J70

J71 J72

J73 J74

J75 J76

J77 J78

J79 J80

J81 J82

J83 J84

J85 J86

J87 J88

J89 J90

J91 J92

J93 J94

J95 J96

J97 J98

J99 J100

J101 J102

J103 J104

J105 J106

J107 J108

J109 J110

J111 J112

J113 J114

J115 J116

J117 J118

J119 J120

J121 J122

J123 J124

J125 J126

J127 J128

J129 J130

J131 J132

J133 J134

J135 J136

J137 J138

J139 J140

J141 J142

J143 J144

J145 J146

J147 J148

J149 J150

J151 J152

J153 J154

J155 J156

J157 J158

J159 J160

J161 J162

J163 J164

J165 J166

J167 J168

J169 J170

J171 J172

J173 J174

J175 J176

J177 J178

J179 J180

J181 J182

J183 J184

J185 J186

J187 J188

J189 J190

J191 J192

J193 J194

J195 J196

J197 J198

J199 J200

J201 J202

J203 J204

J205 J206

J207 J208

J209 J210

J211 J212

J213 J214

J215 J216

J217 J218

J219 J220

J221 J222

J223 J224

J225 J226

J227 J228

J229 J230

J231 J232

J233 J234

J235 J236

J237 J238

J239 J240

J241 J242

J243 J244

J245 J246

J247 J248

J249 J250

J251 J252

J253 J254

J255 J256

J257 J258

J259 J260

J261 J262

J263 J264

J265 J266

J267 J268

J269 J270

J271 J272

J273 J274

J275 J276

J277 J278

J279 J280

J281 J282

J283 J284

J285 J286

J287 J288

J289 J290

J291 J292

J293 J294

J295 J296

J297 J298

J299 J300

J301 J302

J303 J304

J305 J306

J307 J308

J309 J310

J311 J312

J313 J314

J315 J316

J317 J318

J319 J320

J321 J322

J323 J324

J325 J326

J327 J328

J329 J330

J331 J332

J333 J334

J335 J336

J337 J338

J339 J340

J341 J342

J343 J344

J345 J346

J347 J348

J349 J350

J351 J352

J353 J354

J355 J356

J357 J358

J359 J360

J361 J362

J363 J364

J365 J366

J367 J368

J369 J370

J371 J372

J373 J374

J375 J376

J377 J378

J379 J380

J381 J382

J383 J384

J385 J386

J387 J388

J389 J390

J391 J392

J393 J394

J395 J396

J397 J398

J399 J400

J401 J402

J403 J404

J405 J406

J407 J408

J409 J410

J411 J412

J413 J414

J415 J416

J417 J418

J419 J420

J421 J422

J423 J424

J425 J426

J427 J428

J429 J430

J431 J432

J433 J434

J435 J436

J437 J438

J439 J440

J441 J442

J443 J444

J445 J446

J447 J448

J449 J450

J451 J452

J453 J454

J455 J456

J457 J458

J459 J460

J461 J462

J463 J464

J465 J466

J467 J468

J469 J470

J471 J472

J473 J474

J475 J476

J477 J478

J479 J480

J481 J482

J483 J484

J485 J486

J487 J488

J489 J490

J491 J492

J493 J494

J495 J496

J497 J498

J499 J500

J501 J502

J503 J504

J505 J506

J507 J508

J509 J510

J511 J512

J513 J514

J515 J516

J517 J518

J519 J520

J521 J522

J523 J524

J525 J526

J527 J528

J529 J530

J531 J532

J533 J534

J535 J536

J537 J538

J539 J540

J541 J542

J543 J544

J545 J546

J547 J548

J549 J550

J551 J552

J553 J554

J555 J556

J557 J558

J559 J560

J561 J562

J563 J564

J565 J566

J567 J568

J569 J570

J571 J572

J573 J574

J575 J576

J577 J578

J579 J580

J581 J582

J583 J584

J585 J586

J587 J588

J589 J590

J591 J592

J593 J594

J595 J596

J597 J598

J599 J600

J601 J602

J603 J604

J605 J606

J607 J608

J

[illegible]

26

LM49101 Reference Demo Board Bill Of Materials

Table 8. Bill Of Materials

Designator	Value	Tolerance	Part Description	Comment
R ₁ , R ₂	5.1kΩ	5%	1/10W, 0603 Resistors	
R ₃ , R ₄	10Ω	1%	1/10W, 0603 Resistors	
R ₅	100kΩ	5%	1/10W, 0805 Resistor	
C _{IN1} , C _{IN2} C _{IN3} , C _{IN4}	1μF	10%	1206, X7R Ceramic Capacitor	
C _{S1} , C _{S4} C _{S5} , C _B	2.2μF	10%	Size A, Tantalum Capacitor	
C _{S2}	0.1μF	10%	0805, 16V, X7R Ceramic Capacitor	
C _{S3} , C ₁	2.2μF	10%	0603, 10V, X7R Ceramic Capacitor	
U ₁			LM49101TM	
J ₁ , J ₂ , J ₃ J ₅ , J ₇ , J ₈ J ₉ , J ₁₀ , J ₁₄			0.100" 1x2 header, vertical mount	Input, Output, V _{DD} , GND
J ₁₁ , J ₁₂ , J ₁₃			0.100" 1x3 header, vertical mount	V _{DD} Selects, V _{DD} , I ² C V _{DD} , GND
J ₆			16 pin header	I ² C Connector
J ₄			Headphone Jack	
SW ₁			Momentary Push Switch	RESET function

PCB Layout Guidelines

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

General Mixed Signal Layout Recommendations

SINGLE-POINT POWER AND GROUND CONNECTIONS

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing high frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

PLACEMENT OF DIGITAL AND ANALOG COMPONENTS

All digital components and high-speed digital signals traces should be located as far away as possible from analog components and circuit traces.

AVOIDING TYPICAL DESIGN AND LAYOUT PROBLEMS

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

Revision History

Rev	Date	Description
0.01	10/18/08	Initial released.
A	04/08/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM49101TM/NOPB	ACTIVE	DSBGA	YFQ	25	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GL4	Samples
LM49101TMX/NOPB	ACTIVE	DSBGA	YFQ	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GL4	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM49101TM/NOPB	DSBGA	YFQ	25	250	178.0	8.4	2.18	2.18	0.76	4.0	8.0	Q1
LM49101TMX/NOPB	DSBGA	YFQ	25	3000	178.0	8.4	2.18	2.18	0.76	4.0	8.0	Q1

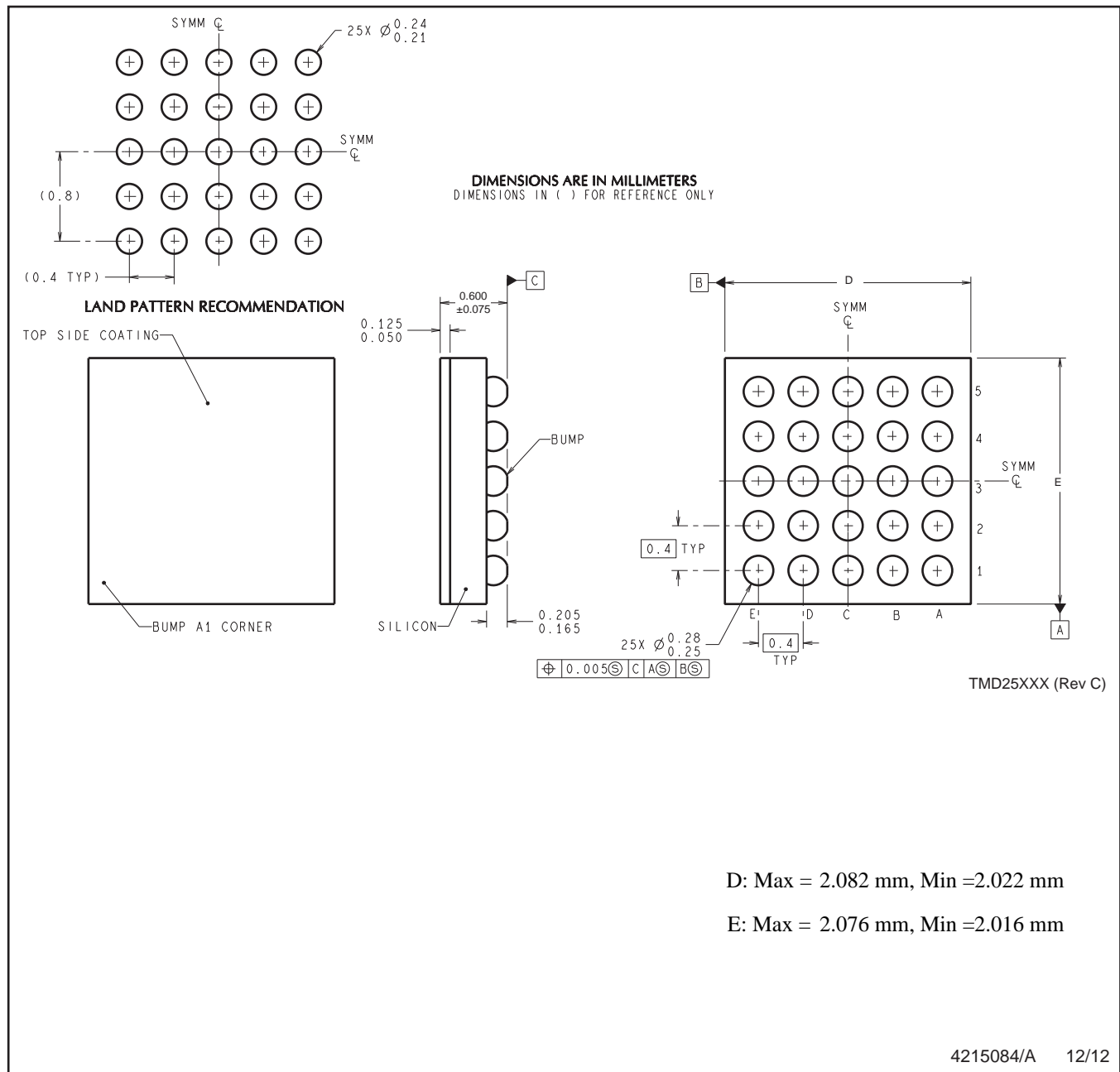
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM49101TM/NOPB	DSBGA	YFQ	25	250	210.0	185.0	35.0
LM49101TMX/NOPB	DSBGA	YFQ	25	3000	210.0	185.0	35.0

YFQ0025



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com