LM4842 Boomer® Audio Power Amplifier Series Stereo 2W Amplifiers with DC Volume Control, Input MUX, Transient Free Outputs, and Cap-less Headphone Drive

Check for Samples: LM4842

FEATURES

- **Stereo Headphone Amplifier Mode that Eliminates the Output Coupling Capacitors (Patent Pending)**
- **Advanced "Click and Pop" Suppression Circuitry**
- **Acoustically Enhanced DC Volume Control Taper**
- **2 Channel Stereo Input MUX**
- **System Beep Detect**
- **Stereo Switchable Bridged/Single-ended Power Amplifiers**
- **Selectable Internal/External Gain and Bass Boost**
- **Thermal Shutdown Protection Circuitry**

APPLICATIONS

- **Portable and Desktop Computers**
- **Multimedia Monitors**
- **Portable Radios, PDAs, and Portable TVs**

KEY SPECIFICATIONS

- **P_O at 1% THD+N**
  - **Into 3Ω (MH and LQ): 2.2W (typ)**
  - **Into 4Ω (MH and LQ): 2.0W (typ)**
  - **Into 8Ω (MT, MH, and LQ): 1.1W (typ)**
- **Single-Ended THD+N at 85mW into 32Ω: 1.0% (typ)**
- **Shutdown Current (Shutdown Low): 0.2µA (typ)**

DESCRIPTION

The LM4842 is a monolithic integrated circuit that provides DC volume control, and stereo bridged audio power amplifiers capable of producing 2W into 4Ω or 2.2W into 3Ω with less than 1.0% THD+N (see (1) (2)).

Boomer® audio integrated circuits were designed specifically to provide high quality audio while requiring a minimum amount of external components. The LM4842 incorporates a DC volume control, stereo bridged audio power amplifiers, new cap-less headphone driver circuit (patent pending), selectable gain or bass boost, and an input mux making it optimally suited for multimedia monitors, portable radios, desktop, and portable computer applications.

The LM4842 features an externally controlled, low-power consumption shutdown mode (Shutdown Low), and both a power amplifier and headphone mute for maximum system flexibility and performance.

(1) When properly mounted to the circuit board, the LM4842MH will deliver 2W into 4Ω. The LM4842MT will deliver 1.1W into 8Ω. See the APPLICATION INFORMATION section for LM4842MH usage information.

(2) An LM4842MH that has been properly mounted to the circuit board and forced-air cooled will deliver 2.2W into 3Ω.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Boomer is a registered trademark of Rockford Corporation.
All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2002–2013, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CONNECTION DIAGRAM

TSSOP Package (Top View)

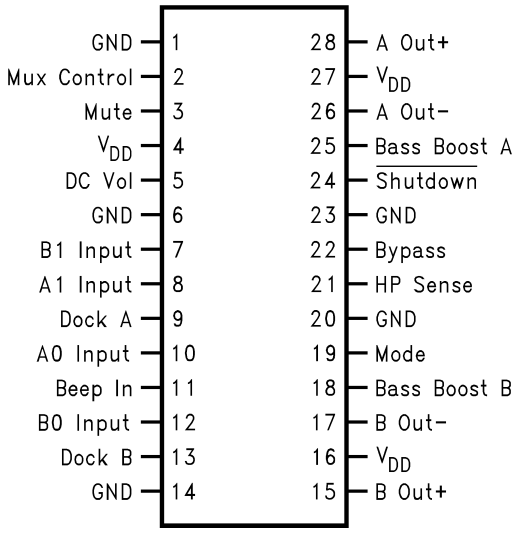


Figure 1. See Package Number PW0028A and Package Number PWP0028A for Exposed-DAP

LM4842LQ Pinout (Top View)

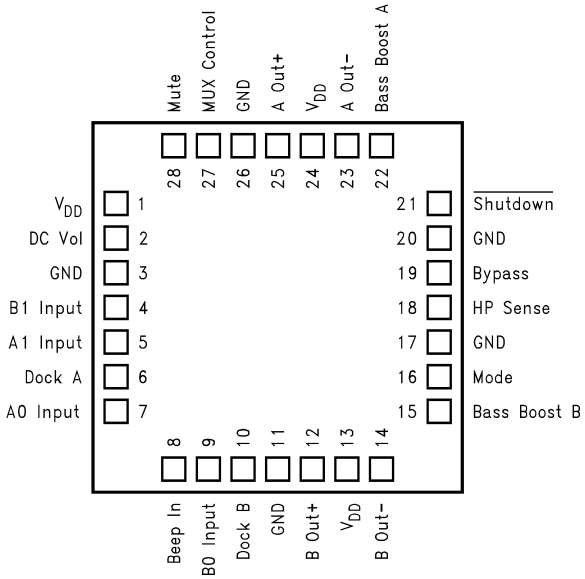


Figure 2. See Package Number NJB0028A for Exposed-DAP (WQFN)

Copyright © 2002–2013, Texas Instruments Incorporated

BLOCK DIAGRAM

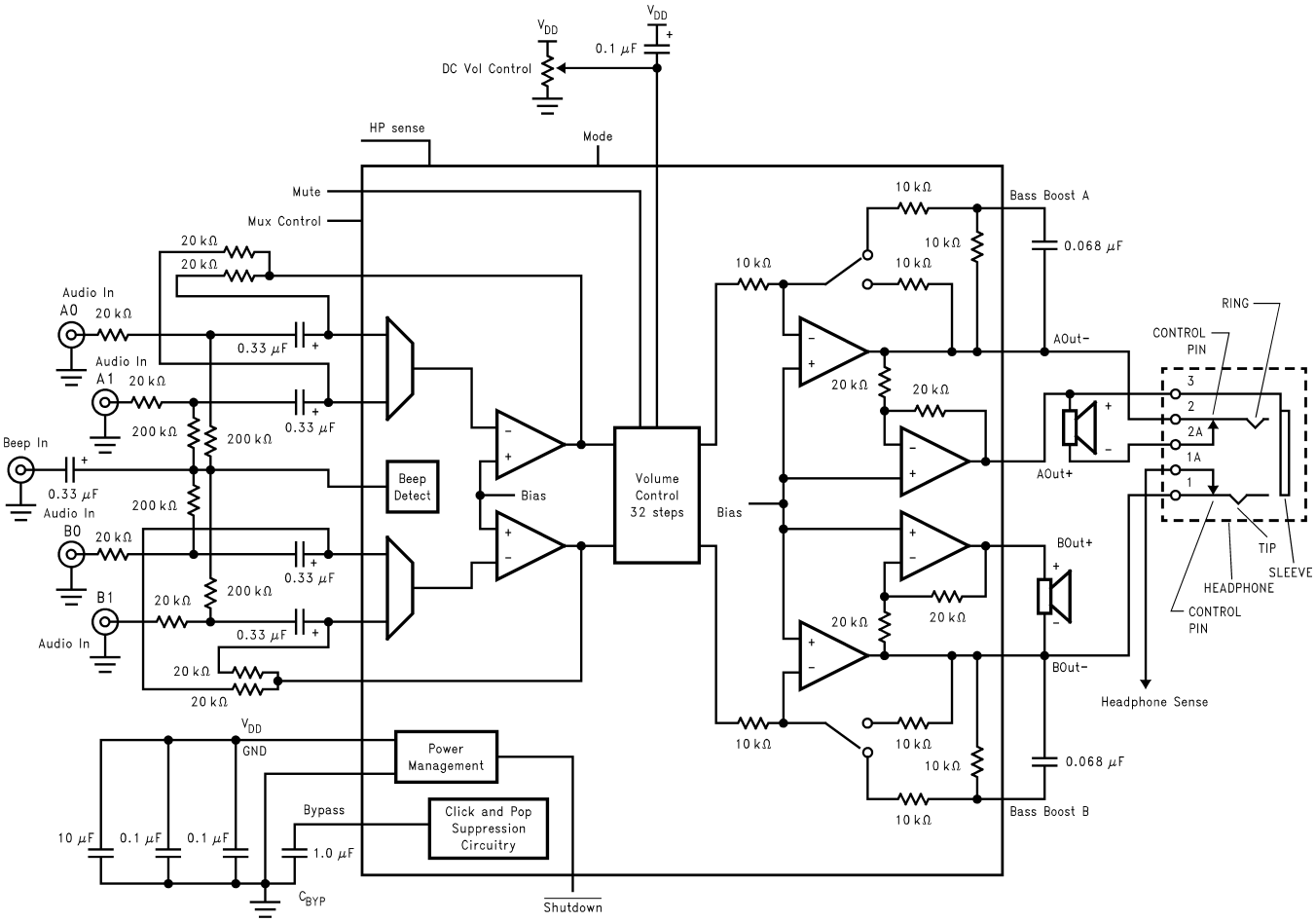


Figure 3. Typical Application Circuit

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage	6.0V
Storage Temperature	-65°C to +150°C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation(3)	Internally limited
ESD Susceptibility(4)	
All pins except Pin 28	2500V
Pin 28	6500V
ESD Susceptibility(5)	200V
Junction Temperature	150°C
Soldering Information Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
θ_{JC} (typ)—NJB0028A	3°C/W
θ_{JA} (typ)—NJB0028A	42°C/W
θ_{JC} (typ)—PW0028A	20°C/W
θ_{JA} (typ)—PW0028A	80°C/W
θ_{JC} (typ)—PWP0028A	2°C/W
θ_{JA} (typ)—PWP0028A (exposed DAP)(6)	41°C/W
θ_{JA} (typ)—PWP0028A (exposed DAP)(7)	54°C/W
θ_{JA} (typ)—PWP0028A (exposed DAP)(8)	59°C/W
θ_{JA} (typ)—PWP0028A (exposed DAP)(9)	93°C/W

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. For the LM4842MT and LM4842LQ, T_{JMAX} = 150°C. See POWER DISSIPATION for further information.

(4) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

(5) Machine Model, 220 pF–240 pF discharged through all pins.

(6) The θ_{JA} given is for an PWP0028A package whose exposed-DAP is soldered to a $2in^2$ piece of 1 ounce printed circuit board copper on a bottom side layer through 21 8mil vias.

(7) The θ_{JA} given is for an PWP0028A package whose exposed-DAP is soldered to an exposed $2in^2$ piece of 1 ounce printed circuit board copper.

(8) The θ_{JA} given is for an PWP0028A package whose exposed-DAP is soldered to an exposed $1in^2$ piece of 1 ounce printed circuit board copper.

(9) The θ_{JA} given is for an PWP0028A package whose exposed-DAP is not soldered to any copper.

OPERATING RATINGS

Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤TA ≤ 85°C
Supply Voltage	2.7V≤ V_{DD} ≤ 5.5V

Copyright © 2002–2013, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS FOR ENTIRE IC(1)(2)

The following specifications apply for V_{DD} = 5V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	LM4842		Units (Limits)
			Typical (3)	Limit (4)	
V_{DD}	Supply Voltage			2.7	V (min)
				5.5	V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A	15	30	mA (max)
I_{SD}	Shutdown Current	$V_{\overline{Shutdown}}$ = GND	0.7	2.0	µA (max)
V_{IH}	VIN High on all Logic Inputs			0.8 x V_{DD}	V (min)
V_{IL}	VIN Low on all Logic Inputs			0.2 x V_{DD}	V (max)
TH_{um}	Un-Mute Threshold Voltage	$V_{\overline{Shutdown}}$ = V_{DD}, Gain 1st Stage = 1	22	10 40	mV_{RMS} mV_{RMS}

(1) All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in Figure 4.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to AOQL (Average Outgoing Quality Level.) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

ELECTRICAL CHARACTERISTICS FOR VOLUME ATTENUATORS(1)(2)

The following specifications apply for V_{DD} = 5V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	LM4842		Units (Limits)
			Typical (3)	Limit (4)	
C_{RANGE}	Attenuator Range	Gain with V_{DCVol} = 5.0V, No Load		±0.75	dB (max)
C_{RANGE}	Attenuator Range	Attenuation with V_{DCVol} = 0V (BM & SE)		-75	dB (min)
A_M	Mute Attenuation	V_{mute} = 5V, Bridged Mode (BM)		-78	dB (min)
		V_{mute} = 5V, Single-Ended Mode (SE)		-78	dB (min)

(1) All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in Figure 4.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to AOQL (Average Outgoing Quality Level.) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

Copyright © 2002–2013, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS FOR SINGLE-ENDED MODE OPERATION(1)(2)

The following specifications apply for V_{DD} = 5V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	LM4842		Units (Limits)
			Typical (3)	Limit (4)	
P_O	Output Power	THD+N = 1.0%; f = 1kHz; R_L = 32Ω	85		mW
		THD+N = 10%; f = 1 kHz; R_L = 32Ω	95		mW
THD+N	Total Harmonic Distortion+Noise	V_{OUT} = 1V_{RMS}, f=1kHz, R_L = 10kΩ, A_{VD} = 1	0.065		%
PSRR	Power Supply Rejection Ratio	C_B = 1.0 µF, f =120 Hz, V_{RIPPLE} = 200 mVrms	58		dB
SNR	Signal to Noise Ratio	P_{OUT} =75 mW, R_L = 32Ω, A-Wtd Filter	102		dB
X_{talk}	Channel Separation	f=1kHz, C_B = 1.0 µF	65		dB

(1) All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in Figure 4.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to AOQL (Average Outgoing Quality Level.) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

ELECTRICAL CHARACTERISTICS FOR BRIDGED MODE OPERATION(1)(2)

The following specifications apply for V_{DD} = 5V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	LM4842		Units (Limits)
			Typical (3)	Limit (4)	
V_{OS}	Output Offset Voltage	V_{IN} = 0V, No Load	5	±50	mV (max)
P_O	Output Power	THD + N = 1.0%; f=1kHz; R_L = 3Ω (5)	2.2		W
		THD + N = 1.0%; f=1kHz; R_L = 4Ω (6)	2		W
		THD = 1.0% (max);f = 1 kHz; R_L = 8Ω	1.1	1.0	W (min)
		THD+N = 10%;f = 1 kHz; R_L = 8Ω	1.5		W
THD+N	Total Harmonic Distortion+Noise	P_O = 1W, 20 Hz< f < 20 kHz, R_L = 8Ω, A_{VD} = 2	0.3		%
		P_O = 340 mW, R_L = 32Ω	1.0		%
PSRR	Power Supply Rejection Ratio	C_B = 1.0 µF, f = 120 Hz, V_{RIPPLE} = 200 mVrms; R_L = 8Ω	74		dB
SNR	Signal to Noise Ratio	V_{DD} = 5V, P_{OUT} = 1.1W, R_L = 8Ω, A-Wtd Filter	93		dB
X_{talk}	Channel Separation	f=1kHz, C_B = 1.0 µF	70		dB

(1) All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in Figure 4.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to AOQL (Average Outgoing Quality Level.) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(5) When driving 3Ω loads from a 5V supply the LM4842MH and LM4842LQ exposed DAP must be soldered to the circuit board and forced-air cooled.
(6) When driving 4Ω loads from a 5V supply the LM4842MH and LM4842LQ exposed DAP must be soldered to the circuit board.

Copyright © 2002–2013, Texas Instruments Incorporated

TYPICAL APPLICATION

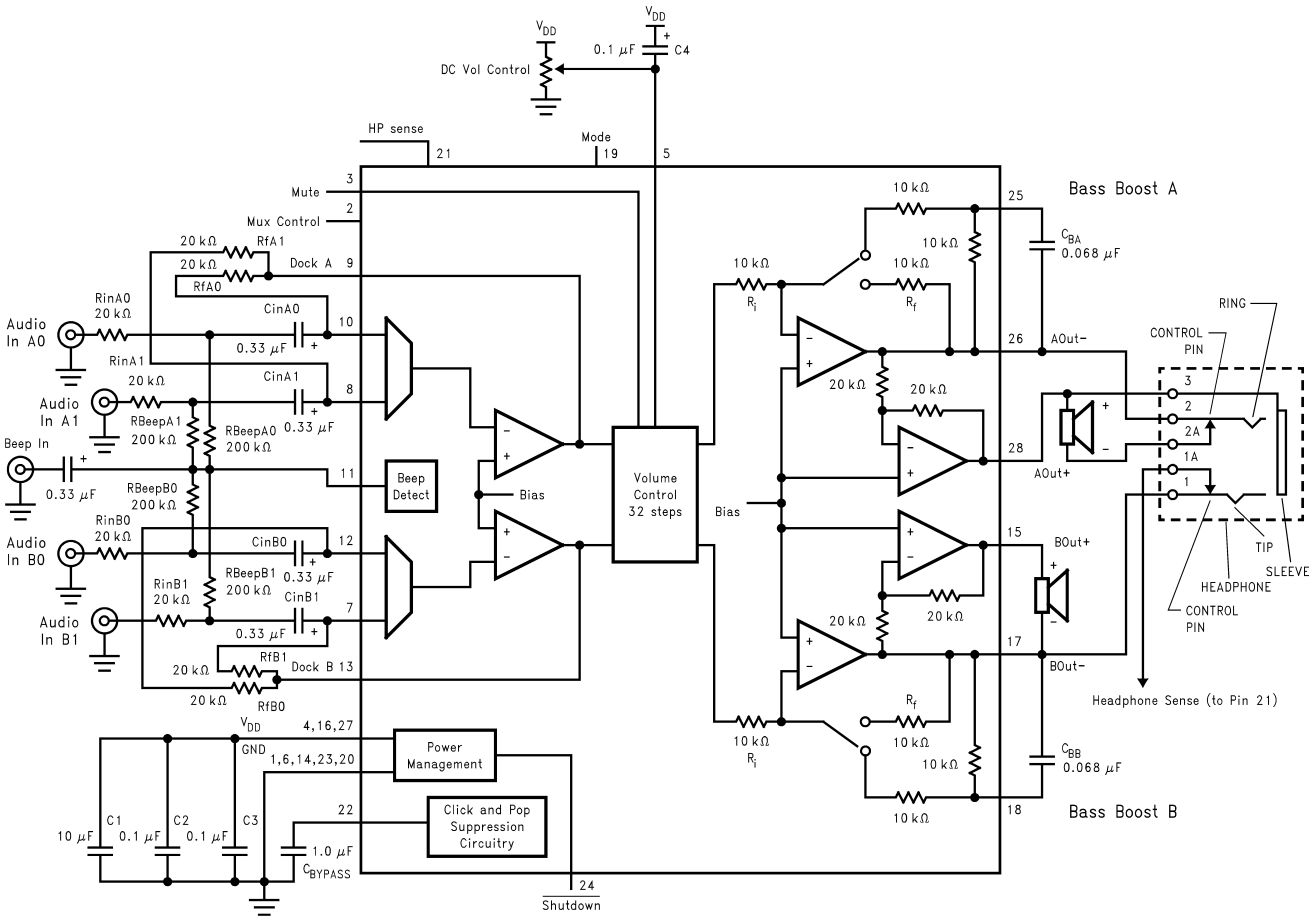


Figure 4. Typical Application Circuit (MT & MH pinout)

TRUTH TABLE FOR LOGIC INPUTS(1)

Mute	Mode	Mux Control	HP Sense	Bass Boost	Inputs Selected	Bridged Output	Single-Ended Output
0	0	0	0	on	A0 & B0	Vol. Adjustable	-
0	0	0	1	off	A0 & B0	Muted	Vol. Adjustable
0	0	1	0	on	A1 & B1	Vol. Adjustable	-
0	0	1	1	off	A1 & B1	Muted	Vol. Adjustable
0	1	X	0	on	A0 & B0	Vol. Adjustable	-
0	1	X	1	off	A1 & B1	Muted	Vol. Adjustable
1	X	X	X	muted	X	Muted	Muted

(1) If system beep is detected on the Beep In and the beep signal is fed to the inputs, the system beep will be passed through the bridged amplifier regardless of the logic of the Mute, HP sense, or DC Volume Control pins.

Copyright © 2002–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE MH/LQ SPECIFIC CHARACTERISTICS

LM4842MH/LQ THD+N vs Output Power

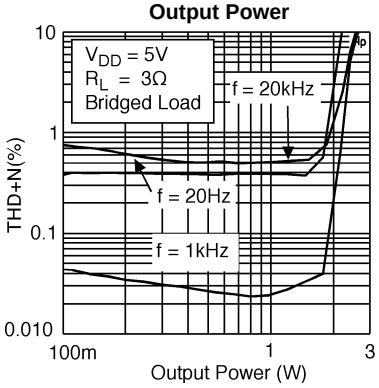


Figure 5.

LM4842MH/LQ THD+N vs Frequency

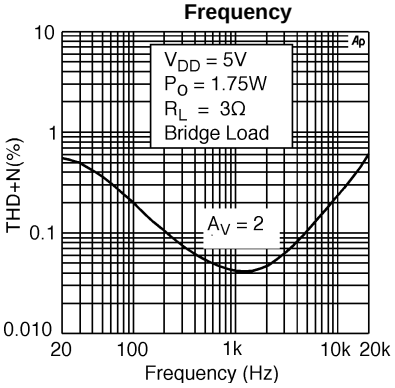


Figure 6.

LM4842MH/LQ THD+N vs Output Power

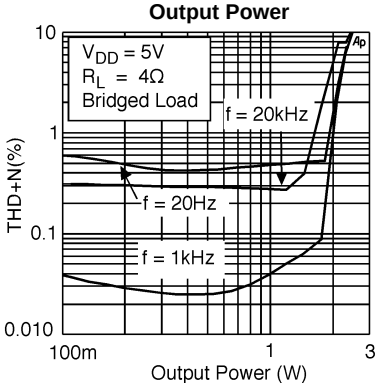


Figure 7.

LM4842MH/LQ THD+N vs Frequency

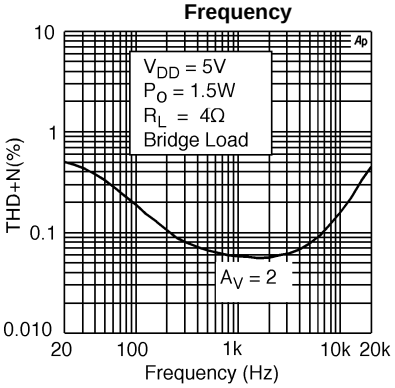


Figure 8.

LM4842MH/LQ Power Dissipation vs Output Power

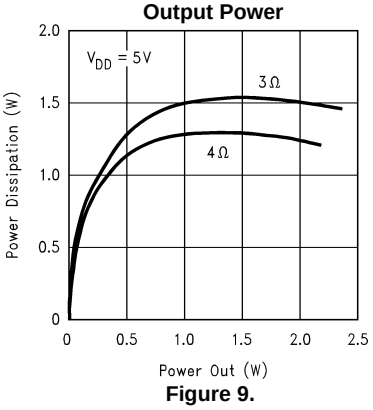


Figure 9.

LM4842MH/LQ Power Derating Curve (1)

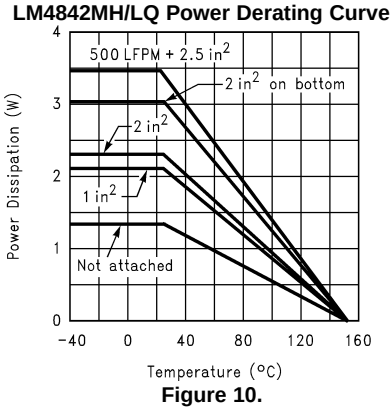


Figure 10.

(1) These curves show the thermal dissipation ability of the LM4842MH/LQ at different ambient temperatures given these conditions:
500LFPM + 2in^2: The part is soldered to a 2in^2, 1 oz. copper plane with 500 linear feet per minute of forced-air flow across it.
2in^{2}on bottom: The part is soldered to a 2in^2, 1oz. copper plane that is on the bottom side of the PC board through 21 8 mil vias.
2in^2: The part is soldered to a 2in^2, 1oz. copper plane.
1in^2: The part is soldered to a 1in^2, 1oz. copper plane.
Not Attached: The part is not soldered down and is not forced-air cooled.

Copyright © 2002–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE NON-MH/LQ SPECIFIC CHARACTERISTICS

THD+N vs Frequency

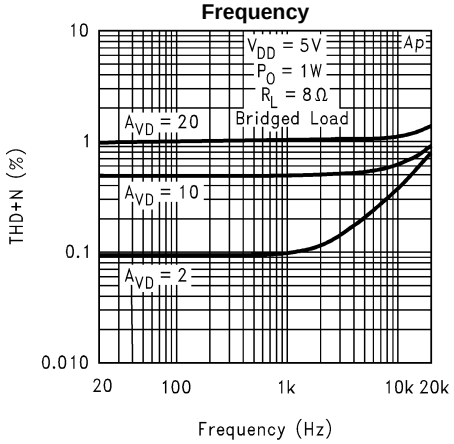


Figure 11.

THD+N vs Frequency

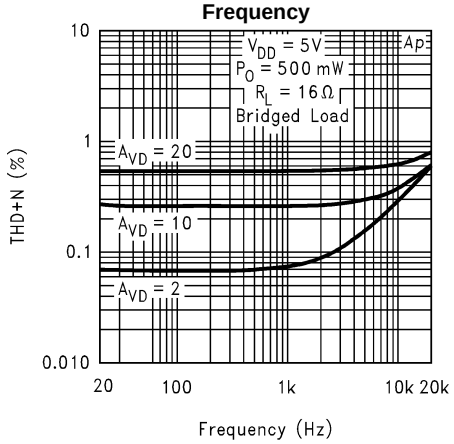


Figure 12.

THD+N vs Frequency

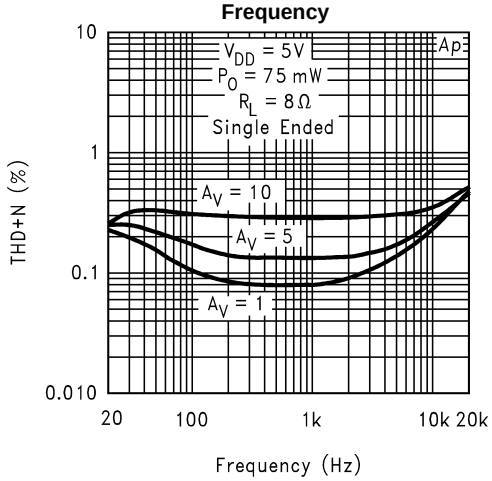


Figure 13.

THD+N vs Frequency

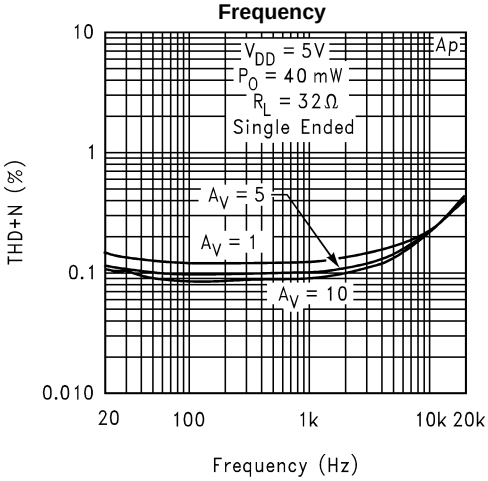


Figure 14.

THD+N vs Frequency

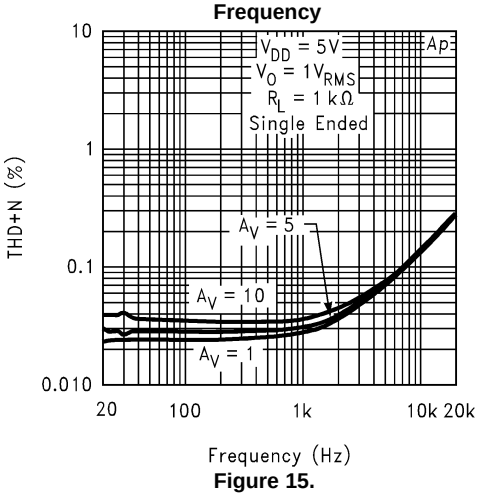


Figure 15.

THD+N vs Frequency

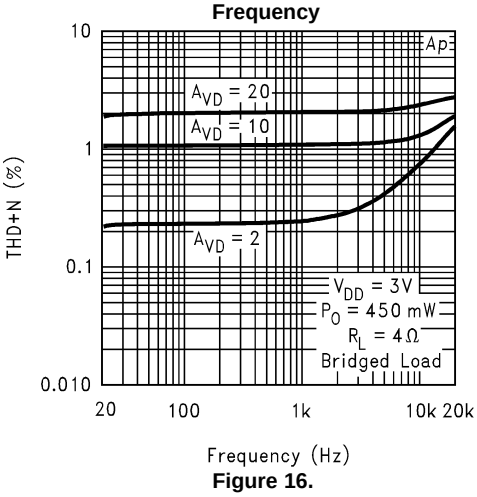


Figure 16.

TYPICAL PERFORMANCE NON-MH/LQ SPECIFIC CHARACTERISTICS (continued)

THD+N vs Frequency

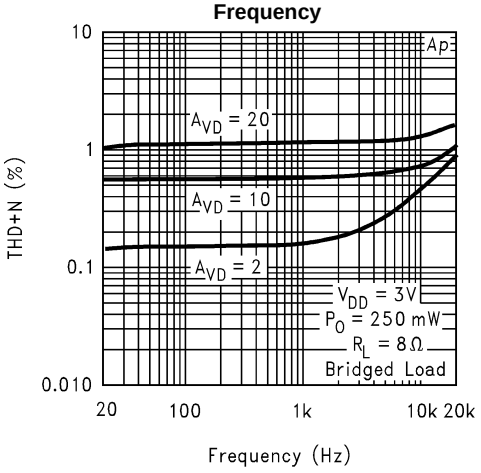


Figure 17.

THD+N vs Frequency

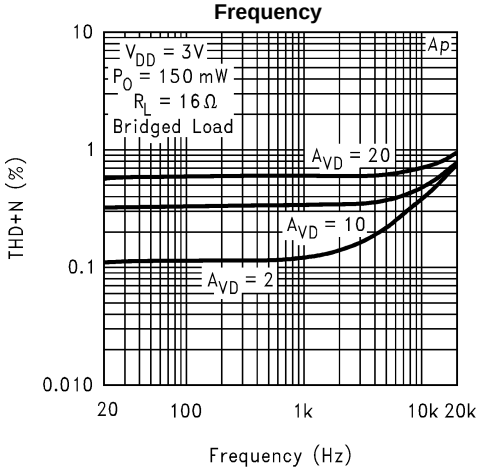


Figure 18.

THD+N vs Frequency

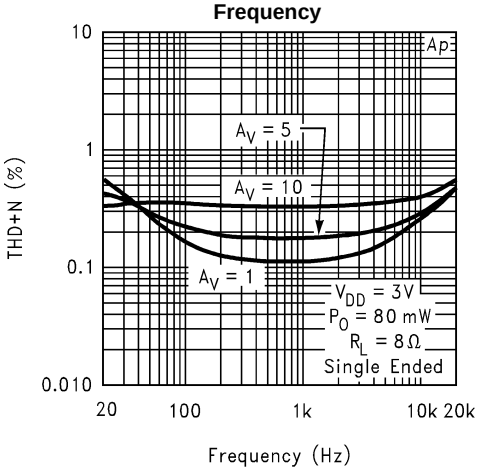


Figure 19.

THD+N vs Frequency

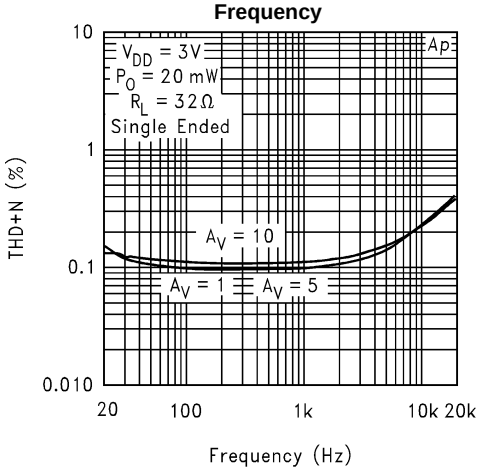


Figure 20.

THD+N vs Frequency

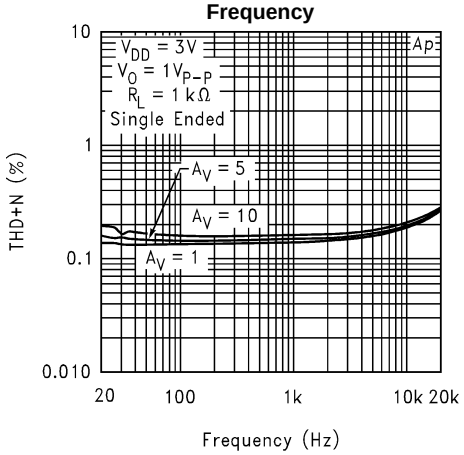


Figure 21.

THD+N vs Output Power

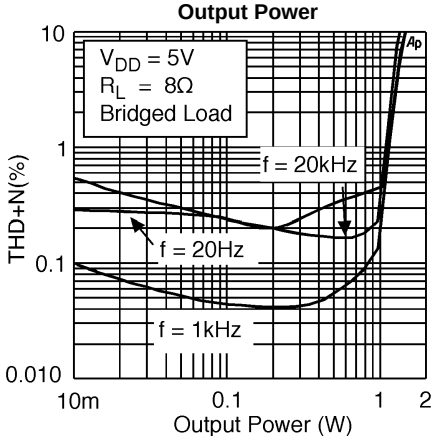


Figure 22.

Copyright © 2002–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE NON-MH/LQ SPECIFIC CHARACTERISTICS (continued)

THD+N vs Output Power

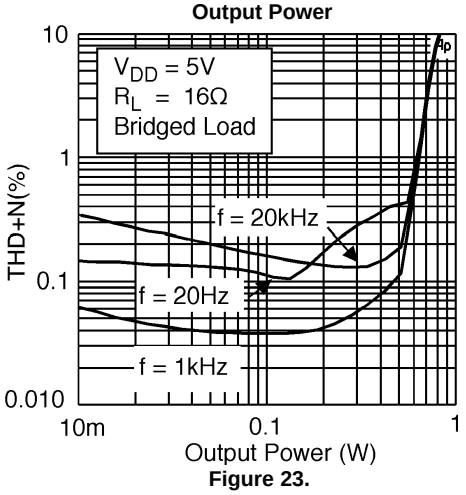


Figure 23.

THD+N vs Output Power

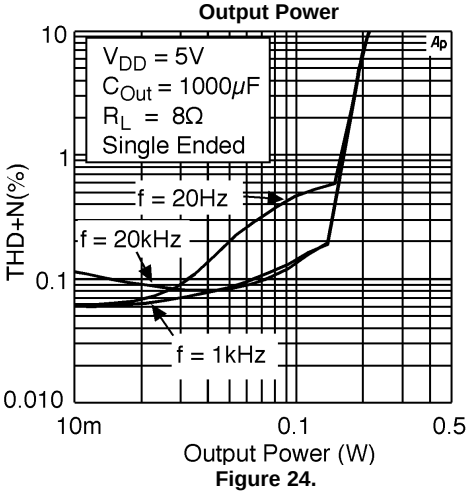


Figure 24.

THD+N vs Output Power

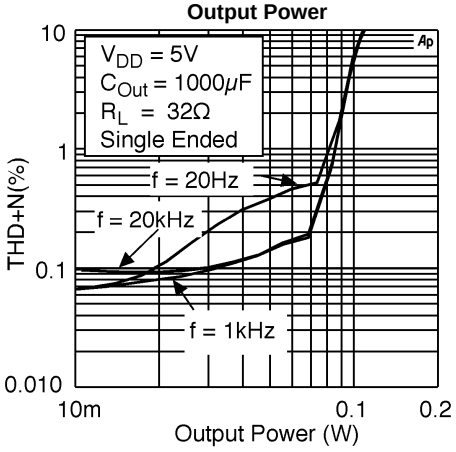


Figure 25.

THD+N vs Output Power

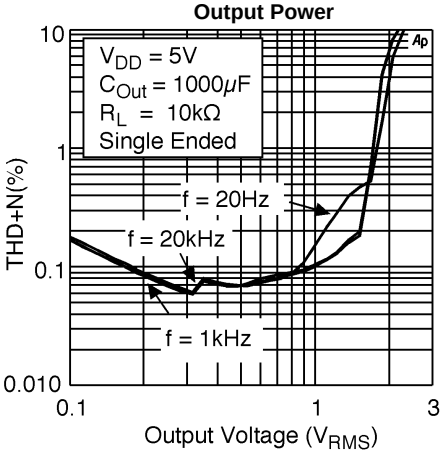


Figure 26.

THD+N vs Output Power

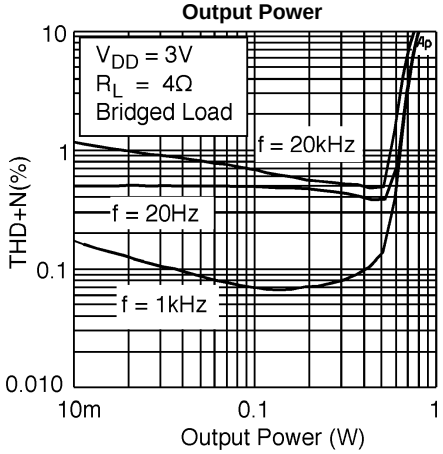


Figure 27.

THD+N vs Output Power

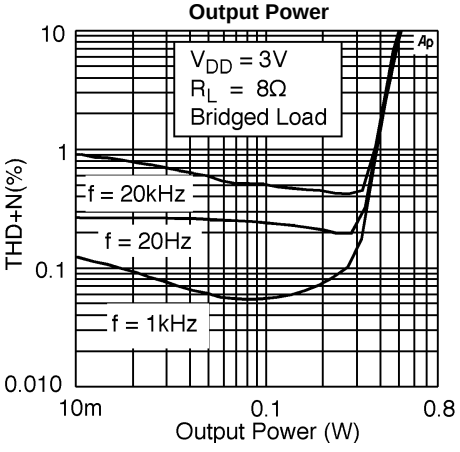


Figure 28.

Copyright © 2002–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE NON-MH/LQ SPECIFIC CHARACTERISTICS (continued)

THD+N vs Output Power

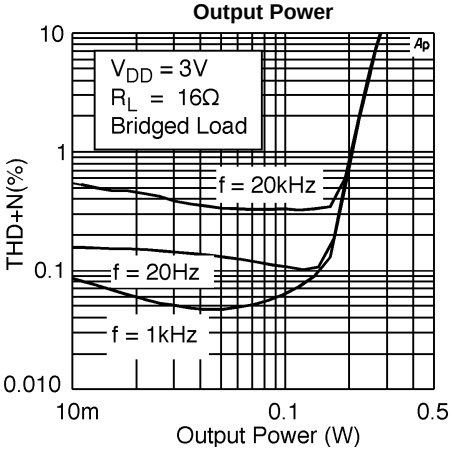


Figure 29.

THD+N vs Output Power

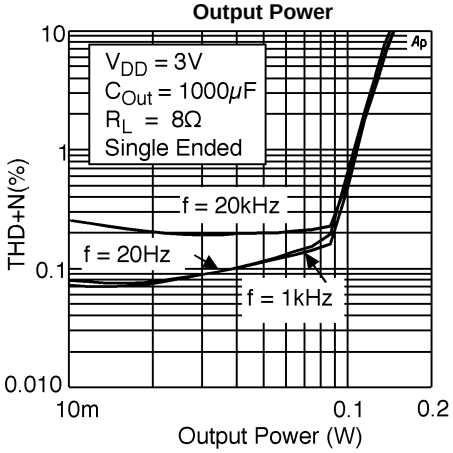


Figure 30.

THD+N vs Output Power

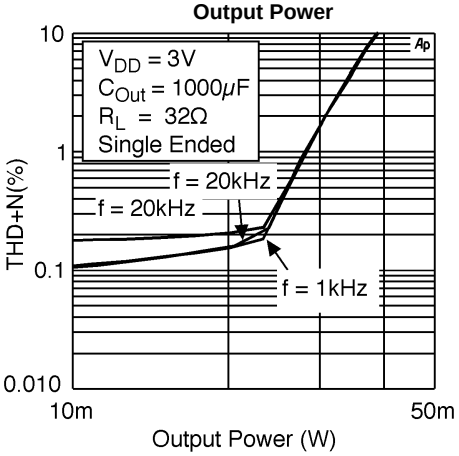


Figure 31.

THD+N vs Output Power

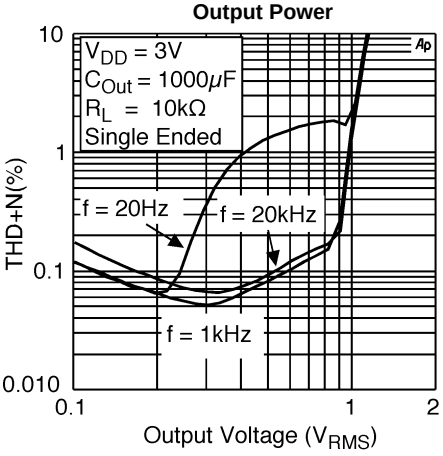


Figure 32.

THD+N vs Output Voltage Docking Station Pins

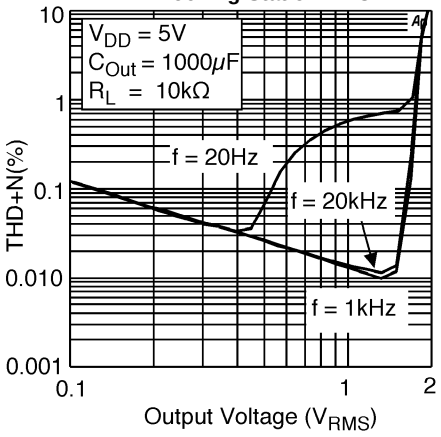


Figure 33.

THD+N vs Output Voltage Docking Station Pins

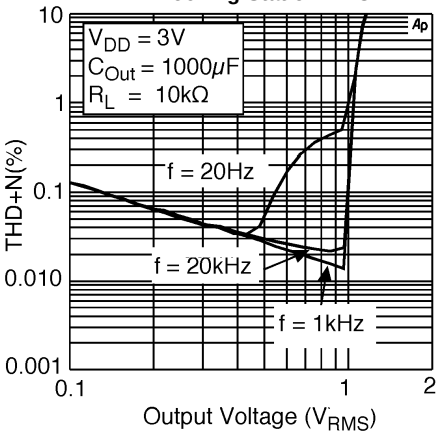


Figure 34.

Copyright © 2002–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE NON-MH/LQ SPECIFIC CHARACTERISTICS (continued)

Output Power vs Load Resistance

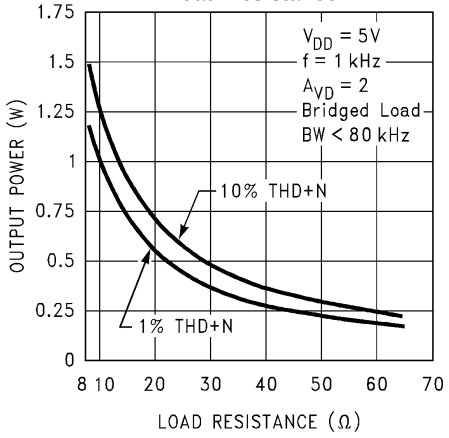


Figure 35.

Output Power vs Load Resistance

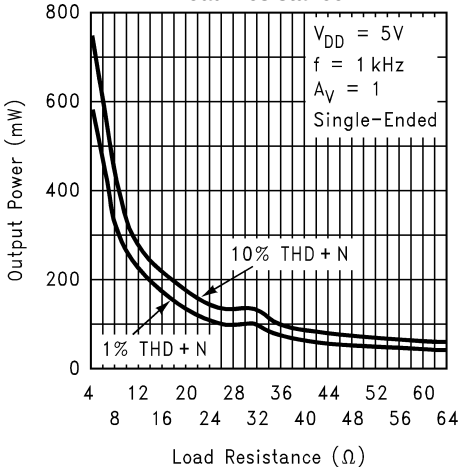


Figure 36.

Output Power vs Load Resistance

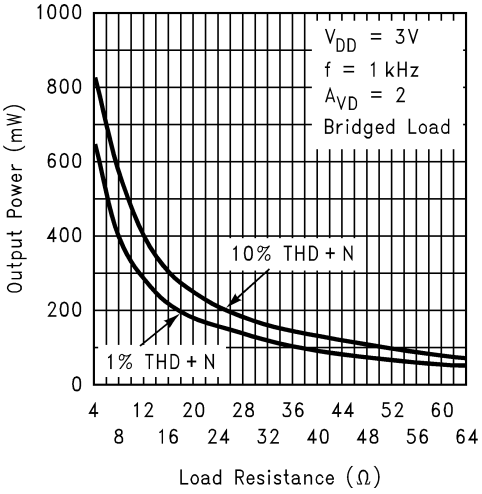


Figure 37.

Output Power vs Load Resistance

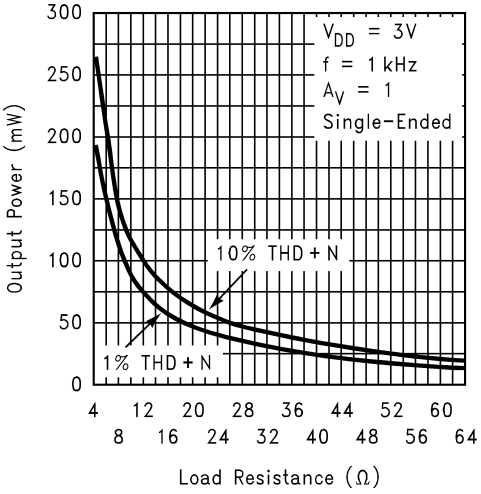


Figure 38.

Dropout Voltage

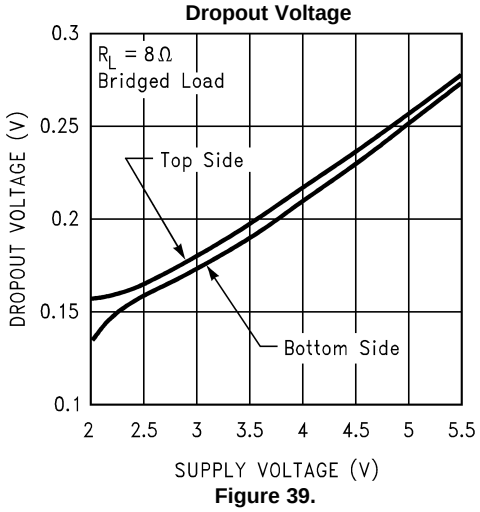


Figure 39.

Power Dissipation vs Output Power

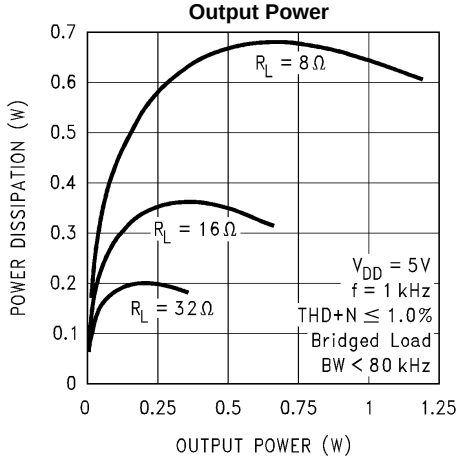


Figure 40.

Copyright © 2002–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE NON-MH/LQ SPECIFIC CHARACTERISTICS (continued)

Power Supply Rejection Ratio

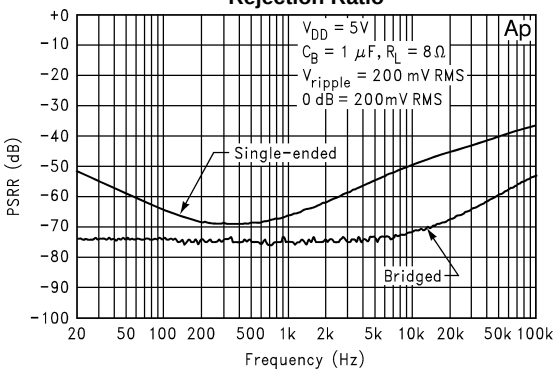


Figure 41.

Volume Control Characteristics

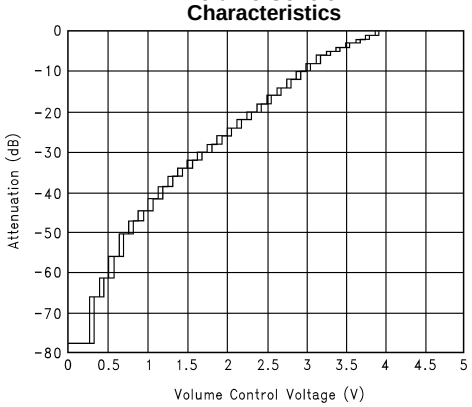


Figure 42.

Power Dissipation vs Output Power

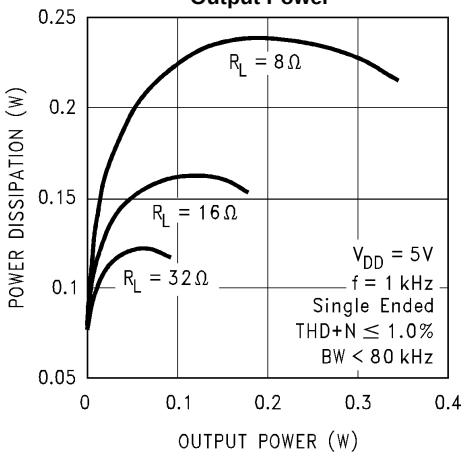


Figure 43.

External Gain/Bass Boost Characteristics

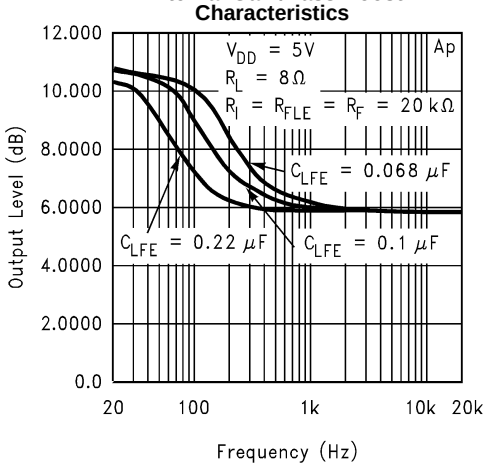


Figure 44.

Power Derating Curve

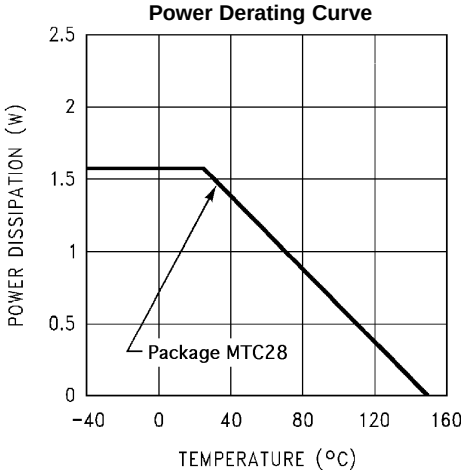


Figure 45.

Crosstalk

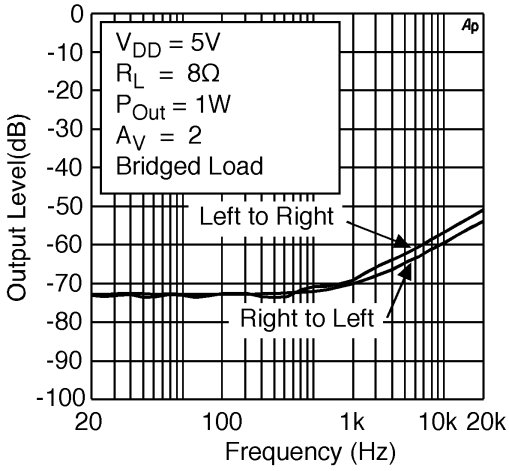


Figure 46.

Copyright © 2002–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE NON-MH/LQ SPECIFIC CHARACTERISTICS (continued)

Output Power vs Supply voltage

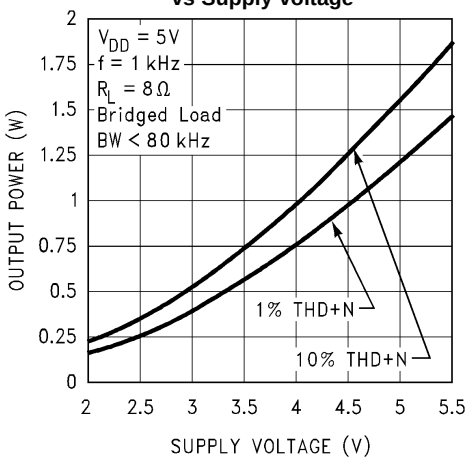


Figure 47.

Output Power vs Supply Voltage

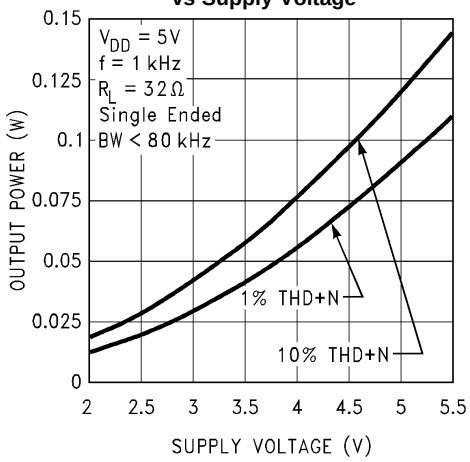


Figure 48.

Supply Current vs Supply Voltage

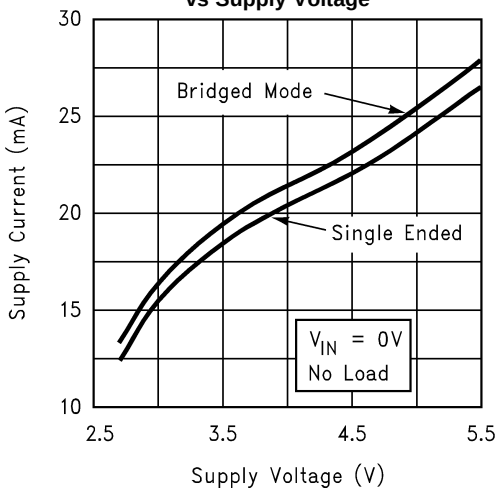


Figure 49.

APPLICATION INFORMATION

ELIMINATING OUTPUT COUPLING CAPACITORS

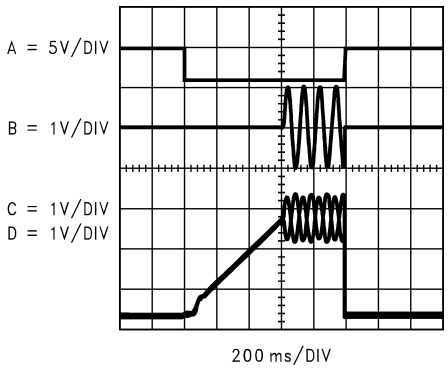
Typical single-supply audio amplifiers that can switch between driving bridge-tied-load (BTL) speakers and single-ended (SE) headphones use a coupling capacitor on each SE output. This capacitor blocks the half-supply voltage to which the output amplifiers are typically biased and couples the audio signal to the headphones. The signal return to circuit ground is through the headphone jack's sleeve.

The LM4842 eliminates these coupling capacitors. AmplifierA+ (pin 28 on MT/MH) is internally configured to apply $V_{DD}/2$ to a stereo headphone jack's sleeve. This voltage matches the quiescent voltage present on the AmpAout- and AmpBout- outputs that drive the headphones. The headphones operate in a manner very similar to a bridge-tied-load (BTL). The same DC voltage is applied to both headphone speaker terminals. This results in no net DC current flow through the speaker. AC current flows through a headphone speaker as an audio signal's output amplitude increases on the speaker's terminal.

When operating as a headphone amplifier, the headphone jack sleeve is not connected to circuit ground. Using the headphone output jack as a line-level output will place the LM4842's one-half supply voltage on a plug's sleeve connection. Driving a portable notebook computer or audio-visual display equipment is possible. This presents no difficulty when the external equipment uses capacitively coupled inputs. For the very small minority of equipment that is DC-coupled, the LM4842 monitors the current supplied by the amplifier that drives the headphone jack's sleeve. If this current exceeds $500mA_{PK}$, the amplifier is shutdown, protecting the LM4842 and the external equipment.

OUTPUT TRANSIENT ("POPS AND CLICKS") ELIMINATED

The LM4842 contains advanced circuitry that eliminates output transients ("pop and click"). This circuitry prevents all traces of transients when the supply voltage is first applied, when the part resumes operation after shutdown, or when switching between BTL speakers and SE headphones. Two circuits combine to eliminate pop and click. One circuit mutes the output when switching between speaker loads. Another circuit monitors the input signal. It maintains the muted condition until there is sufficient input signal magnitude (>$22mV_{RMS}$, typ) to mask any remaining transient that may occur. (See TURN ON CHARACTERISTICS).

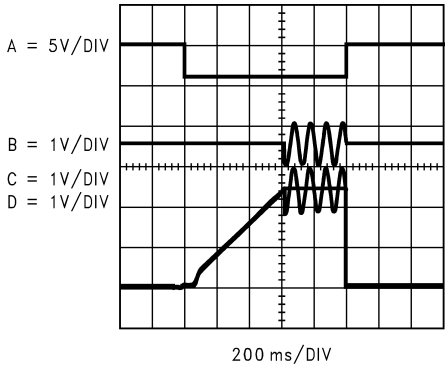


Differential output signal (Trace B) is devoid of transients. The SHUTDOWN pin is driven by a shutdown signal (Trace A). The inverting output (Trace C) and the non-inverting output (Trace D) are applied across an 8Ω BTL load.

Figure 50.

Figure 50 shows the LM4842's lack of transients in the differential signal (Trace B) across a BTL 8Ω load. The LM4842's active-high SHUTDOWN pin is driven by the logic signal shown in Trace A. Trace C is the VOUT- output signal and trace D is the VOUT+ output signal. The shutdown signal frequency is 1Hz with a 50% duty cycle. Figure 51 is generated with the same conditions except that the output drives a 32Ω single-ended (SE) load. Again, no trace of output transients on Trace B can be observed.

Copyright © 2002–2013, Texas Instruments Incorporated



Single-ended output signal (Trace B) is devoid of transients. The SHUTDOWN pin is driven by a shutdown signal (Trace A). The inverting output (Trace C) and the V_{BYPASS} output (Trace D) are applied across a 32Ω BTL load.

Figure 51.

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The LM4842's exposed-DAP (die attach paddle) package (MH,LQ) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air. The result is a low voltage audio power amplifier that produces 2.1W at ≤ 1% THD with a 4Ω load. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4842's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The MH and LQ packages must have their exposed DAPs soldered to a grounded copper pad on the PCB. The DAP's PCB copper pad is connected to a large grounded plane of continuous unbroken copper. This plane forms a thermal mass heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the DAP copper pad to the inner layer or backside copper heat sink area with 32(4x8) MH or 6(3x2) LQ vias. The via diameter should be 0.012in–0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plating-through and solder-filling the vias.

Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal 2.5in^2 (min) area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the LM4842MH and LQ packages should be 5in^2 (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25°C ambient temperature. Increase the area to compensate for ambient temperatures above 25°C. The junction temperature must be held below 150°C to prevent activating the LM4842's thermal shutdown protection. The LM4842's power de-rating curve in the TYPICAL PERFORMANCE MH/LQ SPECIFIC CHARACTERISTICS shows the maximum power dissipation versus temperature. Example PCB layouts for the exposed-DAP TSSOP and LQ packages are shown in the RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT section. Further detailed and specific information concerning PCB layout and fabrication is available in Texas Instrument's AN1187.

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 2.1W to 2.0W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Copyright © 2002–2013, Texas Instruments Incorporated

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 4, the LM4842 output stage consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. (Though the following discusses channel A, it applies equally to channel B.)

Figure 4 shows that the first amplifier's negative (-) output serves as the second amplifier's input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between −OUTA and +OUTA and driven differentially (commonly referred to as “bridge mode”). This results in a differential gain of

$$A_{VD} = 2 * (R_f/R_i) \quad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: **its differential output doubles the voltage swing across the load.** This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the AUDIO POWER AMPLIFIER DESIGN section.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \quad \text{Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The LM4842 has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation 3, assuming a 5V power supply and a 4Ω load, the maximum single channel power dissipation is 1.27W or 2.54W for stereo operation.

$$P_{DMAX} = 4 * (V_{DD})^2/(2\pi^2 R_L) \quad \text{Bridge Mode} \quad (3)$$

The LM4842's power dissipation is twice (2 channels) that given by Equation 2 or Equation 3 when operating in the single-ended mode or bridge mode, respectively. Twice the maximum power dissipation point given by Equation 3 must not exceed the power dissipation given by Equation 4:

$$P_{DMAX}' = (T_{JMAX} - T_A)/\theta_{JA} \quad (4)$$

The LM4842's T_{JMAX} = 150°C. In the LQ package soldered to a DAP pad that expands to a copper area of 5in^2 on a PCB, the LM4842's θ_{JA} = 20°C/W. In the MH and LQ packages soldered to a DAP pad that expands to a copper area of 2in^2 on a PCB, the LM4842MH's and LQ's θ_{JA} is 41°C/W. For the LM4842MT package, θ_{JA} = 80°C/W. At any given ambient temperature T_A, use Equation 4 to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 4 and substituting P_{DMAX} for P_{DMAX}' results in Equation 5. This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4842's maximum junction temperature.

$$T_A = T_{JMAX} - 2*P_{DMAX}\,\theta_{JA} \quad (5)$$

Copyright © 2002–2013, Texas Instruments Incorporated

For a typical application with a 5V power supply and an 4Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 45°C for the MH package.

$$T_{JMAX} = P_{DMAX}\,\theta_{JA} + T_A \quad (6)$$

Equation 6 gives the maximum junction temperature T_{JMAX}. If the result violates the LM4842's 150°C T_{JMAX}, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation 2 is greater than that of Equation 3, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance.) Refer to the TYPICAL PERFORMANCE MH/LQ SPECIFIC CHARACTERISTICS curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitor to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the LM4842's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation. Keep the length of leads and traces that connect capacitors between the LM4842's power supply pin and ground as short as possible. Connecting a 1µF capacitor, C_{BYPASS}, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large a capacitor, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially C_{BYPASS}, depends on desired PSRR requirements, click and pop performance (as explained in the section, PROPER SELECTION OF EXTERNAL COMPONENTS), system cost, and size constraints.

PROPER SELECTION OF EXTERNAL COMPONENTS

Optimizing the LM4842's performance requires properly selecting external components. Though the LM4842 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The LM4842 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain circuits demand input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to the AUDIO POWER AMPLIFIER DESIGN section for more information on selecting the proper gain.

INPUT CAPACITOR VALUE SELECTION

Amplifying the lowest audio frequencies requires a high value input coupling capacitor (0.33µF in Figure 3). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using a large input capacitor.

Copyright © 2002–2013, Texas Instruments Incorporated

Besides effecting system cost and size, the input coupling capacitor has an affect on the LM4842's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually $V_{DD}/2$) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistor, R_f. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −3dB frequency.

As shown in Figure 1, the input resistors (RIN = 20K) and the input capacitors (CIN = 0.33µF) produce a −6dB high pass filter cutoff frequency that is found using Equation 7.

$$f_{-6\,dB} = \frac{1}{2\pi R_{IN} C_{IN}} \quad (7)$$

As an example when using a speaker with a low frequency limit of 150Hz, the input coupling capacitor using Equation 7, is 0.053µF. The 0.33µF input coupling capacitor shown in Figure 3 allows the LM4842 to drive high efficiency, full range speaker whose response extends below 30Hz.

TURN ON CHARACTERISTICS

The LM4842 contains advanced circuitry that minimizes turn-on and shutdown transients or “clicks and pops”. For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. While the power supply is ramping to its final value, the LM4842's internal amplifiers are configured as unity gain buffers. An internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the BYPASS pin reaches 1/2 V_{DD}. As soon as the voltage on the BYPASS pin is stable, the LM4842 is ready to be fully turned on. To turn the device on, the input signal must exceed $22mV_{rms}$. This is accomplished through a threshold detect circuit that enables all appropriate output amplifiers after the 22mVrms limit is reached. Until this threshold is reached, some of the amplifiers remain in a tri-state mode. This insures that there is no current flowing through to the speakers or headphones during power up. Without current flow, the speakers or headphones remain silent. During headphone mode, A+, B-, and B+ are in tri-state mode during power up. During speaker mode, A+ and B+ are in tri-state mode during power up.

Although the BYPASS pin current cannot be modified, changing the size of C_{BYPASS} alters the device's turn-on time. As the size of C_{BYPASS} increases, the turn-on time increases. There is a linear relationship between the size of C_{BYPASS} and the turn-on time. Here are some typical turn-on times for various values of C_{BYPASS}:

C_{BYPASS}	T_{ON}
0.01µF	2ms
0.1µF	20ms
0.22µF	44ms
0.47µF	94ms
1.0µF	200ms

DOCKING STATION INTERFACE

Applications such as notebook computers can take advantage of a docking station to connect to external devices such as monitors or audio/visual equipment that sends or receives line level signals. The LM4842 has two outputs, Dock A and Dock B, which connect to outputs of the internal input amplifiers that drive the volume control inputs. These input amplifiers can drive loads of >1kΩ (such as powered speakers) with a rail-to-rail signal. Since the output signal present on the Dock A and Dock B pins are biased to $V_{DD}/2$, coupling capacitors should be connected in series with the load when using these outputs. Typical values for the output coupling capacitors are 0.33µF to 1.0µF. If polarized coupling capacitors are used, connect their "+" terminals to the respective output pin.

Since the Dock outputs precede the internal volume control, the signal amplitude will be equal to the input signal's magnitude and cannot be adjusted. However, the input amplifier's closed-loop gain can be adjusted using external resistors. These 20k resistors (R_{FA} and R_{FB}) are shown in Figure 4 and they set each input amplifier's gain to -1. Use Equation 7 to determine the input and feedback resistor values for a desired gain.

Copyright © 2002–2013, Texas Instruments Incorporated

$$- A_v = R_F / R_{IN} \quad (8)$$

Adjusting the input amplifier's gain sets the minimum gain for that channel. Although the single ended output of the Bridge Output Amplifiers can be used to drive line level outputs, it is recommended that the A & B Dock Outputs simpler signal path be used for better performance.

MUX CONTROL AND MODE PINS

The LM4842 has two pairs of stereo inputs. The MUX CONTROL pin determines which of these stereo pairs of inputs are active. Applying 0V to the MUX CONTROL pin (with the Mode pin tied low) selects inputs A0 and B0. Applying V_{DD} to the MUX CONTROL (with the Mode pin tied low) pin selects inputs A1 and B1 (See Truth Table for Logic Inputs).

When the Mode pin is pulled high the MUX Control is disabled and the Headphone Sense Pin controls the A and B input pairs as follows:

- Headphone Sense enabled (Headphone plugged in) selects inputs A1 and B1.
- Headphone Sense disabled (Headphone not plugged in) selects inputs A0 and B0.

When the MODE pin is high the HP SENSE controls the MUX inputs. This configuration can be very useful, for example, when the headphone acoustic output needs to be much lower than the BTL Speaker Output. Two different gains can be hardwired into the two pairs of MUX input circuits. This allows the user to have the HP SENSE automatically change the output level for either of the MUX input pairs by switching between the two pairs of MUX inputs, if the same input signal is connected to both MUX inputs.

When the MODE pin is low the MUX pin switches the MUX input pairs directly.

BEEP DETECT FUNCTION

Computers and notebooks produce a system "beep" signal that drives a small speaker. The speaker's auditory output signifies that the system requires user attention or input. To accommodate this system alert signal, the LM4842's beep input pin is a mono input that accepts the beep signal. Internal level detection circuitry at this input monitors the beep signal's magnitude. When a signal level greater than $V_{DD}/2$ is detected on the BEEP IN pin, the bridge output amplifiers are enabled. The beep signal is amplified and applied to the load connected to the output amplifiers. A valid beep signal will be applied to the load even when MUTE is active. Use the input resistors connected between the BEEP IN pin and the stereo input pins to accommodate different beep signal amplitudes. These resistors are shown as 200kΩ devices in Figure 3. Use higher value resistors to reduce the gain applied to the beep signal. The resistors must be used to pass the beep signal to the stereo inputs. The BEEP IN pin is used only to detect the beep signal's magnitude: it does not pass the signal to the output amplifiers. The LM4842's shutdown mode must be deactivated before a system alert signal is applied to the BEEP IN pin.

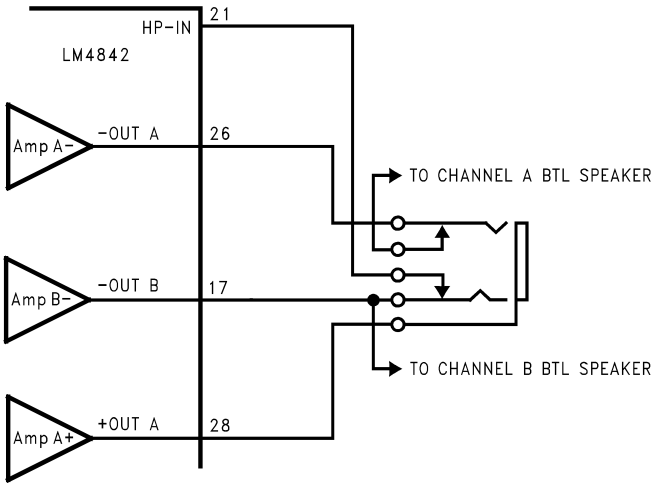


Figure 52. Headphone Sensing Circuit

CAP-LESS HEADPHONE (SINGLE-ENDED) AMPLIFIER OPERATION

An internal pull−up circuit is connected to the HP Sense (Pin 21 HP-IN on the MT/MH packages) headphone amplifier control pin. When this pin is left unconnected, V_{DD} is applied to the HP−IN. This turns off Amp B +OUT (not seen in Figure 52, see Figure 4 Pin 15) and switches Amp A +OUT's input signal from an audio signal to the $V_{DD}/2$ voltage present on pin 28 (Amp A + OUT). The result is muted bridge-connected loads. Quiescent current consumption is reduced when the IC is in this single−ended mode.

Figure 52 above shows the implementation of the LM4842's headphone control function. An internal comparator with a nominal 400mV offset monitors the signal present at the −OUT B output. It compares this signal against the signal applied to the HP−IN pin (Notice in Figure 52, Pin 21 is shorted to Pin 17 without a headphone plugged in). When these signals are equal, as in the case when a BTL is connected to the amplifier, an internal comparator forces the LM4842 to maintain bridged−amplifier operation. When the HP−IN pin is externally floated, such as when headphones are connected to the jack shown in Figure 52, an internal pull−up forces V_{DD} on the internal comparator's HP−IN inputs. This changes the comparator's output state and enables the headphone function: it turns off Amp B +OUT (not seen in Figure 52, see Figure 4 Pin 15), switches the Amp A +OUT input signal from an audio signal to the $V_{DD}/2$ DC voltage present on pin 28, and mutes the bridge-connected loads. Amp A -OUT and Amp B -OUT drive the headphones.

Figure 4 and Figure 53 also show suggested headphone jack electrical connections. The jack is designed to mate with a three−wire plug. The plug's tip and ring should each carry one of the two stereo output signals, whereas the sleeve provides the return to Amp A +OUT. A headphone jack with one control pin contact is sufficient to drive the HP−IN pin when connecting headphones.

A switch can replace the headphone jack contact pin. When a switch shorts the HP−IN pin to V_{DD} (An open switch contact will accomplish this because there is an internal pull-up resistor), the bridge−connected speakers are muted and Amp A -OUT and Amp B -OUT drive the stereo headphones. When a switch shorts the HP−IN pin to GND (pulling down the internal pull-up resistor), the LM4842 operates in bridge mode. If headphone drive is not needed, short the HP−IN pin to the −OUTB pin.

Figure 53 shows an optional resistor connected between the amplifier output that drives the headphone jack sleeve and ground. This resistor provides a ground path that suppresses power supply hum. This hum may occur in applications such as notebook computers in a shutdown condition and connected to an external powered speaker. The resistor's 100Ω value is a suggested starting point. Its final value must be determined based on the tradeoff between the amount of noise suppression that may be needed and minimizing the additional current drawn by the resistor (25mA for a 100Ω resistor and a 5V supply).

MUTE FUNCTION

The LM4842 mutes the amplifier and DOCK outputs when V_{DD} is applied to the MUTE pin. Even while muted, the LM4842 will amplify a system alert (beep) signal whose magnitude satisfies the BEEP DETECT circuitry. Applying 0V to the MUTE pin returns the LM4842 to normal, unmuted operation. Prevent unanticipated mute behavior by connecting the MUTE pin to V_{DD} or ground. Do not let the mute pin float.

MICRO-POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the LM4842's shutdown function. Activate micro-power shutdown by applying ground (logic low) to the SHUTDOWN pin. When activated, the LM4842's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. On the demo board, the micro-power shutdown feature is controlled by a single pole switch that connects the shutdown pin to either V_{DD}, for normal operation, or directly to ground to enable shutdown. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin.

BASS BOOST

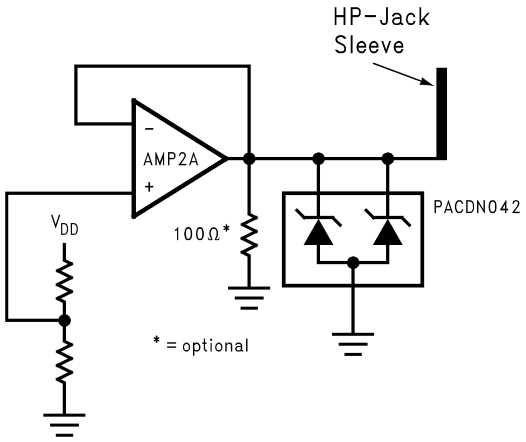
The "Bass Boost Mode" is enabled whenever the LM4842 is NOT in headphone mode (please refer to the " Cap-less Headphone" description in the previous section for headphone on/off conditions). In BTL output mode, the Bass Boost feature is enabled and the low frequency gain of the A and B Channel amplifiers can be set by installing the external bass boost capacitors, C_{BA} across pins 25 and 26 and C_{BB} across pins 17 and 18, as shown in Figure 4 (MT/MH package pin numbers). If the Bass Boost feature is not desired, then the capacitors can be left out of the circuit. When the capacitors are installed and the bass boost is enabled, the output amplifiers will be internally set at a gain of 4 in bridged mode, as shown in Figure 4. At low frequencies, C_{BA} and C_{BB} will be virtual open circuits and have no effect on the overall gain of the circuit. However at higher

Copyright © 2002–2013, Texas Instruments Incorporated

frequencies, the capacitors will be virtual short circuits and this will cause the gain of the bridge amplifiers to be reduced from a gain of 4 to a gain of 2. An example of actual values for this circuit are as follows: a first order pole is formed with a corner frequency at: fc = 1/(2π10kΩ C_{BA}) (9) With C_{BA} = 0.1µF, which results in a corner frequency of 160Hz. This bass boost feature can be useful in systems where speakers are housed in small enclosures and require a little more acoustic output at lower frequencies to make the sound more natural and balanced.

ESD PROTECTION

As stated in the Absolute Maximum Ratings, pin 28 on the MT and MH packages have a maximum ESD susceptibility rating of 6500V. For higher ESD voltages, the addition of an PACDN042 dual transil (from California Micro Devices), as shown in Figure 53, will provide additional protection.



The PCDN042 provides additional ESD protection beyond the 6500V shown in the Absolute Maximum Ratings for the AMP2A output

Figure 53.

DC VOLUME CONTROL

The LM4842 has an internal stereo volume control whose setting is a function of the DC voltage applied to the DC VOL CONTROL pin.

The LM4842 volume control consists of 31 steps that are individually selected by a variable DC voltage level on the volume control pin. The range of the steps, controlled by the DC voltage, are from 0dB - 78dB. Each gain step corresponds to a specific input voltage range, as shown in VOLUME CONTROL TABLE.

To minimize the effect of noise on the volume control pin, which can affect the selected gain level, hysteresis has been implemented. The amount of hysteresis corresponds to half of the step width, as shown in Figure 42 (DS200133-40).

For highest accuracy, the voltage shown in the 'recommended voltage' column of the table is used to select a desired gain. This recommended voltage is exactly halfway between the two nearest transitions to the next highest or next lowest gain levels.

The gain levels are 1dB/step from 0dB to -6dB, 2dB/step from -6dB to -36dB, 3dB/step from -36dB to -47dB, 4dB/step from -47db to -51dB, 5dB/step from -51dB to -66dB, and 12dB to the last step at -78dB.

Copyright © 2002–2013, Texas Instruments Incorporated

VOLUME CONTROL TABLE

Gain (dB)	Voltage Range (% of Vdd)			Voltage Range (Vdd = 5)			Voltage Range (Vdd = 3)		
	Low	High	Recommended	Low	High	Recommended	Low	High	Recommended
0	77.5%	100.00%	100.000%	3.875	5.000	5.000	2.325	3.000	3.000
-1	75.0%	78.5%	76.875%	3.750	3.938	3.844	2.250	2.363	2.306
-2	72.5%	76.25%	74.375%	3.625	3.813	3.719	2.175	2.288	2.231
-3	70.0%	73.75%	71.875%	3.500	3.688	3.594	2.100	2.213	2.156
-4	67.5%	71.25%	69.375%	3.375	3.563	3.469	2.025	2.138	2.081
-5	65.0%	68.75%	66.875%	3.250	3.438	3.344	1.950	2.063	2.006
-6	62.5%	66.25%	64.375%	3.125	3.313	3.219	1.875	1.988	1.931
-8	60.0%	63.75%	61.875%	3.000	3.188	3.094	1.800	1.913	1.856
-10	57.5%	61.25%	59.375%	2.875	3.063	2.969	1.725	1.838	1.781
-12	55.0%	58.75%	56.875%	2.750	2.938	2.844	1.650	1.763	1.706
-14	52.5%	56.25%	54.375%	2.625	2.813	2.719	1.575	1.688	1.631
-16	50.0%	53.75%	51.875%	2.500	2.688	2.594	1.500	1.613	1.556
-18	47.5%	51.25%	49.375%	2.375	2.563	2.469	1.425	1.538	1.481
-20	45.0%	48.75%	46.875%	2.250	2.438	2.344	1.350	1.463	1.406
-22	42.5%	46.25%	44.375%	2.125	2.313	2.219	1.275	1.388	1.331
-24	40.0%	43.75%	41.875%	2.000	2.188	2.094	1.200	1.313	1.256
-26	37.5%	41.25%	39.375%	1.875	2.063	1.969	1.125	1.238	1.181
-28	35.0%	38.75%	36.875%	1.750	1.938	1.844	1.050	1.163	1.106
-30	32.5%	36.25%	34.375%	1.625	1.813	1.719	0.975	1.088	1.031
-32	30.0%	33.75%	31.875%	1.500	1.688	1.594	0.900	1.013	0.956
-34	27.5%	31.25%	29.375%	1.375	1.563	1.469	0.825	0.937	0.881
-36	25.0%	28.75%	26.875%	1.250	1.438	1.344	0.750	0.862	0.806
-39	22.5%	26.25%	24.375%	1.125	1.313	1.219	0.675	0.787	0.731
-42	20.0%	23.75%	21.875%	1.000	1.188	1.094	0.600	0.712	0.656
-45	17.5%	21.25%	19.375%	0.875	1.063	0.969	0.525	0.637	0.581
-47	15.0%	18.75%	16.875%	0.750	0.937	0.844	0.450	0.562	0.506
-51	12.5%	16.25%	14.375%	0.625	0.812	0.719	0.375	0.487	0.431
-56	10.0%	13.75%	11.875%	0.500	0.687	0.594	0.300	0.412	0.356
-61	7.5%	11.25%	9.375%	0.375	0.562	0.469	0.225	0.337	0.281
-66	5.0%	8.75%	6.875%	0.250	0.437	0.344	0.150	0.262	0.206
-78	0.0%	6.25%	0.000%	0.000	0.312	0.000	0.000	0.187	0.000

AUDIO POWER AMPLIFIER DESIGN

AUDIO AMPLIFIER DESIGN: DRIVING 1W INTO AN 8Ω LOAD

The following are the desired operational parameters:

Power Output:	1 W_{RMS}
Load Impedance:	8Ω
Input Level:	1 V_{RMS}
Input Impedance:	20 kΩ
Bandwidth:	100 Hz−20 kHz ± 0.25 dB

Copyright © 2002–2013, Texas Instruments Incorporated

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs Supply Voltage curve in the TYPICAL PERFORMANCE MH/LQ SPECIFIC CHARACTERISTICS section. Another way, using Equation 9, is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs Supply Voltage in the TYPICAL PERFORMANCE MH/LQ SPECIFIC CHARACTERISTICS curves, must be added to the result obtained by Equation 9. The result is Equation 10.

$$V_{outpeak} = \sqrt{(2R_L P_O)} \quad (9)$$

$$V_{DD} \geq (V_{OUTPEAK} + (V_{ODTOP} + V_{ODBOT})) \quad (10)$$

The Output Power vs Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.6V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the LM4842 to produce peak output power in excess of 1W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates of maximum power dissipation as explained above in the POWER DISSIPATION section.

After satisfying the LM4842's power dissipation requirements, the minimum differential gain needed to achieve 1W dissipation in an 8Ω load is found using Equation 11.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (11)$$

Thus, a minimum overall gain of 2.83 allows the LM4842's to reach full output swing and maintain low noise and THD+N performance.

The last step in this design example is setting the amplifier's −3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are shown below:

$$f_L = 100Hz/5 = 20Hz \quad (12)$$

and

$$f_H = 20kHz \times 5 = 100kHz \quad (13)$$

As mentioned in the PROPER SELECTION OF EXTERNAL COMPONENTS section, R_i (Right & Left) and C_i (Right & Left) create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation 14.

$$C_i \geq 1/(2\pi R_i f_L) \quad (14)$$

The result is

$$1/(2\pi * 20k\Omega * 20Hz) = 0.397\mu F \quad (15)$$

Use a 0.39µF capacitor, the closest standard value.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain A_{VD}, determines the upper passband response limit. With A_{VD} = 3 and f_H = 100kHz, the closed-loop gain bandwidth product (GBWP) is 300kHz. This is less than the LM4842's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance,restricting bandwidth limitations.

RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

Figure 54 through Figure 56 show the recommended 2 later PC board layout that is optimized for the MT/MH packaged LM4842 and associated external components. Figure 57 through Figure 59 show the recommended 2 layer PC board layout that is optimized for the LQ packaged LM4842 and associated external components. These circuits are designed for use with an external 5V supply and 4Ω or 8Ω speakers.

These circuit boards are easy to use. Apply 5V and ground to the board's V_{DD} and GND pads, respectively. Connect 4Ω or 8Ω speakers between the board's −OUTA and +OUTA and OUTB and +OUTB pads.

Copyright © 2002–2013, Texas Instruments Incorporated

RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT - MH/MT PACKAGES

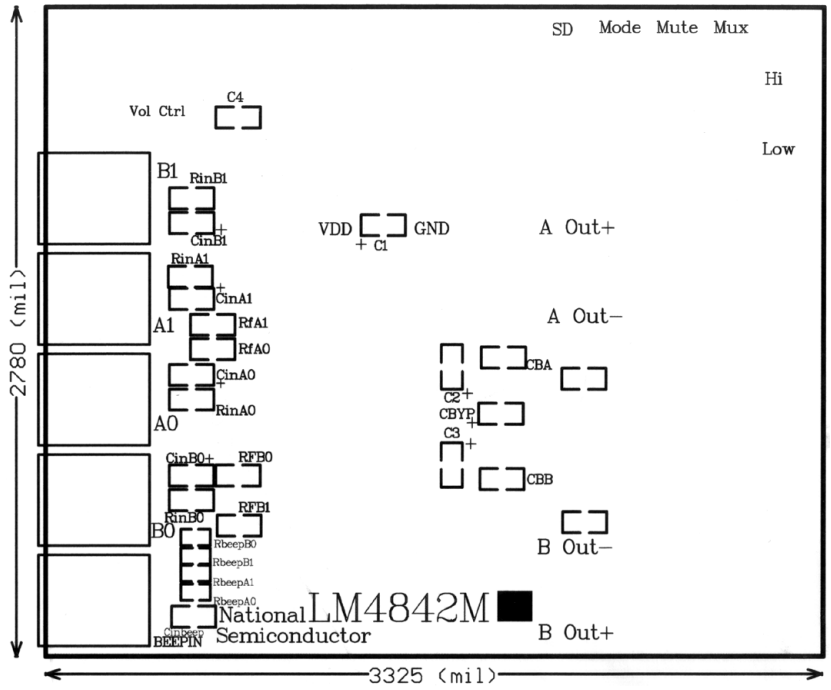


Figure 54. Top Layer SilkScreen - (Not to Scale)

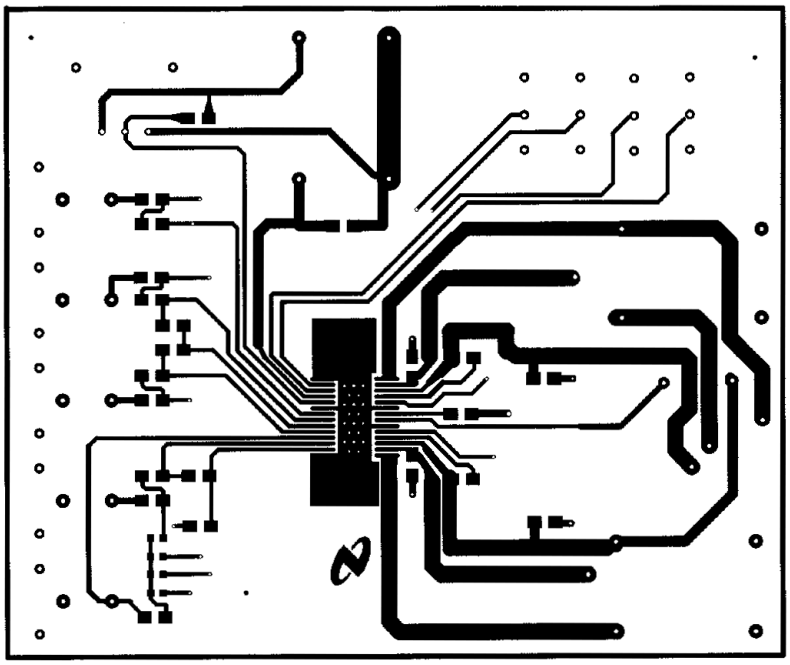


Figure 55. Top Layer - (Not to Scale)

Copyright © 2002–2013, Texas Instruments Incorporated

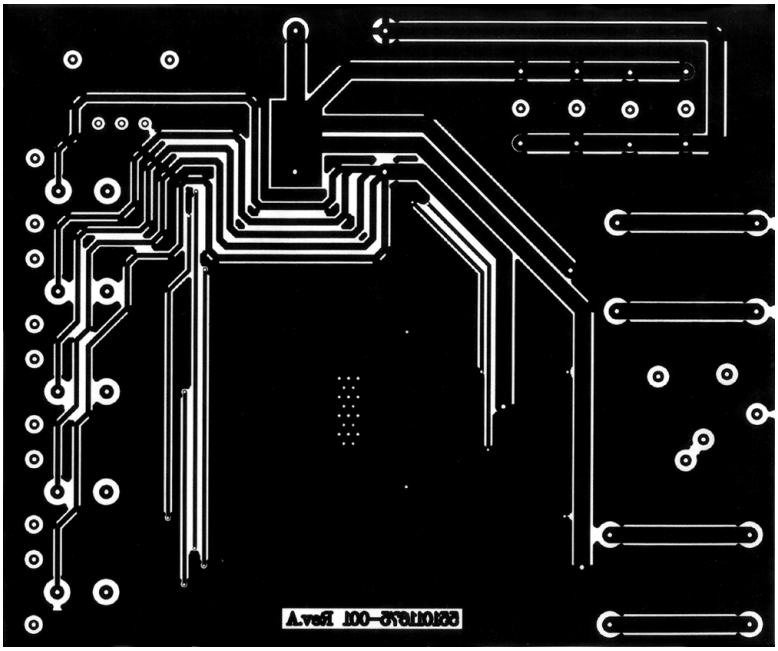


Figure 56. Bottom Layer - (Not to Scale)

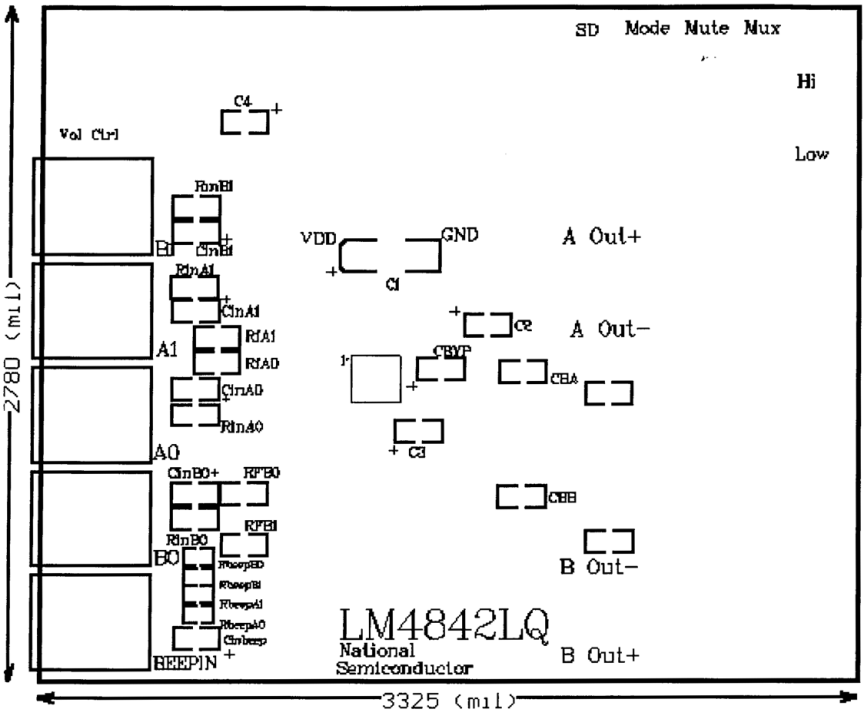


Figure 57. Top Layer SilkScreen - (Not to Scale)

RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT - LQ PACKAGE

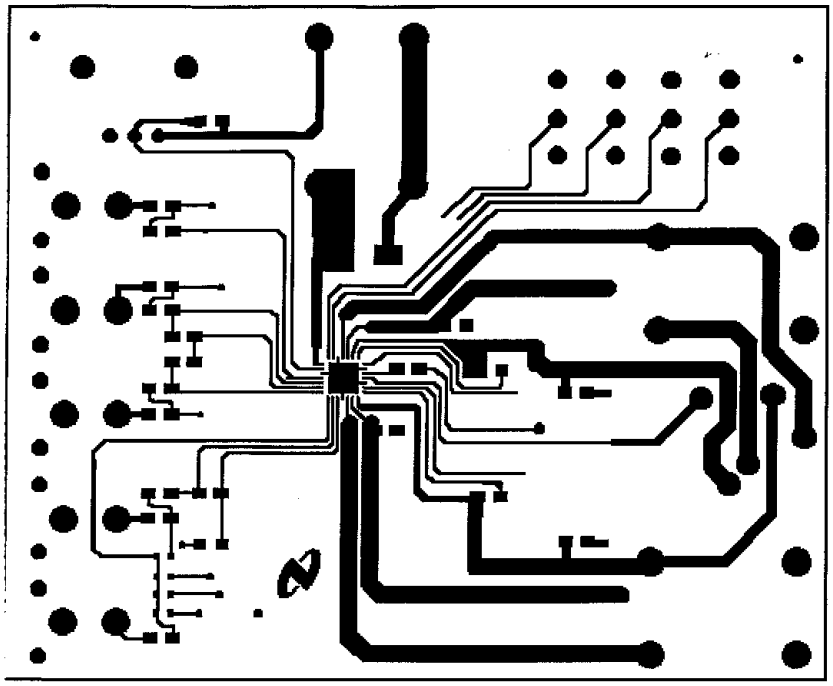


Figure 58. Top Layer - (Not to Scale)

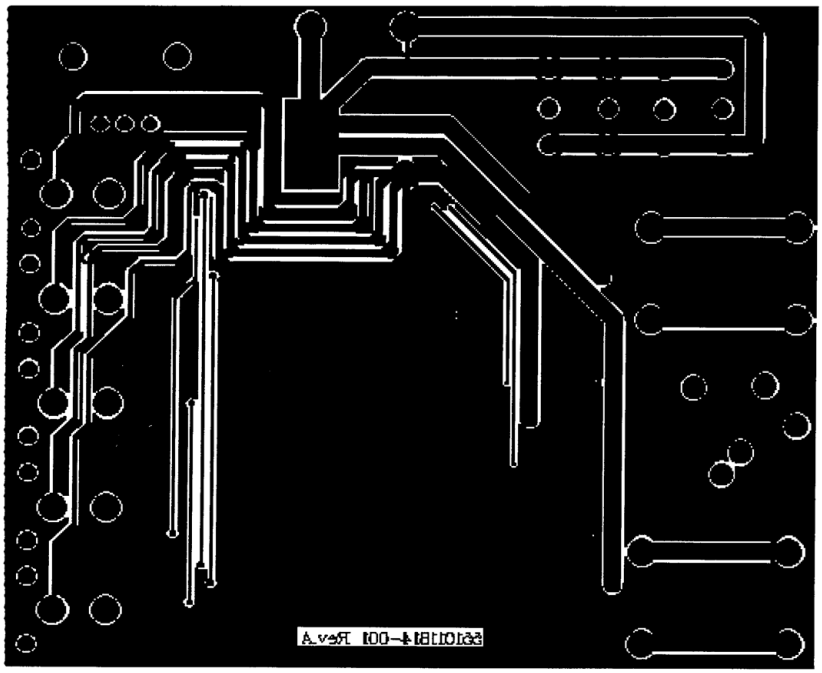


Figure 59. Bottom Layer - (Not to Scale)

Table 1. Analog Audio LM4842 TSSOP and LQ Eval Boards
Assembly Part Number: 980011373-100
Revision: A

Copyright © 2002–2013, Texas Instruments Incorporated

Table 1. Analog Audio LM4842 TSSOP and LQ Eval Boards
Assembly Part Number: 980011373-100
Revision: A
Bill of Material (continued)

Bill of Material

Item	Part Number	Part Description	Qty	Ref Designator (on PCB)	Remark
1	551011373-001	LM4842 Eval Board PCB etch 001	1		
10	482911373-001	LM4842 TSSOP or LQ	1		
20	151911368-001	Cer Cap 0.068µF 50V 10% 1206	2	C_{BA}, C_{BB}	
25	152911368-001	Tant Cap 0.1µF 10V 10% Size = A 3216	3	C2, C3, C4	
26	152911368-002	Tant Cap 0.33µF 10V 10% Size = A 3216	5	C_{inA0}, C_{inA1}, C_{inB0}, C_{inB1}, C_{inbeep}	
27	152911368-003	Tant Cap 1µF 16V 10% Size = A 3216	1	C_{BYPASS}	
28	152911368-004	Tant Cap 10µF 10V 10% Size = C 6032	1	C1	
31	472911368-002	Res 20K Ohm 1/8W 1% 1206	8	R_{inA0}, R_{inA1}, R_{inB0}, R_{inB1} R_{FA0}, R_{FA1}, R_{FB0}, R_{FB1}	
33	472911368-004	Res 200K Ohm 1/16W 1% 0603	4	R_{BEEPA0}, R_{BEEPA1}, R_{BEEPB0}, R_{BEEPB1}	
40	131911368-001	Stereo Headphone Jack W/ Switch	1		Switchcraft #35RAPC4BH3
41	131911368-002	Slide Switch	4	Mute, MUX, SD, Mode	Mouser # 10SP003
42	131911368-003	Potentiometer	1	Volume Control	Mouser # 317-2090-100K
43	131911368-004	RCA Jack	5	A0, A1, B0, B1, BeepIn	Mouser # 16PJ097
44	131911368-005	Banana Jack, Black	3	AOUT-, BOUT-, GND	Mouser # ME164-6219
45	131911368-006	Banana Jack, Red	3	AOUT+, BOUT+, VDD	Mouser # ME164-6218

Copyright © 2002–2013, Texas Instruments Incorporated

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	29

Copyright © 2002–2013, Texas Instruments Incorporated

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated