

LM3712 Microprocessor Supervisory Circuits with Separate Watchdog Timer Output, Power Fail Input and Manual Reset

Check for Samples: [LM3712](#)

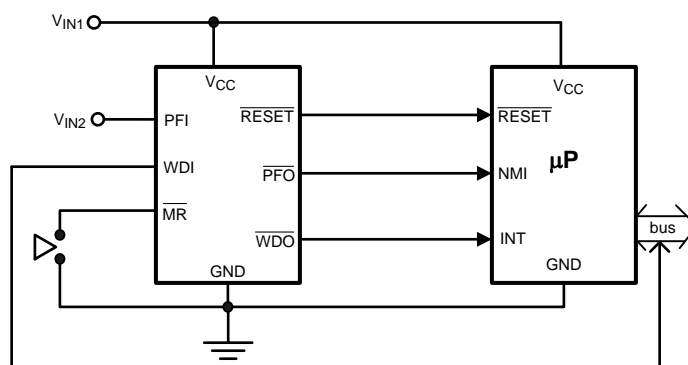
FEATURES

- **Standard Reset Threshold Voltage: 3.08V**
- **Custom Reset Threshold Voltages: For Other Voltages between 2.2V and 5.0V in 10mV Increments, Contact TI.**
- **No External Components Required**
- **Manual-Reset Input**
- **RESET Output**
- **Precision Supply Voltage Monitor**
- **Factory Programmable Reset and Watchdog Timeout Delays**
- **Separate Watchdog Output**
- **Separate Power Fail Comparator**
- **Available in DSBGA Package for Minimum Footprint**
- **±0.5% Reset Threshold Accuracy at Room Temperature**
- **±2% Reset Threshold Accuracy Over Temperature Extremes**
- **Reset Assertion Down to 1V V_{CC}**
- **28 μA V_{CC} Supply Current**

APPLICATIONS

- **Embedded Controllers and Processors**
- **Intelligent Instruments**
- **Automotive Systems**
- **Critical μP Power Monitoring**

Typical Application



DESCRIPTION

The LM3712 series of microprocessor supervisory circuits provide the maximum flexibility for monitoring power supplies and battery controlled functions in systems without backup batteries. The LM3712 series are available in a 9-bump DSBGA package.

Built-in features include the following:

Reset: Reset is asserted during power-up, power-down, and brownout conditions. RESET is specified down to V_{CC} of 1.0V.

Manual Reset Input: An input that asserts reset when pulled low.

Power-Fail Input: A 1.225V threshold detector for power fail warning, or to monitor a power supply other than V_{CC} .

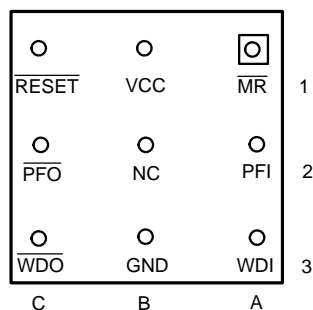
Watchdog Timer: The WDI (Watchdog Input) monitors one of the μP 's output lines for activity. If no output transition occurs during the watchdog timeout period, the watchdog output (WDO) pulls low.



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Connection Diagram



**Figure 1. Top View
(looking from the coating side)
DSBGA 9 Bump Package
BPA09**

PIN DESCRIPTIONS

Bump No.	Name	Function
A1	$\overline{\text{MR}}$	Manual-Reset input. When $\overline{\text{MR}}$ is less than V_{MRT} (Manual Reset Threshold) $\overline{\text{RESET}}$ is engaged.
B1	V_{CC}	Power Supply input.
C1	$\overline{\text{RESET}}$	Reset Logic Output. Pulses low for t_{RP} (Reset Timeout Period) when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{\text{MR}}$ is below V_{MRT} . It remains low for t_{RP} after either V_{CC} rises above the reset threshold, or after $\overline{\text{MR}}$ input rises above V_{MRT} .
C2	$\overline{\text{PFO}}$	Power-Fail Logic Output. When PFI is below V_{PFT} $\overline{\text{PFO}}$ goes low; otherwise, $\overline{\text{PFO}}$ remains high.
C3	$\overline{\text{WDO}}$	Watchdog Output. If no digital activity is detected on WDI (Watchdog Input) for a period exceeding t_{WD} , this output pulls low.
B3	GND	Ground reference for all signals.
A3	WDI	Watchdog Input Transition Monitor: If no transition activity occurs for a period exceeding t_{WD} (Watchdog Timeout Period), reset is engaged.
A2	PFI	Power-Fail Comparator Input. When PFI is less than V_{PFT} (Power-Fail Reset Threshold), the $\overline{\text{PFO}}$ goes low; otherwise, $\overline{\text{PFO}}$ remains high.
B2	NC	No Connect. Test input used at factory only. Leave floating.

Block Diagram

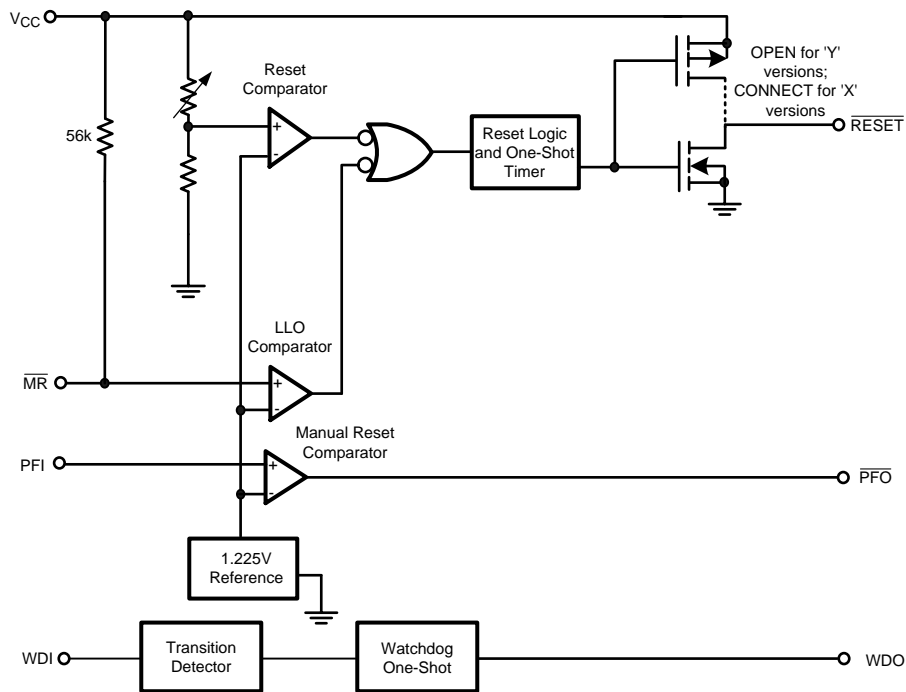


Table 1. Table Of Functions

Part Number	Active Low Reset	Active High Reset	Output (X = totem-pole) (Y = open-drain)	Reset Timeout Period	Watchdog Timeout Period	Manual Reset	Power Fail Comparator
LM3712	x		X, Y ⁽¹⁾	Customized	Customized	x	x

(1) = available upon request. Contact TI



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

Supply Voltage (V _{CC})		-0.3V to 6.0V
All Other Inputs		-0.3V to V _{CC} + 0.3V
ESD Ratings ⁽³⁾	Human Body Model	1.5kV
	Machine Model	150V
Power Dissipation		See ⁽⁴⁾

- (1) **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. **Operating Ratings** indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed conditions.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) The Human Body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.
- (4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using:

$$P_{(MAX)} = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$$

Where the value of θ_{J-A} for the DSBGA package is 220°C/W.

OPERATING RATINGS⁽¹⁾

Temperature Range	$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$
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- (1) **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. **Operating Ratings** indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed conditions.

ELECTRICAL CHARACTERISTICS

Limits in the standard typeface are for $T_J = 25^{\circ}\text{C}$ and limits in **boldface type** apply over full operating range. Unless otherwise specified: $V_{CC} = +2.2\text{V}$ to 5.5V .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V _{CC}	Operating Voltage Range: V _{CC}		1.0		5.5	V
I _{CC}	V _{CC} Supply Current	All inputs = V _{CC} ; all outputs floating		28	50	μA
RESET THRESHOLD						
V _{RST}	Reset Threshold	V _{CC} falling	-0.5 -2	V _{RST}	+0.5 +2	%
		V _{CC} falling: T _A = 0°C to 70°C	-1.5		+1.5	
V _{RSTH}	Reset Threshold Hysteresis			0.0032•V _{RST}		mV
t _{RP}	Reset Timeout Period	Reset Timeout Period = E, J, N, S Reset Timeout Period = F, K, P, T Reset Timeout Period = G, L, Q, U Reset Timeout Period = H, M, R, V	1 20 140 1120	1.4 28 200 1600	2 40 280 2240	ms
t _{RD}	V _{CC} to Reset Delay	V _{CC} falling at 1mV/μs		20		μs
RESET						
V _{OL}	$\overline{\text{RESET}}$	V _{CC} > 1.0V, I _{SINK} = 50μA			0.3	V
		V _{CC} > 1.2V, I _{SINK} = 100μA			0.3	
		V _{CC} > 2.25V, I _{SINK} = 900μA			0.3	
		V _{CC} > 2.7V, I _{SINK} = 1.2mA			0.3	
		V _{CC} > 4.5V, I _{SINK} = 3.2mA			0.4	
V _{OH}	$\overline{\text{RESET}}$	V _{CC} > 2.25V, I _{SOURCE} = 300μA	0.8 V _{CC}			
		V _{CC} > 2.7V, I _{SOURCE} = 500μA	0.8 V _{CC}			
		V _{CC} > 4.5V, I _{SOURCE} = 800μA	V _{CC} - 1.5V			
WDI						
WDI	Watchdog Input Current		-1		+1	μA
WDI _T	Watchdog Input Threshold		0.2•V _{CC}	1.225	0.8•V _{CC}	V
t _{WD}	Watchdog Timeout Period	Watchdog Timeout Period = E, F, G, H Watchdog Timeout Period = J, K, L, M Watchdog Timeout Period = N, P, Q, R Watchdog Timeout Period = S, T, U, V	4.3 71 1120 17900	6.2 102 1600 25600	9.3 153 2400 38400	ms
PFI/ $\overline{\text{MR}}$						
V _{PFT}	PFI Input Threshold		1.200	1.225	1.250	V
V _{MRT}	$\overline{\text{MR}}$ Input Threshold	$\overline{\text{MR}}$, Low			0.8	V
		$\overline{\text{MR}}$, High	2.0			
V _{PFTH} / V _{MRTH}	PFI/ $\overline{\text{MR}}$ Threshold Hysteresis	PFI/ $\overline{\text{MR}}$ falling: V _{CC} = V _{RST} MAX to 5.5V		0.0032•V _{RST}		mV
I _{PFI}	Input Current (PFI only)		-75		75	nA
R _{MR}	$\overline{\text{MR}}$ Pull-up Resistance		35	56	75	kΩ
t _{MD}	$\overline{\text{MR}}$ to Reset Delay			12		μS
t _{MR}	$\overline{\text{MR}}$ Pulse Width		25			μS

ELECTRICAL CHARACTERISTICS (continued)

Limits in the standard typeface are for $T_J = 25^\circ\text{C}$ and limits in **boldface type** apply over full operating range. Unless otherwise specified: $V_{CC} = +2.2\text{V}$ to 5.5V .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PFO, WDO						
V _{OL}	PFO, WDO Output Voltage	V _{CC} > 2.25V, I _{SINK} = 900μA			0.3	V
		V _{CC} > 2.7V, I _{SINK} = 1.2mA			0.3	
		V _{CC} > 4.5V, I _{SINK} = 3.2mA			0.4	
V _{OH}		V _{CC} > 2.25V, I _{SOURCE} = 300μA	0.8 V _{CC}			
		V _{CC} > 2.7V, I _{SOURCE} = 500μA	0.8 V _{CC}			
		V _{CC} > 4.5V, I _{SOURCE} = 800μA	V _{CC} - 1.5V			
LLO OUTPUT						
V _{LLOT}	LLO Output Threshold (V _{LLO} - V _{RST} , V _{CC} falling)		1.01•V _{RST}	1.02•V _{RST}	1.03•V _{RST}	V
V _{LLOTH}	Low-Line Comparator Hysteresis			0.0032•V _{RST}		mV
t _{CD}	Low-Line Comparator Delay	V _{CC} falling at 1mV/μs		20		μs

TYPICAL PERFORMANCE CHARACTERISTICS

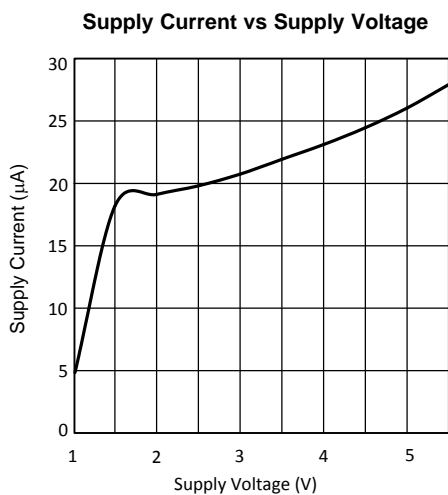


Figure 2.

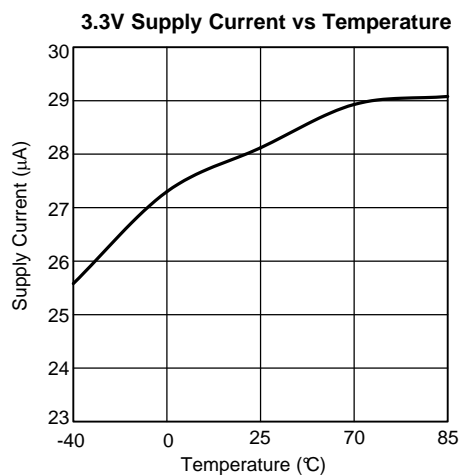


Figure 3.

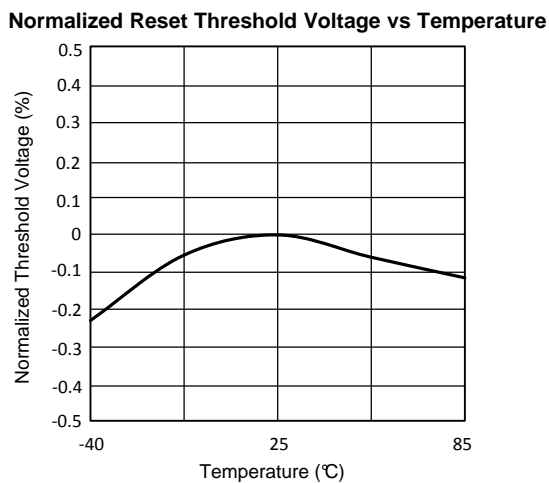


Figure 4.

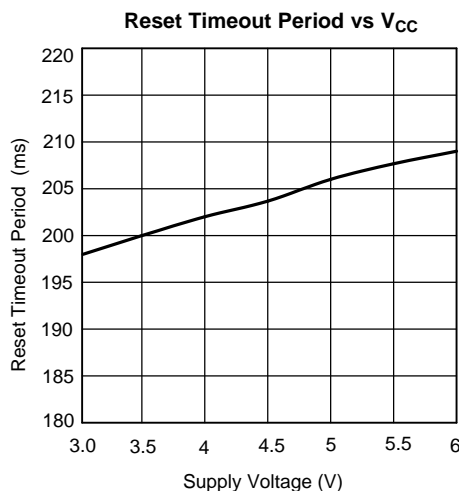


Figure 5.

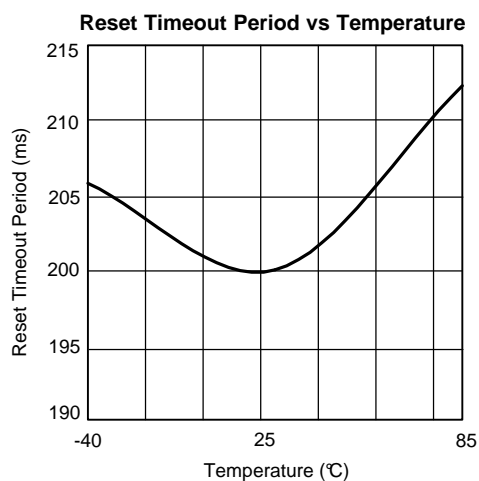


Figure 6.

**Max. Transient Duration vs Reset Comparator Overdrive
($V_{CC} = 3.3V$)**

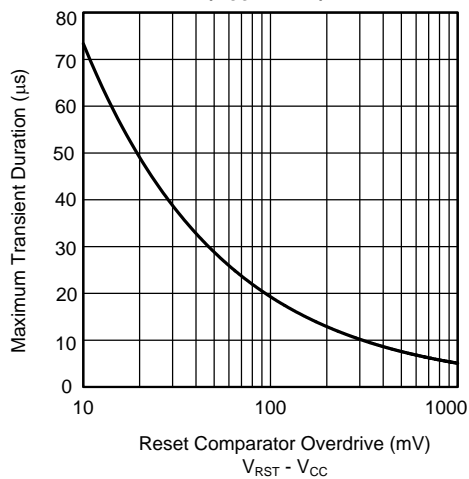


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Watchdog Timeout Period vs Temperature
(t_{wd} programmed as 6.2ms)

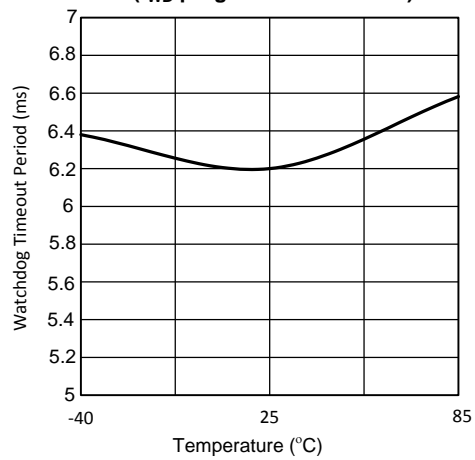


Figure 8.

CIRCUIT INFORMATION

RESET OUTPUT

The Reset input of a μP initializes the device into a known state. The LM3712 microprocessor supervisory circuits assert a forced reset output to prevent code execution errors during power-up, power-down, and brownout conditions.

$\overline{\text{RESET}}$ is ensured valid for $V_{\text{CC}} > 1\text{V}$. Once V_{CC} exceeds the reset threshold, an internal timer maintains the output for the reset timeout period. After this interval, reset goes high. The LM3712 offers an active-low $\overline{\text{RESET}}$.

Any time V_{CC} drops below the reset threshold (such as during a brownout), the reset activates. When V_{CC} again rises above the reset threshold, the internal timer starts. Reset holds until V_{CC} exceeds the reset threshold for longer than the reset timeout period. After this time, reset releases.

The Manual Reset input ($\overline{\text{MR}}$) will initiate a forced reset also. See the [MANUAL RESET INPUT \(\$\overline{\text{MR}}\$ \)](#) section.

RESET THRESHOLD

The LM3712 family is available with a reset voltage of 3.08V. Other reset thresholds in the 2.20V to 5.0V range, in steps of 10 mV, are available; contact TI for details.

MANUAL RESET INPUT ($\overline{\text{MR}}$)

Many μP -based products require a manual reset capability, allowing the operator to initiate a reset. The $\overline{\text{MR}}$ input is fully debounced and provides an internal 56 k Ω pull-up. When the $\overline{\text{MR}}$ input is pulled below V_{MRT} (1.225V) for more than 25 μs , reset is asserted after a typical delay of 12 μs . Reset remains active as long as $\overline{\text{MR}}$ is held low, and releases after the reset timeout period expires after $\overline{\text{MR}}$ rises above V_{MRT} . Use $\overline{\text{MR}}$ with digital logic to assert or to daisy chain supervisory circuits. It may be used as another low-line comparator by adding a buffer.

POWER-FAIL COMPARATOR ($\text{PFI}/\overline{\text{PFO}}$)

The PFI is compared to a 1.225V internal reference, V_{PFT} . If PFI is less than V_{PFT} , the Power Fail Output $\overline{\text{PFO}}$ drops low. The power-fail comparator signals a falling power supply, and is driven typically by an external voltage divider that senses either the unregulated supply or another system supply voltage. The voltage divider generally is chosen so the voltage at PFI drops below V_{PFT} several milliseconds before the main supply voltage drops below the reset threshold, providing advanced warning of a brownout.

The voltage threshold is set by R_1 and R_2 and is calculated as follows:

$$V_{\text{PFT}} = \left(\frac{R_1 + R_2}{R_2} \right) \times 1.225\text{V} \quad (1)$$

Note this comparator is completely separate from the rest of the circuitry, and may be employed for other functions as needed.

WATCHDOG TIMER INPUT (WDI)

The watchdog timer input monitors one of the microprocessor's output lines for activity. Each time a transition occurs on this monitored line, the watchdog counter is reset. However, if no transition occurs and the timeout period is reached, the LM3712 assumes that the microprocessor has locked up and the watchdog output $\overline{\text{WDO}}$ is activated.

WDI is a high impedance input. $\overline{\text{WDO}}$ is an active-low totem pole output.

SPECIAL PRECAUTIONS FOR THE DSBGA PACKAGE

As with most integrated circuits, the LM3712 is sensitive to exposure from visible and infrared (IR) light radiation. Unlike a plastic encapsulated IC, the DSBGA package has very limited shielding from light, and some sensitivity to light reflected from the surface of the PC board or long wavelength IR entering the die from the side may be experienced. This light could have an unpredictable affect on the electrical performance of the IC. Care should be taken to shield the device from direct exposure to bright visible or IR light during operation.

DSBGA MOUNTING

The DSBGA package requires specific mounting techniques which are detailed in TI Application Note AN-1112. Referring to the section **Surface Mount Technology (SMT) Assembly Considerations**, it should be noted that the pad style which must be used with the 9-pin package is the NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

Timing Diagrams

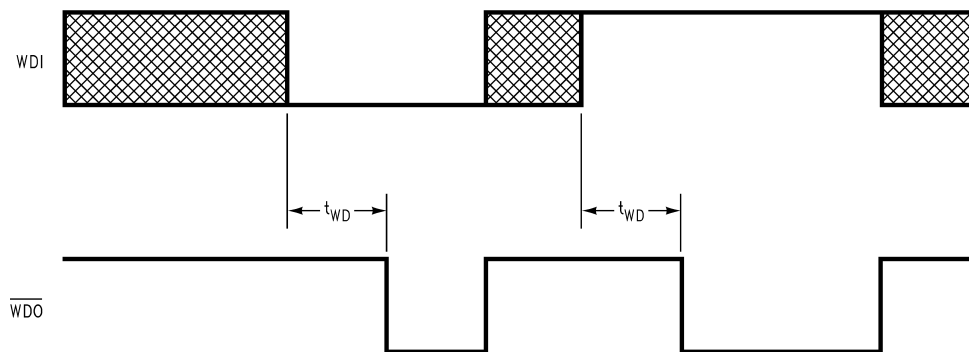


Figure 9. LM3712 Reset Time with \overline{MR}

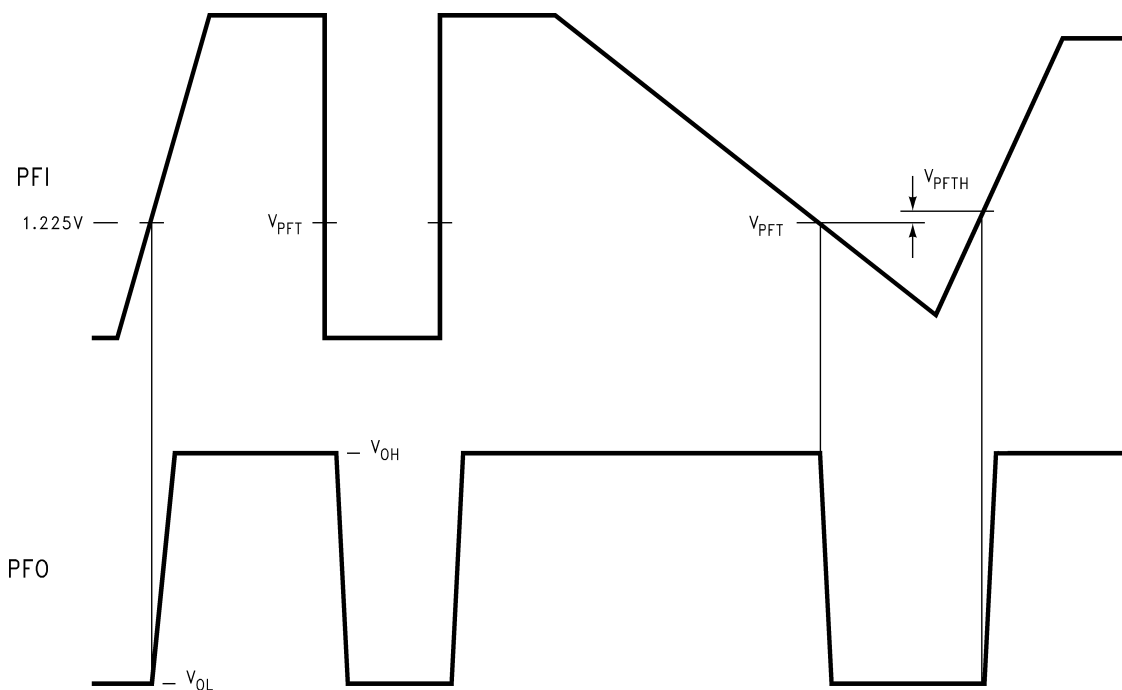


Figure 10. PFI Comparator Timing Diagram

Typical Application Circuits

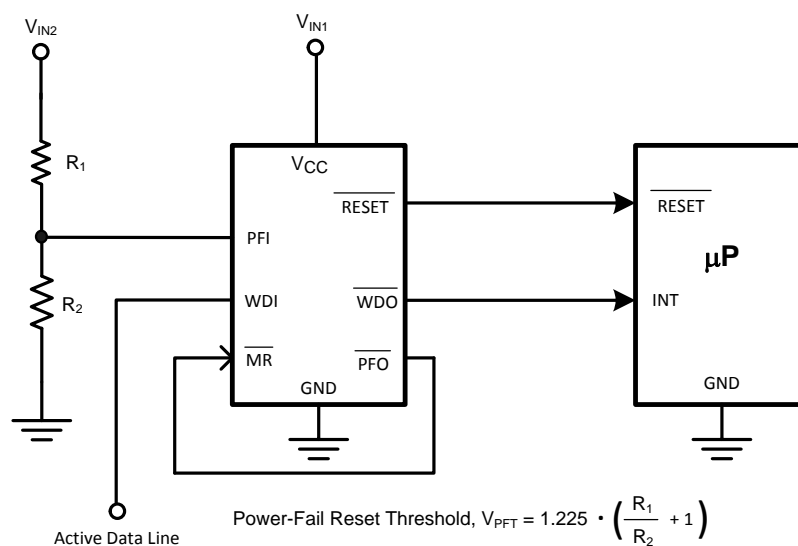


Figure 11. Monitoring Two Critical Supplies Plus Dataline

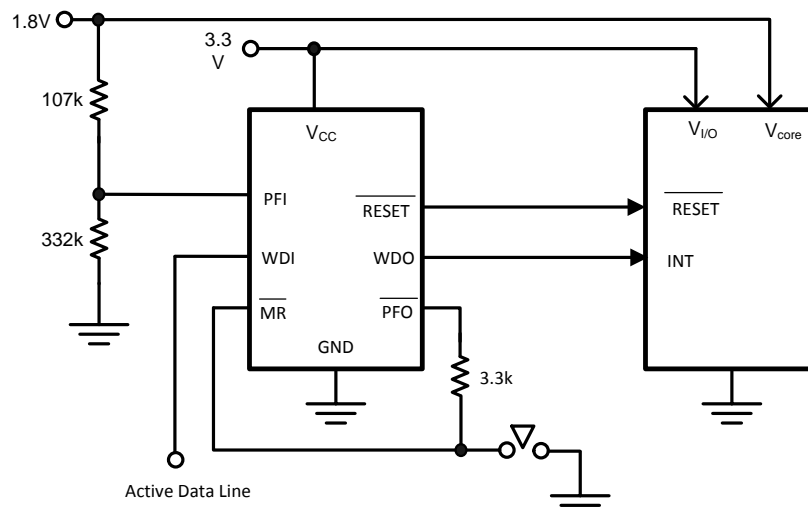


Figure 12. Monitoring Two Supplies plus Manual Reset And Dataline

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F

Page

- Changed layout of National Data Sheet to TI format [10](#)

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