

LM3622 Lithium-Ion Battery Charger Controller

Check for Samples: [LM3622](#)

FEATURES

- Versions for Charging of 1 Cell (4.1V or 4.2V) or 2 Cells (8.2V or 8.4V)
- Versions for Coke or Graphite Anode
- Precision ($\pm 30\text{mV/Cell}$) End-of-Charge Control
- Wide Input Range: 4.5V-24V
- Low Battery Drain Leakage: 200nA
- 15 mA Available to Drive Low Cost PNP

APPLICATIONS

- Cellular Phone Cradle Charger
- PDA/Notebook Cradle Charger
- Camcorder Cradle Charger

DESCRIPTION

The LM3622 is a charge controller for Lithium-Ion batteries. This monolithic integrated circuit accurately controls an external pass transistor for precision Lithium-Ion battery charging. The LM3622 provides a constant voltage or constant current (CVCC) configuration that changes, as necessary, to optimally charge lithium-ion battery cells. Voltage charging versions (4.1V, 4.2V, 8.2V, and 8.4V) are available for one or two cell battery packs and for coke or graphite anode battery chemistry.

The LM3622 accepts input voltages from 4.5V to 24V. Controller accuracy over temperature is $\pm 30\text{mV/cell}$ for A grade and $\pm 50\text{mV/cell}$ for the standard grade. No precision external resistors are required. Furthermore, the LM3622's proprietary output voltage sensing circuit drains less than 200nA from the battery when the input source is disconnected.

The LM3622 circuitry includes functions for regulating the charge voltage with a temperature compensated bandgap reference and regulating the current with an external sense resistor. The internal bandgap insures excellent controller performance over the operating temperature and input supply range.

The LM3622 can sink 15mA minimum at the EXT pin to drive the base of an external PNP pass transistor. It also has low-voltage battery threshold circuitry that removes this drive when the cell voltage drops below a preset limit. The LV_{SEL} pin programs this threshold voltage to either 2.7V/cell or 2.15V/cell. The low-voltage detection, which is a user enabled feature, provides an output signal that can be used to enable a "wake up charge" source automatically to precondition a deeply discharged pack.

The LM3622 is available in a standard 8-lead SOIC surface mount package.



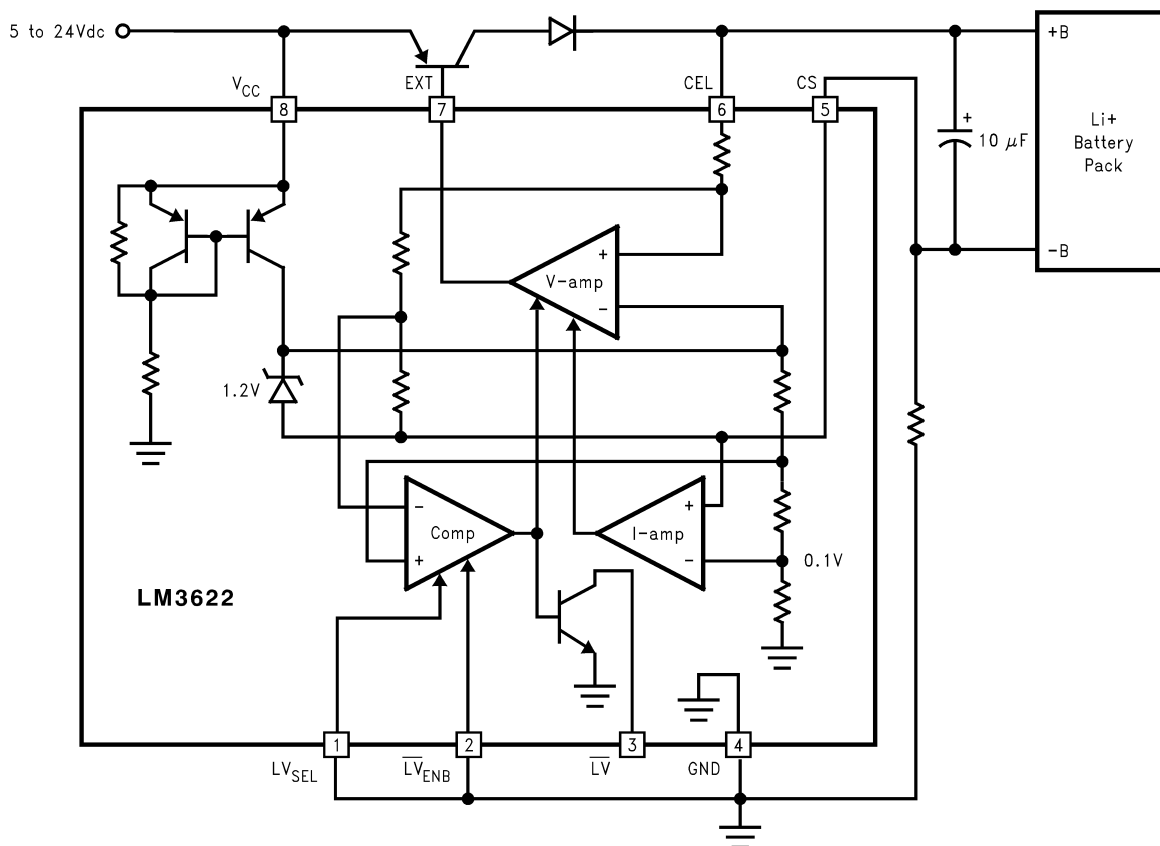
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TYPICAL APPLICATION



CONNECTION DIAGRAM

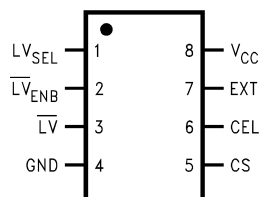


Figure 1. 8-Lead SOIC Package
See Package D0008A

PIN DESCRIPTION

Pin No.	Name	I/O	Description
1	LV _{SEL}	Input	Low-voltage detection threshold Select. The threshold is 2.15V/cell when this pin is pulled low to GND and 2.70V/cell when it is pulled up to V _{CC} . The battery voltage is sensed between CEL and CS pins.
2	$\overline{\text{LV}}_{\text{ENB}}$	Input	Low-voltage detection Enable. The low-voltage detection is enabled when this pin is pulled Low to GND. Pulling this pin HIGH to V _{CC} disables the low-voltage detection.
3	$\overline{\text{LV}}$	Output	Output of the low-voltage detection. This pin is a NPN open-collector output that goes to low impedance state when $\overline{\text{LV}}_{\text{ENB}}$ is pulled LOW and the battery voltage is below the threshold set by LV _{SEL} . $\overline{\text{LV}}$ stays in HIGH impedance state at any battery voltage when $\overline{\text{LV}}_{\text{ENB}}$ is pulled HIGH to V _{CC} . $\overline{\text{LV}}$ can be used for turning on a low current source to recharge a deeply depleted battery.
4	GND	Ground	IC common.
5	CS	Input	Input for battery charge current and battery negative-terminal voltage sensing. Battery charging current is sensed through an external resistor, R _{CS} , connected between the battery's negative terminal and GND. The maximum charge current is regulated to a value of 100mV/R _{CS} .
6	CEL	Input	Battery positive-terminal voltage sensing.
7	EXT	Output	Output of the controller for driving a PNP transistor or P-MOSFET. The controller modulates the current sinking into this pin to control the regulation of either the charge current or the battery voltage.
8	V _{CC}	Power Supply	IC power supply



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

Supply Voltage (V _{CC})		-0.3 to 24V
$\overline{\text{LV}}$		-0.3 to 24V
EXT ⁽³⁾		-0.3 to 24V
LV _{SEL}		-0.3 to 24V
$\overline{\text{LV}}_{\text{ENB}}$		-0.3 to 24V
ESD Susceptibility ⁽⁴⁾		2500V
Storage Temperature		-40°C to +125°C
Lead Temp. Soldering	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
Power Dissipation (T _A = 25°C) ⁽⁵⁾		350mW

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) V_{EXT} is not allowed to exceed (V_{CC} + 0.3V) or damage to the device may occur.
- (4) Rating is for the human body model, a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.
- (5) The maximum power dissipation must be de-rated at elevated temperatures and is limited by T_{JMAX} (maximum junction temperature), θ_{JA} (junction-to-ambient thermal resistance) and T_A (ambient temperature). The maximum power dissipation at any temperature is: PD_{DissMAX} = (T_{JMAX} - T_A) / θ_{JA} up to the value listed in the Absolute Maximum Ratings.

OPERATING RATINGS⁽¹⁾

Supply Voltage (V _{CC})		4.5V to 24V
Ambient Temperature Range		-20°C to 70°C
Junction Temperature Range		-20°C to 85°C
Thermal Resistance, θ _{JA}	SOIC-8	170°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.

ELECTRICAL CHARACTERISTICS LM3622-XX

Unless otherwise specified $V_{CC} = 5V/\text{Cell}$ $T_A = T_J = 25^\circ\text{C}$. Limits with standard typeface apply for $T_J = 25^\circ\text{C}$, and limits in **boldface type** apply over the indicated temperature range.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Operating power supply range		4.5		24.0	V
I_{CC}	Quiescent Current			210		μA
V_{CEL}	Regulation Voltage	$T_J = 0^\circ\text{C}$ to $+70^\circ\text{C}$ $V_{CC} = 4.5V/\text{cell}$ ⁽¹⁾				
	LM3622A-4.1		4.070	4.100	4.130	V
	LM3622A-8.2		8.140	8.200	8.260	V
	LM3622A-4.2		4.170	4.200	4.230	V
	LM3622A-8.4		8.340	8.400	8.460	V
	LM3622-4.1		4.050	4.100	4.150	V
	LM3622-8.2		8.100	8.200	8.300	V
	LM3622-4.2		4.150	4.200	4.250	V
	LM3622-8.4		8.300	8.400	8.500	V
	Long Term Stability	See ⁽²⁾		0.02		%
V_{CS}	Current limit threshold at CS pin	$V_{CEL} = 4V$ for LM3622-4.X $V_{CEL} = 8V$ for LM3622-8.X	90	100	110	mV
I_{CEL}	Current in CEL pin	V_{CC} Supply connected		25		μA
		V_{CC} Supply Open		200		nA
LVth	Low voltage detect threshold (between pins CS and GND)	$\overline{LV}_{ENB} = 0V$ and $LV_{SEL} = 0V$	2.00	2.15	2.30	V/Cell
		$\overline{LV}_{ENB} = 0V$ and $LV_{SEL} = V_{CC}$	2.55	2.70	2.85	V/Cell
I_{EXT}	EXT pin output sink current	$V_{EXT} = 4V$ for LM3622-4.X $V_{EXT} = 8V$ for LM3622-8.X	15	25		mA
I_{IN1}	LV_{SEL} input current	$LV_{SEL} = 5V$, LM3622-4.X $LV_{SEL} = 10V$, LM3622-8.X		20 50		μA
I_{IN2}	\overline{LV}_{ENB} input current	$\overline{LV}_{ENB} = 5V$, LM3622-4.X $\overline{LV}_{ENB} = 10V$, LM3622-8.X		20 50		μA
$I_{\overline{LV}}$	\overline{LV} pin leakage current	$\overline{LV} = 5V/\text{Cell}$			250	nA
$V_{\overline{LV}}$	\overline{LV} pin saturation voltage	$I_{SINK} = 1mA$ $T_J = -20^\circ\text{C}$ to 85°C		0.25	0.40	V

(1) Limits reflect initial accuracy.

(2) $T_J = 85^\circ\text{C}$, 1000 hours. Activation energy of 0.78eV used.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, $T_A = 25^\circ\text{C}$.

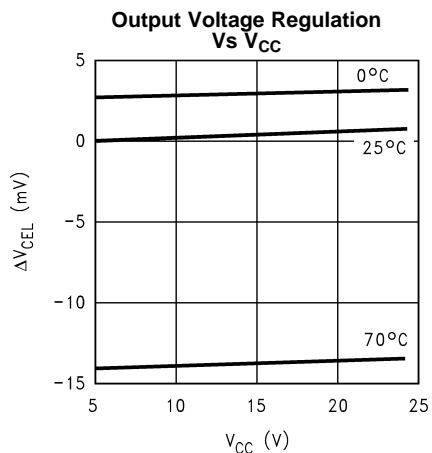


Figure 2.

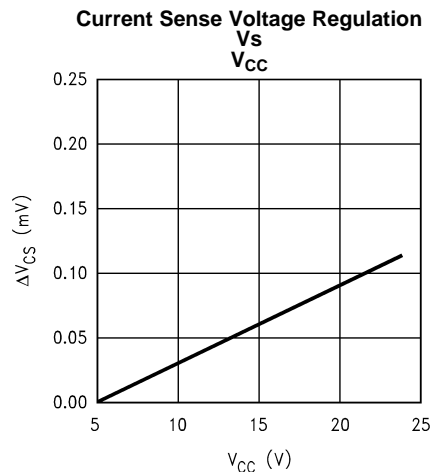


Figure 3.

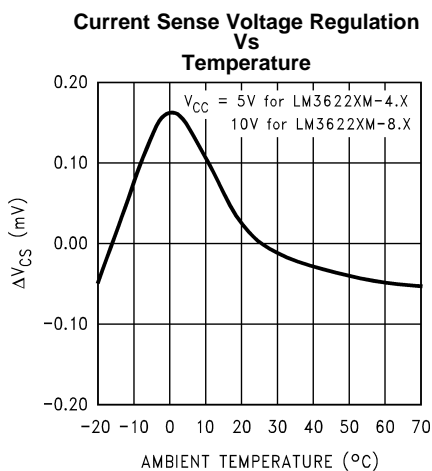


Figure 4.

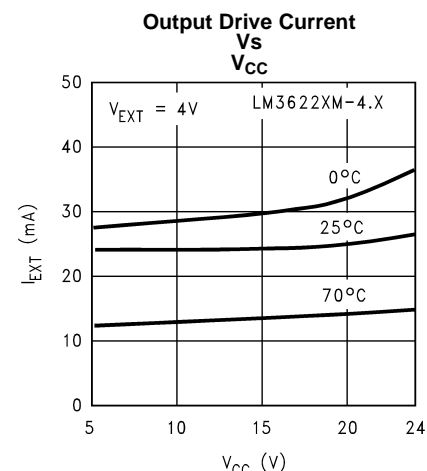


Figure 5.

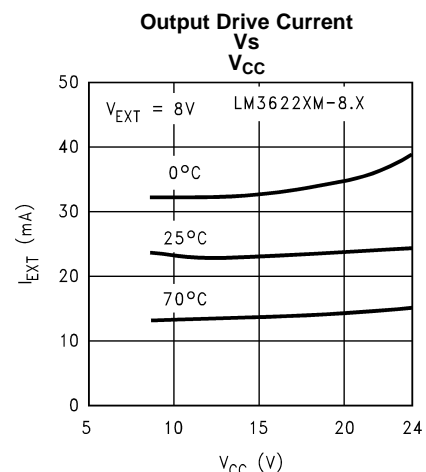


Figure 6.

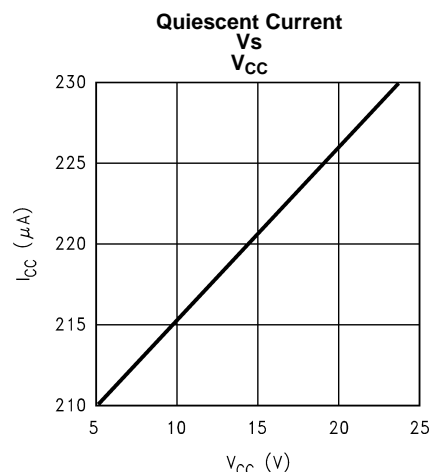


Figure 7.

FUNCTIONAL DESCRIPTION

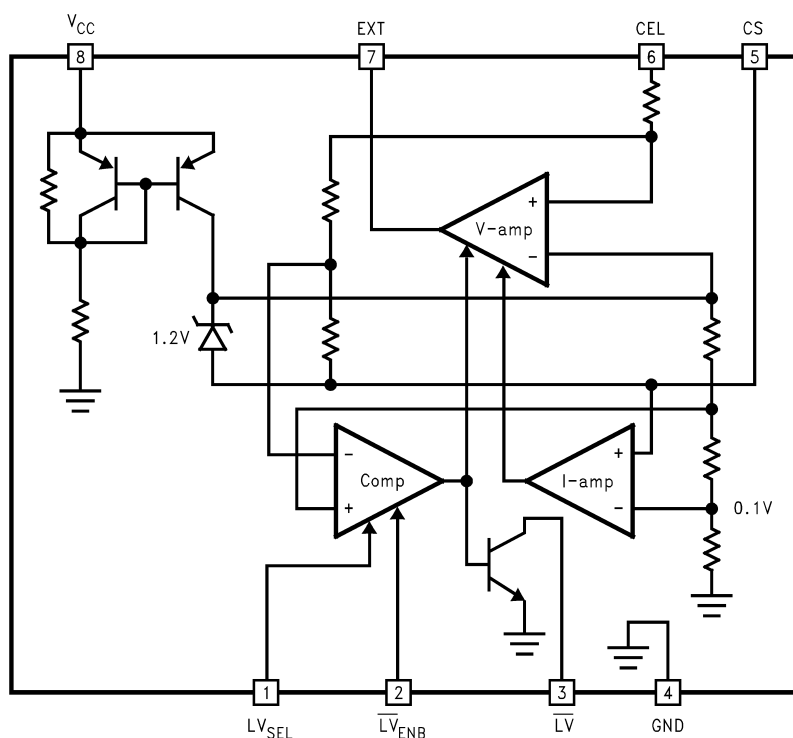


Figure 8. LM3622 Simplified Block Diagram

The simplified LM3622 block diagram in [Figure 8](#) gives a general idea of the circuit operation. The controller integrates the reference, feedback and drive functions on-chip to control a linear, lithium-ion battery charger in constant voltage and constant current (CVCC) charge operation. The regulated output voltage is sensed between CEL and CS, and the battery charge current is sensed across a current-sense resistor between CS and GND. The EXT pin is designed for driving a series pass element, which can be a PNP transistor or a P-MOSFET.

Tying the $\overline{\text{LV}}_{\text{ENB}}$ pin to ground enables the controller's low-voltage detection circuit. When the low-voltage detection circuit is enabled and a battery voltage below a preset threshold is detected, the LM3622 will drive the LV pin low and shut off the current flowing into the EXT pin to suspend the CVCC charge process. The low-voltage threshold is user selectable to be either 2.15V/cell or 2.7V/cell by pulling the LV_{SEL} pin to GND or V_{CC} respectively. The $\overline{\text{LV}}$ pin is a NPN open collector output that can be used to turn on a low current source to wake up charge a deeply depleted battery. When the low-voltage detection is disabled ($\overline{\text{LV}}_{\text{ENB}}$ pulled up to V_{CC}), the LM3622 always starts the charge cycle in constant current mode at any battery voltage below the controller's regulation level, and maintains the $\overline{\text{LV}}$ pin at a high-impedance state.

APPLICATION INFORMATION

CEL PIN CURRENT DRAIN

The LM3622 has an internal power down switch in series with the on-chip resistor divider that is used for sensing the battery voltage. In the event that the V_{CC} supply is removed, the power down switch will disconnect the resistor divider from the CS pin, preventing the battery from discharging through the CEL pin.

EXT PIN

The EXT pin is internally pulled up to V_{CC} via a 20 μ A current source making it possible to eliminate the external base-emitter resistor when driving a PNP transistor, or the gate-source resistor when driving a P-MOSFET. However, the voltage applied to EXT is not allowed to be higher than ($V_{CC} + 0.3V$), otherwise the reverse current from EXT pin to V_{CC} pin may cause damage to the device.

LV PIN CURRENT RATING

The LV pin is a low power, NPN open collector output that is rated to sink 10mA maximum. Therefore, the value of the pull up resistor should be chosen high enough to limit the current to be less than 10mA.

CS PIN

In normal operation, the current limit threshold voltage for the CS pin is 100mV typical. In case of a fault condition, the voltage to this pin should be limited to below 5V.

TYPICAL APPLICATION

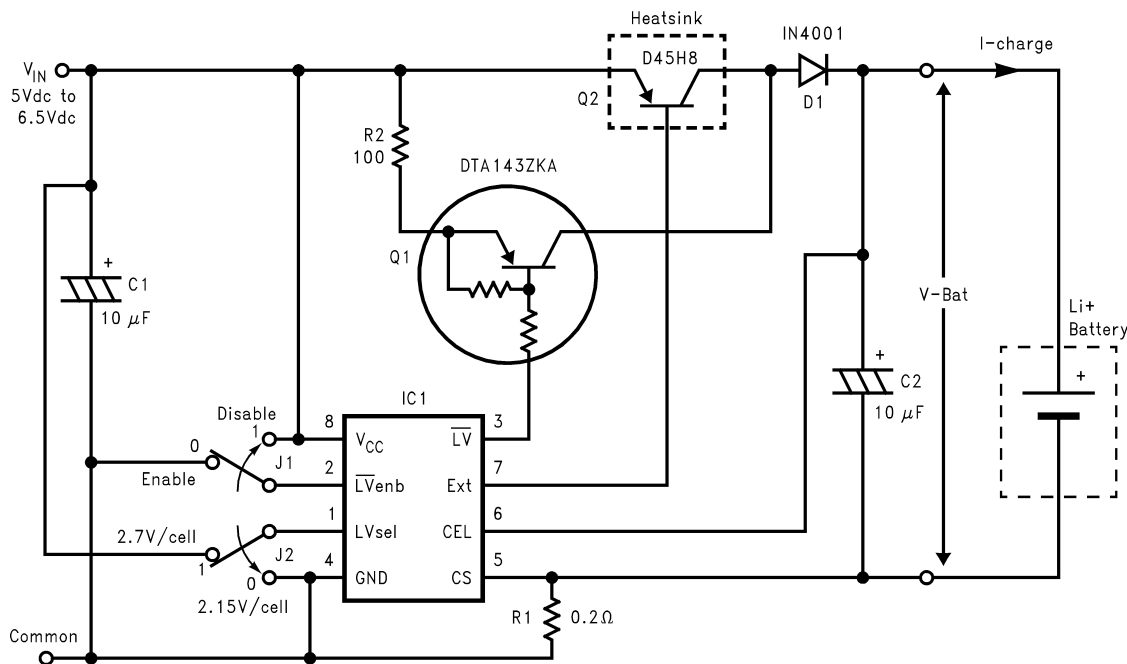


Figure 9. Low Dropout, Constant Current/Constant Voltage Li-ion Battery Charger

The low dropout linear charger shown in Figure 9 provides constant current and constant voltage charging of 1-cell lithium-ion battery packs. J1 and J2 are used for selecting the operation of the low-voltage detection. The LM3622 initializes the charge cycle based on the battery voltage and the enable status of the low-voltage detection.

When the low-voltage detection is disabled, the LM3622 starts the charge cycle constant current mode if the battery voltage is below the controller's regulation level. In constant current mode, the LM3622 modulates the base drive of Q2 to regulate a constant 100mV across the current sense resistor R1, thus generating charge current of

$$I_{\text{charge}} = 0.1V/R1$$

which is equal to 0.5A in this case.

Once the battery voltage reaches the target regulation level set by the LM3622, Q2 is controlled to regulate the voltage across the battery, and the constant voltage mode of the charging cycle starts. Once the charger is in the constant voltage mode, the charger maintains a regulated voltage across the battery and the charging current is dependent on the state of the charge of the battery. As the cell approaches a fully charged condition, the charge current falls to a very low value.

When the low-voltage detection is enabled and the initial battery voltage is below the low-voltage threshold, the LM3622 turns Q2 off and forces the \overline{LV} pin low to drive Q1 on to start a wake up charge phase. Q1 in conjunction with R2 provides a low current source to recondition the battery. During the wake up charge mode, Q1 is driven into saturation and the wake up charge current is programmed by R2,

$$I_{\text{charge (wake)}} = (V_{IN} - V_{CE1} - V_{D1} - LV_{th})/R2$$

where V_{IN} is the input supply voltage, V_{CE1} is the collector-emitter on state voltage of Q1, V_{D1} is the diode forward voltage of D1, and LV_{th} is the low-voltage threshold level set by switch J2.

Once the battery voltage reaches the low-voltage threshold, the \overline{LV} pin transitions to a high-impedance state to end the wake up charge phase, and the EXT pin resumes the base drive of Q2 to start the constant current mode. The charging cycle is completed in constant voltage mode when the battery is fully charged. Figure 10 shows the timing diagram of the charge cycle with the low-voltage detection enabled.

D1 is a general-purpose silicon diode used for isolating the battery from the charger circuitry that could discharge the battery when the input source is removed. Changing D1 to a Schottky diode will reduce the overall dropout voltage of the circuit, but the penalty is higher leakage current associated with Schottky diodes.

TIMING DIAGRAM

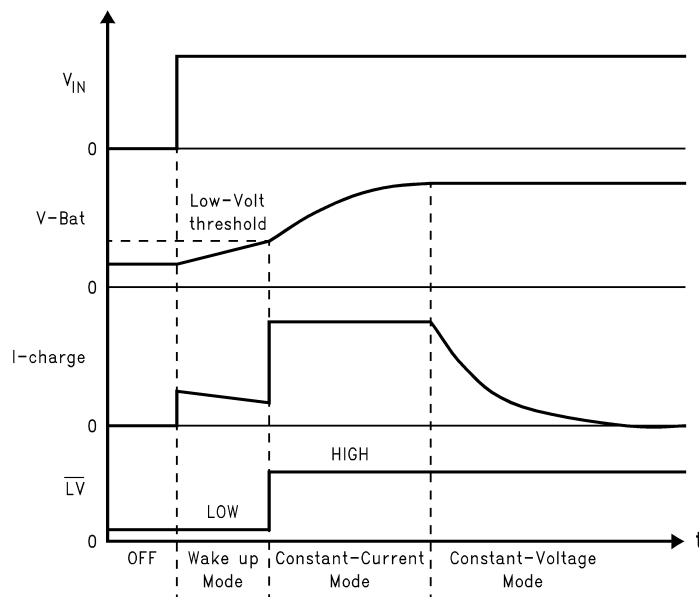


Figure 10. Typical Charge Cycle with Low-Voltage Detection Enabled.

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3622MX-8.2/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN CU SN	Level-1-260C-UNLIM	-20 to 85	3622 M-8.2	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3622MX-8.2/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3622MX-8.2/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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