# 300mA Current Limited Power Switch

**Check for Samples: LM34902**

## FEATURES

- **Input Voltage of 2.8V to 5.3V**
- **0.3A Maximum Switch Current**
- **0.64Ω Typical Total On-Resistance**
- **Load Detection**
- **Enable/Disable**
- **Switch On Indicator**
- **Peak Current Limit**
- **Thermal Shutdown**
- **6-Bump Thin DSBGA Package**

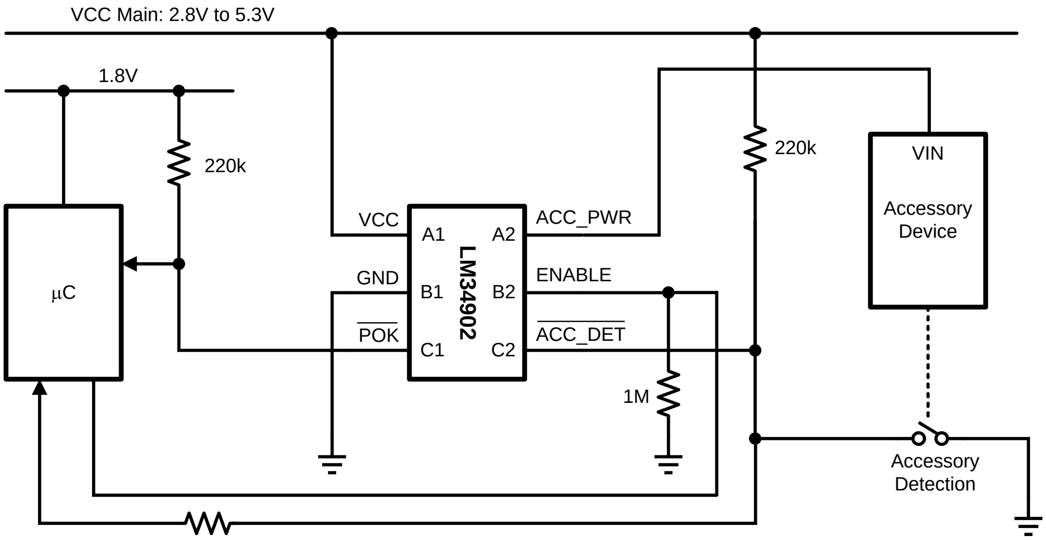
## APPLICATIONS

- **Handsets, Tablets, Notebooks**
- **Portable devices**

## DESCRIPTION

The LM34902 is a 0.3A PFET switch used to control the input voltage of electronic devices. It is easily integrated into system designs that have a 2.8V to 5.3V voltage rail. Besides the 0.45Ω PFET switch, the LM34902 can be enabled or disabled by a logic signal. The IC monitors the presence of a downstream electronic device via a dedicated pin to decide whether to turn on the PFET switch. A power good signal generated by the IC can be used by system control to determine the status of the switch. The LM34902 also provides over-current and over-temperature protection. The IC comes in a tiny 6-bump Thin DSBGA package.

## Typical Application Circuit



## Connection Diagram

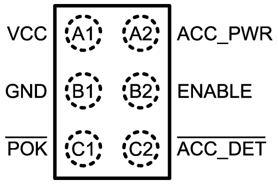


**Figure 1. Top View**
**6-Bump Thin DSBGA Package**
**See Package Number YFQ**

### PIN DESCRIPTION

| Name | Pin Number | Function |
|---|---|---|
| VCC | A1 | Power input of the PFET switch. It also provides power to the entire IC. Connect to the voltage rail that the accessory device is expected to work off. |
| GND | B1 | Common Ground (device substrate). |
| $\overline{\text{POK}}$ | C1 | Open-drain PFET status indicator. When the PFET is off, this pin floats. When PFET is on, it is grounded. |
| $\overline{\text{ACC\_DET}}$ | C2 | Pull this pin low to tell the IC that the downstream accessory device is plugged in. |
| ENABLE | B2 | When this pin is low, the PFET will be turned off and $\overline{\text{POK}}$ will be open-drained. Current limit circuitry will also be disabled. The IC will be in a low-power state. This pin should be held low until VCC is established to ensure proper initial state of internal logic. When ENABLE is high, the PFET switch will be allowed to turn on. |
| ACC_PWR | A2 | Power output terminal of the PFET switch. Connect to input rail of accessory device. |

## Truth Table

| Input | | | | | Output | |
|---|---|---|---|---|---|---|
| **ENABLE** | **$\overline{\text{ACC\_DET}}$** | **Current Limit Detected** | **$T_J$ Limit Exceeded** | **2.8V < VCC < 5.3V** | **PFET Switch Status** | **$\overline{\text{POK}}$** |
| 0 | x | No | No | Yes | Open | Open Drain |
| x | 1 | No | No | Yes | Open | Open Drain |
| 0 to 1 | 0 | No | No | Yes | On | Grounded |
| 0 to 1 | 0 | Yes | No | Yes | Current Limited | Grounded |
| x | x | x | Yes | 2.2V < VCC < 5.3V | Open | Open Drain |
| 0 | x | x | No | 2.2V < VCC < 2.8V | Open | Open Drain |
| Note: "x" stands for "don't care". | | | | | | |

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings(1)

| | |
|---|---|
| VCC | -0.3V to 6V |
| ENABLE, $\overline{\text{POK}}$, $\overline{\text{ACC\_DET}}$, | |
| ACC_PWR(2) | -0.3V to 6V |
| Junction Temperature ($T_J$) | +150°C |
| Storage Temperature Range | −65°C to +150°C |
| ESD Susceptibility, Human Body Model(3) | 2kV |

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics table.
(2) The voltages on these pins should never exceed VCC+0.3V.
(3) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-A114.

## Operating Ratings(1)

| | |
|---|---|
| VCC Voltage(2) | 2.8V to 5.3V |
| Junction Temperature ($T_J$), LM34902 | -40°C to +85°C |

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics table.

(2) For VCC between 2.2V and 2.8V, if ENABLE is a logic low, the LM34902 will not turn on the PFET switch.

## Electrical Characteristics

Unless otherwise stated, the following conditions apply: VCC = 3V. Limits in standard type are for $T_J$ = 25°C only; limits in **boldfacetype** apply over the operating junction temperature ($T_J$) range. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C and are provided for reference purposes only.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage, $\overline{\text{ACC\_DET}}$, ENABLE | | | | **0.45** | V |
| $V_{IH}$ | Input High Voltage, $\overline{\text{ACC\_DET}}$, ENABLE | | **1.35** | | | V |
| $V_{IHS}$ | Input Hysteresis, $\overline{\text{ACC\_DET}}$, ENABLE | | | 55 | | mV |
| $I_{LK}$ | Input Current, $\overline{\text{ACC\_DET}}$, ENABLE | $\overline{\text{ACC\_DET}}$, ENABLE between 0V and VCC | | | 1 | µA |
| $I_{SD}$ | VCC Current in Shutdown Mode | $V_{ENABLE}$ = 0V<br>$V_{VCC}$ = 5.3V | | | 10 | µA |
| $I_Q$ | VCC Quiescent Current | $V_{ENABLE}$ = 1.8V<br>$V_{VCC}$ = 5.3V, $I_{ACC\_PWR}$ = 0A | | 47 | **100** | µA |
| $R_{ON}$ | Total On Resistance Between VCC and ACC_PWR Pins | $V_{VCC}$ = 3V<br>$I_{ACC\_PWR}$ = 0.3A | | 0.64 | **1** | Ω |
| $I_{LK\_ACC}$ | ACC_PWR Leakage Current When PFET is Off | $V_{ACC\_PWR}$ = 0V to VCC<br>$V_{VCC}$ = 5.3V<br>$V_{ENABLE}$ = 0V | | | 1 | µA |
| $I_{LIMIT}$ | PFET Switch Current Limit | $V_{VCC}$ = 2.8V to 5.3V<br>$V_{ACC\_PWR}$ = 0V | **0.3** | 0.45 | **0.65** | A |
| $V_{POK}$ | $\overline{\text{POK}}$ Current Sink Capability | $\overline{\text{POK}}$ asserted. 1mA sink current. | | | 0.4 | V |
| $I_{POK}$ | $\overline{\text{POK}}$ Leakage Current | $\overline{\text{POK}}$ de-asserted.<br>$V_{\overline{POK}}$ = 3.3V | | | 1 | µA |
| $T_1$ | $\overline{\text{ACC\_DET}}$ Response Time | $\overline{\text{ACC\_DET}}$ rising to either PFET or $\overline{\text{POK}}$ FET turn-off | | 40 | | ns |
| $T_2$ | ENABLE Response Time | ENABLE rising to either PFET or $\overline{\text{POK}}$ FET turn-on | | 10 | | µs |
| $T_3$ | Minimum ENABLE Cycle Time(1) | $\overline{\text{ACC\_DET}}$ tied to ground. ENABLE logic high = 1.8V. VCC = 2.8V to 5.3V. | | 300 | | ns |

(1) If ENABLE toggles low from a high state, it needs to stay low for at least $T_3$ long before toggling back to high. Otherwise the internal flip-flop may not be set and the PFET switch may not turn on.

## Thermal Characteristics

| Symbol | Description | Conditions | Typical Value | Unit |
|---|---|---|---|---|
| $\theta_{JA1}$ | Junction-to-Ambient Thermal Resistance | Mount device on a standard 4-layer 4" x 3" JEDEC board. Apply known amount of power to the package. Measure junction temperature and surrounding air temperature. No air flow. Refer to JESD51-7 for more information. | 104 | °C/W |
| $\theta_{JA2}$ | Junction-to-Ambient Thermal Resistance | Mount device on a 2-layer 2.19" x 2.9" board. Copper thickness is 1 oz per layer. No airflow. Power dissipation is 0.5W. | 136 | °C/W |
| $T_{SD}$ | Thermal Shutdown Threshold | Raise $T_J$ from below 150°C until $\overline{\text{POK}}$ is de-asserted. No load is connected at ACC_PWR. | 170 | °C |

## Typical Performance Characteristics

Unless indicated otherwise, VCC = 3V and $T_J$ = 25°C.

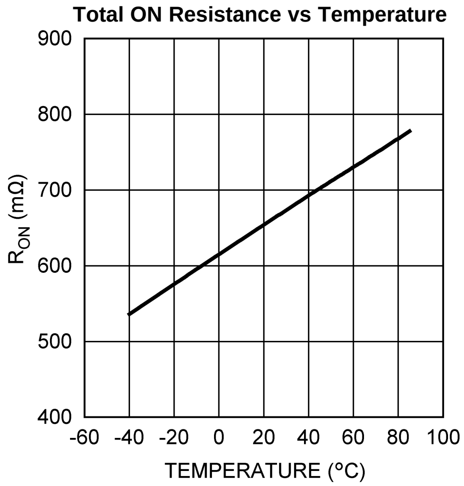

Total ON Resistance vs Temperature

Figure 2.

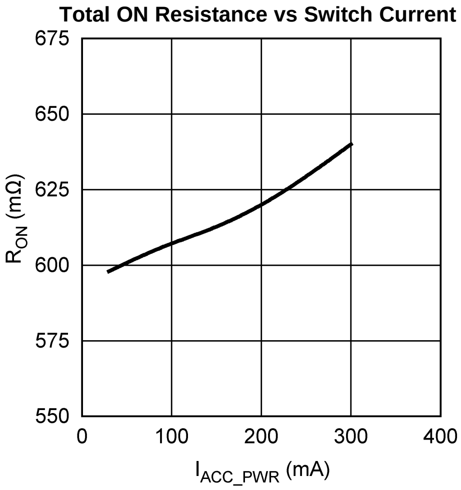

Total ON Resistance vs Switch Current

Figure 3.

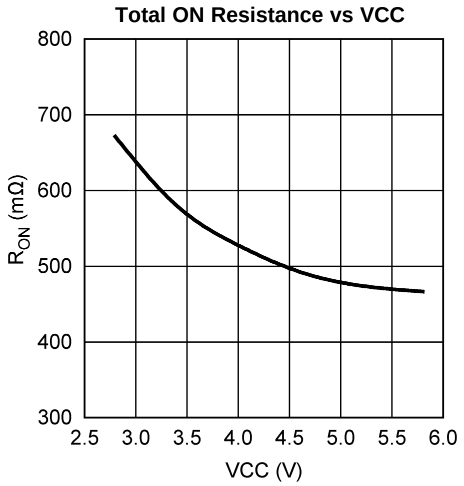

Total ON Resistance vs VCC

Figure 4.

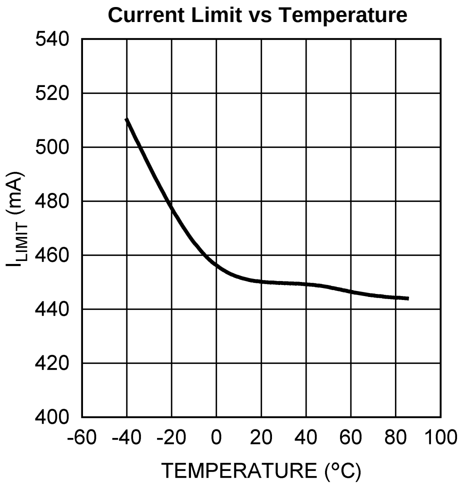

Current Limit vs Temperature

Figure 5.

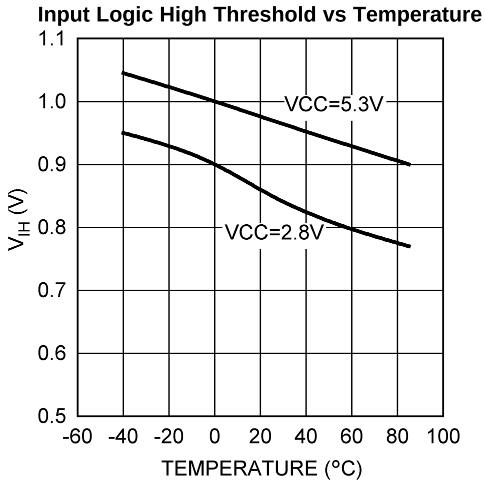

Input Logic High Threshold vs Temperature

Figure 6.

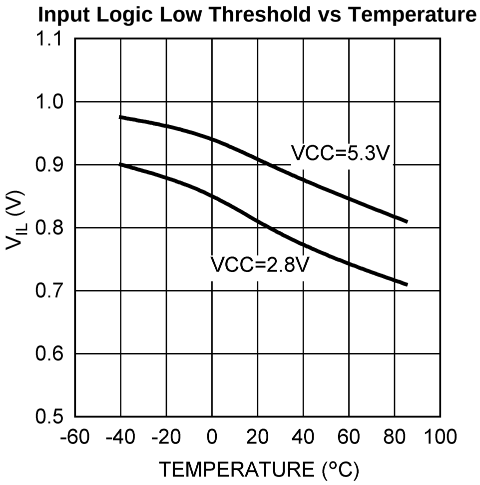
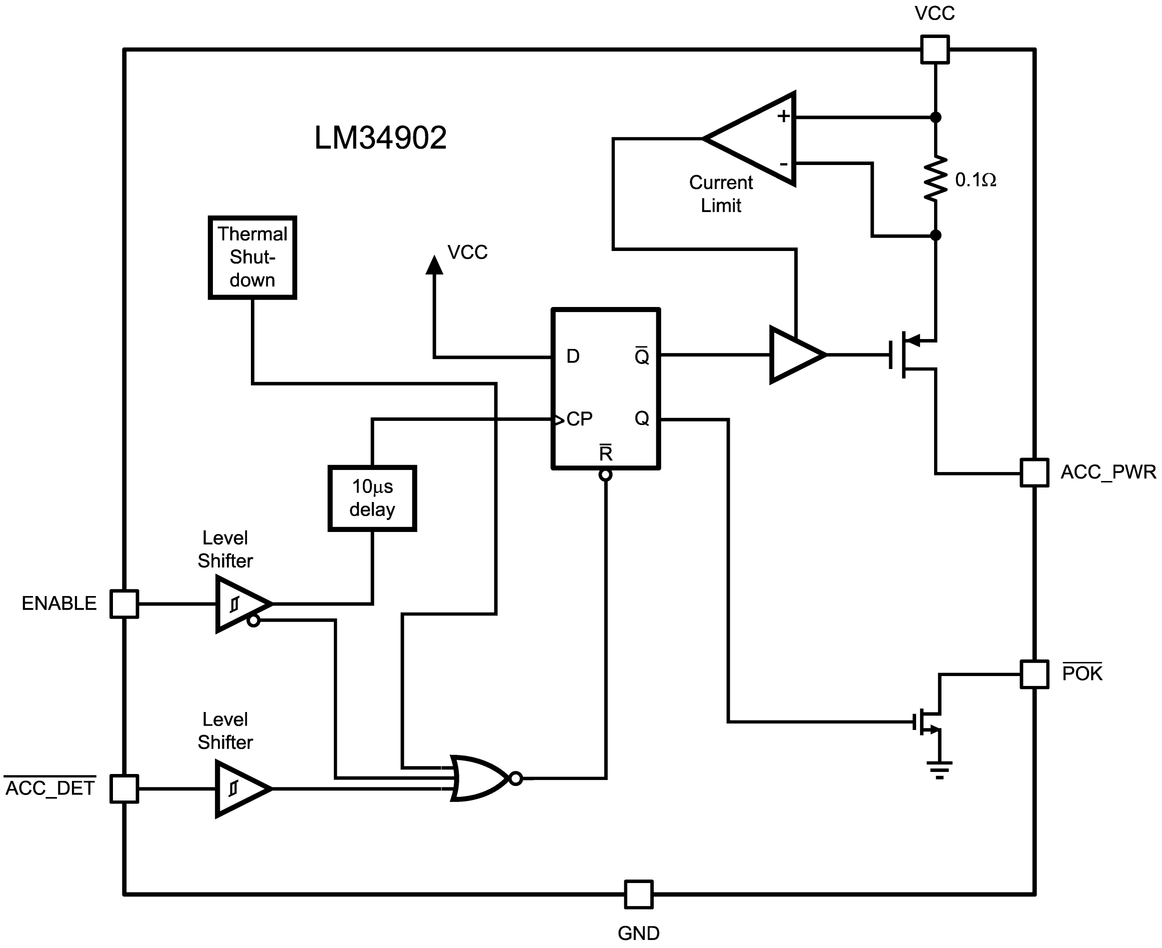

Input Logic Low Threshold vs Temperature

Figure 7.

## BLOCK DIAGRAM



## APPLICATION HINTS

To turn on the PFET switch, both the ENABLE and the ACC_DET pins need to be asserted. In addition, ACC_DET needs to be asserted no later than the rising edge of the ENABLE signal. De-assertion of either the ENABLE or the ACC_DET will result in turned-off PFET switch and de-asserted POK signal.

To prevent a glitch in the otherwise asserted ACC_DET from keeping the FETs turned off, it is a good practice to cycle the ENABLE following every falling edge in the ACC_DET signal. When cycling the ENABLE, make sure it stays low for at least $T_3$ long before toggling back high. If ENABLE logic high level is not 1.8V, make sure ENABLE stays low for at least 1µs.

When laying out the PCB, try to keep the ENABLE and ACC_DET traces as short as possible and away from noisy traces.

## REVISION HISTORY

| **Changes from Revision A (April 2013) to Revision B** | **Page** |
|---|---|
| • Changed layout of National Data Sheet to TI format | 5 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM34902ITM/NOPB | ACTIVE | DSBGA | YFQ | 6 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | K | Samples |
| LM34902ITMX/NOPB | ACTIVE | DSBGA | YFQ | 6 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | K | Samples |
| LM34902ITMZ/NOPB | ACTIVE | DSBGA | YFQ | 6 | | TBD | Call TI | Call TI | -40 to 85 | | Samples |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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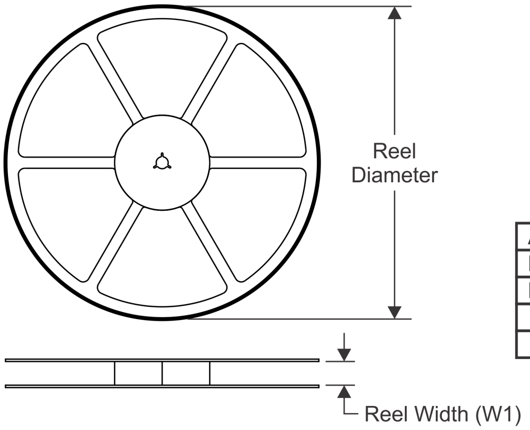
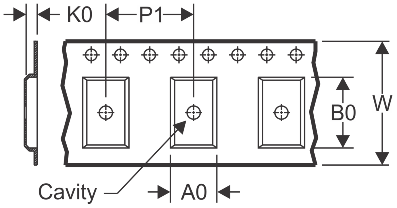
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

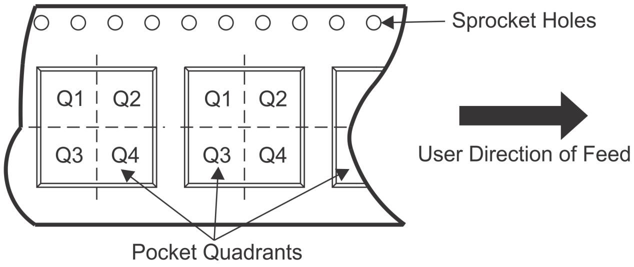


### TAPE DIMENSIONS



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

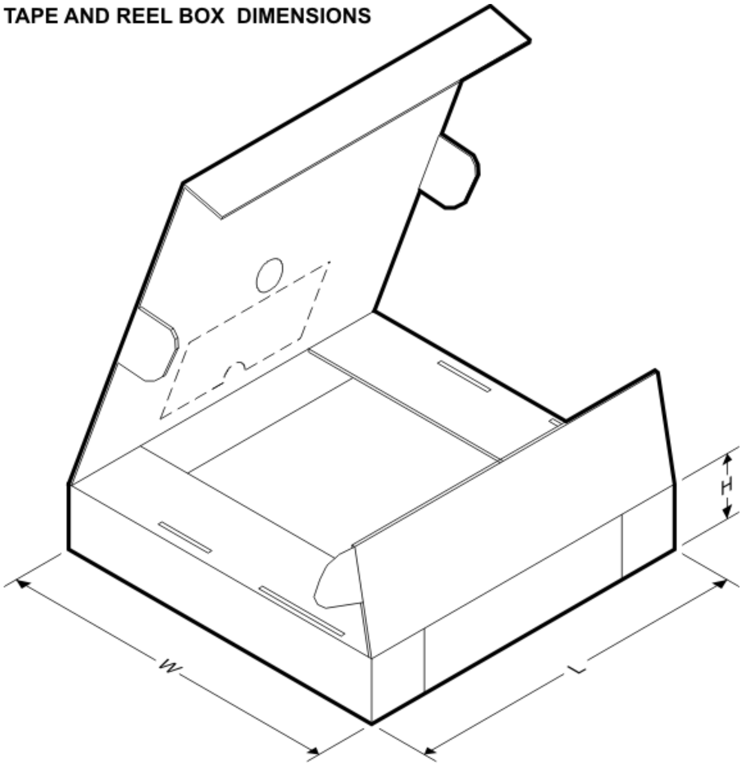
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM34902ITM/NOPB | DSBGA | YFQ | 6 | 250 | 178.0 | 8.4 | 0.89 | 1.3 | 0.7 | 4.0 | 8.0 | Q1 |
| LM34902ITMX/NOPB | DSBGA | YFQ | 6 | 3000 | 178.0 | 8.4 | 0.89 | 1.3 | 0.7 | 4.0 | 8.0 | Q1 |

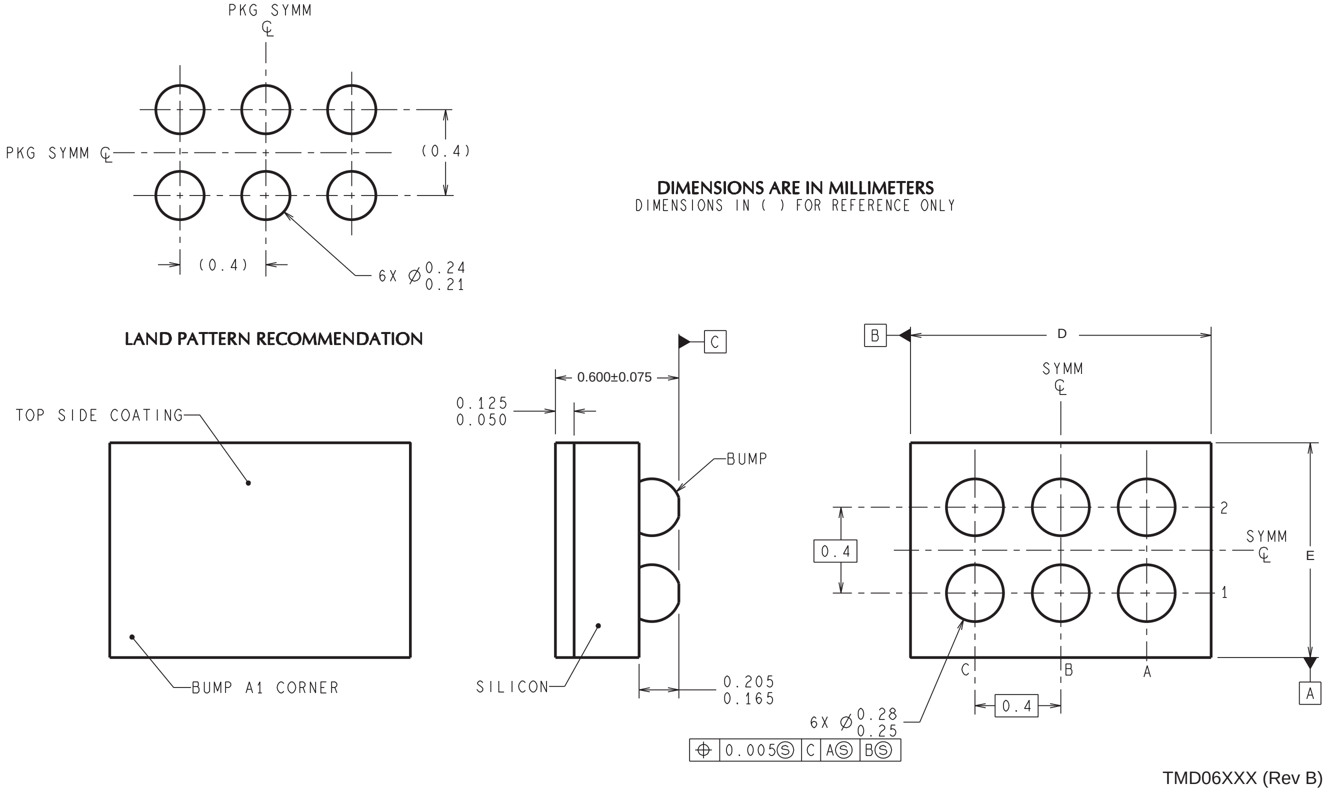
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM34902ITM/NOPB | DSBGA | YFQ | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LM34902ITMX/NOPB | DSBGA | YFQ | 6 | 3000 | 210.0 | 185.0 | 35.0 |

# YFQ0006



D: Max = 1.24 mm, Min = 1.18 mm

E: Max = 0.84 mm, Min = 0.78 mm

4215075/A 12/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265