LM3212 Step-Down DC-DC Converter with Analog Bypass Mode for RF Power Amplifiers

Check for Samples: LM3212

FEATURES

- **1.6 MHz (typ.) PWM Switching Frequency**
- **ACB Reduces Inductor Requirements and Size**
- **Operates From a Single Li-Ion Cell (2.7V to 5.5V)**
- **Dynamically Adjustable Output Voltage (0.5V to 3.4V)**
- **2.5A Maximum Load Current**
- **Analog Bypass Function With Low Bypass Resistance (33 mΩ typ.)**
- **High Efficiency to 95% with Internal Synchronous Rectification**
- **16-bump DSBGA Package**
- **Current Overload Protection**
- **Thermal Overload Protection**

APPLICATIONS

- **Battery-Powered 2G/3G/4G RF Power Amplifiers**
- **Hand-Held Radios**
- **RF PC Cards**

DESCRIPTION

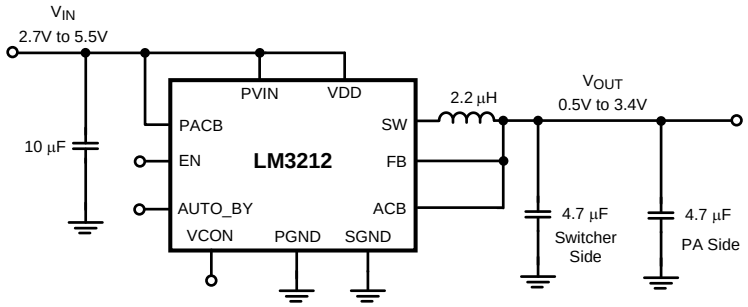
The LM3212 is a DC-DC converter optimized for powering GSM RF power amplifiers (PAs) from a single Lithium-Ion cell; however, it may also be used in other applications. The LM3212 steps down an input voltage from 2.7V to 5.5V to a dynamically adjustable output voltage of 0.5V to 3.4V. The output voltage is set through a VCON analog input that adjusts the output voltage to ensure efficient operation at all power levels of the RF PA.

The LM3212 has a unique Active Current Bypass (ACB) feature that speeds up output voltage transition times, provides extra drive and a low-resistance analog bypass. The LM3212 has an AUTO_BY pin to force the LM3212 into bypass mode during low input-voltage operation thus overriding the automatic analog bypass feature. Forced bypass can also be achieved by setting VCON > VIN/2.5.

In addition the LM3212 offers a fixed-frequency PWM mode to minimize RF interference and a shutdown mode to turn the device off and reduce battery consumption to 0.02 µA (typ.)

The LM3212 is available in a 16-bump lead-free DSBGA package. A 1.6 MHz switching frequency allows use of tiny surface-mount components for the required inductor and two ceramic capacitors.

Typical Application



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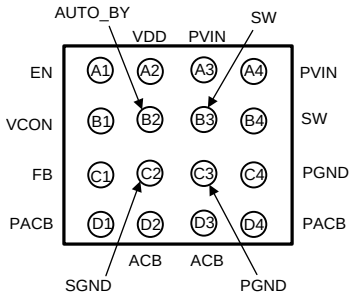
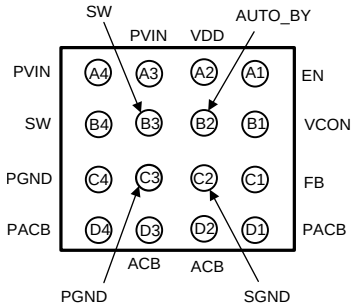
Connection Diagrams

16-Bump 0.5 mm DSBGA Package, Large Bump



Top View



Bottom View

PIN DESCRIPTIONS

Pin #	Name	Description
A3, A4	PVIN	Power Supply Voltage Input to the internal PFET switch.
A2	VDD	Analog Supply Input.
A1	EN	Enable Input. Set this digital input high for normal operation. For shutdown, set low. Pin has an 800 kΩ internal pulldown resistor.
B4, B3	SW	Switching Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor.
B1	VCON	Voltage Control Analog input. VCON controls VOUT in PWM mode. When VCON < 0.15V the switches are turned off (output in tri-state).
B2	AUTO_BY	The AUTO_BY Pin determines the bypass mode function. Set AUTO_BY high for normal automatic bypass mode operation. Set AUTO_BY low for forced bypass (independent of the state of the EN pin). The pin has an internal 800 kΩ pullup resistor.
C4, C3	PGND	Power Ground
C2	SGND	Analog and Control Ground
C1	FB	Feedback Analog Input. Connect to the output at the output filter capacitor.
D3, D2	ACB	Active Current Assist source/sink and Bypass. Connect to the output at the output filter capacitor.
D4, D1	PACB	Power-to-active current/bypass circuit.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

VDD, PVIN to SGND		−0.2V to +6.0V
PGND to SGND		−0.2V to +0.2V
EN, FB, VCON, AUTO_BY		(SGND −0.2V) to (VDD +0.2V) w/6.0V max
SW, ACB		(PGND −0.2V) to (PVIN +0.2V) w/6.0V max
PVIN to VDD		−0.2V to +0.2V
Continuous Power Dissipation(4)		Internally Limited
Junction Temperature (T_{J-MAX})		+150°C
Storage Temperature Range		−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec)		+260°C
ESD Rating(5)(6)	Human Body Model	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins. The LM3212 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 125°C (typ.).
(5) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7) The machine model is a 200 pF capacitor discharged directly into each pin.
(6) Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper ESD handling procedures can result in damage.

OPERATING RATINGS(1)(2)

Input Voltage Range	2.7V to 5.5V
Recommended Load Current	0A to 2.5A
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range(3)	−30°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins. The LM3212 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.
(3) In applications where high-power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$. At higher power levels duty cycle usage is assumed to drop (i.e., max power 12.5% usage is assumed) for GS/GPRS mode.

THERMAL PROPERTIES

PARAMETER	UNIT
Junction-to-Ambient Thermal Resistance (θ_{JA}), YZR Package(1)	50°C/W

(1) Junction-to-ambient thermal resistance (θ_{JA}) is taken from thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7.

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ELECTRICAL CHARACTERISTICS[1][2][3]

Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range ($-30°C \le T_A = T_J \le +85°C$). Unless otherwise noted, all specifications apply to the Typical Application Circuit (page 1) with: $PV_{IN} = V_{DD}$ = AUTO_BY = EN = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{FB,\ MIN}$	Feedback voltage at minimum setting	VCON = 0.20V, $V_{IN} \le 4.2V$[3]	**0.465**	0.5	**0.535**	V
		VCON = 0.32V, $V_{IN} =< 5.5V$[3]	**0.765**	0.8	**0.835**	
$V_{FB,\ MAX}$	Feedback voltage at maximum setting	VCON = 1.36V, $V_{IN} = 3.9V$[3]	**3.325**	3.4	**3.475**	V
I_{SHDN}	Shutdown supply current	EN = SW = VCON = 0V[4]		0.02	**4**	µA
I_q	DC bias current into V_{DD}	VCON = 0V, FB = 0V No Switching[5]		0.85	**0.905**	mA
$R_{DSON(P)}$	Pin-pin resistance for large PFET	I_{SW} = 200 mA, VCON = 0.6V		96	120 **150**	mΩ
$R_{DSON(P)}$	Pin-pin resistance for small PFET	I_{SW} = 200 mA, VCON = 0.42V		312	380 **450**	mΩ
$R_{DSON(N)}$	Pin-pin resistance for NFET	I_{SW} = −200 mA, VCON = 0.1V		110	135 **165**	mΩ
R_{ACB}	Active Current Assist Bypass Resistance	VCON = 1V, max value at V_{IN} = 3.1V & I_{ACB} = 200 mA		37	**53**	mΩ
$I_{LIM,PSteady\text{-}State}$	Positive steady-state peak current limit	VCON = 0.6V[6]	**1340**	1450	**1650**	mA
$I_{LIM,\ P_ACB,\ GSM}$	Positive Active Current Assist peak current limit	VCON = 0.6V, V_{ACB} = 3V[6]	**1400**	1600	**1750**	mA
$I_{LIM,\ NFET}$	NFET Switch negative peak current limit	VCON = 1V[6]	**-1125**	-1000	**-875**	mA
$I_{LIM,\ N_ACB,\ GSM}$	Active Current Assist negative peak current limit	VCON = 1V, V_{ACB} = 1.5V[6]		−2300	**−1900**	mA
F_{OSC}	Internal oscillator frequency		**1.44**	1.6	**1.76**	MHz
$V_{IH_AUTO_BY,\ EN}$	Logic high input threshold		**1.2**			V
$V_{IL_AUTO_BY,EN}$	Logic low input threshold				**0.5**	V
I_{PIN_EN}	Pin pull down current			5	**10**	µA
$I_{PIN_AUTO_BY}$	Pin pull up current		**−10**	−5		µA
$V_{CON,\ ON}$	VCON Threshold for turning on switches		**0.1**	0.15		V
I_{CON}	VCON pin leakage current	VCON = 1.0V	**−1**		**1**	µA
Gain	VCON to V_{OUT} Gain	0.20V ≤ VCON ≤ 1.36V		2.5		V/V

(1) All voltages are with respect to the potential at the GND pins. The LM3212 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.

(2) Min and Max limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm. Due to the pulsed nature of the testing $T_A = T_J$ for the electrical characteristics table.

(3) The parameters in the electrical characteristics table are tested under open loop conditions at $PV_{IN} = V_{DD}$ = 3.6V. For performance over the input voltage range and closed-loop results, refer to the datasheet curves.

(4) Shutdown current includes leakage current of PFET.

(5) I_Q specified here is when the part is not switching. For operating input current at no load, refer to datasheet curves.

(6) Current limit is built-in, fixed, and not adjustable.

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SYSTEM CHARACTERISTICS

The following spec table entries are ensured by design providing the component values in the typical application circuit are used (L = 2.2 µH, DCR = 130 mΩ, C_{IN} = 10 µF, 6.3V, 0603 TDK C1608X5RJ106M, C_{OUT} = 4.7 µF + 4.7 µF, 6.3V, 0603, C1608JB0J475). **These parameters are not ensured by production testing.** Min and Max values are specified over the ambient temperature range T_A = −30°C to 85°C. Typical values are specified at PV_{IN} = V_{DD} = EN = 3.6V, AUTO_BY = 3.6V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$T_{VCON\ SETUP}$	On time for SW pin (Setup time for $V_{CON,\ ON}$ enable)	EN = Low to High	30			µs
$T_{RESPONSE}$	Time for V_{OUT} to rise from 0V to 3.4V (90% or 3.16V)	V_{IN} = 4.2V, I_{OUT} < 1mA, VCON = 0V to 1.36V			20	µs
	Time for V_{OUT} to fall from 3.4V to 1.0V (90% or 3.16V)	V_{IN} = 4.2V, R_{LOAD} = 6.8Ω, VCON = 0.4V to 1.36V			20	
	Time for V_{OUT} to fall from 3.4V to 1.0V (10% or 1.24V)	V_{IN} = 4.2V, R_{LOAD} = 6.8Ω			20	
T_{ON}	Turn-on time (time for output to reach 97% of final value after Enable low to high transition)	EN = Low-to-high, V_{IN} = 4.2V, VCON = 1.36V, V_O = 3.4V, I_{OUT} < 1mA			50	µs
T_{Bypass}	Time for V_{OUT} to rise from 0V to PVIN (90% or 3.24V)	EN = V_{IN} = 3.6V, I_{OUT} < 1mA			20	µs
$T_{Bypass,\ ON}$	Turn-on time (time for output to reach 97% of final value after AUTO_BY high to low transition)	EN = Low, V_{IN}= 3.6V, I_{OUT} < 1mA			50	µs
V_{CON} (S→L)	R_{DSON} mgt threshold	Threshold for PFET R_{DSON} to change from 400 mΩ to 100 mΩ		0.52		V
V_{CON} (L→S)	R_{DSON} mgt threshold	Threshold for PFET R_{DSON} to change from 100 mΩ to 400 mΩ		0.5		V
R_{tot_drop}	Total dropout resistance in bypass mode	VCON = 1.5V, Max value at V_{IN} = 3.1V & Inductor ESR ≤ 140 mΩ		33	45	mΩ
C_{CON}	VCON input capacitance	VCON = 1V, Test frequency = 100 KHz		5		pF
$C_{EN,\ AUTO_BY}$	EN and AUTO_BY input capacitance	VCON = 1V, Test frequency = 100 KHz		5		pF
$I_{OUT,\ MAX}$	Maximum output current	V_{IN} = 3.1V to 5.5V, VCON = 0.56V to 1.36V(1)	2.5			A
		V_{IN} = 3.1V to 5.5V, VCON = 0.24V to 0.56V(1)	1.45			
$I_{LIM-BVP}$	Bypass FET current limit Automatic bypass mode or forced bypass mode	VCON = 1.36V, V_{IN} = 3.1V		3.2		A
$I_{OUT,\ PD,\ GSM}$	Maximum output pull-down current	V_{IN} = 3.1V to 5.5V, VCON = 0.56V to 1.36V(1)			−1.8	A
Linearity	Linearity in VCON range 0.32V to 1.36V	V_{IN} = 3.9V(2) Monotonic in nature	−3		+3	%
			−50		+50	mV
η	Efficiency	V_{IN} = 3.6V, V_{OUT} = 1.0V, I_{OUT} = 600 mA		81		%
		V_{IN} = 3.6V, V_{OUT} = 1.5V, I_{OUT} = 900 mA		84		
		V_{IN} = 3.6V, V_{OUT} = 3.4V, I_{OUT} = 2000 mA		90		
		V_{IN} = 3.6V, V_{OUT} = 3.4V, I_{OUT} = 500 mA		95		
V_{O_RIPPLE}	Ripple voltage as a % of output voltage	V_{OUT} = 1.0V to 3.4V, R_{OUT} = 1.7Ω(1)		2		%
	Ripple voltage at no pulse skipping condition	V_{IN} = 2.7V - 4.5V, V_{OUT} = 1.0V to 3.4V, Differential voltage = V_{IN} − V_{OUT} = 1.4V, R_{OUT} = 1.7Ω(3)		15		mVpp
	Ripple voltage at pulse skipping condition	V_{IN} = 5.5V to dropout, V_{OUT} = 3.4V, I_{OUT} = 2A(3)		35		mVp-p

(1) Current limit is built-in, fixed, and not adjustable.
(2) Linearity limits are ±3% or ±50 mV, whichever is larger.
(3) Ripple voltage should be measured at C_{OUT} electrode on a well-designed PC board and using the suggested inductor and capacitors.

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SYSTEM CHARACTERISTICS (continued)

The following spec table entries are ensured by design providing the component values in the typical application circuit are used (L = 2.2 µH, DCR = 130 mΩ, C_{IN} = 10 µF, 6.3V, 0603 TDK C1608X5RJ106M, C_{OUT} = 4.7 µF + 4.7 µF, 6.3V, 0603, C1608JB0J475). **These parameters are not ensured by production testing.** Min and Max values are specified over the ambient temperature range T_A = −30°C to 85°C. Typical values are specified at PV_{IN} = V_{DD} = EN = 3.6V, AUTO_BY = 3.6V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Line_tr	Line transient response	V_{IN} = 3.6V to 4.2V, TR = TF = 10 µs, V_{OUT} = 1V, I_{OUT} = 600 mA		50		mVpk
Load_tr	Load transient response	V_{OUT} = 1V, TR = TF = 10 µs, I_{OUT} = 600 mA to 700 mA		50		mVpk
Max Duty cycle	Maximum duty cycle		100			%

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TYPICAL PERFORMANCE CHARACTERISTICS

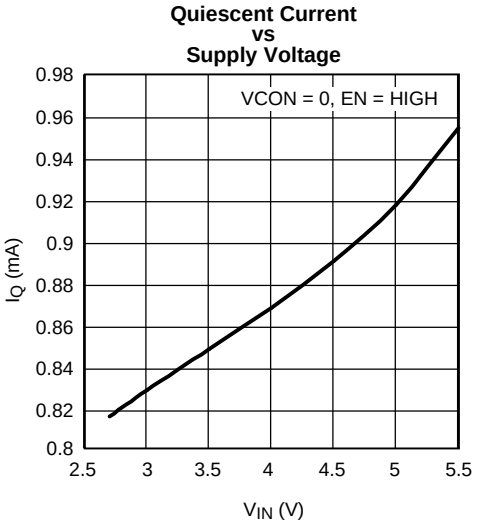

Figure 1.

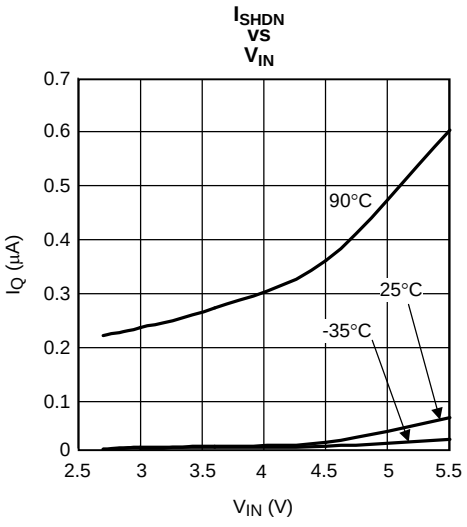

Figure 2.

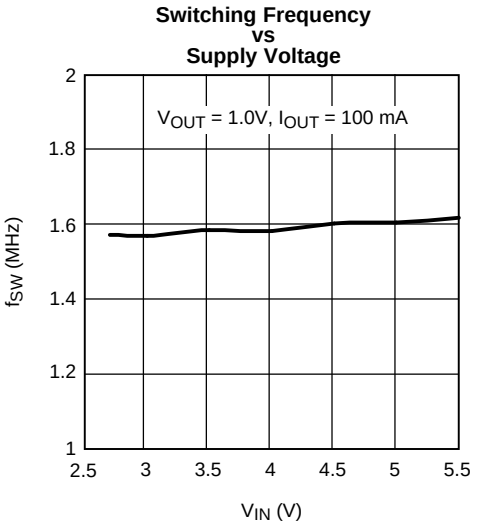

Figure 3.

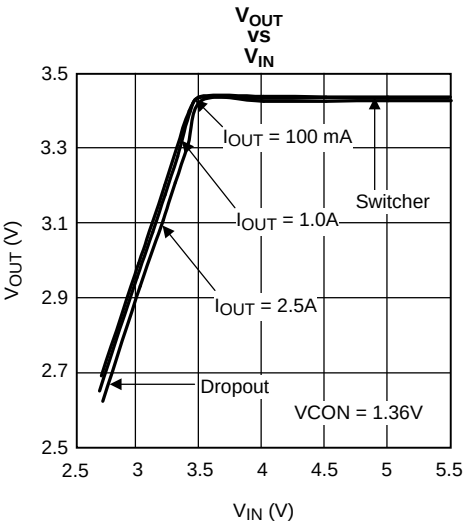

Figure 4.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{OUT} vs V_{IN} (AUTO_BY = LOW)

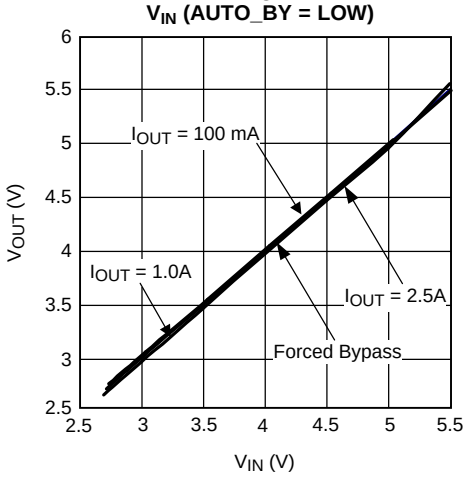

Figure 5.

Peak Current Limit ($I_{LIMPFET\ Peak}$) vs V_{IN} (AUTO_BY = HIGH)

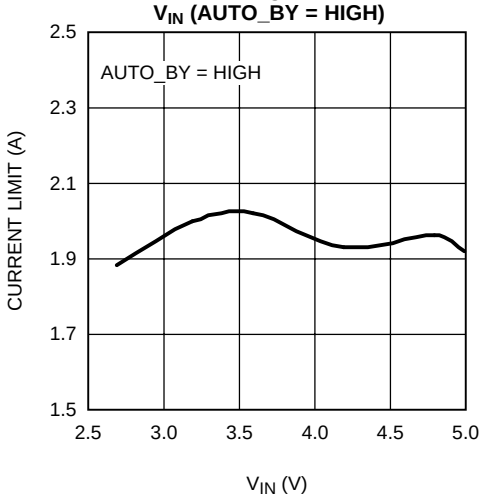

Figure 6.

VCON vs V_{OUT}

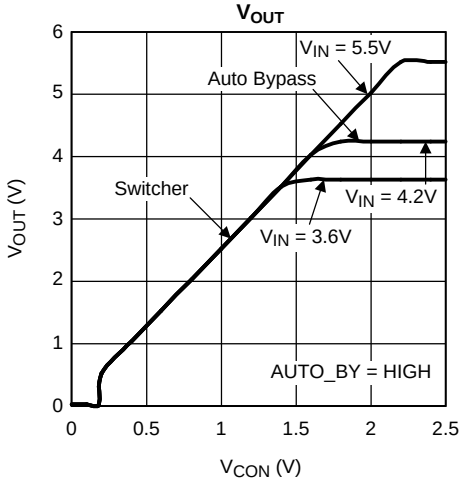

Figure 7.

V_{IN} - V_{OUT} vs I_{OUT} (AUTO_BY = LOW)

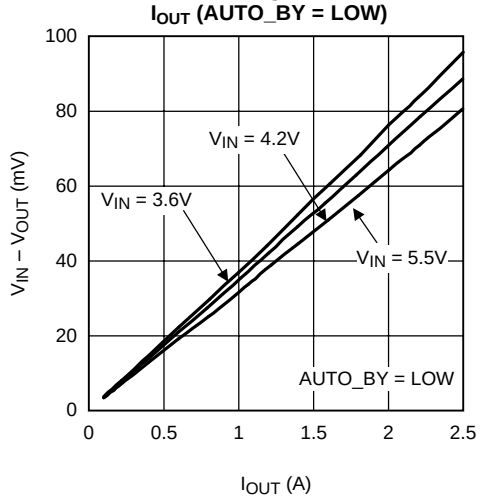

Figure 8.

Load Transient (AUTO_BY = HIGH, V_{IN} = 4.2V, V_{OUT} = 0.8V, I_{LOAD} = 0 - 1.5A)

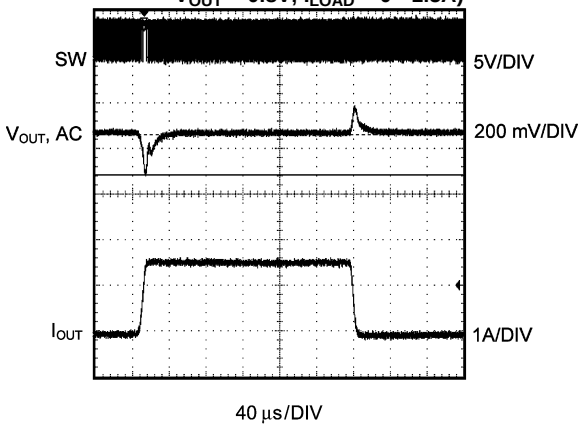

Figure 9.

Load Transient (AUTO_BY = HIGH, V_{IN} = 4.2V, V_{OUT} = 3.4V, I_{LOAD} = 0 - 1.5A)

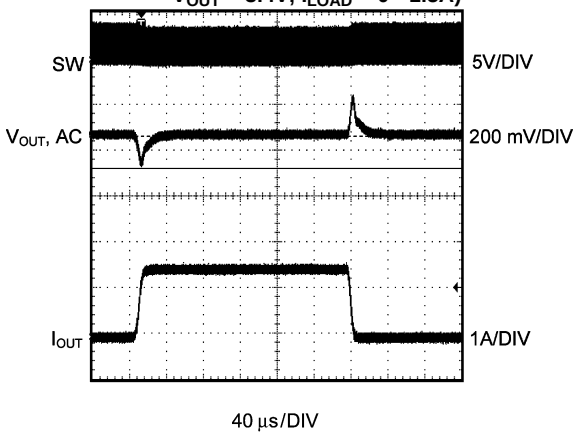

Figure 10.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Load Transient
(AUTO_BY = LOW, V_{IN} = 3.6V, I_{LOAD} = 0 - 1.5A)

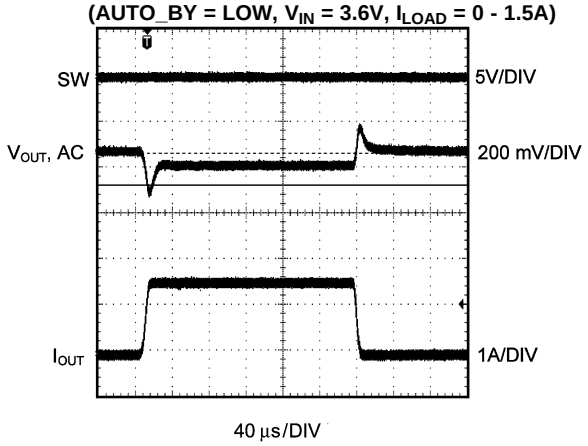

Figure 11.

Load Transient
(AUTO_BY = LOW, V_{IN} = 4.2V, I_{LOAD} = 0 - 1.5A)

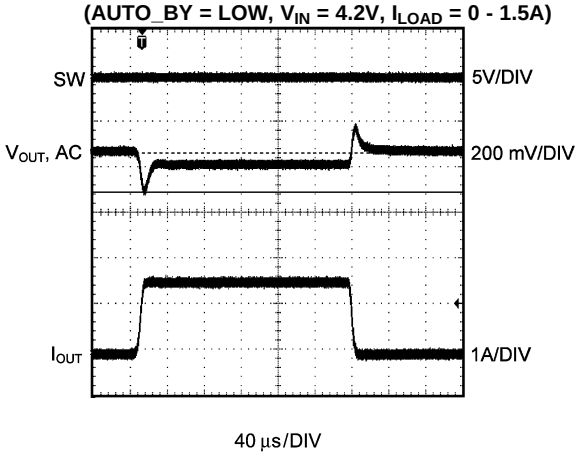

Figure 12.

Start-up (AUTO_BY = HIGH, V_{IN} = 4.2V, V_{OUT} = 3.4V, R_{LOAD} = 10 kΩ)

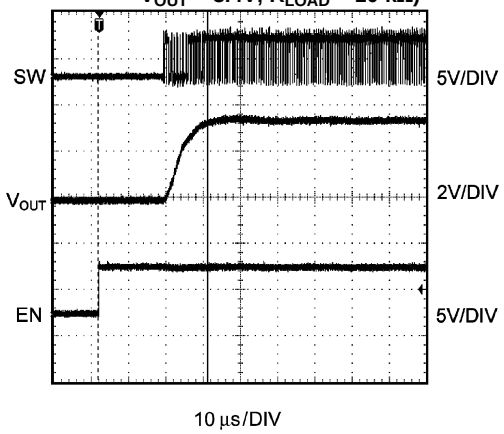

Figure 13.

Start-up (AUTO_BY = HIGH, V_{IN} = 3.6V, V_{OUT} = 1.0V, R_{LOAD} = 10 kΩ)

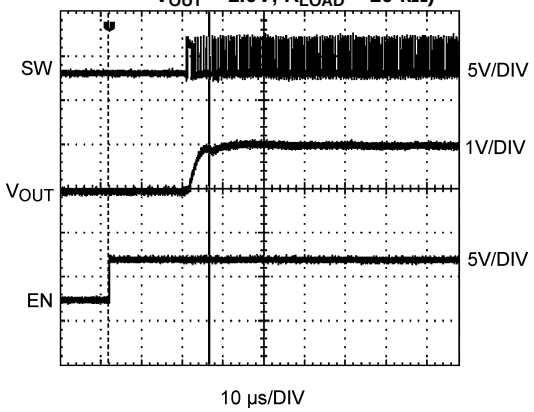

Figure 14.

AUTO_BY Start-up
(EN = LOW, V_{IN} = 3.6V, R_{LOAD} = 10 kΩ)

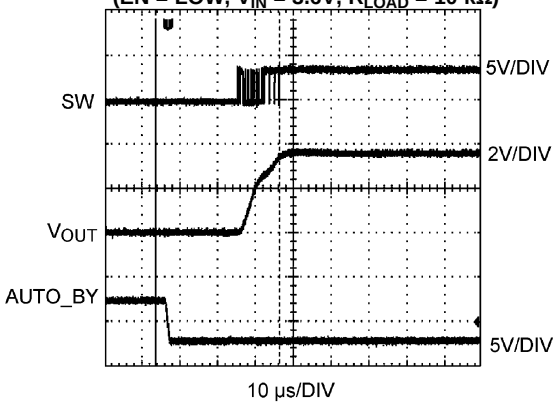

Figure 15.

AUTO_BY Start-up
(EN = LOW, V_{IN} = 4.2V, R_{LOAD} = 10 kΩ)

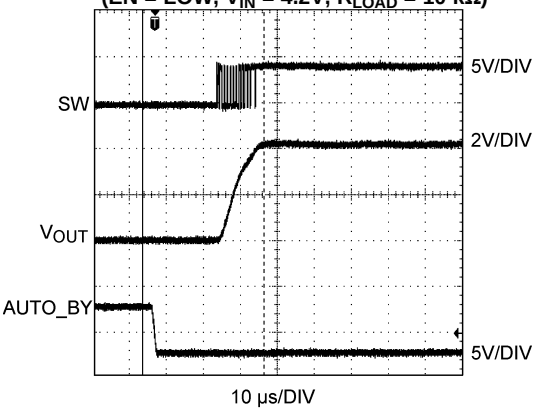

Figure 16.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Shutdown (AUTO_BY = HIGH, V_{IN} = 4.2V, V_{OUT} = 3.4V, R_{LOAD} = 10 kΩ)

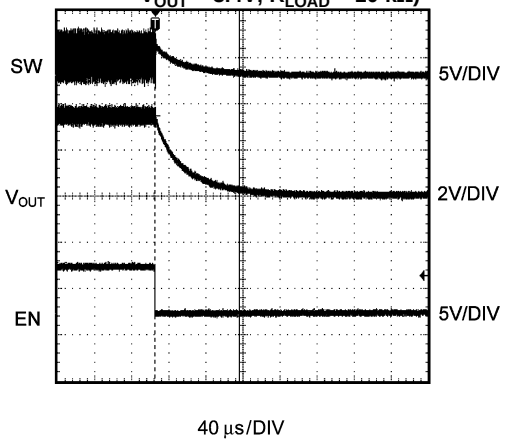

Figure 17.

Line Transient (AUTO_BY = HIGH, V_{IN} Step from 2.7V to 3.4V, V_{OUT} = 2.5V, R_{LOAD} = 6.8Ω)

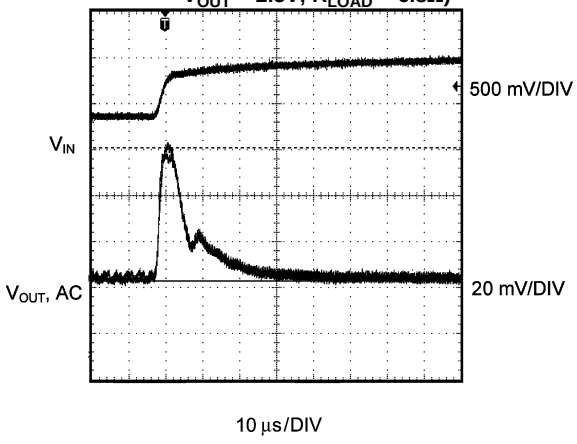

Figure 18.

VCON Transient (AUTO_BY = HIGH, V_{IN} = 4.2, V_{OUT} from 1V to 3.4V, R_{LOAD} = 6.8Ω)

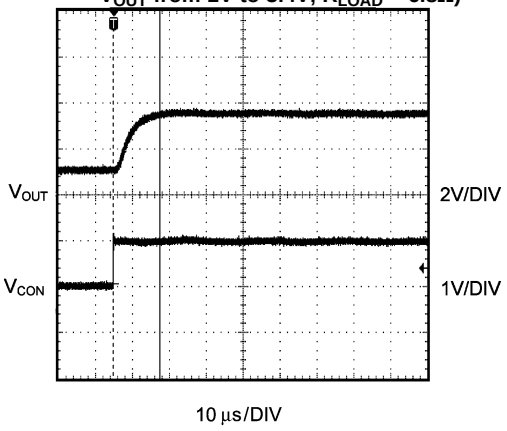

Figure 19.

Timed Current Limit Response

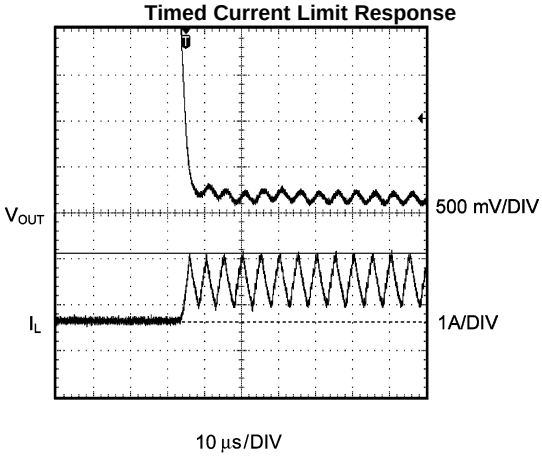

Figure 20.

Output Voltage Ripple (V_{IN} = 3.6V, V_{OUT} = 1.0V, I_{LOAD} = 100 mA)

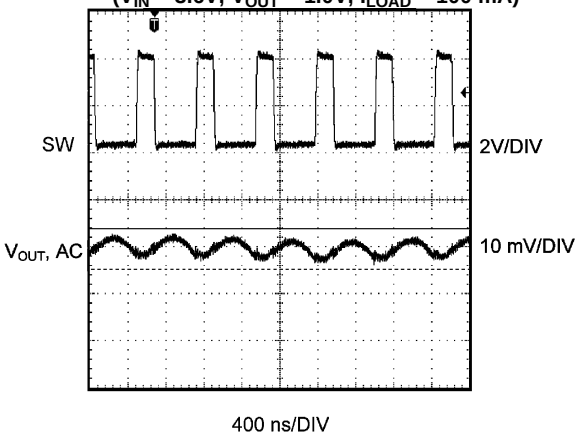

Figure 21.

Output Voltage Ripple (V_{IN} = 3.6V, V_{OUT} = 3.4V, I_{LOAD} = 100 mA)

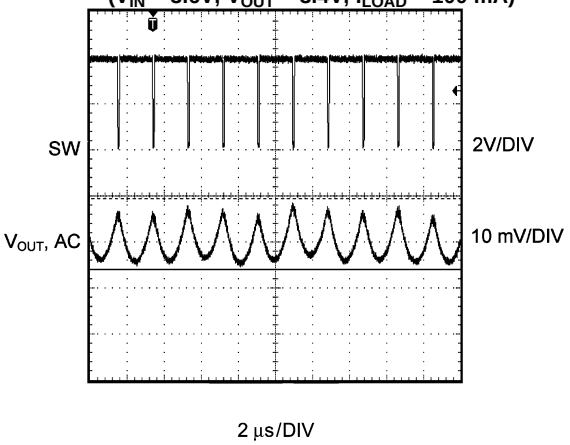

Figure 22.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

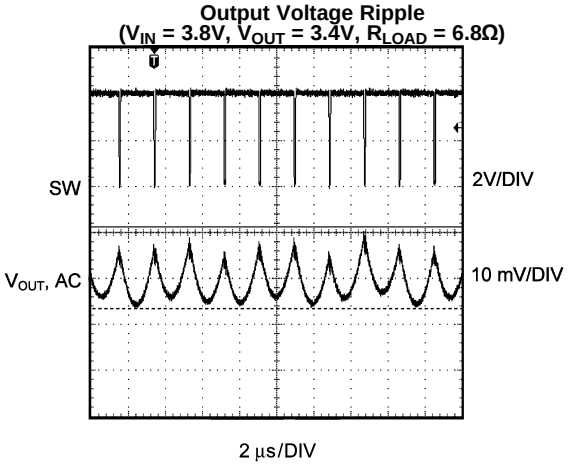

Figure 23.

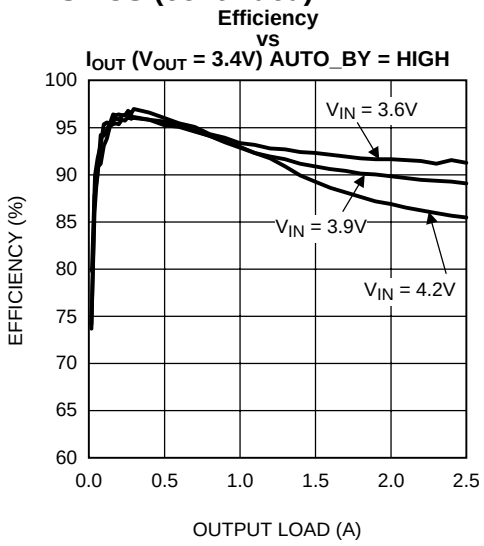

Figure 24.

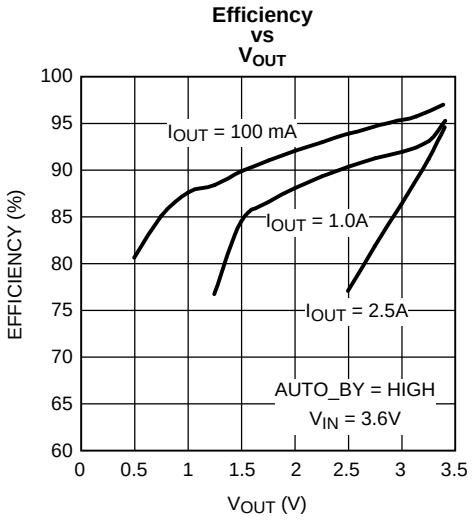

Figure 25.

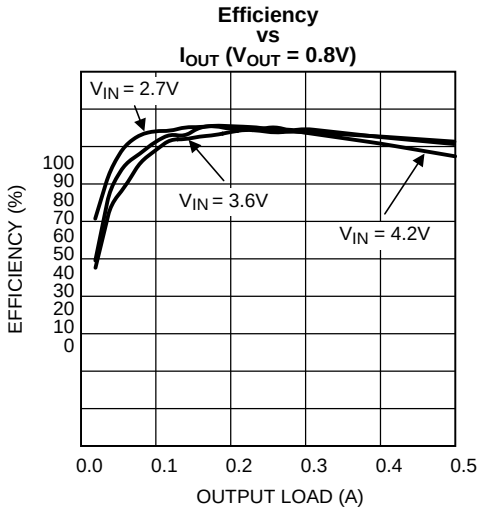

Figure 26.

OPERATION DESCRIPTION

The LM3212 is a simple step-down DC-DC converter optimized to power the RF power amplifier (PA) in cell-phones, portable communication devices, or battery powered RF devices. The LM3212 is designed to allow the RF PA to operate at maximum efficiency over a wide range of power levels and to operate efficiently with a single Li-ion battery.

The unique Active Current Bypass (ACB) circuit optimizes the efficiency and size requirements of the power supply for GSM PA operation. It allows for an inductor with relaxed saturation current and DCR requirements, thus allowing for a smaller form factor than would otherwise be possible. The Active Current Bypass enables the converter to respond to a fast load transients of 2.5A by assisting the switcher before it reaches its current limit. Similarly, it will also produce faster VCON output voltage transition times. The ACB also performs the function of analog bypass. Depending upon input voltage, output voltage and load current, the Active Current Bypass circuit automatically transitions the converter into and out of ACB by applying no more assistance than is needed. Transitions including analog bypass are done with minimal output voltage disturbance.

The LM3212 operates either in Fixed-frequency PWM mode (with auto analog bypass mode) or in forced bypass mode. The fixed-frequency PWM mode provides high efficiency and minimizes interference. The LM3212 can be forced into bypass mode by setting AUTO_BY pin low (see SHUTDOWN MODE). The shutdown mode turns the LM3212 off and reduces current consumption to 0.02 µA (typ). The LM3212 implements a unique R_{DSON} management scheme for V_{OUT} < 1.25V . The LM3212 can dynamically program the output voltage from 0.5V (typ.) to 3.4V (typ.) by adjusting the voltage on the VCON pin. Dynamic voltage adjustment and the unique R_{DSON} management scheme ensures efficient operation for all power levels of PA operation. Current overload protection and thermal overload shutdown are also provided.

The DSBGA package is best suited for applications within cases that are opaque to red and infrared light; it requires special design considerations for implementation. (Refer to DSBGA Package Assembly And Use section). As the LM3212 does not implement UVLO, the system controller should set EN low and set AUTO_BY high or floating during power-up and UVLO conditions. (Refer to SHUTDOWN MODE below).

CIRCUIT OPERATION

Initially the controller turns the internal PFET ON, allowing the current to flow from the input to the output filter through the inductor. The inductor current starts ramping up with a slope of $(V_{IN} – V_{OUT})/L$, thus storing magnetic energy. When the inductor current reaches the current required by the controller, the controller turns OFF the PFET and turns ON the NFET. The inductor current starts ramping down with a slope of V_{OUT}/L. The output filter capacitor stores charge as the inductor current rises and releases energy as the inductor current falls, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time. The circuit generates a duty-cycle modulated rectangular signal that is averaged using a low pass filter. The output voltage will be equal to the average of the duty-cycle modulated rectangular signal.

PWM OPERATION

In PWM (Pulse Width Modulation) mode, the switching frequency is constant. The current control architecture, in PWM mode, regulates the output by changing the energy per cycle to support the load required. Energy per cycle to the load is controlled by modulating the PFET on-time, which controls the peak inductor current. In current control architecture, the inductor current is compared with the slope compensated error signal of the error amplifier. At the rising edge of clock, the PFET is turned ON, ramping up the current with a slope of $(V_{IN} – V_{OUT})/L$. PFET is ON until the inductor current equals the error signal. Then the PFET is turned OFF and the NFET is turned ON, ramping down the current with a slope of V_{OUT}/L. At the next rising edge of clock, the cycle repeats. An increase of load pulls the output voltage down, increasing the error signal. As the error signal is more, the peak inductor current is higher, increasing the average inductor current and responds to the increased load. To ensure stability, a slope compensation ramp is subtracted from the error signal. The minimum on-time of the PFET is 48 ns (typ.)

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SHUTDOWN MODE

To shutdown the LM3212 pull the EN pin low (<0.5V) and AUTO_BY pin must be high or floating. In the shutdown mode, the current consumption is 0.02 µA (typ). In shutdown mode, PFET switch, NFET synchronous rectifier, reference voltage source, control and bias circuit are turned OFF. To enable LM3212 pull EN high (>1.2V) and the mode of operation will be dependent on the state of AUTO_BY pin. If AUTO_BY pin is set low it will force the part to be powered up independent of the state of the EN pin and LM3212 will start up in Forced Bypass Mode.

As the LM3212 does not implement UVLO (Under Voltage Lock-Out) circuit, the EN pin should be set LOW and AUTO_BY should be either HIGH or floating to turn off the LM3212 during power-up and during UVLO conditions. For cell-phone applications, the system controller determines the power supply sequence and space constraints do not allow the inclusion of UVLO Circuit.

INTERNAL SYNCHRONOUS RECTIFICATION

The LM3212 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and to increase efficiency. The reduced forward voltage drop in the internal NFET synchronous rectifier significantly improves efficiency for low output voltage operation. The NFET is designed to conduct through its intrinsic body diode during transient interval, eliminating the need of an external diode.

$R_{DSON(P)}$ MANAGEMENT

The LM3212 has a unique $R_{DSON(P)}$ management function to improve efficiency for output voltage lower than 1.25V. For VCON less than 0.50V (typ.), the LM3212 uses only a small part of the PFET. For VCON greater than 0.52V (typ.), the entire PFET is used to minimize $R_{DSON(P)}$ loss. The threshold has 20 mV of hysteresis.

$V_{CON,ON}$

The output is disabled when VCON is below 125 mV (typ.). It is enabled when VCON is above 150 mV (typ.). The threshold has 25 mV (typ.) of hysteresis.

CURRENT LIMIT

The LM3212 current limit feature protects the converter during current overload condition. Both SW and ACB pins have positive and negative current limits. The positive and negative current limits limit the SW and ACB currents in both directions. SW pin has two positive current limits. The $I_{LIM,PFET\ Steady\text{-}State}$ is current limit that triggers the ACB circuit. Once the peak inductor current crosses $I_{LIM,PFET\ SteadyState}$, the ACB circuit starts assisting the switcher and provides enough current to prevent the SW current from hitting $I_{LIM,PFET\ Steady\text{-}State}$, allowing the switcher to operate at maximum efficiency. The output voltage starts falling only after both SW and ACB pin's current reach their respective current limit of $I_{LIMPFET\ Peak}$ and $I_{LIM,P_ACB,GSM}$ respectively.

TIMED CURRENT LIMIT

If the load pulls the output voltage below 0.375V, the LM3212 switches to a timed current limit mode. In this mode the internal PFET switch is turned OFF after the current limit comparator trips and the beginning of the next cycle is inhibited for 3.5 µs to force the instantaneous inductor current to ramp down. The synchronous rectifier is always OFF in timed current limit mode. The timed current limit prevents the loss of current control when the output voltage is pulled low under serious overload conditions. The ACB is disabled during timed current limit mode.

ACTIVE CURRENT ASSIST

GSM PA time mask requirement needs high current to be sourced or sinked from the LM3212. These high currents are required for fast output voltage transients or under a heavy load. Over-rating the switching inductor for a transient current will increase the solution size and will not be an optimum solution. So to allow an optimal inductor size for such a load, an alternate current path is provided through the ACB pin. Once the switcher current limit $I_{LIM,PFET\ Steady\text{-}State}$ is reached, ACB starts providing additional current to the load. The ACB circuit also minimizes the dropout voltage by having the analog Bypass FET in parallel with V_{OUT}.

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BYPASS FUNCTION

The Active Current Bypass Circuit provides an analog bypass function with very low dropout resistance (33 mΩ typ.) for $V_{IN} \geq V_{OUT}$. When AUTO_BY pin is set high (preferred mode) the part will be in automatic analog bypass mode which will automatically increase and decrease the amount of bypass resistance as needed. In analog bypass mode, the switcher will stay in regulation until full bypass is reached and it drops out. To override the automatic bypass mode, either set VCON > (V_{IN})/(2.5), VCON should not be higher than V_{IN}, or set AUTO_BY = 0V, for forced bypass function. The Bypass pin can be controlled by a GPIO pin. Forced bypass function is valid for $0V < V_{IN} < 5.5V$. In bypass mode, the ACB provides current to the output in parallel with the switcher output for a minimum drop-out resistance. The LM3212 can provide up to 2.5A of current in bypass mode with a 3.2A current limit.

DYNAMICALLY ADJUSTABLE OUTPUT VOLTAGE

The LM3212 can dynamically adjust output voltage by changing the voltage on VCON pin. The feedback voltage changes from $V_{FB,MIN}$ to $V_{FB,MAX}$ depending upon voltage on VCON pin. In PA applications, peak power is required when the handset is far away from the base station. Power requirement is lower in other instances. To maximize power savings, LM3212 output should be set just high enough to achieve desired PA linearity. Hence, during low-power requirements, reduction of supply voltage to PA can reduce power consumption from PA, making the operation more efficient and promote longer battery life. See the SETTING THE OUTPUT VOLTAGE section for further details. LM3212 goes into pulse skipping mode if off-time of PFET is below 20 ns (typ.), increasing the output voltage ripple slightly.

THERMAL OVERLOAD PROTECTION

The LM3212 has a thermal overload protection function that protects the converter from short-term misuse and overload conditions. If the junction temperature exceeds 150°C, the LM3212 shuts down. Normal operation resumes after the temperature drops below 130°C. Prolonged operation in thermal overload condition may damage the device and is considered bad practice.

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APPLICATION INFORMATION

SETTING THE OUTPUT VOLTAGE

DAC Control

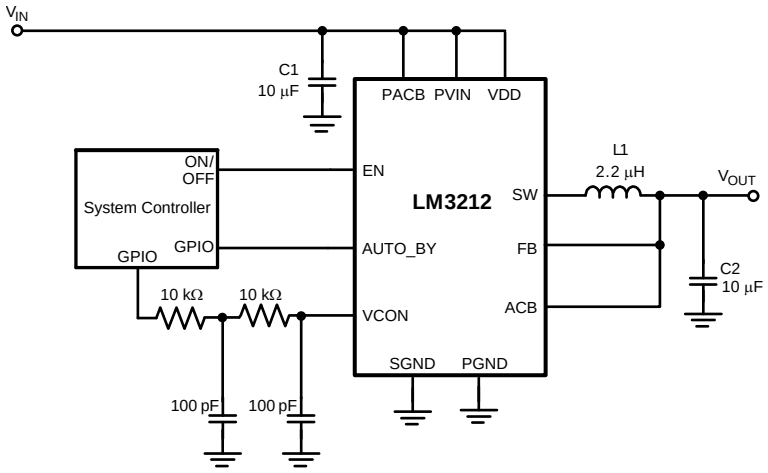
An analog voltage to the VCON pin can dynamically program the output voltage from 0.5V (typ.) to 3.4V (typ.) without the need for external resistors. The output voltage is governed by Table 1.

Table 1. Output Voltage Selection

VCON (V)	V_{OUT} (V)
VCON = 0.20 to 1.36	2.5 x VCON

Output voltage is regulated according to Table 1 only for 0.20V < VCON < 1.36V. For VCON < 0.32V, the output voltage may not regulate due to dropout conditions. The output voltage can go lower than 0.8V for a limited V_{IN} range (V_{OUT} = 0.5V for V_{IN} ≤ 4.2V). Refer to the datasheet curve in GSM startup sections (VCON Voltage vs. Output Voltage) for details. For VCON < 0.15V (typ.), the switches turn OFF. The quiescent current for VCON = LOW and V_{EN} = HI is 800 µA.

Dynamic Adjustment of Output Voltage with GPIO



GPIO Control

Dynamic Adjustment of Output Voltage with GPIO shows the application circuit that enables the LM3212 to dynamically adjust the output voltage using a GPIO pin from the system controller. The PWM signal of the GPIO is filtered using a low-pass filter and fed to the VCON pin. As the duty ratio of the PWM signal changes, the voltage on the VCON pin changes. So, the duty ratio on the GPIO pin can dynamically adjust the output voltage. The double low-pass filter reduces the ripple at VCON below 5 mV to avoid any oscillation at the output voltage.

Equation 1 governs the relationship between output voltage and PWM duty cycle. Refer to datasheet curves section for further details.

$$V_{OUT} = V * D * 2.5 \quad (1)$$

V_{OUT} = Output Voltage

D = Duty Cycle of PWM

V = GPIO peak voltage

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INDUCTOR SELECTION

For 2G operation it is recommended to use a 2.2 µH inductor with I_{SAT} above 1.5A (30% reduction in L). In the case of GSM / EDGE where the current bursts during transmission, the effective overall RMS current requirement should reduce. Therefore, it is wise to consult with the inductor manufacturers to determine if some of their smaller components will meet your application needs even though the classical inductor specification does not appear to meet the LM3212 RMS current specifications.

LM3212 manages the inductor Peak and RMS (or steady current peak) current through the SW pin automatically. The SW pin has two positive current limits. The first is the 1.9A typical (or 2.1A maximum) $I_{LIMPFET\ Peak}$ over-limit current protection. It limits the maximum peak inductor current during large signal transients (i.e., < 20 µs). For this reason it is also recommended that the selected inductor performance does not degrade severely at 2.1A. The second is at 1.45A typical (or 1.65A maximum) steady-state peak-current limit ($I_{LIM,PFET\ Steady\text{-}State}$ as detailed in the Electrical Characteristics). The ACB circuit automatically adjusts its output current to keep the steady-state inductor current below the steady-state peak current limit. Thus, the inductor RMS current will effectively always be less than the $I_{LIM,PFET\ Steady\text{-}State}$ during the transmit burst. In addition, as in the case with GSM / EDGE where the output current comes in bursts, the effective overall RMS current requirement would be much lower.

For low-cost applications, an unshielded bobbin inductor is suggested and for noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to layout the board with footprints accommodating both types for design flexibility. This allows substitution of a low-noise toroidal inductor in the event that noise from low-cost bobbin models is unacceptable. Saturation occurs when the magnetic flux density from the current through the windings of the inductor exceeds what the inductor's core material can support with a corresponding magnetic field. This can cause poor efficiency or regulation errors from DC-DC converters such as the LM3212.

For good efficiency, the inductor's resistance should be less than 0.2Ω, low DCR inductors (<0.2Ω) are recommended. Table 2 suggests some inductors and suppliers.

Table 2. Suggested Inductors and Their Suppliers

Model	Vendor	Size
PST25201T-2R2M5	Cyntec Co.	2.5 mm x 2.0 mm, 1.0 mm height
CIG22H2R2MNE	Samsung	2.5 mm x 2.0 mm, 1.2 mm height
VLS252010T-2R2M	TDK	2.5 mm x 2.0 mm, 1.0 mm height
VLS252012T-2R2M	TDK	2.5 mm x 2.0 mm, 1.2 mm height
1239AS-H-2R2N (DFE252012C)	Toko	2.5 mm x 2.0 mm, 1.2 mm height

CAPACITOR SELECTION

The LM3212 is designed for ceramic capacitors for its input and output filters. Use a 10 µF ceramic capacitor for the input and a 10 µF ceramic total output capacitance. Ceramic capacitor types such as X5R, X7R are recommended for both filters. These provide an optimal balance between small size, cost, reliability and performance for cell phones and similar applications. Table 3 lists suggested part numbers and suppliers. DC bias characteristics of the capacitors must be considered while selecting the voltage rating and case size of the capacitor. Smaller case sizes for the output capacitor mitigate piezo-electric vibrations of the capacitor when the output voltage is stepped up and down at fast rates. However they have a bigger percentage drop in value with dc bias. Use of multiple 2.2 µF or 1µF capacitors can also be considered. For RF Power Amplifier applications, split the output capacitor between DC-DC converter and RF Power Amplifier(s). (4.7 µF + 4.7 µF is recommended.) The optimum capacitance split is application dependent; for stability the total capacitance should be approximately 10 µF. Place all the output capacitors very close to their respective device.

Table 3. Suggested Capacitors And Their Suppliers

Model	Vendor
C1608X5R0J106M, 10 µF, 6.3V	TDK
C1608JB0J225M, 2.2 µF, 6.3V	TDK
C1608JB0J475K, 4.7 µF, 6.3V	TDK

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The input filter capacitor supplies AC current drawn by the PFET switch of the LM3212 in the first part of each cycle and reduces the voltage ripple imposed on the input power source. The output filter capacitor absorbs the AC inductor current, thus maintaining a steady output voltage during transient load changes and reducing output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR (Equivalent Series Resistance) to perform these functions. The ESR of the filter capacitors is generally a major factor in voltage ripple.

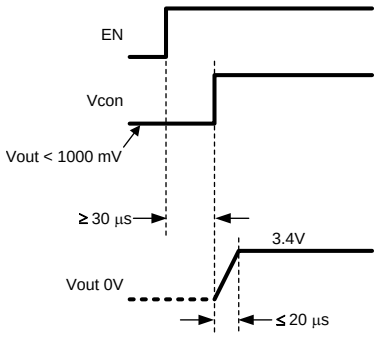
EN PIN CONTROL

Use the system controller to drive the EN HIGH or LOW with a comparator, Schmitt trigger or logic gate. Set EN HIGH (>1.2V) for normal operation and LOW (<0.5V) for shutdown mode to reduce current consumption to 0.02 µA (typ.) current. Note: Forced Bypass Mode (AUTO_BY = 0V) overrides the EN pin.

STARTUP

The Startup Diagram below shows the startup condition, with AUTO_BY = HIGH. During startup, it is best to put EN HIGH for at least 30 µs before VCON is pulled HIGH as various functional blocks in LM3212 require up to 30 µs to start. During the initial 30 µs, the output is in high impedance state (output voltage is 0V if a load is present). Once all the functional blocks are turned ON, the VCON is set to desired level to set the output voltage. The output voltage settles within 20 µs after the VCON voltage is applied. If VCON is high before EN, output transitions within 50 µs.

Startup Diagram

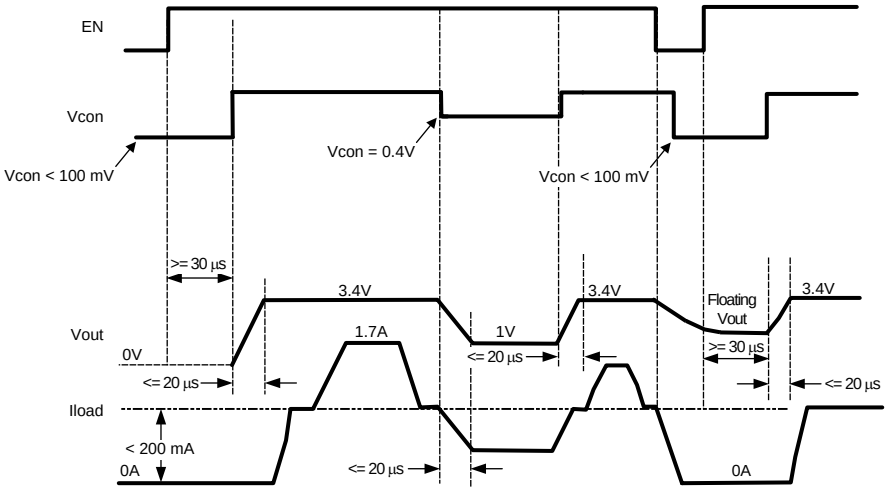


GSM MULTIPLE BURSTS OPERATION

The LM3212 handles GSM multiple-burst operation in the following two ways:

Method 1

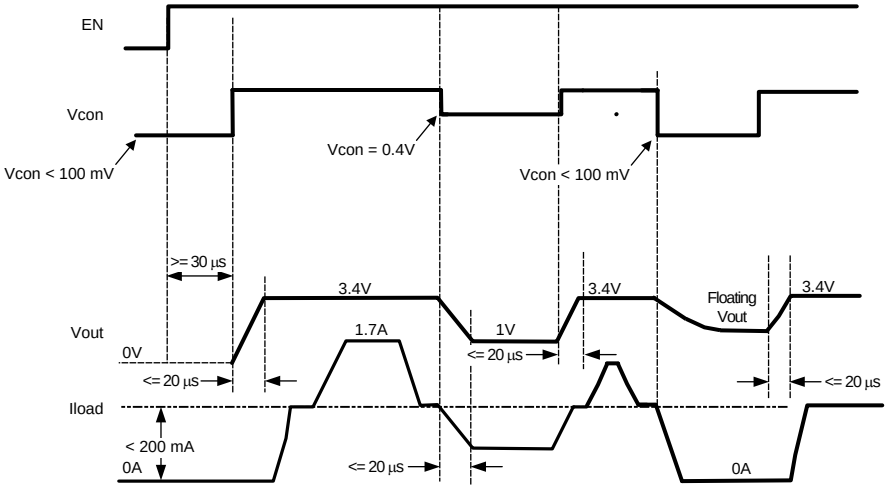
GSM Multiple-Burst Operation Using EN and VCON



Method 2

Use EN and VCON to power down if the GSM timing allows for the extra time. shows an operation where EN is pulled HIGH followed by two GSM burst. After the GSM burst, a complete power down is followed by a power up. The figure below shows the expected response from the LM3212.

GSM Multiple-Burst Operation Using VCON



If the GSM timing does not allow for a complete power down between bursts then use the VCON to either set a new output voltage or conduct a partial power down. shows a power up, followed by two bursts and then a partial power down (~ 0.8 mA I_q) and finally a power up.

DSBGA Package Assembly And Use

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in Texas Instruments Application Note 1112 SNVA009. Refer to the section *Surface Mount Technology (SMD) Assembly Considerations.* For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device.

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The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See Application Note 1112 SNVA009 for specific instructions how to do this.

The 16–bump package used for LM3212 has 300 micron solder balls and requires 10.82 mil pads for mounting the circuit board. The trace to each pad should enter the pad with a 90°entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 6-7 mil wide, for a section approximately 6 mil long or longer, as a thermal relief. Then each trace should neck up or down to its optimal width. An important criterion is symmetry to insure the solder bumps on the LM3212 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps B3, C3 and D3. Because PGND and PVIN are typically connected to large copper planes, inadequate thermal reliefs can result in late or inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges that are sensitive to light in the read and infrared range shining on the package's exposed die edges.

Board Layout Considerations

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and the board pads, which can result in erratic or degraded performance. Good layout for the LM3212 can be implemented by following a few simple design rules.

1. Place the LM3212 on 10.82 mil pads. As a thermal relief, connect to each pad with a 7 mil wide, approximately 7 mil long traces, and then incrementally increase each trace to its optimal width. The important criterion is symmetry to insure the solder bumps on the LM3212 re-flow evenly (see DSBGA Package Assembly And Use).
2. Place the LM3212, inductor and filter capacitors close together and make the trace short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Place the capacitors and inductor within 0.2 inch (5 mm) of the LM3212.
3. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor through the LM3212 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground through the LM3212 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
4. Connect the ground pins of the LM3212 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3212 by giving it a low-impedance ground connection.
5. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
6. R_{OUT} noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components. The voltage feedback trace must remain close to the LM3212 circuit and should be routed directly from FB to V_{OUT} at the output capacitor and should be routed opposite to noise components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.
7. Split up output capacitors between LM3212 output and PA(s). Suggestion is to place one-half of output capacitance as close as possible to LM3212 output and the rest as close as possible to PA(s).

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3212TL/NOPB	ACTIVE	DSBGA	YZR	16	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	3212	Samples
LM3212TLX/NOPB	ACTIVE	DSBGA	YZR	16	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	3212	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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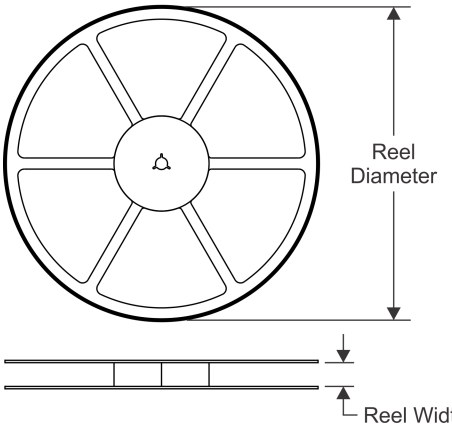
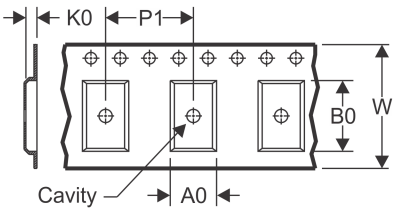
TAPE AND REEL INFORMATION

REEL DIMENSIONS

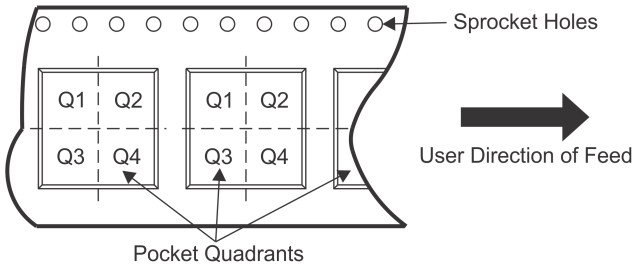


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

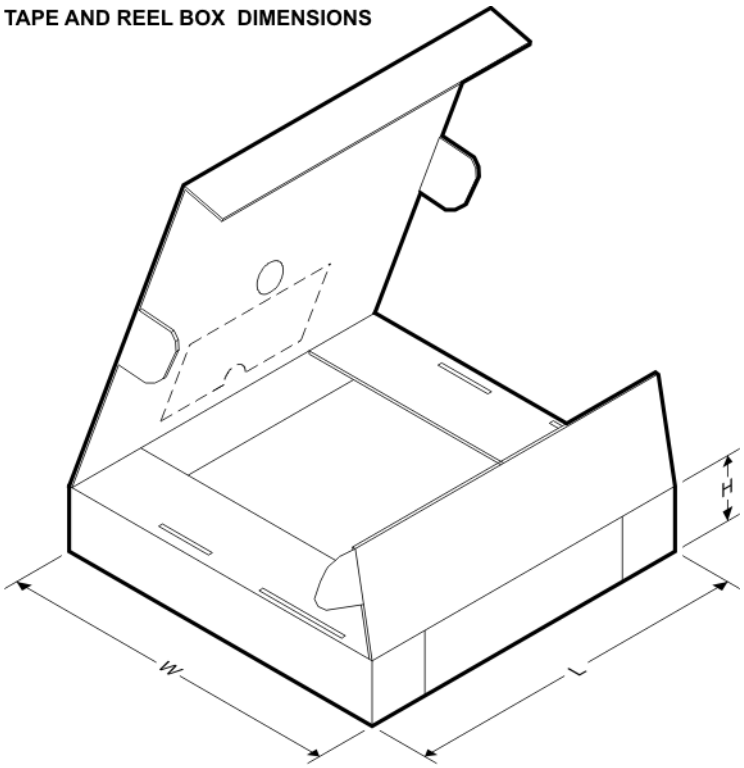
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3212TL/NOPB	DSBGA	YZR	16	250	178.0	8.4	2.43	2.48	0.75	4.0	8.0	Q1
LM3212TLX/NOPB	DSBGA	YZR	16	3000	178.0	8.4	2.43	2.48	0.75	4.0	8.0	Q1

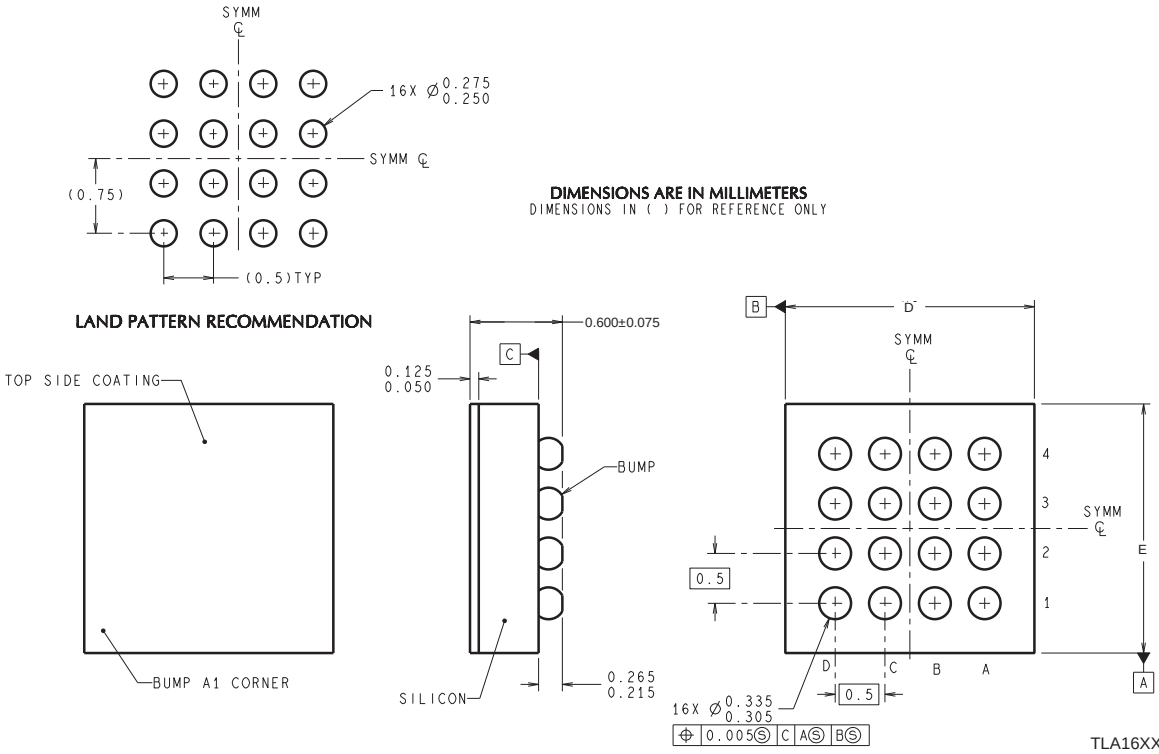
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3212TL/NOPB	DSBGA	YZR	16	250	210.0	185.0	35.0
LM3212TLX/NOPB	DSBGA	YZR	16	3000	210.0	185.0	35.0

YZR0016



D: Max = 2.326 mm, Min =2.266 mm

E: Max = 2.226 mm, Min =2.165 mm

4215051/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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