

PRECISION, GAIN OF 0.2 LEVEL TRANSLATION DIFFERENCE AMPLIFIER

FEATURES

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- Gain of 0.2 to Interface ±10-V Signals to Single-Supply ADCs
- Gain Accuracy: ±0.024% (max)
- Wide Bandwidth: 1.5 MHz
- High Slew Rate: 15 V/µs
- Low Offset Voltage: ±100 μV
- Low Offset Drift: ±1.5 μV/°C
- Single-Supply Operation Down to 1.8 V

APPLICATIONS

- Industrial Process Controls
- Instrumentation
- Differential to Single-Ended Conversion
- Audio Line Receivers

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (-55°C/125°C) Temperature Range⁽¹⁾
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability
- (1) Additional temperature ranges are available contact factory

DESCRIPTION

The INA159 is a high slew rate, G = 1/5 difference amplifier consisting of a precision op amp with a precision resistor network. The gain of 1/5 makes the INA159 useful to couple ±10-V signals to single-supply analog-to-digital converters (ADCs), particularly those operating on a single +5-V supply. The on-chip resistors are laser-trimmed for accurate gain and high common-mode rejection. Excellent temperature coefficient of resistance (TCR) tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. The input common-mode voltage range extends beyond the positive and negative supply rails. It operates on a total of 1.8-V to 5.5-V single or split supplies. The INA159 reference input uses two resistors for easy mid-supply or reference biasing.

The difference amplifier is the foundation of many commonly-used circuits. The INA159 provides this circuit function without using an expensive external precision resistor network. The INA159 is available in an MSOP-8 surface-mount package and is specified for operation over the extended industrial temperature range, -55°C to 125°C.



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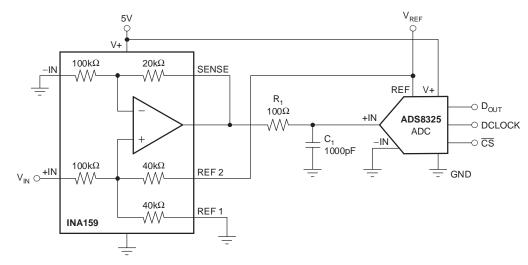


Figure 1. Typical Application



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

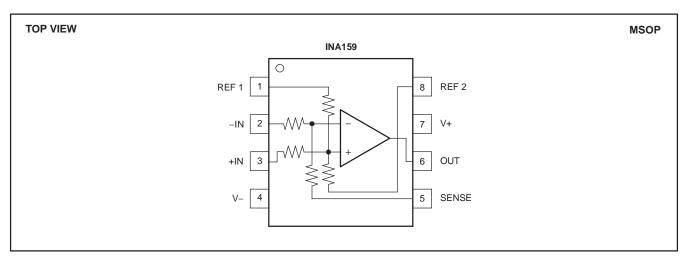
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

TEMPERATURE	ORDERABLE PART NUMBER ⁽²⁾	PACKAGE LEAD	PACKAGE DESIGNATOR	TOP-SIDE MARKING	
-55°C to 125°C	INA159AMDGKTEP	MSOP-8 Tape and reel	DGK	OAA	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.





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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage			+5.5	V
Signal input terminals (-IN and +IN), voltage			±30	V
Reference (REF 1 and REF2) and sense pins	Current		±10	mA
	Voltage	(V–) – 0.5	(V+) + 0.5	V
Output short circuit			Continuous	
Operating temperature		-55	+125	°C
Storage temperature		-65	+150	°C
Junction temperature			+150	°C
ESD rating	Human-Body Model		4000	V
	Charged-Device Model		1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.



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ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, $T_A = -55^{\circ}C$ to $+125^{\circ}C$. At $T_A = +25^{\circ}C$, $R_L = 10 \text{ k}\Omega$ connected to $V_S/2$, REF pin 1 connected to ground, and REF pin 2 connected to $V_{REF} = 5 \text{ V}$, unless otherwise noted.

PARAMETER	CONDITIONS		NA159	UNIT
		MIN	TYP MAX	
OFFSET VOLTAGE ⁽¹⁾	RTO			
Initial ⁽¹⁾ V _{OS}	$V_{S} = \pm 2.5 V$, Reference and Input Pins Grounded		±100 ±500	μV
Over Temperature			±1450	μ
vs Power Supply PSRR	$V_{S} = \pm 0.9 \text{ V}$ to $\pm 2.75 \text{ V}$		±20 ±100	μV/V
Over Temperature PSRR	$V_{S} = \pm 0.9 \text{ V to } \pm 2.75 \text{ V}$		±200	μV/V
Reference Divider Accuracy ⁽²⁾			±0.002 ±0.024	%
over Temperature			±0.002 ±0.050	%
INPUT IMPEDANCE ⁽³⁾				
Differential			240	kΩ
Common-Mode			60	kΩ
INPUT VOLTAGE RANGE	RTI			
Common-Mode Voltage Range V _{CM}				
Positive			17.5	V
Negative			-12.5	V
Common-Mode Rejection Ratio CMRR	$V_{CM} = -10$ V to +10 V, $R_S = 0$ Ω	80	96	dB
over Temperature		74	94	dB
	RTO			
f = 0.1 Hz to 10 Hz			10	μVPP
f = 10 kHz			30	nV/√Hz
GAIN	$ \begin{array}{l} V_{REF2} = 4.096 \ V, \\ R_L \ Connected \ to \ GND, \\ (V_{IN+}) - (VIN-) = -10 \ V \ to \ +10 \ V, \\ V_{CM} = 0 \ V \end{array} $			
Initial G			0.2	V/V
Error			±0.005 ±0.024	%
vs Temperature			±0.035	%
Nonlinearity			±0.0002	% of FS
OUTPUT				
Voltage, Positive	$V_{REF2} = 4.096 V,$ R _L Connected to GND	(V+) – 0.1	(V+) - 0.02	V
over Temperature	·	(V+) – 0.2		v
Voltage, Negative	$V_{REF2} = 4.096 V,$ R _L Connected to GND	(V–) + 0.048	(V–) + 0.01	V
over Temperature		(V–) + 0.070		v
Current Limit, Continuous to Common			±60	mA
Capacitive Load		See Typic	al Characteristic	pF
Open-Loop Output Impedance R _O	f = 1 MHz, I _O = 0		110	Ω
FREQUENCY RESPONSE				
Small-Signal Bandwidth	–3 dB		1.5	MHz
Slew Rate SR			15	V/µs
	4 V Output Step, C _L = 100 pF		1	μs

Includes effects of amplifier input bias and offset currents.
 Reference divider accuracy specifies the match between the reference divider resistors using the configuration in Figure 2.

(3)Internal resistors are ratio matched but have 20% absolute value.

(4) Includes effects of amplifier input current noise and thermal noise contribution of resistor network.

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ELECTRICAL CHARACTERISTICS (continued)

Boldface limits apply over the specified temperature range, $T_A = -55^{\circ}C$ to $+125^{\circ}C$. At $T_A = +25^{\circ}C$, $R_L = 10 \text{ k}\Omega$ connected to $V_S/2$, REF pin 1 connected to ground, and REF pin 2 connected to $V_{REF} = 5 \text{ V}$, unless otherwise noted.

	CONDITIONS		INA159			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	
Overload Recovery Time	50% Overdrive		250		ns	
POWER SUPPLY						
Specified Voltage Range V _S				+5	V	
Operating Voltage Range		+1.8		+5.5	V	
Quiescent Current I _Q	$I_O = 0$ mA, $V_S = \pm 2.5$ V, Reference and Input Pins Grounded		1.1	1.5	mA	
over Temperature				2.0	mA	
TEMPERATURE RANGE						
Specified Range		-55		+125	°C	
Operating Range		-55		+125	°C	
Storage Range		-65		+150	°C	
Thermal Resistance 0JA						
MSOP-8	Surface Mount		150		°C/W	

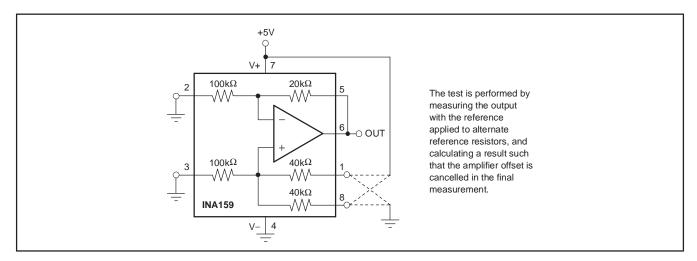
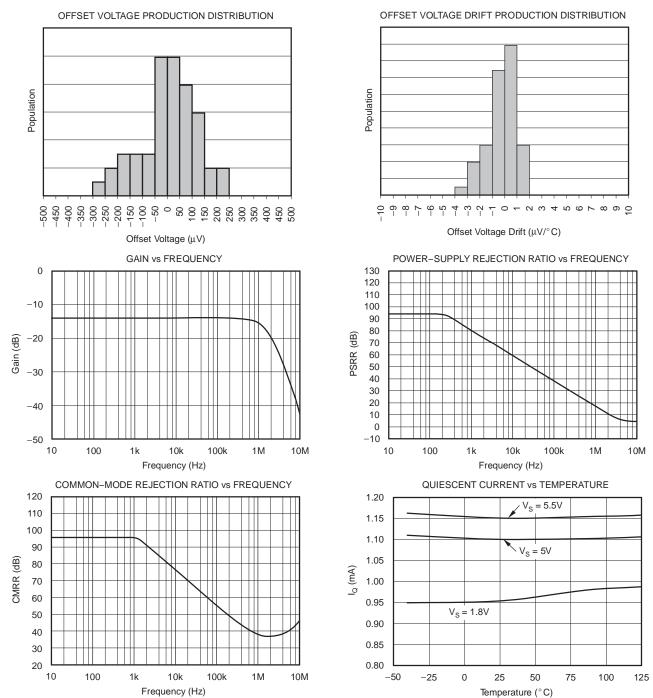


Figure 2. Test Circuit for Reference Divider Accuracy

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$$\label{eq:TYPICAL CHARACTERISTICS} \begin{split} \text{At } T_{\text{A}} = +25^{\circ}\text{C}, \ \text{R}_{\text{L}} = 10 \ \text{k}\Omega \text{ connected to } \text{V}_{\text{S}}\text{/2}, \ \text{REF pin 1 connected to ground, and REF pin 2 connected to } \text{V}_{\text{REF}} = 5 \ \text{V}, \\ \text{unless otherwise noted.} \end{split}$$





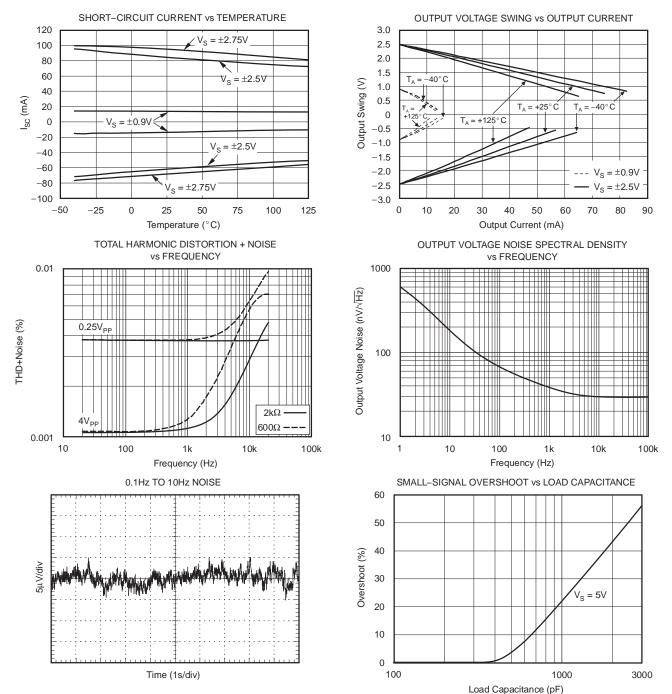
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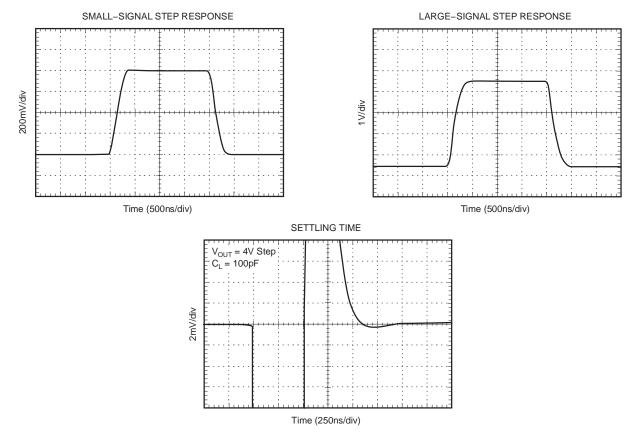
TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^{\circ}$ C, $R_L = 10 \text{ k}\Omega$ connected to $V_S/2$, REF pin 1 connected to ground, and REF pin 2 connected to $V_{REF} = 5 \text{ V}$, unless otherwise noted.



TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^{\circ}$ C, $R_L = 10 \text{ k}\Omega$ connected to $V_S/2$, REF pin 1 connected to ground, and REF pin 2 connected to $V_{REF} = 5 \text{ V}$, unless otherwise noted.



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INSTRUMENTS

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APPLICATION INFORMATION

The internal op amp of the INA159 has a rail-to-rail common-mode voltage capability at its inputs. A rail-to-rail op amp allows the use of ± 10 -V inputs into a circuit biased to 1/2 of a 5-V reference (2.5-V quiescent output). The inputs to the op amp will swing from approximately 400 mV to 3.75 V in this application.

The unique input topology of the INA159 eliminates the input offset transition region typical of most rail-to-rail complementary stage operational amplifiers. This allows the INA159 to provide superior glitch- and transition-free performance over the entire common-mode range.

Good layout practice includes the use of a $0.1\text{-}\mu\text{F}$ bypass capacitor placed closely across the supply pins.

COMMON-MODE RANGE

The common-mode range of the INA159 is a function of supply voltage and reference. Where both pins, REF1 and REF2, are connected together:

$$V_{CM+} = (V+) + 5[(V+) - V_{REF}]$$
(1)

$$V_{CM-} = (V-) - 5[V_{REF} - (V-)]$$
(2)

Where one REF pin is connected to the reference, and the other pin grounded (1/2 reference connection):

$$V_{CM+} = (V+) + 5[(V+) - (0.5V_{REF})]$$
(3)

$$V_{CM-} = (V-) - 5[(0.5V_{REF}) - (V-)]$$
 (4)

Some typical values are shown in Table 1.

Table 1. Common-Mode Range For Various Supply and Reference Voltages

REF 1 and REF 2 Connected Together									
V+	V-	V _{REF}	V _{REF} V _{CM+}						
5	0	3	15	-15					
5	0	2.5	17.5	-12.5					
5	0	1.25	23.75	-6.25					
1/2 Referen	1/2 Reference Connection								
V+	V-	V _{REF}	V _{CM+}	V _{CM} -					
5	0	5	17.5	-12.5					
5	0	4.096	19.76	-10.24					
5	0	2.5	23.75	-6.25					
3.3	0	3.3	11.55	-8.25					
3.3	0	2.5	13.55	-6.25					
3.3	0	1.25	16.675	-3.125					

4.096		2.048	0 -10	(±2V swing) 0.048
3.3		1.65	+10 0 -7.885	3.65 (–1.577V, +2V swing) 0.048
2.5	$V_{IN} \bigcirc \underbrace{+IN}_{VIN} \bigcirc \underbrace{100k\Omega}_{VIN} & \underbrace{40k\Omega}_{REF 2} \bigcirc V_{REF}$	1.25	+10 (also +5) 0 -6 (also -5)	3.25 (–1.2V, +2V swing) 0.048
1.8	INA159 	0.9	+10 0 -4.26	2.9 (–0.852V, +2V swing) 0.048
2.5	5V V+	2.5	+10 0 -10	4.5 (=2V swing) 0.5
1.8	-IN 100kΩ 20kΩ SENSE	1.8	+10 0 -8.76	3.8 (–1.752V, +2V swing) 0.048
1.2	V _{IN} Ο ^{+IN} 100kΩ 40kΩ REF 2 O V _{REF} 40kΩ REF 2 O V _{REF} 40kΩ REF 1	1.2	+10 0 –5.76	3.2 (–1.15V, +2V swing) 0.048

Input and Output Relationships for Various Reference and Connection Combinations

REF CONNECTION

20kΩ

 \sim

SENSE

5V

<u>_++</u>

 $100 k\Omega$

 \sim

IN

 V_{OUT} for $V_{IN} = 0$ (V)

2.5

LINEAR V_{IN} RANGE (V)

+10

0 -10

10

V_{REF} (V)

5

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USEFUL V_{OUT} SWING (V)

4.5

(±2V swing) 0.5

4.048

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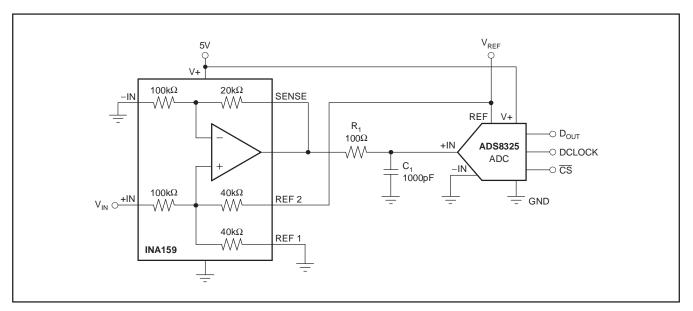


Figure 3. Typical Application Circuit Interfacing to Medium-Speed, Single-Supply ADCs

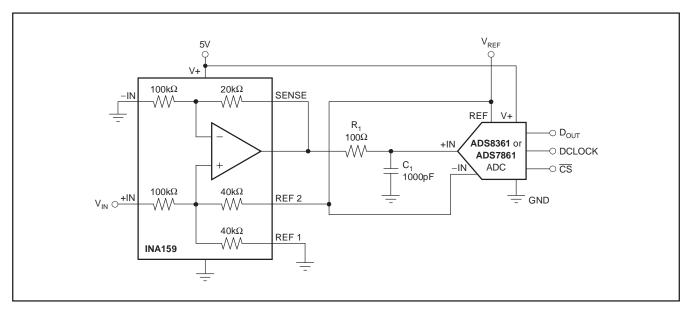


Figure 4. Typical Application Circuit Interfacing to Medium-Speed, Single-Supply ADCs with Pseudo-Differential Inputs (such as the ADS7861 and ADS8361)

INA159-EP

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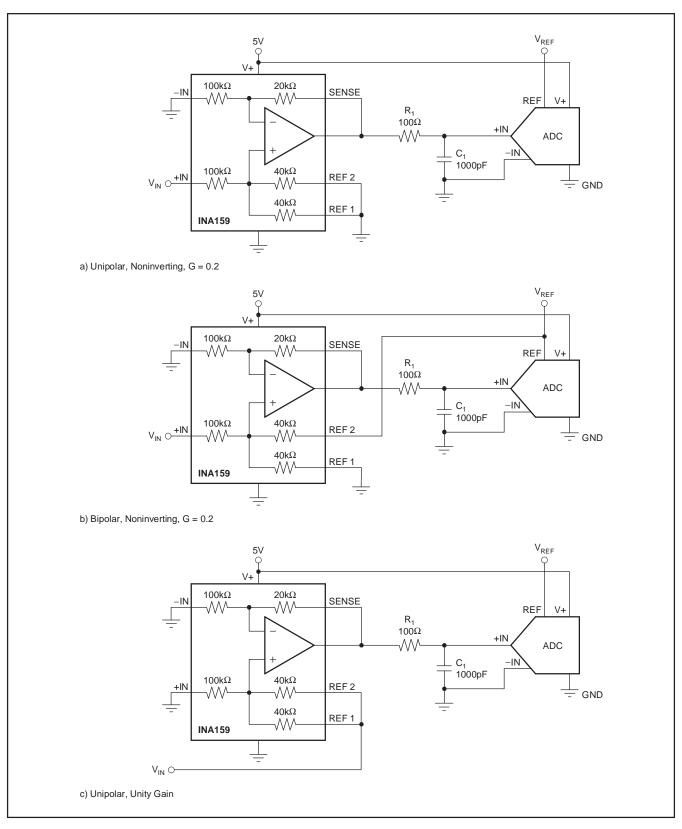


Figure 5. Basic INA159 Configurations



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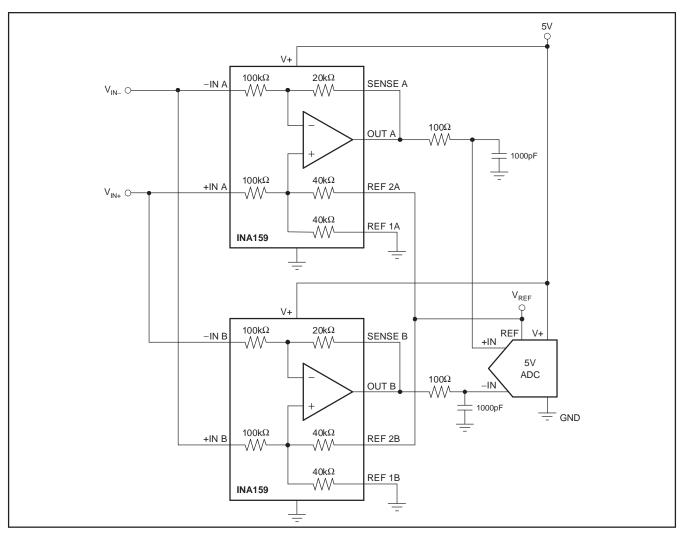


Figure 6. Differential ADC Drive



11-Apr-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	•	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing		Qty	(2)		(3)		(4)	
INA159AMDGKTEP	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	OAA	Samples
V62/09613-01XE	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	OAA	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF INA159-EP :



PACKAGE OPTION ADDENDUM

11-Apr-2013

Catalog: INA159

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.



DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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