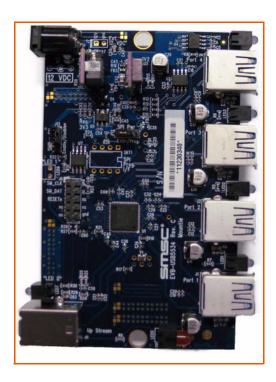


EVB-USB5534 Evaluation Board Revision C User Manual



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EVB-USB5534 Revision C Evaluation Board is for the SMSC USB5534 Hi-Speed 4-port USB hub solution. The hub is fully compliant with the *USB 3.0 USB Specification* and supports SuperSpeed (SS), Hi-Speed (HS), Full-Speed (FS), and Low-Speed (LS) USB signalling for complete coverage of all defined USB operating speeds. Additionally, it provides an upstream port compliant to both the USB 2.0 and 3.0 specifications. All four of the downstream ports are USB 2.0 and USB 3.0 compliant. All LED and port control signal pins are under firmware control in order to allow for maximum operational flexibility, and are available as GPIOs for customer-specific use. The EVB-USB5534 demonstrates driver compatibility with Microsoft Windows 7, WinXP, Mac OS X 10.4+ and Linux Hub Drivers.

1.1 Features

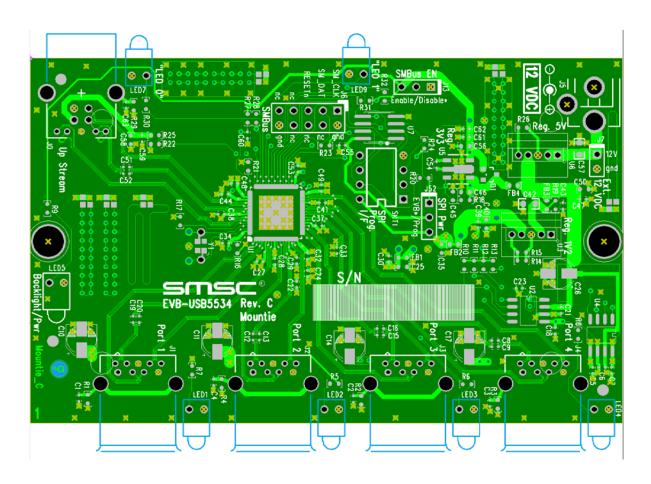
- Features the USB5534 in a 64-pin QFN RoHS compliant package
- USB 3.0 compliant (SS, HS, FS, and LS operation); USB pins are 5 V tolerant
- One USB 2.0/3.0 upstream hub port
- Self powered operation
- Four downstream USB 3.0 ports, which also support USB 2.0
- All downstream ports support individual port power and over current sense
- Optional onboard SPI Flash for external downloadable firmware
- Low-cost 4-layer space saving design
- Operates from one single voltage (+12.0 V, regulated) 'wall wart' external power supply
- Two GPIO LED indicators (LED0 and LED1)
- Single 25 MHz crystal or external clock input
- Single onboard +3.3 V, 1.5 Amp regulator
- Single onboard +1.2 V, 3 Amp regulator
- +3.3 V and port power LED indicators

1.2 General Description

The EVB-USB5534 is a demonstration and evaluation platform featuring the USB5534 ultra fast four port hub on a 4-layer RoHS-compliant printed circuit board. It supports the legacy USB speeds (HS/FS/LS) through an included USB 2.0 hub controller operating in parallel with the new SuperSpeed (SS) hub controller. This parallel hub operation keeps the SuperSpeed data transfers from being affected by the slower USB 2.0 traffic. The USB5534 is configured for operation through internal default settings and supports custom configurations through an optional external 8-Mbit SPI Flash device, U7.

Figure 1.1 shows the top and bottom level silk screen and copper layer.





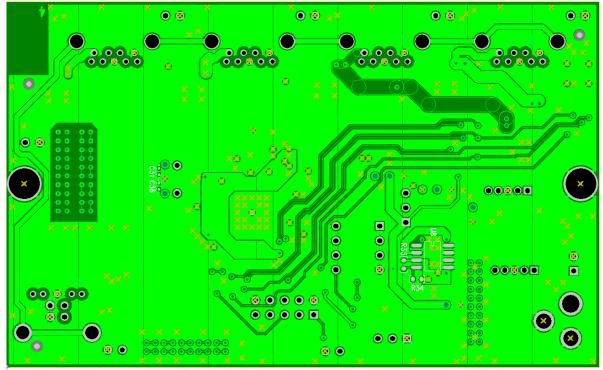


Figure 1.1 Top and Bottom Level Silk Screen and Copper Layers

SMSC EVB-USB5534 Revision 0.1 (08-09-11)

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Chapter 2 Getting Started

The EVB-USB5534 is configured by internal default registers. In this configuration it operates as a USB 3.0/USB 2.0 hub device with a four port USB HUB and SMSC's standard VID/PID/DID settings.

2.1 Configuration

The SMSC EVB-USB5534 is designed for flexible configuration solutions. It can be configured with default internal register settings, through downloadable external firmware to an onboard SPI Flash, or through SMBus.

2.1.1 Configuration Source - Internal Default

When the USB5534 does not detect a valid SPI Flash image or SMBus configuration upon power-up, the EVB-USB5534 uses internal default register settings. It also sets the Vendor ID, Product ID, Language ID, and Device ID, and additional settings from internal ROM code.

2.1.2 Configuration Source - External SPI Flash and SMBus

Upon power-up the USB5534 first looks for an external SPI Flash device. If one is found, the external ROM is enabled and code execution is then initiated from the external SPI device. If a SPI Flash device is not found, the firmware checks to see whether SMBus is enabled. To enable SMBus, pins 2 and 3 must be shorted on the J13 *SMBus EN* header which pulls **SM_CLK** high. This header has pins 1 and 2 shorted by default which disables SMBus by pulling **SM_CLK** low. When SMBus is enabled, the firmware configures the GPIOs to act as an SMBus slave. As an SMBus slave, the firmware will wait indefinitely for the SMBus configuration. The SMBus can operate in either legacy mode (USB 2.0 only) or advanced mode (access to both USB 2.0 and USB 3.0 registers). SMBus data and clock can be controlled via the onboard SMBus header, J6. If the SMBus is not enabled, the USB5534 will then look to load the configuration from an external I²C EEPROM. If no external options are detected, the USB5534 will operate from the internal OTP memory.

By default, the SPI Flash chip U7 is populated. The 10 k Ω pull-up resistors R20, R24, and R31 must also be populated. Finally, the *SPI Power* header J52 must also be populated in order to supply +3.3 V to the SPI chip. Pins 1 and 2 are jumpered on J52 by default so that the SPI chip is powered by onboard +3.3 V. There is an alternative SPI programming interface available as well that is not populated by default. The SPI chip can be programmed via the 8-pin DIP socket SKT1, where the *SPI Power* header J52 must have pins 2 and 3 shorted together so that the SPI chip is powered through the programmer instead of the onboard power supply. Once the part has been programmed, the J52 header can then be switched back so that pins 1 and 2 are jumpered together and the onboard +3.3 V now powers the SPI chip.

If the USB5534 does not detect an SMBus interface, it will then check for an I^2C EEPROM. For I^2C communication, the SMBus header J6 can be used to access the SCL and SDA signals on the USB5534. In order to assure proper operation, the external 10 k Ω pull-up resistor R23 on SM_DAT must be populated and pins 2 and 3 on the SMBus EN header must be shorted so that SM_CLK has a 10 k Ω pull-up resistor (R32) on it.

2.1.3 Configuration Source - 25MHz Crystal

By default, a 2 mm x 1.6 mm Murata 25 MHz crystal, Y1, is populated on the evaluation board. External load capacitance is not required when this crystal is used. If a surface mount HCM49 crystal is used on the EVB instead, two 18 pF load capacitors C60 and C61 must be populated.

2.1.4 Power Source - Self-Powered

The EVB-USB5534 only supports self-powered operation, and is powered through one +12.0 V regulated 'wall wart' external power supply. The +12.0 V 'wall wart' plugs into the 2.5 mm connector



J5 on the board. Alternatively, an external voltage can be injected onto the J7~Ext. 12 V header, which is not populated by default. The +12.0 V feeds a 6 A regulator which outputs +5.0 V across the board. This +5.0 V output controls the +3.3 V and +1.3 V onboard regulators.

2.1.5 Downstream Port Power Control

All four USB downstream port powers are controlled via two 1 A port power devices (AP2176S). All four downstream ports have individual over current sensing available and all sensing signals are pulled high to +3.3 V through external 10 k Ω resistors. The port power devices, U2 and U4, are enabled through the **PRT_CTL[4:1]** signals on the USB5534. The over current sense signals from the port power devices are monitored on the **OCS[4:1]** pins of the USB5534.