

# Spansion<sup>®</sup> Analog and Microcontroller Products



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The following document contains information on Spansion analog and microcontroller products. Although the document is marked with the name "Fujitsu", the company that originally developed the specification, Spansion will continue to offer these products to new and existing customers.

## **Continuity of Specifications**

There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal document improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

## **Continuity of Ordering Part Numbers**

Spansion continues to support existing part numbers beginning with "MB". To order these products, please use only the Ordering Part Numbers listed in this document.

## **For More Information**

Please contact your local sales office for additional information about Spansion memory, analog, and microcontroller products and solutions.

# 16-bit Microcontroller

CMOS

## F<sup>2</sup>MC-16LX MB90335 Series

## MB90337/F337/V330A

### ■ DESCRIPTION

The MB90335 series are 16-bit microcontrollers designed for applications, such as personal computer peripheral devices, that require USB communications. The USB feature supports not only 12-Mbps Function operation but also HOST operation. It is equipped with functions that are suitable for personal computer peripheral devices such as displays and audio devices, and control of mobile devices that support USB communications. While inheriting the AT architecture of the F<sup>2</sup>MC\* family, the instruction set supports the C language and extended addressing modes and contains enhanced signed multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, long word processing is now available by introducing a 32-bit accumulator.

Note : F<sup>2</sup>MC is the abbreviation of FUJITSU Flexible Microcontroller.

### ■ FEATURES

#### • Clock

- Built-in oscillation circuit and PLL clock frequency multiplication circuit
- Oscillation clock
- The main clock is the oscillation clock divided into 2 (for oscillation 6 MHz : 3 MHz)
- Clock for USB is 48 MHz
- Machine clock frequency of 6 MHz, 12 MHz or 24 MHz selectable
- Minimum execution time of instruction : 41.7 ns (6 MHz oscillation clock, 4-time multiplied : machine clock 24 MHz and at operating V<sub>CC</sub> = 3.3 V)

#### • The maximum memory space: 16 Mbytes

#### • 24-bit addressing

#### • Bank addressing

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For the information for microcontroller supports, see the following web site.

This web site includes the "**Customer Design Review Supplement**" which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

<http://edevise.fujitsu.com/micom/en-support/>

# MB90335 Series

- **Instruction system**
  - Data types: Bit, Byte, Word, Long word
  - Addressing mode (23 types)
  - Enhanced high-precision computing with 32-bit accumulator
  - Enhanced Multiply/Divide instructions with sign and the RETI instruction
- **Instruction system compatible with high-level language (C language) and multi-task**
  - Employing system stack pointer
  - Instruction set symmetry and barrel shift instructions
- **Program Patch Function (2 address pointer)**
- **4-byte instruction queue**
- **Interrupt function**
  - Priority levels are programmable
  - 20 interrupts function
- **Data transfer function**
  - Extended intelligent I/O service function (EI<sup>2</sup>OS) : Maximum of 16 channels
  - $\mu$ DMAC : Maximum 16 channels
- **Low Power Consumption Mode**
  - Sleep mode (with the CPU operating clock stopped)
  - Time-base timer mode (with the oscillator clock and time-base timer operating)
  - Stop mode (with the oscillator clock stopped)
  - CPU intermittent operation mode (with the CPU operating at fixed intervals of set cycles)
- **Package**
  - LQFP-64P (FPT-64P-M23 : 0.65 mm pin pitch)
- **Process : CMOS technology**
- **Operation guaranteed temperature: – 40 °C to + 85 °C (0 °C to + 70 °C when USB is in use)**

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- **Internal peripheral function (resource)**

- I/O port : Max 45 ports
- Time-base timer : 1 channel
- Watchdog timer : 1 channel
- 16-bit reload timer : 1 channel
- Multi-functional timer
  - 8/16-bit PPG timer (8-bit  $\times$  4 channels or 16-bit  $\times$  2 channels) the period and duty of the output pulse are freely programmable.
  - 16-bit PWC timer : 1 channel  
Timer function and pulse width measurement function
- UART: 2 channels
  - Equipped with a full duplex (8-bit long) double buffer
  - Selectable asynchronous transfer or clock-synchronous serial (extended I/O serial) transfer.
- Extended I/O serial interface : 1 channel
- DTP/External interrupt circuit (8 channels)
  - Activate the extended intelligent I/O service by external interrupt input
  - Interrupt output by external interrupt input
- Delayed interrupt output module
  - Outputs an interrupt request for task switching
- USB: 1 channel
  - USB function (supports USB Full Speed)
  - Supports Full Speed/Up to 6 endpoints can be specified.
  - Dual port RAM (supports FIFO mode).
  - Transfer type: Control, Interrupt, Bulk or Isochronous transfer possible
  - USB HOST function
- I<sup>2</sup>C Interface: 1 channel
  - Supports Intel SM bus standards and Phillips I<sup>2</sup>C bus standards
  - Two-wire data transfer protocol specification
  - Master and slave transmission/reception

# MB90335 Series

## ■ PRODUCT LINEUP

Part number	MB90V330A	MB90F337	MB90337
Type	For evaluation	Built-in Flash Memory	Built-in MASK ROM
ROM capacity	No	64 Kbytes	
RAM capacity	28 Kbytes	4 Kbytes	
Emulator-specific power supply *	Used bit	—	
CPU functions	Number of basic instructions : 351 instructions Minimum instruction execution time : 41.7 ns / at oscillation of 6 MHz (When 4 times are used : Machine clock of 24 MHz) Addressing type : 23 types Program Patch Function : For 2 address pointers Maximum memory space : 16 Mbytes		
Ports	I/O Ports(CMOS) Max 45 ports		
UART	Equipped with full-duplex double buffer Clock synchronous or asynchronous operation selectable. It can also be used for I/O serial. Built-in special baud-rate generator Built-in 2 channels		
16-bit reload timer	16-bit reload timer operation Built-in 1 channel		
Multi-functional timer	8/16-bit PPG timer (8-bit mode × 4 channels, 16-bit mode × 2 channels) 16-bit PWC timer × 1 channel		
DTP/External interrupt	8 channels Interrupt factor : “L”→“H” edge /“H”→“L” edge /“L” level /“H” level selectable		
I <sup>2</sup> C	1 channel		
Extended I/O serial interface	1 channel		
USB	1 channel USB function (supports USB Full Speed) USB HOST function		
Withstand voltage of 5 V	8 ports (Excluding UTEST and I/O for I <sup>2</sup> C)		
Low Power Consumption Mode	Sleep mode/Timebase timer mode/Stop mode/CPU intermittent mode		
Process	CMOS		
Operating voltage V <sub>cc</sub>	3.3 V ± 0.3 V (at maximum machine clock 24 MHz)		

\* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used. Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply Switching) about details.

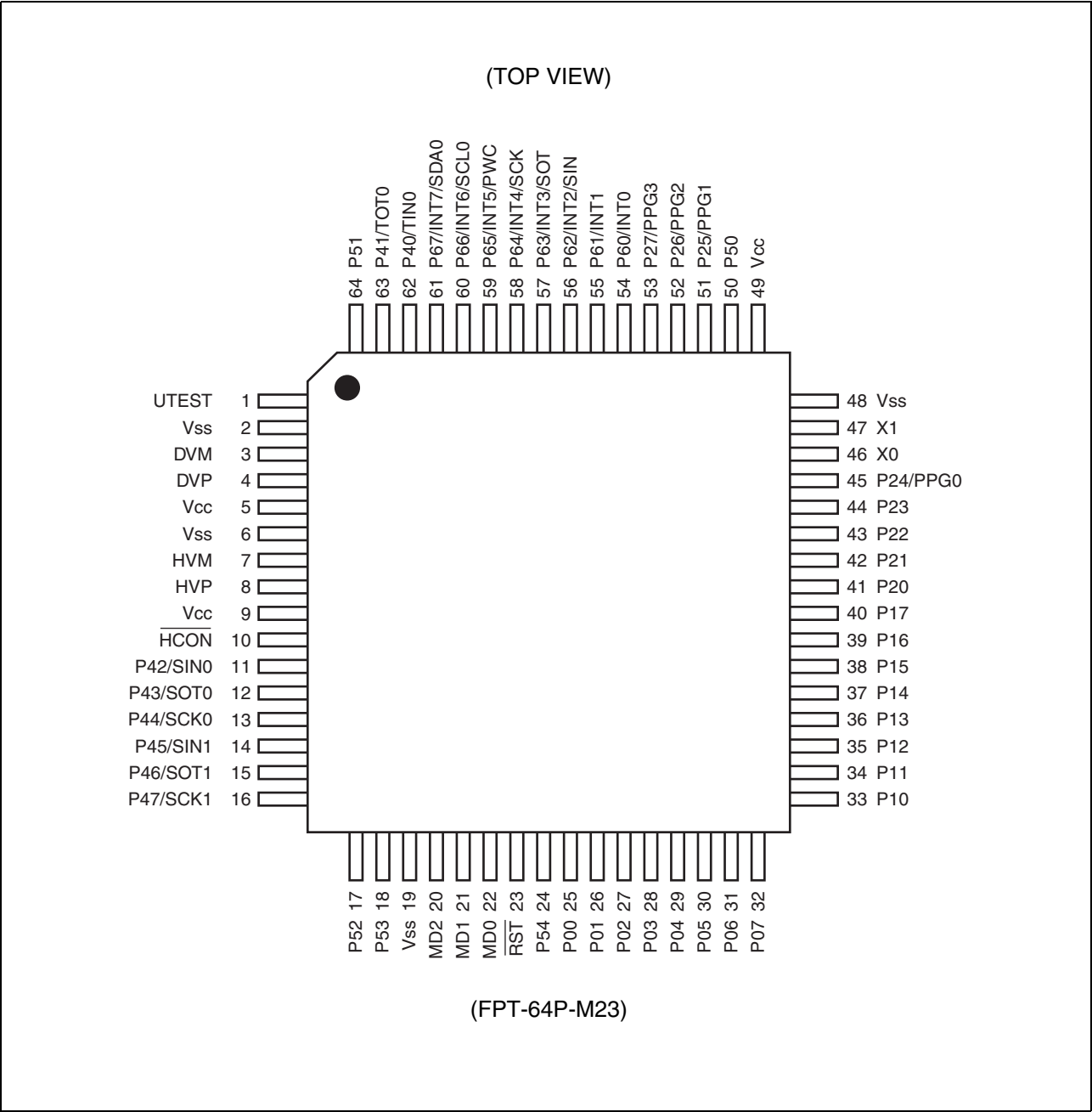
## ■ PACKAGES AND PRODUCT MODELS

Package	MB90337	MB90F337	MB90V330A
FPT-64P-M23 (LQFP)	○	○	×
PGA-299C-A01 (PGA)	×	×	○

○ : Yes    × : No

Note : See “■ PACKAGE DIMENSIONS” for details.

PIN ASSIGNMENT



# MB90335 Series

## ■ PIN DESCRIPTION

Pin no.	Pin name	I/O Circuit type*	Status at reset/ function	Function
46 , 47	X0, X1	A	Oscillation status	It is a terminal which connects the oscillator. When connecting an external clock, leave the X1 pin side unconnected.
23	$\overline{\text{RST}}$	F	Reset input	External reset input pin.
25 to 32	P00 to P07	I	Port input (Hi-Z)	General purpose input/output port. The ports can be set to be added with a pull-up resistor (RD00 to RD07 = 1) by the pull-up resistor setting register (RDR0). (When the power output is set, it is invalid.)
33 to 40	P10 to P17	I		General purpose input/output port. The ports can be set to be added with a pull-up resistor (RD10 to RD17 = 1) by the pull-up resistor setting register (RDR1). (When the power output is set, it is invalid.)
41 to 44	P20 to P23	D		General purpose input/output port.
45	P24	D		General purpose input/output port.
	PPG0			Functions as output pins of PPG timers ch.0.
51 to 53	P25 to P27	D		General purpose input/output port.
	PPG1 to PPG3			Functions as output pins of PPG timers ch.1 to ch.3.
62	P40	H		General purpose input/output port.
	TIN0			Function as event input pin of 16-bit reload timer.
63	P41	H		General purpose input/output port.
	TOT0			Function as output pin of 16-bit reload timer.
11	P42	H		General purpose input/output port.
	SIN0			Functions as a data input pin for UART ch.0.
12	P43	H		General purpose input/output port.
	SOT0			Functions as a data output pin for UART ch.0.
13	P44	H		General purpose input/output port.
	SCK0			Functions as a clock I/O pin for UART ch.0.
14	P45	H		General purpose input/output port.
	SIN1			Functions as a data input pin for UART ch.1.
15	P46	H		General purpose input/output port.
	SOT1			Functions as a data output pin for UART ch.1.
16	P47	H		General purpose input/output port.
	SCK1			Functions as a clock I/O pin for UART ch.1.
50	P50	K		General purpose input/output port.
64	P51	K		General purpose input/output port.
17, 18	P52, P53	K		General purpose input/output port.
24	P54	K		General purpose input/output port.

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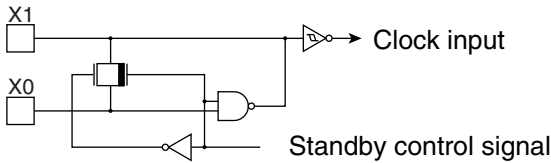
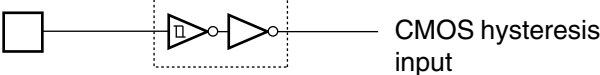
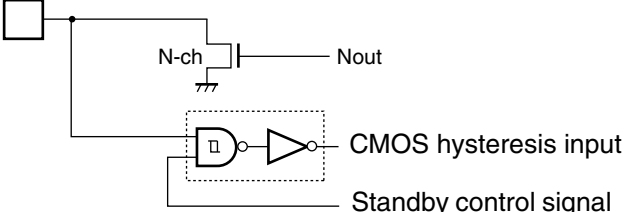
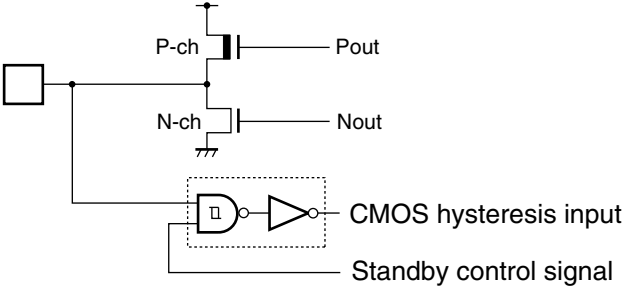
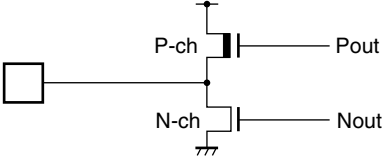
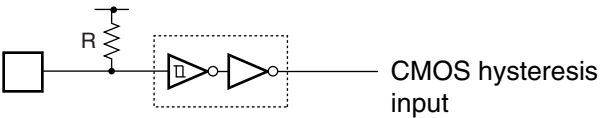
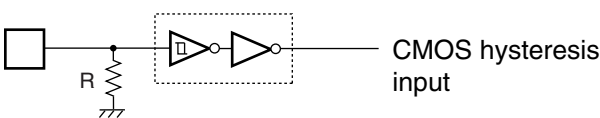
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Pin no.	Pin name	I/O Circuit type*	Status at reset/ function	Function
54, 55	P60, P61	C	Port input (Hi-Z)	General purpose input/output port (withstand voltage of 5 V) .
	INT0, INT1			Functions as the input pin for external interrupt ch.0 and ch.1.
56	P62	C		General purpose input/output port (withstand voltage of 5 V) .
	INT2			Functions as the input pin for external interrupt ch.2.
	SIN			Data input pin for extended I/O serial interface.
57	P63	C		General purpose input/output port (withstand voltage of 5 V) .
	INT3			Functions as the input pin for external interrupt ch.3.
	SOT			Data output pin for extended I/O serial interface.
58	P64	C		General purpose input/output port (withstand voltage of 5 V) .
	INT4			Functions as the input pin for external interrupt ch.4.
	SCK			Clock I/O pin for extended I/O serial interface.
59	P65	C		General purpose input/output port (withstand voltage of 5 V) .
	INT5			Functions as the input pin for external interrupt ch.5.
	PWC			Functions as the PWC input pin.
60	P66	C		General purpose input/output port (withstand voltage of 5 V) .
	INT6			Functions as the input pin for external interrupt ch.6.
	SCL0			Functions as the input/output pin for I <sup>2</sup> C interface clock. The port output must be placed in Hi-Z state during I <sup>2</sup> C interface operation.
61	P67	C		General purpose input/output port (withstand voltage of 5 V) .
	INT7			Functions as the input pin for external interrupt ch.7.
	SDA0			Functions as the I <sup>2</sup> C interface data input/output pin. The port output must be placed in Hi-Z state during I <sup>2</sup> C interface operation.
1	UTEST	C	UTEST input	USB test pin. Connect this to a pull-down resistor during normal usage.
3	DVM	J	USB input (SUSPEND)	USB function D – pin.
4	DVP	J		USB function D + pin.
7	HVM	J		USB HOST D – pin.
8	HVP	J		USB HOST D + pin.
10	HCON	E	High output	External pull-up resistor connection pin.
21, 22	MD1, MD0	B	Mode input	Input pin for selecting operation mode.
20	MD2	G		
5, 9, 49	Vcc	—	Power supply	Power supply pin.
2, 6, 19, 48	Vss			Power supply pin (GND).

\* : For circuit information, refer to “■ I/O CIRCUIT TYPE”.



## ■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	 <p>Clock input</p> <p>Standby control signal</p>	<ul style="list-style-type: none"> <li>Oscillation feedback resistor of approx. 1 MΩ</li> <li>With standby control</li> </ul>
B	 <p>CMOS hysteresis input</p>	CMOS hysteresis input
C	 <p>N-ch</p> <p>Nout</p> <p>CMOS hysteresis input</p> <p>Standby control signal</p>	<ul style="list-style-type: none"> <li>CMOS hysteresis input</li> <li>N-ch open drain output</li> </ul>
D	 <p>P-ch</p> <p>N-ch</p> <p>Pout</p> <p>Nout</p> <p>CMOS hysteresis input</p> <p>Standby control signal</p>	<ul style="list-style-type: none"> <li>CMOS output</li> <li>CMOS hysteresis input (With input interception function at standby)</li> </ul> <p>Notes :</p> <ul style="list-style-type: none"> <li>Share one output buffer because both output of I/O port and internal resource are used.</li> <li>Share one input buffer because both input of I/O port and internal resource are used.</li> </ul>
E	 <p>P-ch</p> <p>N-ch</p> <p>Pout</p> <p>Nout</p>	CMOS output
F	 <p>R</p> <p>CMOS hysteresis input</p>	CMOS hysteresis input with pull-up resistor of approx. 50 kΩ
G	 <p>R</p> <p>CMOS hysteresis input</p>	<ul style="list-style-type: none"> <li>CMOS hysteresis input with pull-down resistor of approx. 50 kΩ</li> <li>Flash product is not provided with pull-down resistor.</li> </ul>

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Type	Circuit	Remarks
H	<p>Open drain control signal</p> <p>CMOS hysteresis input</p> <p>Standby control signal</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS hysteresis input (With input interception function at standby)</li> <li>With open drain control signal</li> </ul>
I	<p>Control signal</p> <p>CMOS input</p> <p>Standby control signal</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input (With input interception function at standby)</li> <li>• Programmable input pull-up resistor</li> </ul>
J	<p>D + input</p> <p>D - input</p> <p>Differential input</p> <p>Full D + output</p> <p>Full D - output</p> <p>Low D + output</p> <p>Low D - output</p> <p>Direction</p> <p>Speed</p>	USB I/O pin
K	<p>CMOS input</p> <p>Standby control signal</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input (With input interception function at standby)</li> </ul>

## ■ HANDLING DEVICES

### 1. Preventing latch-up and turning on power supply

latch-up may occur on CMOS IC under the following conditions:

- If a voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to input and output pins.
- A voltage higher than the rated voltage is applied between  $V_{CC}$  and  $V_{SS}$ .

When latch-up occurs, power supply current increases rapidly and might thermally damage elements. When using CMOS IC, take great care to prevent the occurrence of latch-up.

### 2. Treatment of unused pins

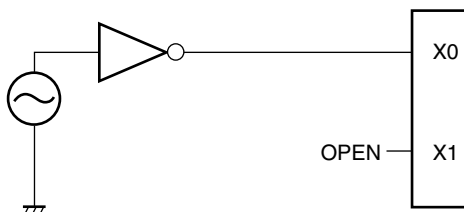
Leaving unused input pins unconnected can cause abnormal operation or latch-up, leading to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 k $\Omega$ . Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it to open.

### 3. About the attention when the external clock is used

Even when using an external clock signal, an oscillation stabilization delay is applied after a power-on reset or when recovering from sub-clock or stop mode. When using an external clock, 25 MHz should be the upper frequency limit.

The following figure shows a sample use of external clock signals.

- Using external clock



### 4. Treatment of power supply pins ( $V_{CC}/V_{SS}$ )

In products with multiple  $V_{CC}$  or  $V_{SS}$  pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the  $V_{CC}$  and  $V_{SS}$  pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1  $\mu$ F between  $V_{CC}$  and  $V_{SS}$  pins near this device.

### 5. About crystal oscillator circuit

Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0 and X1 pins surrounded by ground plane because stable operation can be expected with such a layout.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

### 6. Caution on Operations during PLL Clock Mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

## 7. Stabilization of supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the  $V_{CC}$  supply voltage operating range. For stabilization reference, the supply voltage should be stabilized so that  $V_{CC}$  ripple variations (peak-to-peak value) at commercial frequencies (50 MHz to 60 MHz) fall below 10% of the standard  $V_{CC}$  supply voltage and the transient regulation does not exceed 0.1 V/ms at temporary changes such as power supply switching.

## 8. Writing to flash memory

For serial writing to flash memory, always make sure that the operating voltage  $V_{CC}$  is between 3.13 V and 3.6 V.

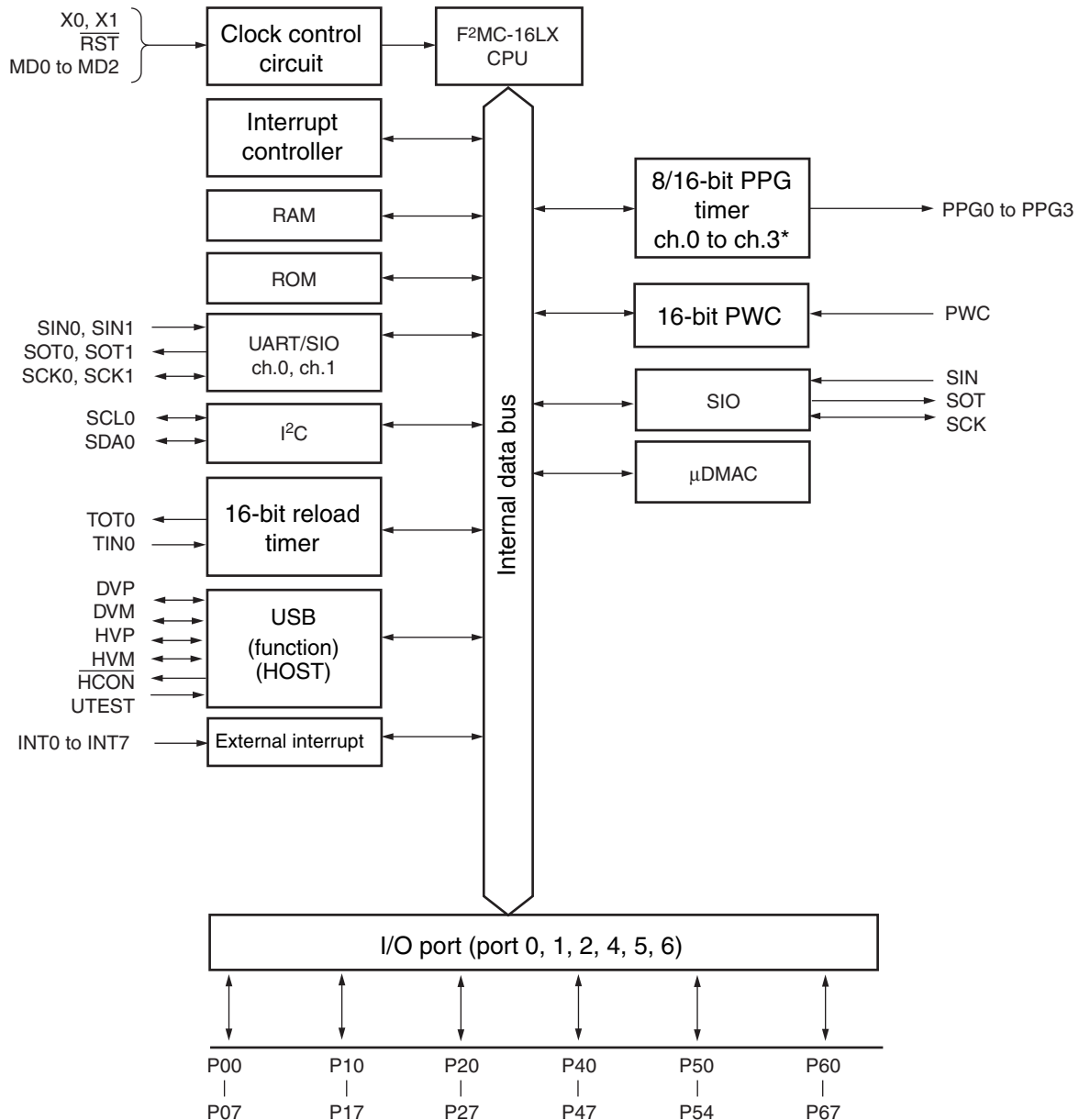
For normal writing to flash memory, always make sure that the operating voltage  $V_{CC}$  is between 3.0 V and 3.6 V.

## 9. Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example, apply a checksum to detect an error. If an error is detected, retransmit the data.

## ■ BLOCK DIAGRAM



\* : Channel for use in 8-bit mode. 2 channels (ch.1, ch.3) are used in 16-bit mode.

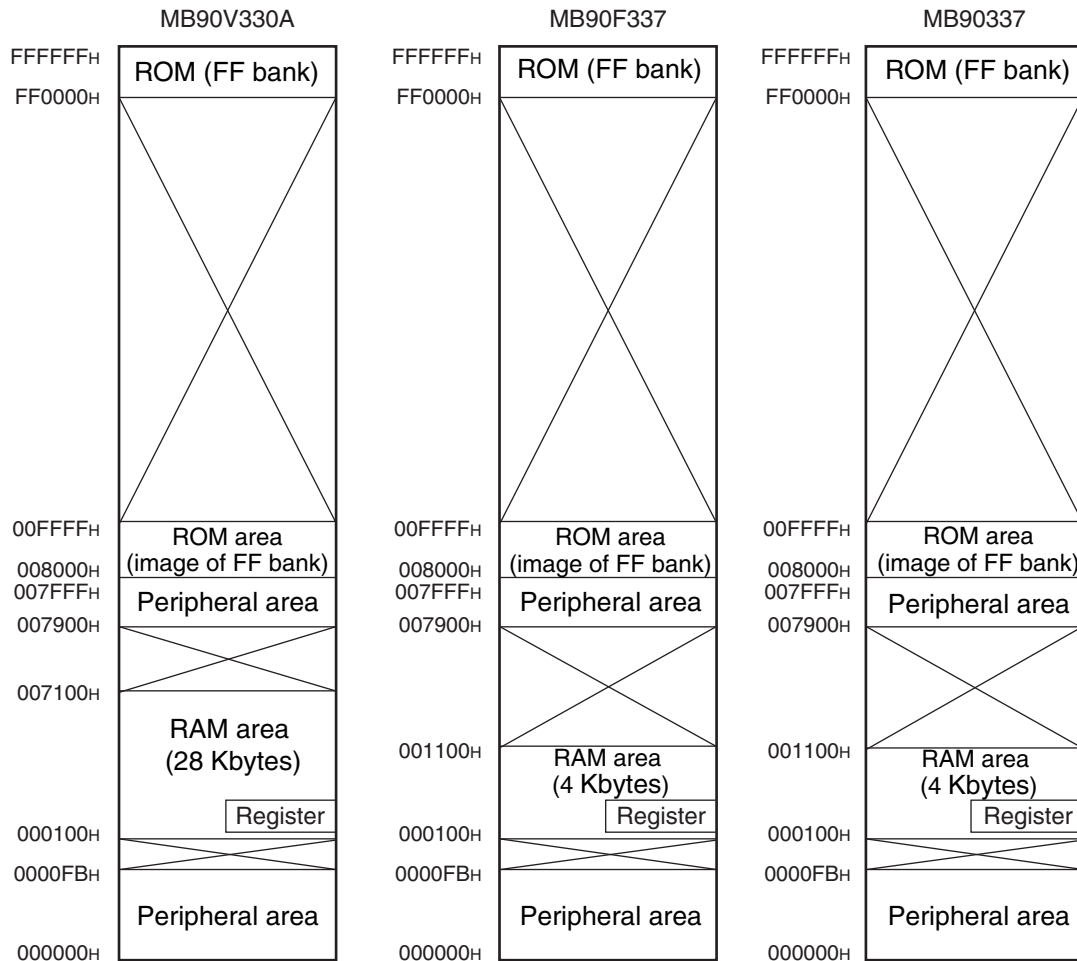
Note : I/O ports share pins with peripheral function (resources) .

For details, refer to "■ PIN ASSIGNMENT" and "■ PIN DESCRIPTION".

Note also that pins used for peripheral function (resources) cannot serve as I/O ports.

## ■ MEMORY MAP

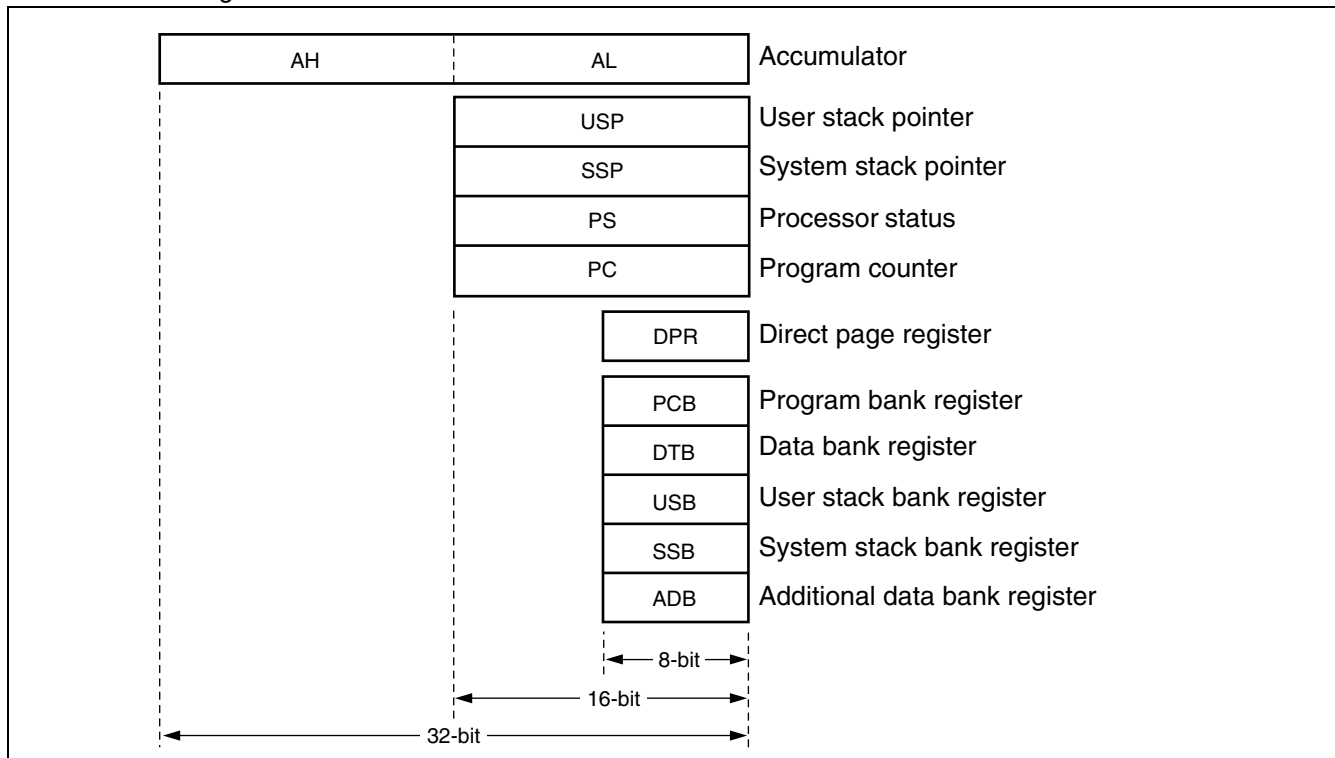
Single chip mode (with ROM mirror function)



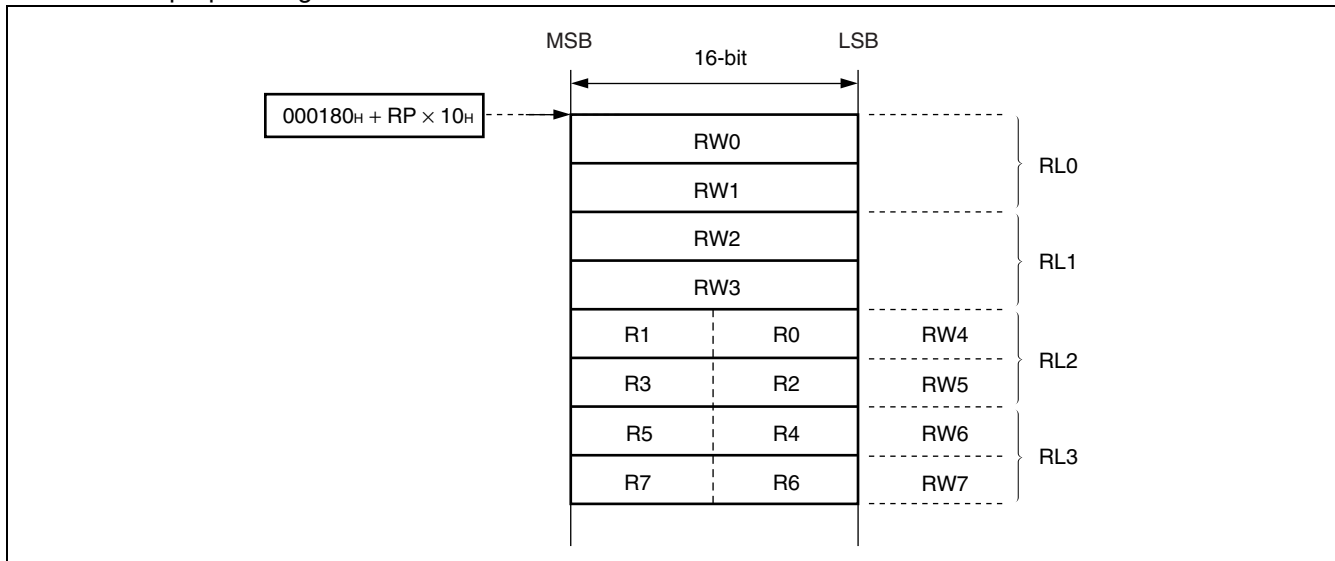
- Notes :
- When the ROM mirror function register has been set, the mirror image data at higher addresses ("FF8000H to FFFFFFFH") of bank FF is visible from the higher addresses ("008000H to 00FFFFH") of bank 00.
  - The ROM mirror function is effective for using the C compiler small model.
  - The lower 16-bit addresses of bank FF are equivalent to those of bank 00. Since the ROM area in bank FF exceeds 48 Kbytes, however, the mirror image of all the data in the ROM area cannot be reproduced in bank 00.
  - When the C compiler small model is used, the data table mirror image can be shown at "008000H to 00FFFFH" by storing the data table at "FF8000H to FFFFFFFH". Therefore, data tables in the ROM area can be referred without declaring the far addressing with the pointer.

## ■ F<sup>2</sup>MC-16L CPU PROGRAMMING MODEL

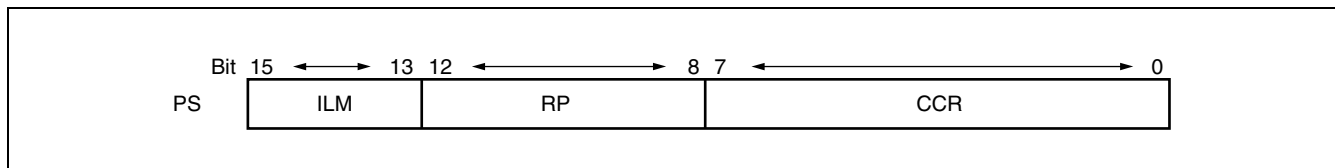
- Dedicated register



- General purpose registers



- Processor status



## ■ I/O MAP

Address	Register abbreviation	Register	Read/Write	Resource name	Initial Value
000000 <sub>H</sub>	PDR0	Port 0 Data Register	R/W	Port 0	XXXXXXXX <sub>B</sub>
000001 <sub>H</sub>	PDR1	Port 1 Data Register	R/W	Port 1	XXXXXXXX <sub>B</sub>
000002 <sub>H</sub>	PDR2	Port 2 Data Register	R/W	Port 2	XXXXXXXX <sub>B</sub>
000003 <sub>H</sub>	Prohibited				
000004 <sub>H</sub>	PDR4	Port 4 Data Register	R/W	Port 4	XXXXXXXX <sub>B</sub>
000005 <sub>H</sub>	PDR5	Port 5 Data Register	R/W	Port 5	- - - XXXXX <sub>B</sub>
000006 <sub>H</sub>	PDR6	Port 6 Data Register	R/W	Port 6	XXXXXXXX <sub>B</sub>
000007 <sub>H</sub> to 00000F <sub>H</sub>	Prohibited				
000010 <sub>H</sub>	DDR0	Port 0 Direction Register	R/W	Port 0	0 0 0 0 0 0 0 0 <sub>B</sub>
000011 <sub>H</sub>	DDR1	Port 1 Direction Register	R/W	Port 1	0 0 0 0 0 0 0 0 <sub>B</sub>
000012 <sub>H</sub>	DDR2	Port 2 Direction Register	R/W	Port 2	0 0 0 0 0 0 0 0 <sub>B</sub>
000013 <sub>H</sub>	Prohibited				
000014 <sub>H</sub>	DDR4	Port 4 Direction Register	R/W	Port 4	0 0 0 0 0 0 0 0 <sub>B</sub>
000015 <sub>H</sub>	DDR5	Port 5 Direction Register	R/W	Port 5	- - - 0 0 0 0 0 <sub>B</sub>
000016 <sub>H</sub>	DDR6	Port 6 Direction Register	R/W	Port 6	0 0 0 0 0 0 0 0 <sub>B</sub>
000017 <sub>H</sub> to 00001A <sub>H</sub>	Prohibited				
00001B <sub>H</sub>	ODR4	Port 4 Output Pin Register	R/W	Port 4 (Open-drain control)	0 0 0 0 0 0 0 0 <sub>B</sub>
00001C <sub>H</sub>	RDR0	Port 0 Pull-up Resistance Register	R/W	Port 0 (PULL-UP)	0 0 0 0 0 0 0 0 <sub>B</sub>
00001D <sub>H</sub>	RDR1	Port 1 Pull-up Resistance Register	R/W	Port 1 (PULL-UP)	0 0 0 0 0 0 0 0 <sub>B</sub>
00001E <sub>H</sub> 00001F <sub>H</sub>	Prohibited				
000020 <sub>H</sub>	SMR0	Serial Mode Register 0	R/W	UART0	0 0 1 0 0 0 0 0 <sub>B</sub>
000021 <sub>H</sub>	SCR0	Serial Control Register 0	R/W		0 0 0 0 0 1 0 0 <sub>B</sub>
000022 <sub>H</sub>	SIDR0	Serial Input Data Register 0	R		XXXXXXXX <sub>B</sub>
	SODR0	Serial Output Data Register 0	W		
000023 <sub>H</sub>	SSR0	Serial Status Register 0	R/W		0 0 0 0 1 0 0 0 <sub>B</sub>
000024 <sub>H</sub>	UTLRO	UART Prescaler Reload Register 0	R/W	Communication Prescaler (UART0)	0 0 0 0 0 0 0 0 <sub>B</sub>
000025 <sub>H</sub>	UTCRO	UART Prescaler Control Register 0	R/W		0 0 0 0 - 0 0 0 <sub>B</sub>
000026 <sub>H</sub>	SMR1	Serial Mode Register 1	R/W	UART1	0 0 1 0 0 0 0 0 <sub>B</sub>
000027 <sub>H</sub>	SCR1	Serial Control Register 1	R/W		0 0 0 0 0 1 0 0 <sub>B</sub>
000028 <sub>H</sub>	SIDR1	Serial Input Data Register 1	R		XXXXXXXX <sub>B</sub>
	SODR1	Serial Output Data Register 1	W		
000029 <sub>H</sub>	SSR1	Serial Status Register 1	R/W		0 0 0 0 1 0 0 0 <sub>B</sub>

(Continued)



# MB90335 Series

Address	Register abbreviation	Register	Read/Write	Resource name	Initial Value
00002A <sub>H</sub>	UTRLR1	UART Prescaler Reload Register 1	R/W	Communication	0 0 0 0 0 0 0 0 <sub>B</sub>
00002B <sub>H</sub>	UTCR1	UART Prescaler Control Register 1	R/W	Prescaler (UART1)	0 0 0 0 - 0 0 0 <sub>B</sub>
00002C <sub>H</sub> to 00003B <sub>H</sub>	Prohibited				
00003C <sub>H</sub>	ENIR	DTP/Interrupt Enable Register	R/W	DTP/External interrupt	0 0 0 0 0 0 0 0 <sub>B</sub>
00003D <sub>H</sub>	EIRR	DTP/Interrupt source Register	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
00003E <sub>H</sub>	ELVR	Request Level Setting Register Lower	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
00003F <sub>H</sub>		Request Level Setting Register Upper	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
000040 <sub>H</sub> to 000045 <sub>H</sub>	Prohibited				
000046 <sub>H</sub>	PPGC0	PPG0 Operation Mode Control Register	R/W	PPG ch.0	0X0 0 0XX1 <sub>B</sub>
000047 <sub>H</sub>	PPGC1	PPG1 Operation Mode Control Register	R/W	PPG ch.1	0X0 0 0 0 0 1 <sub>B</sub>
000048 <sub>H</sub>	PPGC2	PPG2 Operation Mode Control Register	R/W	PPG ch.2	0X0 0 0XX1 <sub>B</sub>
000049 <sub>H</sub>	PPGC3	PPG3 Operation Mode Control Register	R/W	PPG ch.3	0X0 0 0 0 0 1 <sub>B</sub>
00004A <sub>H</sub> 00004B <sub>H</sub>	Prohibited				
00004C <sub>H</sub>	PPG01	PPG0 and PPG1 Output Control Register	R/W	PPG ch.0/ch.1	0 0 0 0 0 0XX <sub>B</sub>
00004D <sub>H</sub>	Prohibited				
00004E <sub>H</sub>	PPG23	PPG2 and PPG3 Output Control Register	R/W	PPG ch.2/ch.3	0 0 0 0 0 0 XX <sub>B</sub>
00004F <sub>H</sub> to 000057 <sub>H</sub>	Prohibited				
000058 <sub>H</sub>	SMCS	Serial Mode Control Status Register	R/W	Extended Serial I/O	XXXX0 0 0 0 <sub>B</sub>
000059 <sub>H</sub>			0 0 0 0 0 0 1 0 <sub>B</sub>		
00005A <sub>H</sub>	SDR	Serial Data Register	R/W		XXXXXXXX <sub>B</sub>
00005B <sub>H</sub>	SDCR	Communication Prescaler Control Register	R/W	Communication Prescaler	0XXX0 0 0 0 <sub>B</sub>
00005C <sub>H</sub>	PWCSR	PWC Control Status Register	R/W	16-bit PWC Timer	0 0 0 0 0 0 0 0 <sub>B</sub>
00005D <sub>H</sub>			0 0 0 0 0 0 0 X <sub>B</sub>		
00005E <sub>H</sub>	PWCR	PWC Data Buffer Register	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
00005F <sub>H</sub>					0 0 0 0 0 0 0 0 <sub>B</sub>
000060 <sub>H</sub>	DIVR	PWC Dividing Ratio Control Register	R/W		- - - - - 0 0 <sub>B</sub>
000061 <sub>H</sub>	Prohibited				
000062 <sub>H</sub>	TMCSR0	Timer Control Status Register	R/W	16-bit Reload Timer	0 0 0 0 0 0 0 0 <sub>B</sub>
000063 <sub>H</sub>					XXXX 0 0 0 0 <sub>B</sub>
000064 <sub>H</sub>	TMR0	16-bit Timer Register Lower	R		XXXXXXXX <sub>B</sub>
	TMRLR0	16-bit Reload Register Lower	W		XXXXXXXX <sub>B</sub>
000065 <sub>H</sub>	TMR0	16-bit Timer Register Upper	R		XXXXXXXX <sub>B</sub>
	TMRLR0	16-bit Reload Register Upper	W		XXXXXXXX <sub>B</sub>

(Continued)

Address	Register abbreviation	Register	Read/Write	Resource name	Initial Value
000066 <sub>H</sub> to 00006E <sub>H</sub>	Prohibited				
00006F <sub>H</sub>	ROMM	ROM Mirroring Function Selection Register	W	ROM Mirror Function Selection Module	----- 1 1 <sub>B</sub>
000070 <sub>H</sub>	IBSR0	I <sup>2</sup> C Bus Status Register	R	I <sup>2</sup> C Bus Interface	0 0 0 0 0 0 0 0 <sub>B</sub>
000071 <sub>H</sub>	IBCR0	I <sup>2</sup> C Bus Control Register	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
000072 <sub>H</sub>	ICCR0	I <sup>2</sup> C Bus Clock Control Register	R/W		XX 0 XXXXX <sub>B</sub>
000073 <sub>H</sub>	IADR0	I <sup>2</sup> C Bus Address Register	R/W		XXXXXXXXX <sub>B</sub>
000074 <sub>H</sub>	IDAR0	I <sup>2</sup> C Bus Data Register	R/W		XXXXXXXXX <sub>B</sub>
000075 <sub>H</sub> to 00009A <sub>H</sub>	Prohibited				
00009B <sub>H</sub>	DCSR	DMA Descriptor Channel Specification Register	R/W	μDMAC	0 0 0 0 0 0 0 0 <sub>B</sub>
00009C <sub>H</sub>	DSRL	DMA Status Register Lower	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
00009D <sub>H</sub>	DSRH	DMA Status Register Upper	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
00009E <sub>H</sub>	PACSR	Program Address Detection Control Status Register	R/W	Address Match Detection	0 0 0 0 0 0 0 0 <sub>B</sub>
00009F <sub>H</sub>	DIRR	Delayed Interrupt Source generate/release Register	R/W	Delayed Interrupt	----- 0 <sub>B</sub>
0000A0 <sub>H</sub>	LPMCR	Low Power Consumption Mode Control Register	R/W	Low Power Consumption control circuit	0 0 0 1 1 0 0 0 <sub>B</sub>
0000A1 <sub>H</sub>	CKSCR	Clock Selection Register	R/W	Clock	1 1 1 1 1 1 0 0 <sub>B</sub>
0000A2 <sub>H</sub>	Prohibited				
0000A3 <sub>H</sub>					
0000A4 <sub>H</sub>	DSSR	DMA Stop Status Register	R/W	μDMAC	0 0 0 0 0 0 0 0 <sub>B</sub>
0000A5 <sub>H</sub> to 0000A7 <sub>H</sub>	Prohibited				
0000A8 <sub>H</sub>	WDTC	Watchdog Timer Control Register	R/W	Watchdog Timer	X - XXX 1 1 1 <sub>B</sub>
0000A9 <sub>H</sub>	TBTC	Time-base Timer Control Register	R/W	Time-base Timer	1 - - 0 0 1 0 0 <sub>B</sub>
0000AA <sub>H</sub>	Prohibited				
0000AB <sub>H</sub>					
0000AC <sub>H</sub>	DERL	DMA Enable Register Lower	R/W	μDMAC	0 0 0 0 0 0 0 0 <sub>B</sub>
0000AD <sub>H</sub>	DERH	DMA Enable Register Upper	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
0000AE <sub>H</sub>	FMCS	Flash Memory Control Status Register	R/W	Flash Memory I/F	0 0 0 X 0 0 0 0 <sub>B</sub>
0000AF <sub>H</sub>	Prohibited				

(Continued)

# MB90335 Series

Address	Register abbreviation	Register	Read/Write	Resource name	Initial Value
0000B0 <sub>H</sub>	ICR00	Interrupt Control Register 00	R/W	Interrupt Controller	0 0 0 0 0 1 1 1 <sub>B</sub>
0000B1 <sub>H</sub>	ICR01	Interrupt Control Register 01	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
0000B2 <sub>H</sub>	ICR02	Interrupt Control Register 02	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
0000B3 <sub>H</sub>	ICR03	Interrupt Control Register 03	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
0000B4 <sub>H</sub>	ICR04	Interrupt Control Register 04	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
0000B5 <sub>H</sub>	ICR05	Interrupt Control Register 05	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
0000B6 <sub>H</sub>	ICR06	Interrupt Control Register 06	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
0000B7 <sub>H</sub>	ICR07	Interrupt Control Register 07	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
0000B8 <sub>H</sub>	ICR08	Interrupt Control Register 08	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
0000B9 <sub>H</sub>	ICR09	Interrupt Control Register 09	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
0000BA <sub>H</sub>	ICR10	Interrupt Control Register 10	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
0000BB <sub>H</sub>	ICR11	Interrupt Control Register 11	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
0000BC <sub>H</sub>	ICR12	Interrupt Control Register 12	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
0000BD <sub>H</sub>	ICR13	Interrupt Control Register 13	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
0000BE <sub>H</sub>	ICR14	Interrupt Control Register 14	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
0000BF <sub>H</sub>	ICR15	Interrupt Control Register 15	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
0000C0 <sub>H</sub>	HCNT0	Host Control Register 0	R/W	USB HOST	0 0 0 0 0 0 0 0 <sub>B</sub>
0000C1 <sub>H</sub>	HCNT1	Host Control Register 1	R/W		0 0 0 0 0 0 0 1 <sub>B</sub>
0000C2 <sub>H</sub>	HIRQ	Host Interruption Register	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
0000C3 <sub>H</sub>	HERR	Host Error Status Register	R/W		0 0 0 0 0 0 1 1 <sub>B</sub>
0000C4 <sub>H</sub>	HSTATE	Host State Status Register	R/W		XX 0 1 0 0 1 0 <sub>B</sub>
0000C5 <sub>H</sub>	HFCOMP	SOF Interrupt FRAME Compare Register	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
0000C6 <sub>H</sub>	HRTIMER	Retry Timer Setting Register	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
0000C7 <sub>H</sub>			R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
0000C8 <sub>H</sub>			R/W		XXXXXX 0 0 <sub>B</sub>
0000C9 <sub>H</sub>	HADR	Host Address Register	R/W		X 0 0 0 0 0 0 0 <sub>B</sub>
0000CA <sub>H</sub>	HEOF	EOF Setting Register	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
0000CB <sub>H</sub>			R/W		XX 0 0 0 0 0 0 <sub>B</sub>
0000CC <sub>H</sub>	HFRAME	FRAME Setting Register	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
0000CD <sub>H</sub>			R/W		XXXXX 0 0 0 <sub>B</sub>
0000CE <sub>H</sub>	HTOKEN	Host Token End Point Register	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
0000CF <sub>H</sub>	Prohibited				
0000D0 <sub>H</sub>	UDCC	UDC Control Register	R/W	USB Function	1 0 1 0 0 0 0 0 <sub>B</sub>
0000D1 <sub>H</sub>			R/W		0 0 0 0 0 0 0 0 <sub>B</sub>

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Address	Register abbreviation	Register	Read/Write	Resource name	Initial Value
0000D2 <sub>H</sub>	EP0C	EP0 Control Register	R/W	USB Function	0 1 0 0 0 0 0 0 <sub>B</sub>
0000D3 <sub>H</sub>			R/W		XXXX 0 0 0 0 <sub>B</sub>
0000D4 <sub>H</sub>	EP1C	EP1 Control Register	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
0000D5 <sub>H</sub>			R/W		0 1 1 0 0 0 0 1 <sub>B</sub>
0000D6 <sub>H</sub>	EP2C	EP2 Control Register	R/W		0 1 0 0 0 0 0 0 <sub>B</sub>
0000D7 <sub>H</sub>			R/W		0 1 1 0 0 0 0 0 <sub>B</sub>
0000D8 <sub>H</sub>	EP3C	EP3 Control Register	R/W		0 1 0 0 0 0 0 0 <sub>B</sub>
0000D9 <sub>H</sub>			R/W		0 1 1 0 0 0 0 0 <sub>B</sub>
0000DA <sub>H</sub>	EP4C	EP4 Control Register	R/W		0 1 0 0 0 0 0 0 <sub>B</sub>
0000DB <sub>H</sub>			R/W		0 1 1 0 0 0 0 0 <sub>B</sub>
0000DC <sub>H</sub>	EP5C	EP5 Control Register	R/W		0 1 0 0 0 0 0 0 <sub>B</sub>
0000DD <sub>H</sub>			R/W		0 1 1 0 0 0 0 0 <sub>B</sub>
0000DE <sub>H</sub>	TMSP	Time Stamp Register	R		0 0 0 0 0 0 0 0 <sub>B</sub>
0000DF <sub>H</sub>			R		XXXXX0 0 0 <sub>B</sub>
0000E0 <sub>H</sub>	UDCS	UDC Status Register	R/W		XX0 0 0 0 0 0 <sub>B</sub>
0000E1 <sub>H</sub>	UDCIE	UDC Interrupt Enable Register	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
0000E2 <sub>H</sub>	EP0IS	EP0I Status Register	R/W		XXXXXXXX <sub>B</sub>
0000E3 <sub>H</sub>			R/W		1 0 XXX 1 XX <sub>B</sub>
0000E4 <sub>H</sub>	EP0OS	EP0O Status Register	R/W, R		0 XXXXXXX <sub>B</sub>
0000E5 <sub>H</sub>			R/W		1 0 0 XX 0 0 0 <sub>B</sub>
0000E6 <sub>H</sub>	EP1S	EP1 Status Register	R		XXXXXXXX <sub>B</sub>
0000E7 <sub>H</sub>			R/W		1 0 0 0 0 0 0 X <sub>B</sub>
0000E8 <sub>H</sub>	EP2S	EP2 Status Register	R		XXXXXXXX <sub>B</sub>
0000E9 <sub>H</sub>			R/W		1 0 0 0 0 0 0 0 <sub>B</sub>
0000EA <sub>H</sub>	EP3S	EP3 Status Register	R		XXXXXXXX <sub>B</sub>
0000EB <sub>H</sub>			R/W		1 0 0 0 0 0 0 0 <sub>B</sub>
0000EC <sub>H</sub>	EP4S	EP4 Status Register	R		XXXXXXXX <sub>B</sub>
0000ED <sub>H</sub>			R/W		1 0 0 0 0 0 0 0 <sub>B</sub>
0000EE <sub>H</sub>	EP5S	EP5 Status Register	R		XXXXXXXX <sub>B</sub>
0000EF <sub>H</sub>			R/W		1 0 0 0 0 0 0 0 <sub>B</sub>
0000F0 <sub>H</sub>	EP0DT	EP0 Data Register	R/W		XXXXXXXX <sub>B</sub>
0000F1 <sub>H</sub>			R/W		XXXXXXXX <sub>B</sub>
0000F2 <sub>H</sub>	EP1DT	EP1 Data Register	R/W		XXXXXXXX <sub>B</sub>
0000F3 <sub>H</sub>			R/W		XXXXXXXX <sub>B</sub>
0000F4 <sub>H</sub>	EP2DT	EP2 Data Register	R/W		XXXXXXXX <sub>B</sub>
0000F5 <sub>H</sub>			R/W		XXXXXXXX <sub>B</sub>
0000F6 <sub>H</sub>	EP3DT	EP3 Data Register	R/W		XXXXXXXX <sub>B</sub>
0000F7 <sub>H</sub>			R/W		XXXXXXXX <sub>B</sub>
0000F8 <sub>H</sub>	EP4DT	EP4 Data Register	R/W		XXXXXXXX <sub>B</sub>
0000F9 <sub>H</sub>			R/W		XXXXXXXX <sub>B</sub>

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# MB90335 Series

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
0000FA <sub>H</sub>	EP5DT	EP5 Data Register	R/W	USB Function	XXXXXXXX <sub>B</sub>
0000FB <sub>H</sub>			R/W		XXXXXXXX <sub>B</sub>
0000FC <sub>H</sub> to 0000FF <sub>H</sub>	Prohibited				
000100 <sub>H</sub> to 001100 <sub>H</sub>	RAM Area				
001FF0 <sub>H</sub>	PADR0	Program Address Detection Register ch.0 Lower	R/W	Address Match Detection	XXXXXXXX <sub>B</sub>
001FF1 <sub>H</sub>		Program Address Detection Register ch.0 Middle	R/W		XXXXXXXX <sub>B</sub>
001FF2 <sub>H</sub>		Program Address Detection Register ch.0 Upper	R/W		XXXXXXXX <sub>B</sub>
001FF3 <sub>H</sub>	PADR1	Program Address Detection Register ch.1 Lower	R/W		XXXXXXXX <sub>B</sub>
001FF4 <sub>H</sub>		Program Address Detection Register ch.1 Middle	R/W		XXXXXXXX <sub>B</sub>
001FF5 <sub>H</sub>		Program Address Detection Register ch.1 Upper	R/W		XXXXXXXX <sub>B</sub>
007900 <sub>H</sub>	PRL0	PPG Reload Register Lower ch.0	R/W	PPG ch.0	XXXXXXXX <sub>B</sub>
007901 <sub>H</sub>	PRLH0	PPG Reload Register Upper ch.0	R/W		XXXXXXXX <sub>B</sub>
007902 <sub>H</sub>	PRL1	PPG Reload Register Lower ch.1	R/W	PPG ch.1	XXXXXXXX <sub>B</sub>
007903 <sub>H</sub>	PRLH1	PPG Reload Register Upper ch.1	R/W		XXXXXXXX <sub>B</sub>
007904 <sub>H</sub>	PRL2	PPG Reload Register Lower ch.2	R/W	PPG ch.2	XXXXXXXX <sub>B</sub>
007905 <sub>H</sub>	PRLH2	PPG Reload Register Upper ch.2	R/W		XXXXXXXX <sub>B</sub>
007906 <sub>H</sub>	PRL3	PPG Reload Register Lower ch.3	R/W	PPG ch.3	XXXXXXXX <sub>B</sub>
007907 <sub>H</sub>	PRLH3	PPG Reload Register Upper ch.3	R/W		XXXXXXXX <sub>B</sub>
007908 <sub>H</sub> to 00790B <sub>H</sub>	Prohibited				
00790C <sub>H</sub>	FWR0	Flash Memory Program Control Register 0	R/W	Flash	0 0 0 0 0 0 0 0 <sub>B</sub>
00790D <sub>H</sub>	FWR1	Flash Memory Program Control Register 1	R/W	Flash	0 0 0 0 0 0 0 0 <sub>B</sub>
00790E <sub>H</sub>	SSR0	Sector Conversion Setting Register	R/W	Flash	0 0 XXXXX0 <sub>B</sub>
00790F <sub>H</sub> to 00791F <sub>H</sub>	Prohibited				

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Address	Register abbreviation	Register	Read/Write	Resource name	Initial Value
007920 <sub>H</sub>	DBAPL	DMA Buffer Address Pointer Lower 8-bit	R/W	μDMAC	XXXXXXXX <sub>B</sub>
007921 <sub>H</sub>	DBAPM	DMA Buffer Address Pointer Middle 8-bit	R/W		XXXXXXXX <sub>B</sub>
007922 <sub>H</sub>	DBAPH	DMA Buffer Address Pointer Upper 8-bit	R/W		XXXXXXXX <sub>B</sub>
007923 <sub>H</sub>	DMACS	DMA Control Register	R/W		XXXXXXXX <sub>B</sub>
007924 <sub>H</sub>	DIOAL	DMA I/O Register Address Pointer Lower 8-bit	R/W		XXXXXXXX <sub>B</sub>
007925 <sub>H</sub>	DIOAH	DMA I/O Register Address Pointer Upper 8-bit	R/W		XXXXXXXX <sub>B</sub>
007926 <sub>H</sub>	DDCTL	DMA Data Counter Lower 8-bit	R/W		XXXXXXXX <sub>B</sub>
007927 <sub>H</sub>	DDCTH	DMA Data Counter Upper 8-bit	R/W		XXXXXXXX <sub>B</sub>
007928 <sub>H</sub> to 007FFF <sub>H</sub>	Prohibited				

- Explanation on read/write

R/W : Readable and Writable

R : Read only

W : Write only

- Explanation of initial values

0 : Initial value is "0".

1 : Initial value is "1".

X : Initial value is undefined.

- : Initial value is undefined (None).

Note : No I/O instruction can be used for registers located between 007900<sub>H</sub> and 007FFF<sub>H</sub>.

# MB90335 Series

## ■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI <sup>2</sup> OS support	μDMAC	Interrupt vector		Interrupt control register		Priority
			Number*1	Address	ICR	Address	
Reset	×	×	#08	08 <sub>H</sub>	FFFFDC <sub>H</sub>	—	High
INT 9 instruction	×	×	#09	09 <sub>H</sub>	FFFFD8 <sub>H</sub>	—	
Exceptional treatment	×	×	#10	0A <sub>H</sub>	FFFFD4 <sub>H</sub>	—	
USB Function1	×	0, 1	#11	0B <sub>H</sub>	FFFFD0 <sub>H</sub>	ICR00	0000B0 <sub>H</sub>
USB Function2	×	2 to 6*2	#12	0C <sub>H</sub>	FFFFCC <sub>H</sub>		
USB Function3	×	×	#13	0D <sub>H</sub>	FFFFC8 <sub>H</sub>	ICR01	0000B1 <sub>H</sub>
USB Function4	×	×	#14	0E <sub>H</sub>	FFFFC4 <sub>H</sub>		
USB HOST1	×	×	#15	0F <sub>H</sub>	FFFFC0 <sub>H</sub>	ICR02	0000B2 <sub>H</sub>
USB HOST2	×	×	#16	10 <sub>H</sub>	FFFFBC <sub>H</sub>		
I <sup>2</sup> C ch.0	×	×	#17	11 <sub>H</sub>	FFFFB8 <sub>H</sub>	ICR03	0000B3 <sub>H</sub>
DTP/External interrupt ch.0/ch.1	○	×	#18	12 <sub>H</sub>	FFFFB4 <sub>H</sub>		
No	—	—	#19	13 <sub>H</sub>	FFFFB0 <sub>H</sub>	ICR04	0000B4 <sub>H</sub>
DTP/External interrupt ch.2/ch.3	○	×	#20	14 <sub>H</sub>	FFFFAC <sub>H</sub>		
No	—	—	#21	15 <sub>H</sub>	FFFFA8 <sub>H</sub>	ICR05	0000B5 <sub>H</sub>
DTP/External interrupt ch.4/ch.5	○	×	#22	16 <sub>H</sub>	FFFFA4 <sub>H</sub>		
PWC/Reload timer ch.0	△	14	#23	17 <sub>H</sub>	FFFFA0 <sub>H</sub>	ICR06	0000B6 <sub>H</sub>
DTP/External interrupt ch.6/ch.7	△	×	#24	18 <sub>H</sub>	FFFF9C <sub>H</sub>		
No	—	—	#25	19 <sub>H</sub>	FFFF98 <sub>H</sub>	ICR07	0000B7 <sub>H</sub>
No	—	—	#26	1A <sub>H</sub>	FFFF94 <sub>H</sub>		
No	—	—	#27	1B <sub>H</sub>	FFFF90 <sub>H</sub>	ICR08	0000B8 <sub>H</sub>
No	—	—	#28	1C <sub>H</sub>	FFFF8C <sub>H</sub>		
No	—	—	#29	1D <sub>H</sub>	FFFF88 <sub>H</sub>	ICR09	0000B9 <sub>H</sub>
PPG ch.0/ch.1	×	×	#30	1E <sub>H</sub>	FFFF84 <sub>H</sub>		
No	—	—	#31	1F <sub>H</sub>	FFFF80 <sub>H</sub>	ICR10	0000BA <sub>H</sub>
PPG ch.2/ch.3	×	×	#32	20 <sub>H</sub>	FFFF7C <sub>H</sub>		
No	—	—	#33	21 <sub>H</sub>	FFFF78 <sub>H</sub>	ICR11	0000BB <sub>H</sub>
No	—	—	#34	22 <sub>H</sub>	FFFF74 <sub>H</sub>		
No	—	—	#35	23 <sub>H</sub>	FFFF70 <sub>H</sub>	ICR12	0000BC <sub>H</sub>
No	—	—	#36	24 <sub>H</sub>	FFFF6C <sub>H</sub>		
UART (Send completed) ch.0/ch.1	○	13	#37	25 <sub>H</sub>	FFFF68 <sub>H</sub>	ICR13	0000BD <sub>H</sub>
Extended serial I/O	×	9	#38	26 <sub>H</sub>	FFFF64 <sub>H</sub>		
UART(Reception completed) ch.0/ch.1	◎	12	#39	27 <sub>H</sub>	FFFF60 <sub>H</sub>	ICR14	0000BE <sub>H</sub>
Time-base timer	×	×	#40	28 <sub>H</sub>	FFFF5C <sub>H</sub>		
Flash memory status	×	×	#41	29 <sub>H</sub>	FFFF58 <sub>H</sub>	ICR15	0000BF <sub>H</sub>
Delay interrupt output module	×	×	#42	2A <sub>H</sub>	FFFF54 <sub>H</sub>		

(Continued)

(Continued)

- ◎ : Available. EI<sup>2</sup>OS stop function provided (The interrupt request flag is cleared by the interrupt clear signal. With a stop request).
- : Available (The interrupt request flag is cleared by the interrupt clear signal).
- △ : Available when any interrupt source sharing ICR is not used.
- × : Unavailable

\*1 : If the same level interrupt is output simultaneously, the lower interrupt factor of interrupt vector number has priority.

\*2 : Ch.2 and ch.3 can be used in USB HOST operation.

- Notes :
- If the same interrupt control register (ICR) has two interrupt factors and the use of the EI<sup>2</sup>OS is permitted, the EI<sup>2</sup>OS is activated when either of the factors is detected. As any interrupt other than the activation factor is masked while the EI<sup>2</sup>OS is running, it is recommended that you should mask either of the interrupt requests when using the EI<sup>2</sup>OS.
  - The interrupt flag is cleared by the EI<sup>2</sup>OS interrupt clear signal for the resource that has two interrupt factors in the same interrupt control register (ICR).
  - If a resource has two interrupt sources for the same interrupt number, both of the interrupt request flags are cleared by the  $\mu$ DMAC interrupt clear signal. Therefore, when you use either of two interrupt factors for the DMAC function, another interrupt function is disabled. Set the interrupt request permission bit to "0" in the appropriate resource, and take measures by software polling.

## ■ CONTENT OF USB INTERRUPTION FACTOR

USB interrupt factor	Details
USB function 1	End Point 0-IN, End Point 0-OUT
USB function 2	End Point 1-5 *
USB function 3	SUSP, SOF, BRST, WKOP, COHF
USB function 4	SPIT
USB HOST1	DIRQ, CHHIRQ, URIRQ, RWKIRQ
USB HOST2	SOFIRQ, CMPIRQ

\* : End Point 1 and 2 can be used in USB HOST operation.



## ■ USB

### 1. USB Function

The USB function is an interface supporting the USB (Universal Serial Bus) communications protocol.

Features of USB function

- Supports USB Full Speed
- Supports full speed (12 Mbps).
- The device status is auto-answer.
- Bit stripping, bit stuffing, and automatic generation and check of CRC5 and CRC16.
- Toggle check by data synchronization bit.
- Automatic response to all standard commands except Get/SetDescriptor and SynchFrame commands (these three commands can be processed the same way as the class vendor commands).
- The class vendor commands can be received as data and responded via firmware.
- Supports up to a maximum of six EndPoints (EndPoint0 is fixed to control transfer).
- Two built-in transfer data buffers for each end point (one IN buffer and one OUT buffer for end point 0).
- Supports automatic transfer mode for transfer data via DMA (except buffers for EndPoint0).

## 2. USB HOST

USB HOST provides minimal host operations required and is a function that enables data to be transferred between devices without PC intervention.

- Features of USB HOST
  - Automatic detection of Low Speed/Full Speed transfer
  - Low Speed/Full Speed transfer support
  - Automatic detection of connection and cutting device
  - Reset sending function support to USB-bus
  - Support of IN/OUT/SETUP/SOF token
  - In-token handshake packet automatic transmission (excluding STALL)
  - Handshake packet automatic detection at out-token
  - Supports a maximum packet length of 256 bytes
  - Error (CRC error/toggle error/time-out) various supports
  - Wake-Up function support

### • Restrictions on USB HOST

		USB HOST
HUB support		○ *
Transfer	Bulk transfer	○
	Control transfer	○
	Interrupt transfer	○
	Isochronous transfer	×
Transfer speed	Low Speed	○
	Full Speed	○
PRE packet support		×
SOF packet support		○
Error	CRC error	○
	Toggle error	○
	Time-out	○
	Maximum packet < receive data	○
Detection of connection and cutting of device		○
Transfer speed detection		○

○ : Supported

× : Not supported

\* : Only supports full speed, and supports hubs up to one level.

## ■ SECTOR CONFIGURATION OF FLASH MEMORY

512 Kbits flash memory is located in FF<sub>H</sub> bank in the CPU memory map.

Flash Memory    CPU address    Writer address \*

SA0 (4 Kbytes)	FF0000H	70000H	Lower Bank
	FF0FFFH	70FFFH	
SA1 (4 Kbytes)	FF1000H	71000H	
	FF1FFFH	71FFFH	
SA2 (4 Kbytes)	FF2000H	72000H	
	FF2FFFH	72FFFH	
SA3 (4 Kbytes)	FF3000H	73000H	Upper Bank
	FF3FFFH	73FFFH	
SA4 (16 Kbytes)	FF4000H	74000H	
	FF7FFFH	77FFFH	
SA5 (16 Kbytes)	FF8000H	78000H	
	FFBFFFH	7BFFFH	
SA6 (4 Kbytes)	FFC000H	7C000H	Upper Bank
	FFCFFFH	7CFFFH	
SA7 (4 Kbytes)	FFD000H	7D000H	
	FFDFFFH	7DFFFH	
SA8 (4 Kbytes)	FFE000H	7E000H	
	FFEFFFH	7EFFFH	
SA9 (4Kbytes)	FFF000H	7F000H	
	FFFFFFH	7FFFFH	

\* : Flash memory writer address indicates the address equivalent to the CPU address when data is written to the flash memory using a parallel writer. Programming and erasing by the general-purpose parallel programmer are executed based on writer addresses.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	$V_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	
Input voltage*1	$V_I$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	*2
		$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	N-ch open-drain (Withstand voltage I/O of 5 V)*3
		- 0.5	$V_{SS} + 4.5$	V	USB I/O
Output voltage*1	$V_O$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	*2
		- 0.5	$V_{SS} + 4.5$	V	USB I/O
Maximum clamp current	$I_{CLAMP}$	- 2.0	+2.0	mA	*4
Total maximum clamp current	$\Sigma  I_{CLAMP} $	—	20	mA	*4
“L” level maximum output current	$I_{OL1}$	—	10	mA	Other than USB I/O*5
	$I_{OL2}$	—	43	mA	USB I/O*5
“L” level average output current	$I_{OLAV1}$	—	4	mA	*6
	$I_{OLAV2}$	—	15/4.5	mA	USB-IO (Full speed/Low speed) *6
“L” level maximum total output current	$\Sigma I_{OL}$	—	100	mA	
“L” level average total output current	$\Sigma I_{OLAV}$	—	50	mA	*7
“H” level maximum output current	$I_{OH1}$	—	- 10	mA	Other than USB I/O*5
	$I_{OH2}$	—	- 43	mA	USB I/O*5
“H” level average output current	$I_{OHAV1}$	—	- 4	mA	*6
	$I_{OHAV2}$	—	-15/-4.5	mA	USB-IO (Full speed/Low speed) *6
“H” level maximum total output current	$\Sigma I_{OH}$	—	- 100	mA	
“H” level average total output current	$\Sigma I_{OHAV}$	—	- 50	mA	*7
Power consumption	$P_d$	—	270	mW	
Operating temperature	$T_A$	- 40	+ 85	°C	
Storage temperature	$T_{stg}$	- 55	+ 150	°C	
		- 55	+ 125	°C	USB I/O

\*1 : The parameter is based on  $V_{SS} = 0.0$  V.

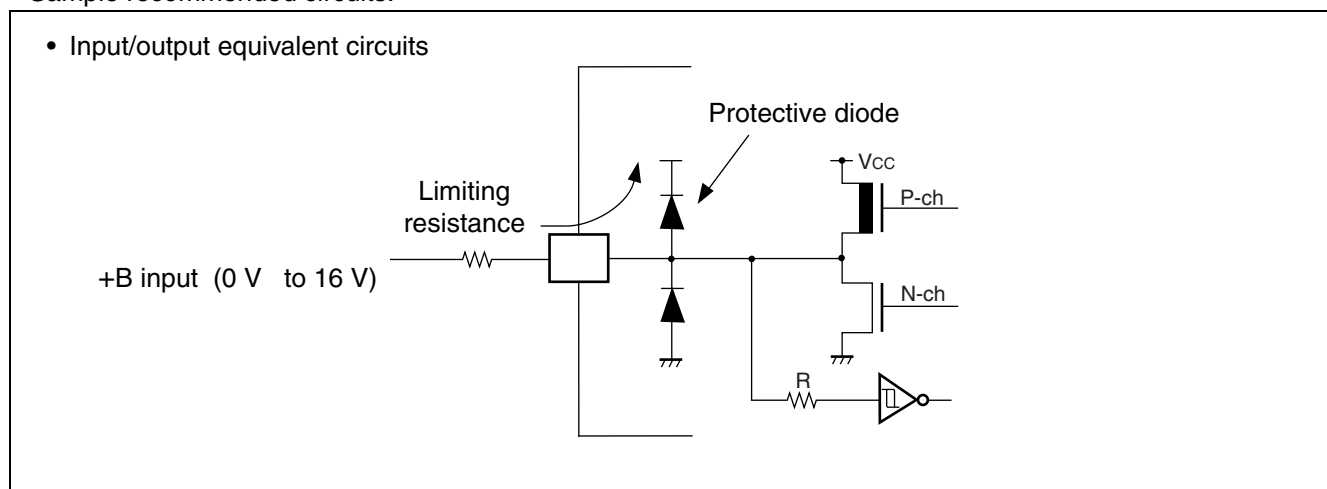
\*2 :  $V_I$  and  $V_O$  must not exceed  $V_{CC} + 0.3$  V. However, if the maximum current to/from an input is limited by some means with external components, the  $I_{CLAMP}$  rating supersedes the  $V_I$  rating.

\*3 : Applicable to pins : P60 to P67, UTEST

(Continued)

(Continued)

- \*4 :
- Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P54
  - Use within recommended operating conditions.
  - Use at DC voltage (current)
  - The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
  - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
  - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the  $V_{CC}$  pin, and this may affect other devices.
  - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
  - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
  - Care must be taken not to leave the +B input pin open.
  - Note that analog system input/output pins other than P60 to P67, DVP, DVM, HVP, HVM, UTEST,  $\overline{HCON}$
- Sample recommended circuits:



- \*5 : A peak value of an applicable one pin is specified as a maximum output current.
- \*6 : The average output current specifies the mean value of the current flowing in the relevant single pin during a period of 100 ms.
- \*7 : The average total output current specifies the mean value of the currents flowing in all of the relevant pins during a period of 100 ms.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

( $V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	$V_{CC}$	3.0	3.6	V	At normal operation (When using USB)
		2.7	3.6	V	At normal operation (When not using USB)
		1.8	3.6	V	Hold state of stop operation
Input "H" voltage	$V_{IH}$	$0.7 V_{CC}$	$V_{CC} + 0.3$	V	CMOS input pin
	$V_{IHS1}$	$0.8 V_{CC}$	$V_{CC} + 0.3$	V	CMOS hysteresis input pin
	$V_{IHS2}$	$0.8 V_{CC}$	$V_{SS} + 5.3$	V	N-ch open-drain (Withstand voltage I/O of 5 V)*
	$V_{IHM}$	$V_{CC} - 0.3$	$V_{CC} + 0.3$	V	MD pin input
	$V_{IHUSB}$	2.0	$V_{CC} + 0.3$	V	USB pin input
Input "L" voltage	$V_{IL}$	$V_{SS} - 0.3$	$0.3 V_{CC}$	V	CMOS input pin
	$V_{ILS}$	$V_{SS} - 0.3$	$0.2 V_{CC}$	V	CMOS hysteresis input pin
	$V_{ILM}$	$V_{SS} - 0.3$	$V_{SS} + 0.3$	V	MD pin input
	$V_{ILUSB}$	$V_{SS}$	0.8	V	USB pin input
Differential input sensitivity	$V_{DI}$	0.2	—	V	USB pin input
Differential common mode input voltage range	$V_{CM}$	0.8	2.5	V	USB pin input
Operating temperature	$T_A$	- 40	+ 85	°C	When not using USB
		0	+ 70	°C	When using USB

\* : Applicable to pins : P60 to P67, UTEST

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.

Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

# MB90335 Series

## 3. DC Characteristics

( $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^{\circ}\text{C}$  to  $+85 \text{ }^{\circ}\text{C}$ )

Parameter	Sym- bol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output “H” voltage	V <sub>OH</sub>	Output pins other than P60 to P67, HVP, HVM, DVP, DVM	I <sub>OH</sub> = −4.0 mA	V <sub>CC</sub> − 0.5	—	V <sub>CC</sub>	V	
		HVP, HVM, DVP, DVM	R <sub>L</sub> = 15 kΩ ± 5%	2.8	—	3.6	V	
Output “L” voltage	V <sub>OL</sub>	Output pins other than HVP, HVM, DVP, DVM	I <sub>OL</sub> = 4.0 mA	V <sub>SS</sub>	—	V <sub>SS</sub> + 0.4	V	
		HVP, HVM, DVP, DVM	R <sub>L</sub> = 1.5 kΩ ± 5%	0	—	0.3	V	
Input leak current	I <sub>IL</sub>	Input pins other than P60 to P67, HVP, HVM, DVP, DVM	V <sub>CC</sub> = 3.3 V, V <sub>SS</sub> < V <sub>I</sub> < V <sub>CC</sub>	− 10	—	+ 10	μA	
		HVP, HVM, DVP, DVM	—	− 5	—	+ 5	μA	
Pull-up resistance	R <sub>PULL</sub>	P00 to P07, P10 to P17	V <sub>CC</sub> = 3.3 V, T <sub>A</sub> = + 25 °C	25	50	100	kΩ	
Open drain output leak current	I <sub>LIOD</sub>	P60 to P67	—	—	0.1	10	μA	
Power supply current	I <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub> = 3.3 V, Internal frequency 24 MHz, At normal operating At USB operating (USTP = 0)	—	55	65	mA	MB90F337
				—	50	60	mA	MB90337
			V <sub>CC</sub> = 3.3 V, Internal frequency 24 MHz, At normal operating At non-operating USB (USTP = 1)	—	50	60	mA	MB90F337
				—	45	55	mA	MB90337
	I <sub>CCS</sub>		V <sub>CC</sub> = 3.3 V, Internal frequency 24 MHz, At sleep mode	—	25	40	mA	
	I <sub>CTS</sub>		V <sub>CC</sub> = 3.3 V, Internal frequency 24 MHz, At timer mode	—	3.5	10	mA	
			V <sub>CC</sub> = 3.3 V, Internal frequency 3 MHz, At timer mode	—	1.0	2.0	mA	
	I <sub>CCH</sub>		T <sub>A</sub> = +25 °C, At stop mode	—	1	40	μA	

(Continued)

(Continued)

( $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^{\circ}\text{C}$  to  $+85 \text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input capacitance	$C_{IN}$	Other than Vcc and Vss	—	—	5	15	pF	
Pull-up resistor	$R_{up}$	$\overline{RST}$	—	25	50	100	k $\Omega$	
Pull-down resistor	$R_{down}$	MD2	$V_{CC} = 3.0 \text{ V}$ At $T_A = +25 \text{ }^{\circ}\text{C}$	25	50	100	k $\Omega$	MB90337
USB I/O output impedance	$Z_{USB}$	DVP, DVM HVP, HVM	—	3	—	14	$\Omega$	

Note : P60 to P67 are N-ch open-drain pins usually used as CMOS.



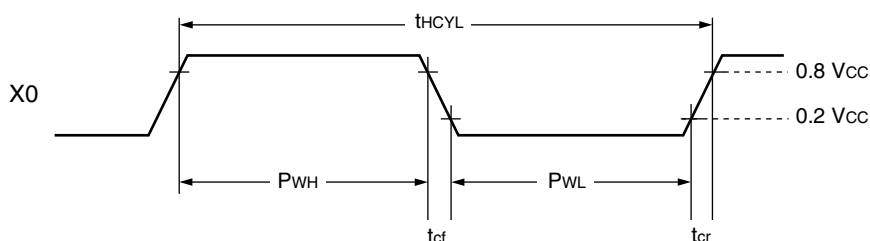
## 4. AC Characteristics

### (1) Clock input timing

( $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^{\circ}\text{C}$  to  $+85 \text{ }^{\circ}\text{C}$ )

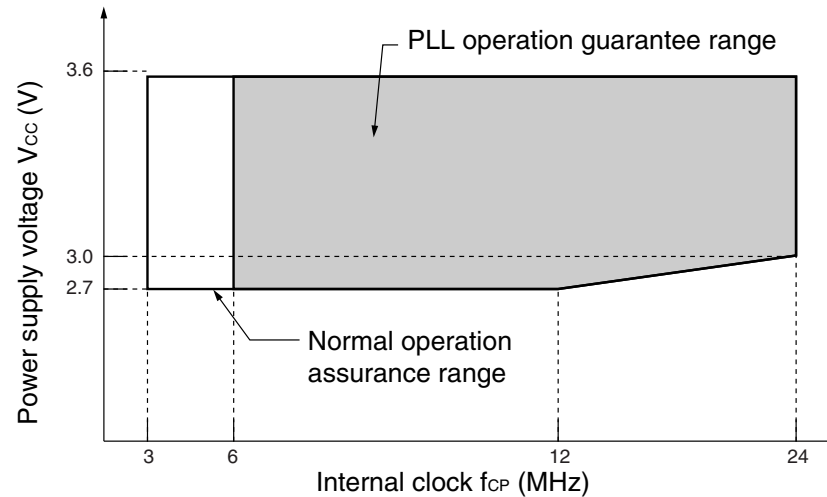
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	$f_{CH}$	X0, X1	—	6	—	MHz	When oscillator is used
			6	—	24	MHz	External clock input
Clock cycle time	$t_{HCYL}$	X0, X1	—	166.7	—	ns	When oscillator is used
			166.7	—	41.7	ns	External clock input
Input clock pulse width	$P_{WH}$ $P_{WL}$	X0	10	—	—	ns	A reference duty ratio is 30% to 70%.
Input clock rise time and fall time	$t_{cr}$ $t_{cf}$	X0	—	—	5	ns	At external clock
Internal operating clock frequency	$f_{CP}$	—	3	—	24	MHz	When main clock is used
Internal operating clock cycle time	$t_{CP}$	—	42	—	333	ns	When main clock is used

#### • Clock Timing



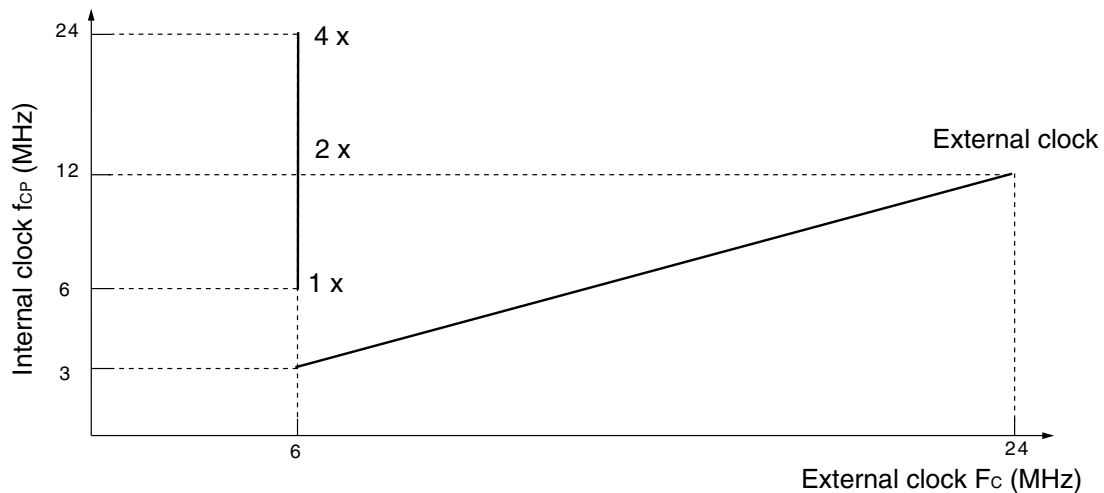
- PLL operation guarantee range

Relation between power supply voltage and internal operation clock frequency



Note : When the USB is used, operation is guaranteed at voltages between 3.0 V to 3.6 V.

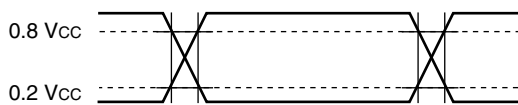
Relation between internal operation clock frequency and external clock frequency



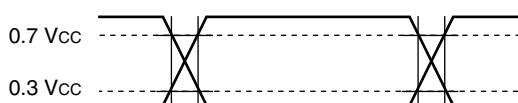
The AC standards provide that the following measurement reference voltages.

- Input signal waveform

Hysteresis input pin

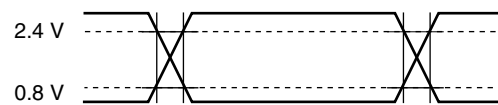


Hysteresis input/other than MD input pin



- Output signal waveform

Output pin



# MB90335 Series

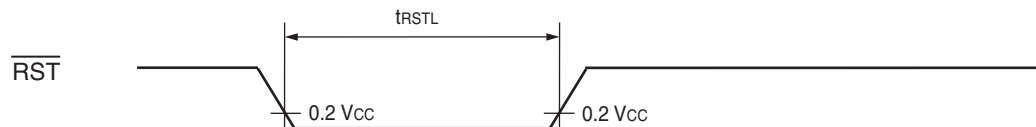
## (2) Reset

( $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

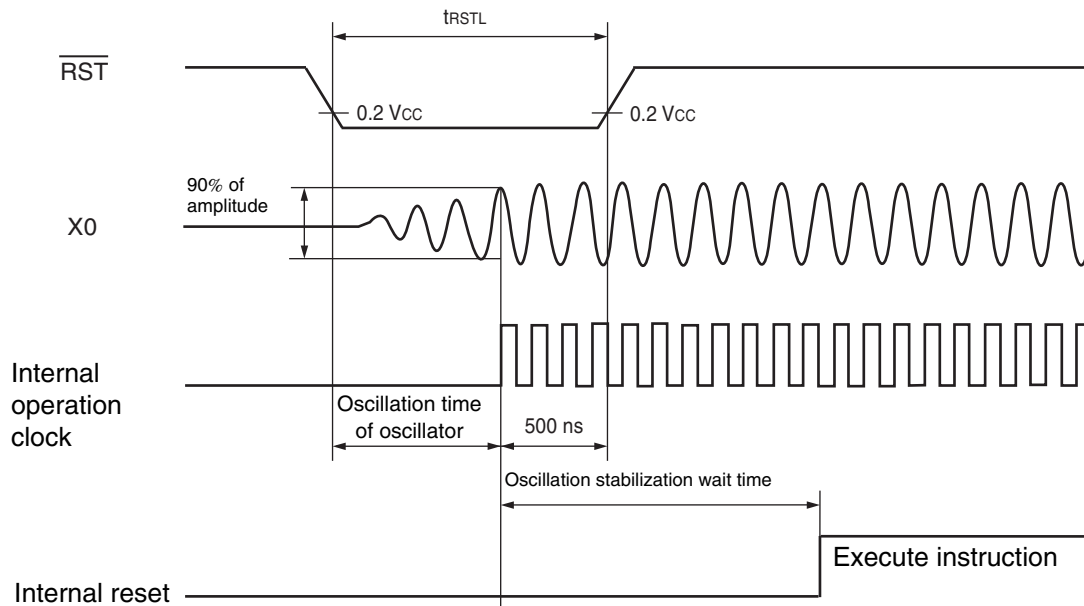
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	$t_{RSTL}$	$\overline{\text{RST}}$	—	500	—	ns	At normal operating, At time base timer mode, At main sleep mode, At PLL sleep mode
				Oscillation time of oscillator* + 500 ns	—	$\mu\text{s}$	At stop mode

\* : Oscillation time of oscillator is the time that the amplitude reaches 90 %. It takes several milliseconds to several dozens of milliseconds on a crystal oscillator, several hundreds of microseconds to several milliseconds on a ceramic oscillator, and 0 milliseconds on an external clock.

- During normal operation, time-base timer mode, main sleep mode and PLL sleep mode



- During stop mode

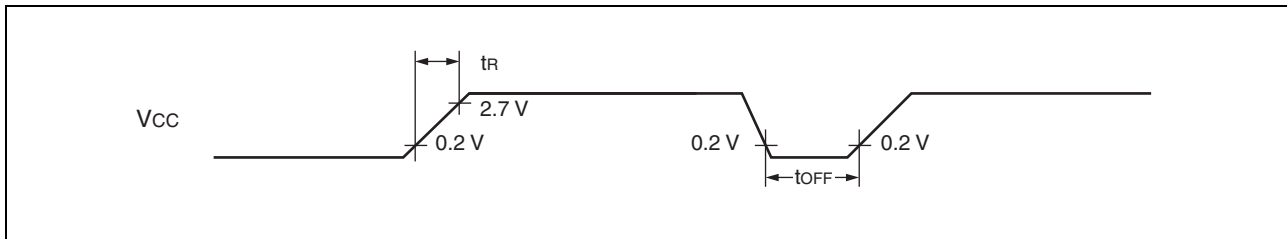


## (3) Power-on reset

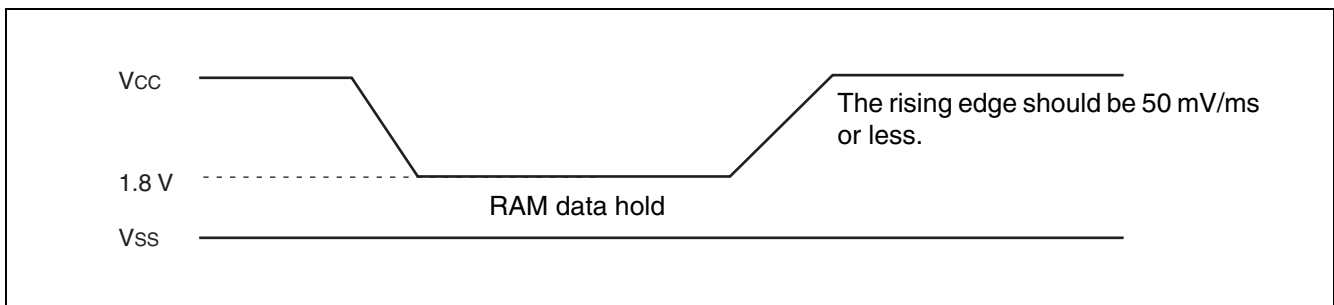
( $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^{\circ}\text{C}$  to  $+85 \text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rising time	$t_R$	$V_{CC}$	—	0.05	30	ms	
Power supply shutdown time	$t_{OFF}$	$V_{CC}$		1	—	ms	Waiting time until power-on

- Notes :
- $V_{CC}$  must be lower than 0.2 V before the power supply is turned on.
  - The above standard is a value for performing a power-on reset.
  - In the device, there are internal registers which is initialized only by a power-on reset. When the initialization of these items is expected, turn on the power supply according to the standards.



Note : Sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during operation as illustrated below, voltage fluctuation should be minimized so that the voltage rises as smoothly as possible. When raising the power, do not use PLL clock. However, if voltage drop is 1 V/s or less, use of PLL clock is allowed during operation.



# MB90335 Series

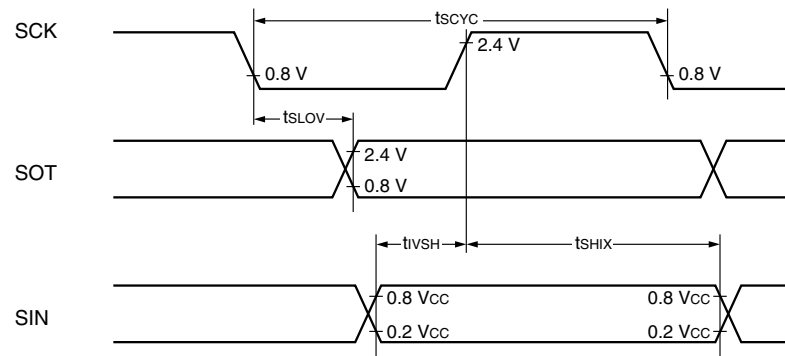
## (4) UART0, UART1 I/O extended serial timing

( $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

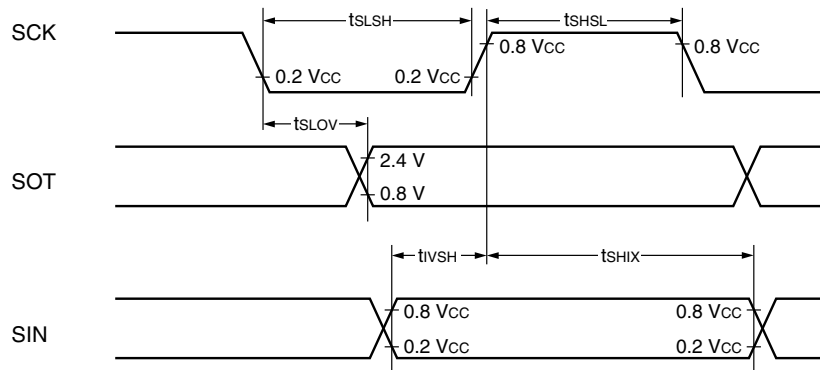
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCKx	Internal shift clock Mode output pin is $C_L = 80 \text{ pF} + 1 \text{ TTL}$	8 $t_{CP}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	$t_{SLOV}$	SCKx SOTx		- 80	+ 80	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	$t_{IVSH}$	SCKx SINx		100	—	ns
SCK $\uparrow \rightarrow$ valid SIN hold time	$t_{SHIX}$	SCKx SINx		60	—	ns
Serial clock H pulse width	$t_{SHSL}$	SCKx, SINx	External shift clock Mode output pin is $C_L = 80 \text{ pF} + 1 \text{ TTL}$	4 $t_{CP}$	—	ns
Serial clock L pulse width	$t_{SLSH}$	SCKx, SINx		4 $t_{CP}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	$t_{SLOV}$	SCKx SOTx		—	150	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	$t_{IVSH}$	SCKx SINx		60	—	ns
SCK $\uparrow \rightarrow$ valid SIN hold time	$t_{SHIX}$	SCKx SINx		60	—	ns

- Notes :
- Above rating is the case of CLK synchronous mode.
  - $C_L$  is a load capacitance value on pins for testing.
  - $t_{CP}$  is the machine cycle period (unit : ns) . Refer to “(1) Clock input timing”.

### • Internal shift clock mode



### • External shift clock mode



## (5) I<sup>2</sup>C timing

(V<sub>CC</sub> = 3.3 V ± 0.3 V, V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCL clock frequency	f <sub>SCL</sub>	Power-supply of external pull-up resistor at 5.0 V R = 1.2 kΩ, C = 50 pF*2 Power-supply of external pull-up resistor at 3.6 V R = 1.0 kΩ, C = 50 pF*2	0	100	kHz
(Repeat) [start] condition hold time SDA ↓ → SCL ↓	t <sub>HDSTA</sub>		4.0	—	μs
SCL clock “L” width	t <sub>LOW</sub>		4.7	—	μs
SCL clock “H” width	t <sub>HIGH</sub>		4.0	—	μs
Repeat [start] condition setup time SCL ↑ → SDA ↓	t <sub>SUSTA</sub>		4.7	—	μs
Data hold time SCL ↓ → SDA ↓ ↑	t <sub>HDDAT</sub>		0	3.45*3	μs
Data setup time SDA ↓ ↑ → SCL ↑	t <sub>SUDAT</sub>	Power-supply of external pull-up resistor at 5.0 V f <sub>CP</sub> *1 ≤ 20 MHz, R = 1.2 kΩ, C = 50 pF*2 Power-supply of external pull-up resistor at 3.6 V f <sub>CP</sub> *1 ≤ 20 MHz, R = 1.0 kΩ, C = 50 pF*2	250*4	—	ns
		Power-supply of external pull-up resistor at 5.0 V f <sub>CP</sub> *1 > 20 MHz, R = 1.2 kΩ, C = 50 pF*2 Power-supply of external pull-up resistor at 3.6 V f <sub>CP</sub> *1 > 20 MHz, R = 1.0 kΩ, C = 50 pF*2	200*4	—	
[Stop] condition setup time SCL ↑ → SDA ↑	t <sub>SUSTO</sub>	Power-supply of external pull-up resistor at 5.0 V R = 1.2 kΩ, C = 50 pF*2	4.0	—	μs
Bus free time between [stop] condition and [start] condition	t <sub>BUS</sub>	Power-supply of external pull-up resistor at 3.6 V R = 1.0 kΩ, C = 50 pF*2	4.7	—	μs

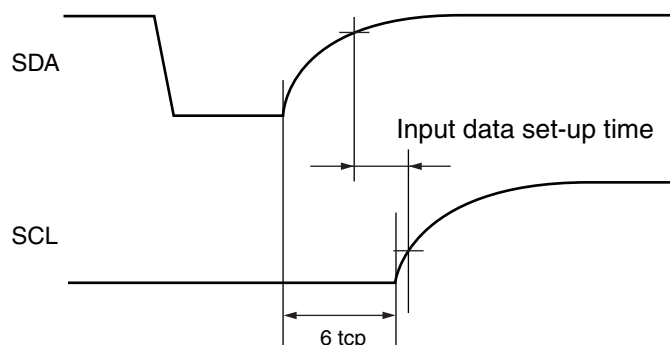
\*1 : f<sub>CP</sub> is internal operating clock frequency. Refer to “(1) Clock input timing”.

\*2 : R and C are pull-up resistance of SCL and SDA lines and load capacitance.

\*3 : The maximum t<sub>HDDAT</sub> only has to be met if the device does not stretch the “L” width (t<sub>LOW</sub>) of the SCL signal.

\*4 : Refer to “• Note of SDA, SCL set-up time”.

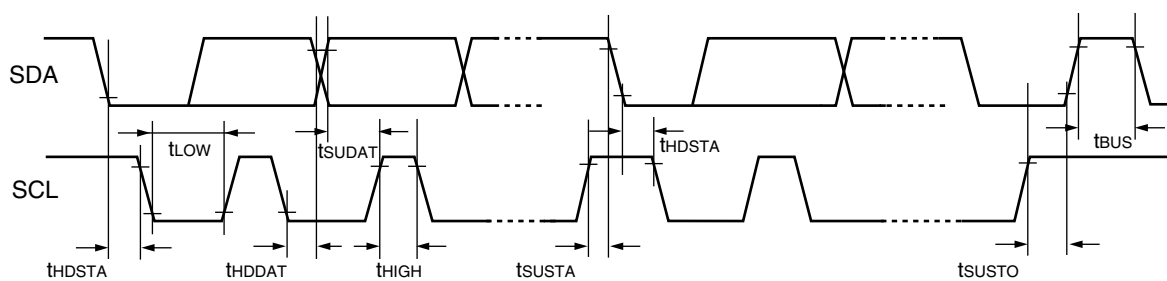
## •Note of SDA, SCL set-up time



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.

Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

## •Timing definition

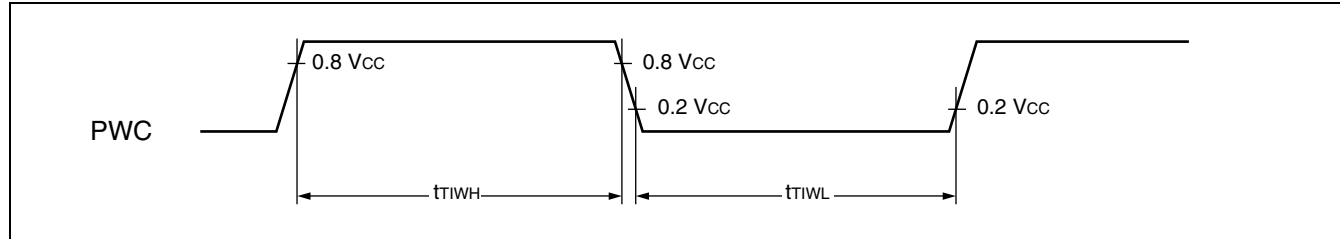


## (6) Timer Input Timing

( $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	$t_{TIWH}$ $t_{TIWL}$	PWC	—	$4\ t_{CP}$	—	ns

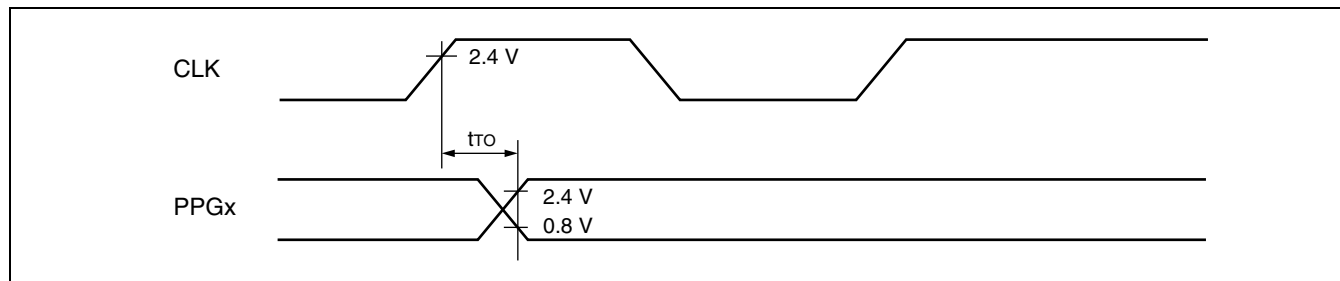
Note :  $t_{CP}$  is the machine cycle period (unit : ns) . Refer to “ (1) Clock input timing”.



## (7) Timer output timing

( $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
CLK $\uparrow \rightarrow T_{OUT}$ change time PPG0 to PPG3 change time	$t_{TO}$	PPGx	—	30	—	ns

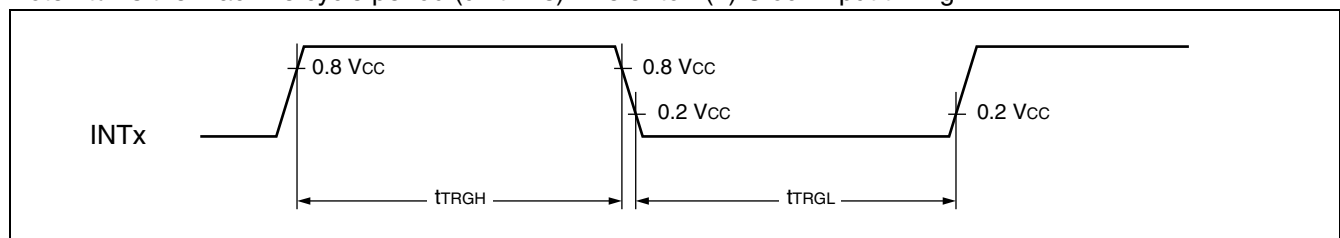


## (8) Trigger Input Timing

( $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TRGH}$	INTx	—	$5\ t_{CP}$	—	ns	At normal operating
	$t_{TRGL}$			1	—	$\mu\text{s}$	At Stop mode

Note :  $t_{CP}$  is the machine cycle period (unit : ns) . Refer to “ (1) Clock input timing”.





# MB90335 Series

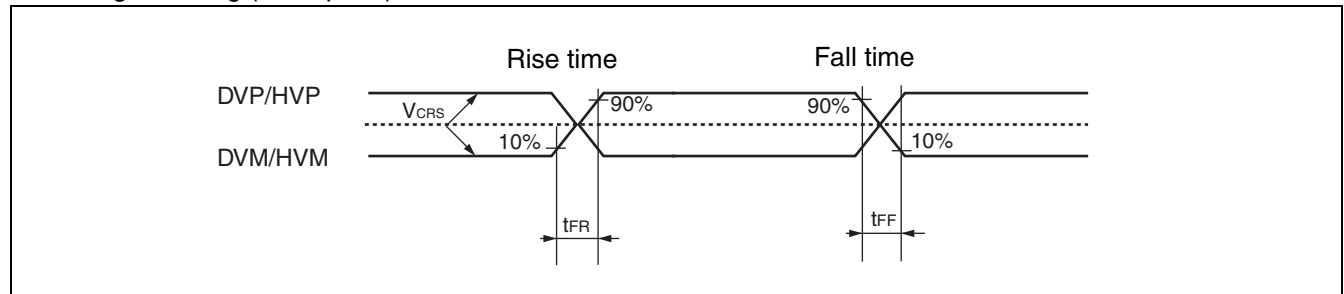
## 5. USB characteristics

( $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_A = 0^\circ \text{C}$  to  $+70^\circ \text{C}$ )

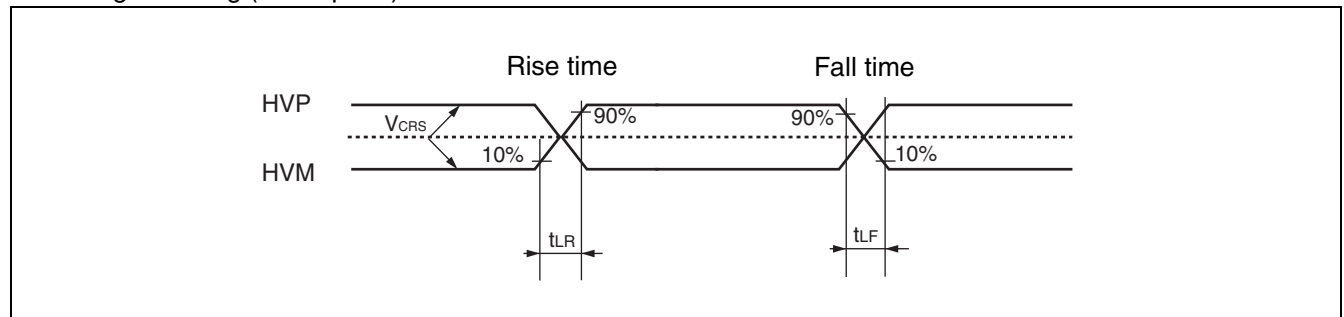
Parameter	Symbol	Sym- bol	Value		Unit	Remarks
			Min	Max		
Input characteristics	Input High level voltage	V <sub>IH</sub>	2.0	—	V	
	Input Low level voltage	V <sub>IL</sub>	—	0.8	V	
	Differential input sensitivity	V <sub>DI</sub>	0.2	—	V	
	Differential common mode range	V <sub>CM</sub>	0.8	2.5	V	
Output characteristics	Output High level voltage	V <sub>OH</sub>	2.8	3.6	V	I <sub>OH</sub> = −200 μA
	Output Low level voltage	V <sub>OL</sub>	0.0	0.3	V	I <sub>OL</sub> = 2 mA
	Cross over voltage	V <sub>CRS</sub>	1.3	2.0	V	
	Rise time	t <sub>FR</sub>	4	20	ns	Full Speed
		t <sub>LR</sub>	75	300	ns	Low Speed
	Fall time	t <sub>FF</sub>	4	20	ns	Full Speed
		t <sub>LF</sub>	75	300	ns	Low Speed
	Rising/falling time matching	t <sub>RFM</sub>	90	111.11	%	(T <sub>FR</sub> /T <sub>FF</sub> )
		t <sub>RLM</sub>	80	125	%	(T <sub>LR</sub> /T <sub>LF</sub> )
Output impedance	Z <sub>DRV</sub>	28	44	Ω	Including R <sub>s</sub> = 27 Ω	
Series resistance		R <sub>S</sub>	25	30	Ω	Recommended value = 27 Ω at using USB*

\* : Arrange the series resistance  $R_s$  values in order to set the impedance value within the output impedance ZSRV.

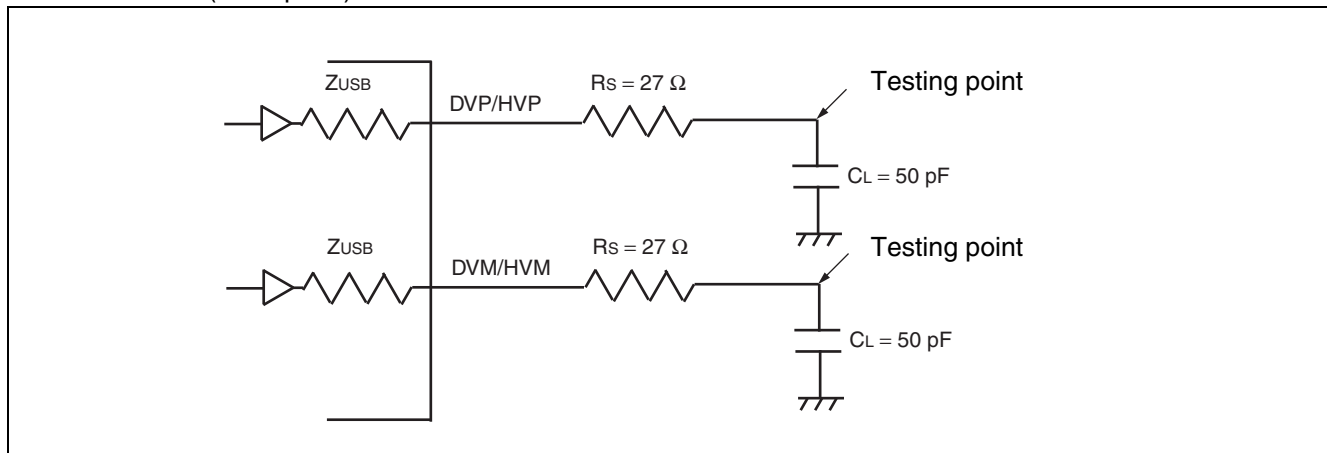
### • Data signal timing (Full Speed)



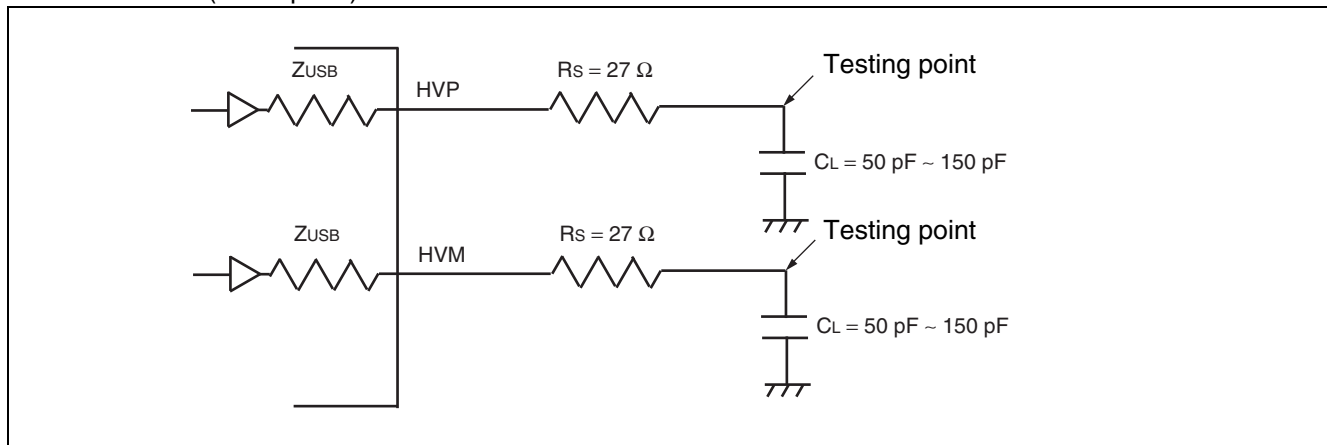
### • Data signal timing (Low Speed)



- Load condition (Full Speed)



- Load condition (Low Speed)



## 6. Flash memory write/erase characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	T <sub>A</sub> = + 25 °C V <sub>CC</sub> = 3.0 V	—	0.2	0.5	s	Excludes 00 <sub>H</sub> programming prior to erasure.
Sector erase time (16 Kbytes sector)		—	0.5	7.5	s	Excludes 00 <sub>H</sub> programming prior to erasure.
Chip erase time		—	2.6	—	s	Excludes 00 <sub>H</sub> programming prior to erasure.
Word (8 bits width) programming time		—	16	3600	μs	Except for over head time of system
Program/erase cycle	—	10000	—	—	cycle	
Flash data retention time	Average T <sub>A</sub> = + 85 °C	20	—	—	year	*

\* : This value comes from the technology qualification. (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C)

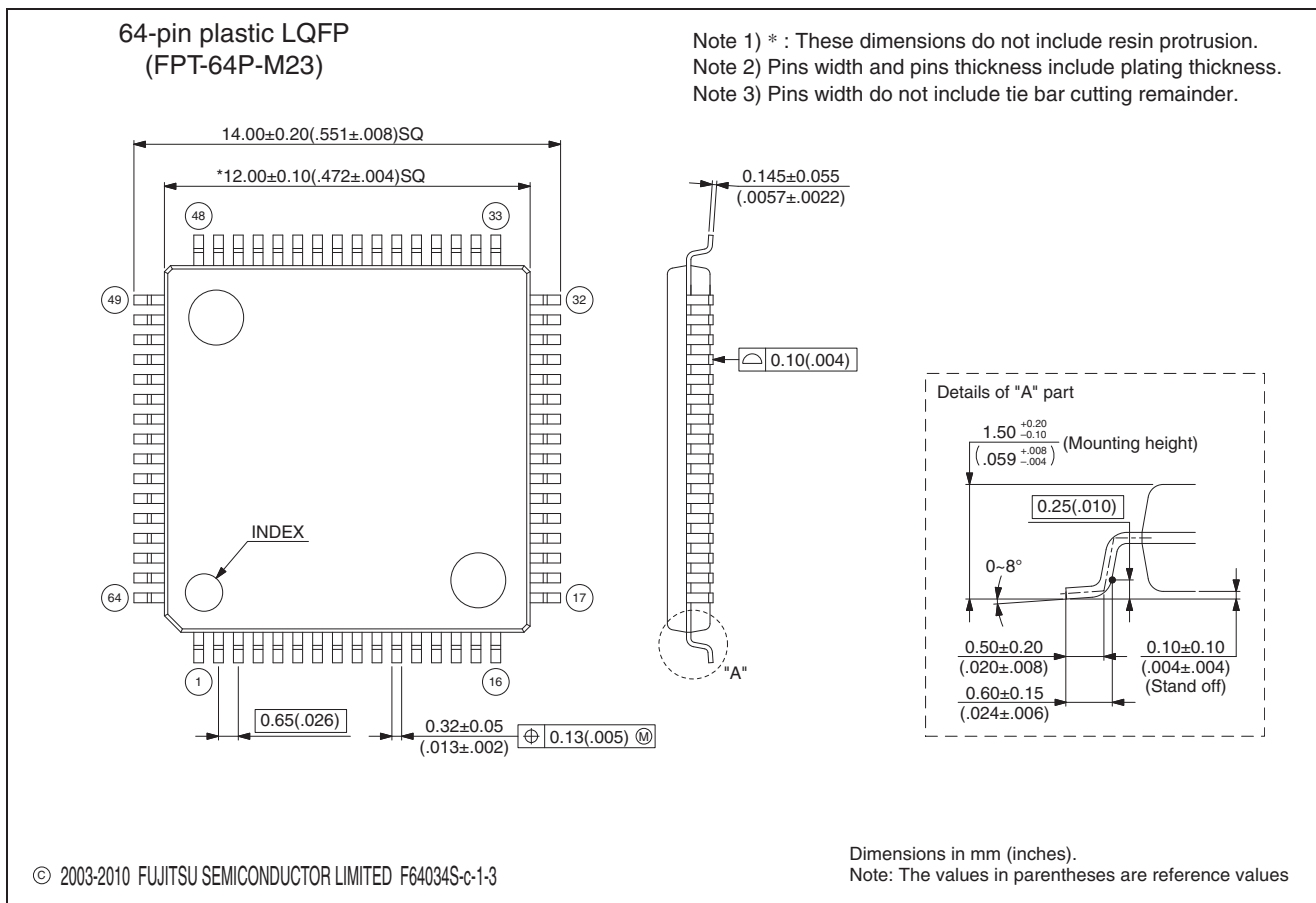
## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F337PMC MB90337PMC	64-pin plastic LQFP (FPT-64P-M23)	
MB90V330ACR	299-pin ceramic PGA (PGA-299C-A01)	For evaluation

# MB90335 Series

## ■ PACKAGE DIMENSION

<p>64-pin plastic LQFP</p> <p>(FPT-64P-M23)</p>	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g
	Code (Reference)	P-LQFP64-12×12-0.65



Please check the latest package dimension at the following URL.  
<http://edevic.fujitsu.com/package/en-search/>

## ■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
35	■ ELECTRICAL CHARACTERISTICS 4.AC Characteristics (3) Power-on reset	Corrected as follows; Voltage of RAM data hold: 3.0 V → 1.8 V

The vertical lines marked in the left side of the page show the changes.

**MEMO**

**MEMO**



# MB90335 Series

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