DS92LV222A

DS92LV222A Two Channel Bus LVDS MUXed Repeater



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General Description

The DS92LV222A is a repeater designed specifically for the bridging of multiple backplanes in a rack. The DS92LV222A utilizes low voltage differential signaling to deliver high speed while consuming minimal power with reduced EMI. The RSEL pin and DE pins allow maximum flexibility as to which receiver/driver are used. The DS92LV222A repeats signals between backplanes and accepts or drives signals onto the local bus. It also features a flow through pin out which allows easy PCB routing for short stubs between its pins and the connector.

The driver is selectable between 3.5 mA ($100\Omega \log ad$) and 8.5 mA ($27\Omega \log ad$) output loop currents depending upon the level applied to the ISEL pin. This allows for single termination (point-to-point) and also double termination (multipoint) applications while maintain similar differential levels.

The receiver threshold is ± 100 mV, while providing $\pm 1V$ common mode range.

Features

- Bus LVDS Signaling (BLVDS)
- Designed for Double Termination Applications
- Low power CMOS design
- High Signaling Rate Capability (above 100 Mbps)
- Ultra Low Power Dissipation (13.2 mW quiescent)
- Balanced Output Impedance
- Lite Bus Loading 5 pF typical
- Selectable Drive Capability (3.5 mA or 8.5 mA)
- 3.3V operation
- ±1V Common Mode Range
- ±100 mV Receiver Sensitivity
- Available in 16 pin SOIC package.

Connection Diagram



Block Diagram



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Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ . Distributors for availability and specifications.

Supply Voltage (V _{CC})	6.0V
Enable Input Voltage (DE)	–0.3V to (V _{CC} + 0.3V)
Current Select Voltage (ISEL)	-0.3V to (V _{CC} + 0.3V)
Receiver Select Voltage (RSEL)	-0.3V to (V _{CC} + 0.3V)
Bus Pin Voltage (DO/RI±)	-0.3V to +3.9V
Driver Short Circuit Current	Continuous
ESD (HBM 1.5 kΩ, 100 pF)	>2 kV
Maximum Package Power Dissi	pation at 25°C
SOIC	970 mW

Derate SOIC Package	
above 25°C	8mW/°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
(Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	3.0	3.6	V
Receiver Input Voltage	0.0	2.9	V
Operating Free Air Temperature	-40	+85	°C

DC Electrical Characteristics

 T_{A} = -40°C to +85°C unless otherwise noted, V_{CC} = 3.3V \pm 0.3V (Notes 2, 3)

Symbol	Parameter	Conditions	Pin	Min	Тур	Max	Units
DIFFERE	NTIAL DRIVER CHARACTE	RISTICS		-	-		
V _{OD}	Output Differential Voltage	$R_L = 27\Omega$ Figure 1 Isel = 0V	DO+, DO–	170	220	280	mV
ΔV_{OD}	VOD Magnitude Change				2	10	mV
V _{os}	Offset Voltage			1.0	1.25	1.6	V
ΔV _{OS}	Offset Magnitude Change				10	20	mV
V _{OD}	Output Differential Voltage	$R_{L} = 100\Omega \ Figure \ 1$ Isel = 3.3V		250	360	480	mV
ΔV_{OD}	VOD Magnitude Change				2	10	mV
Vos	Offset Voltage			0.9	1.25	1.6	V
ΔV_{OS}	Offset Magnitude Change				10	20	mV
I _{OZD}	TRI-STATE [®] Leakage	$V_{O} = V_{CC}$ or GND, DE = 0			±1	±10	μA
I _{OXD}	Power-Off Leakage	$V_{O} = 2.9V \text{ or GND},$ $V_{CC} = 0V$			±1	±10	μA
I _{OSD}	Output Short Circuit Current	$ISEL = V_{CC}$ $V_O = 0V$			-11	-13	mA
DIFFERE	NTIAL RECEIVER CHARAC	TERISTICS		•	•		
V _{TH}	Input Threshold High		RI+, RI–			+100	mV
V _{TL}	Input Threshold Low			-100			mV
I _{IN}	Input Current	$V_{IN} = +2.9V, \text{ or } 0V, V_{CC}$ = 3.6 V or 0 V		-10	±1	+10	μA
DEVICE (CHARACTERISTICS						
V _{IH}	Minimum Input High Voltage		DE0, DE1,	2.0		V _{cc}	V
V _{IL}	Maximum Input Low Voltage		RSEL, ISEL0,	GND		0.8	V
IIH	Input High Current	$V_{IN} = V_{CC} \text{ or } 2.4 V$	ISEL1		±1	±10	μA
IIL	Input Low Current	$V_{IN} = GND \text{ or } 0.4V$]		±1	±10	μA
V _{CL}	Input Diode Clamp Voltage	$I_{CLAMP} = -18 \text{ mA}$		-1.5	-0.8		V

DC Electrical Characteristics (Continued)

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 T_{A} = -40°C to +85°C unless otherwise noted, V_{CC} = 3.3V \pm 0.3V (Notes 2, 3)

Symbol	Parameter	Conditions	Pin	Min	Тур	Мах	Units
DEVICE CHARACTERISTICS							
I _{CCD}	Power Supply Current	No Load; DE = RSEL = V _{cc} Isel = 0 V	V _{cc}		25	45	mA
		$R_L = 27\Omega$; DE = RSEL = V _{CC} lsel = 0 V			24	40	mA
I _{ccz}		$DE = 0V; RSEL = V_{CC}$			4	8	mA
C _{input}	Capacitance at		RO+/RO-		5		pF
C _{output}	Capacitance at		DO+/DO-		5		pF

Note 1: "Absolute Maximum Ratings" are these beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = +3.3V and T $_{\rm A}$ = +25°C, unless otherwise stated.

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF) > 2 kV EIAJ (0Ω, 200 pF) > 200V

Note 5: CL includes probe and fixture capacitance.

Note 6: Generator waveforms for all tests unless otherwise specified: f = 1MHz, ZO = 50 Ω , t_f = < 6.0 ns (0%-100%).

Note 7: The DS92LV222A is a current mode device and only functions datasheet specifications when a resistive load is applied to the drivers outputs.

Note 8: During receiver select transition(s), data must be held in a steady state 15 ns before and 15 ns after the RSEL pin changes state.

Note 9: Channel-to-channel skew is the measurement between outputs of D0 and D1.

AC Electrical Characteristics

 $T_A = -40^{\circ}C$ to +85°C, $V_{CC} = 3.3V \pm 0.3V$ (Note 6)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
t _{TLH}	Transition Time Low to High	$R_L = 27\Omega$ Figures 2, 3	0.15	0.4	2.0	ns
t _{THL}	Transition Time High to Low	$C_L = 10 \text{ pF } Figures 2, 3$	0.15	0.4	2.0	ns
t _{PHZ}	Disable Time High to Z	$R_L = 27\Omega$ Figures 4, 5	2.0	6.0	9.0	ns
t _{PLZ}	Disable Time Low to Z	$C_{L} = 10 \text{ pF } Figures 4, 5$	2.0	6.0	9.0	ns
t _{PZH}	Enable Time Z to High		2.0	6.0	9.0	ns
t _{PZL}	Enable Time Z to Low		2.0	6.0	9.0	ns
DIFFERENTIAL RECEIVER TO DRIVER TIMING REQUIREMENTS						
t _{PHL_RD}	Differential Prop. Delay High to Low	$R_L = 27\Omega$ Figures 2, 3	3.0	7.7	13	ns
t _{PLH_RD}	Differential Prop. Delay Low to High	$C_L = 10 \text{ pF } Figures 2, 3$	3.0	8.0	13	ns
t _{SK_RD}	Pulse SKEW t PHL -tPLH		0	0.3	2.0	ns
t _{PHL_RS0}	Prop. Delay High to Low	RSEL to Driver Outputs $P_{r} = 270$ Figures 6, 7	2.0	7.5	13	ns
t _{PLH_RS1}	Prop. Delay Low to High	$R_{L} = 2732 \text{ Figures 0, 7}$ $C_{L} = 10 \text{ pF} (Note 8)$	2.0	8.0	13	ns
t _{PHL_R0 Dx}	Channel-to-Channel Skew R $_{\rm 0}$ to D $_{\rm x}$	$R_L = 27\Omega$		0.3	0.8	ns
t _{PLH_R0 Dx}	Channel-to-Channel Skew R $_0$ to D _x	C _L = 10 pF		0.3	0.8	ns
t _{PHL_R1 Dx}	Channel-to-Channel Skew R $_1$ to D _x	(Note 9)		0.3	0.8	ns
t _{PLH_R1 Dx}	Channel-to-Channel Skew R $_1$ to D _x			0.3	0.8	ns

Test Circuits and Timing Waveforms D0+ Power **∩**∢ Supply RI+ $R_{L/2}$ R RI- $R_{1./2}$ Power Driver Enabled Supply DO-DS100055-3 FIGURE 1. Differential Driver DC Test Circuit RI+ • DO+ Pulse D **Š** R_L RI-Generator DO-Ş **\$** 50Ω 50Ω DS100055-4 FIGURE 2. Differential Receiver to Driver Propagation Delay and Driver Transition Time Test Circuit RI-+1.3V V_{ID} = 200 mV OV Differential (1.2V CM) +1.1V RI+ → t_{PLH} → t_{PHL} D0-+1.3V $V_{ID} = 200 \text{ mV}$ 0V Differential (1.2V CM) •+1.1V DO+ 80% 80% 20% 20% {(DO+)-(DO-)} t_{TLH} → t_{THL} -> DS100055-5 FIGURE 3. Differential Receiver to Driver Propagation Delay and Driver Transition Time Waveforms D0+ $R_{L/2}$ RI+ Pulse RI-R Generator +1.2V $R_{L/2}$ **\$** 50Ω 50Ω DE Pulse Generator ξ 50Ω DS100055-6 FIGURE 4. Driver TRI-STATE Delay Test Circuit



RI±	4	I	Bus LVDS Receiver Inputs
DO±	4	0	Bus LVDS Driver Outputs
RSEL	1	I	Receiver Select TTL Input, (see Truth Tables)
DE	2	I	Driver Enable TTL Input, Active High
ISEL	2	I	IOL Control Pin (Select High = 3.5 mA (100 Ω Load), Select Low = 8.5mA (27 Ω Load))
GND	1	NA	Ground Reference
V _{CC}	1	NA	Power Supply
Reserved	1	NA	Reserved Pin

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Function Select Table

MODE SELECTED	DE0	DE1	RSEL
Receiver Zero ON, Driver Zero ON, Driver One OFF	н	L	L
Receiver Zero ON, Driver Zero OFF, Driver One ON	L	н	L
Receiver One ON, Driver Zero ON, Driver One OFF	н	L	н
Receiver One ON, Driver Zero OFF, Driver One ON	L	Н	н
Receiver Zero ON, Driver Zero ON, Driver One ON	Н	н	L
Receiver One ON, Driver Zero ON, Driver One ON	Н	Н	н
Driver Zero and Driver One TRI-STATE	L	L	X

Truth Table for Receiver Zero

	INPUTS			
DE0	RSEL	(RI0+)–(RI0–)	DO+	DO-
Н	L	L	L	Н
Н	L	Н	Н	L
Н	L	100 mV > & > -100 mV	Х	Х
L	Х	Х	Z	Z

Truth Table for Receiver One

	INPUTS				
DE1	DE1 RSEL (RI1+)–(RI1–)				
Н	Н	L	L	Н	
Н	Н	Н	н	L	
Н	Н	100 mV > & > -100 mV	Х	Х	
L	Х	Х	Z	Z	

X = High or low logic state

Z = High impedance state

L = Low state

Truth Table for Current Drive

X =	High	or	low	logic	state	

Z = High impedance state

L = Low state

Driver	Current Drive	ISEL0	ISEL1
Driver 0	3.5 mA	Н	Х
Driver 0	8.5 mA	L	Х
Driver 1	3.5 mA	Х	Н
Driver 1	8.5 mA	Х	L

Applications Information

There are few common practices which should be employed when designing PCB for Bus LVDS signaling. Recommended practices are:

- Use at least 4 PCB board layer (Bus LVDS signals, ground, power and TTL signals).
- Keep drivers and receivers as close to the (Bus LVDS port side) connector as possible.
- Bypass each Bus LVDS device and also use distributed bulk capacitance. Surface mount capacitors placed close to power and ground pins work best. Two or three multi-layer ceramic (MLC) surface mount capacitors (0.1 μ and 0.01 μ F in parallel should be used between each V_{CC} and ground. The capacitors should be as close as possible to the V_{CC} pin.
- Use controlled impedance traces which match the differential impedance of your transmission medium (i.e., Cable) and termination resistor.
- Use the termination resistor which best matches the differential impedance of your transmission line.
- Leave unused Bus LVDS receiver inputs open (floating).
- Isolate TTL signals from Bus LVDS signals.

MEDIA (CABLE, CONNECTOR OR BACKPLANE) SELECTION:

 Use controlled impedance media. The cables and connectors should have a matched differential impedance.

- Balanced cables (e.g., twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax) for noise reduction and signal quality.
- There are different types of failsafe situations to consider, these are Open Input, Terminated Input, and other special cases. The first, Open input failsafe occurs when only one receiver is being used (R0 for example). The unused receiver (R1) inputs should be left open for noise minimization. The second case is for terminated inputs. This occurs when the inputs have a low impedance (typically 100 Ohm) termination (R $_{T}$) across them, and the cable is unplugged. For this case, and if the output state needs to maintain a known state, two external bias resistors may be used to provide a strong common mode bias point. For this a 10K Ohm pull up and pull down resistor may be used to set the output high. Note that R1 and R2 should be much larger (2 orders of magnitude) compared to R $_{T}$ to minimize loading effects to the Bus LVDS driver when it is active.

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Applications Information (Continued)





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National Semiconductor Corporation Americas Tel: 1-800-272-9959 Fax: 1-800-737-7018 Email: support@nsc.com www.national.com National Semiconductor Europe Fax: +49 (0) 180-530 85 86 Email: europe.support@nsc.com Deutsch Tel: +49 (0) 69 9508 6208 English Tel: +44 (0) 870 24 0 2171 Français Tel: +33 (0) 1 41 91 8790 National Semiconductor Asia Pacific Customer Response Group Tel: 65-2544466 Fax: 65-2504466 Email: ap.support@nsc.com National Semiconductor Japan Ltd. Tel: 81-3-5639-7560 Fax: 81-3-5639-7507

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