

## DS91M047 125 MHz Quad M-LVDS Line Driver

Check for Samples: [DS91M047](#)

### FEATURES

- DC - 125 MHz / 250 Mbps Low Jitter, Low Skew, Low Power Operation
- Conforms to TIA/EIA-899 M-LVDS Standard
- Controlled Transition Times (2 ns typ) Minimize Reflections
- 8 kV ESD on M-LVDS Pins Protects Adjoining Components
- Flow-Through Pinout Simplifies PCB Layout
- Industrial Operating Temperature Range (–40°C to +85°C)
- Available in a Space Saving SOIC-16 Package

### APPLICATIONS

- Multidrop / Multipoint Clock and Data Distribution
- High-Speed, Low Power, Short-Reach Alternative to TIA/EIA-485/422
- Clock Distribution in AdvancedTCA (ATCA) and MicroTCA (μTCA, uTCA) Backplanes

### DESCRIPTION

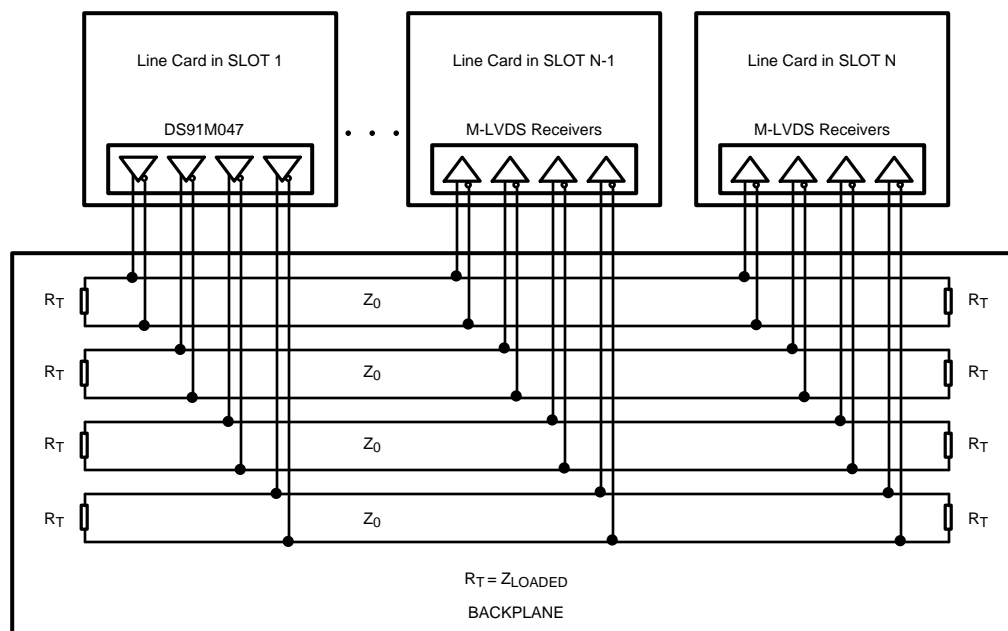
The DS91M047 is a high-speed quad M-LVDS line driver designed for driving clock or data signals to up to four multipoint networks.

M-LVDS (Multipoint LVDS) is a new family of bus interface devices based on LVDS technology specifically designed for multipoint and multidrop cable and backplane applications. It differs from standard LVDS in providing increased drive current to handle double terminations that are required in multipoint applications. Controlled transition times minimize reflections that are common in multipoint configurations due to unterminated stubs.

The DS91M047 accepts LVTTTL/LVCMOS input levels and translates them to M-LVDS signal levels with transition times of greater than 1 ns. The device provides the DE and  $\overline{\text{DE}}$  inputs that are ANDed together and control the TRI-STATE outputs. The DE and  $\overline{\text{DE}}$  inputs are common to all four drivers.

The DS91M047 has a flow-through pinout for easy PCB layout. The DS91M047 provides a new alternative for high speed multipoint interface applications. It is packaged in a space saving SOIC-16 package.

### TYPICAL APPLICATION



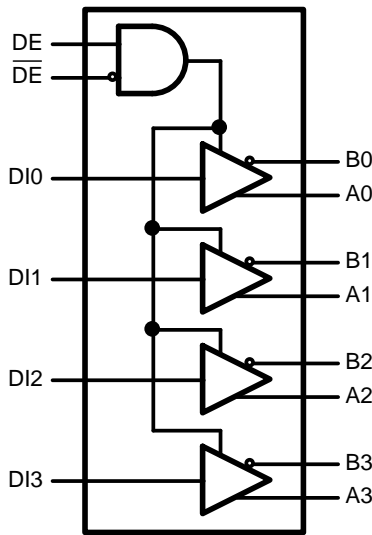
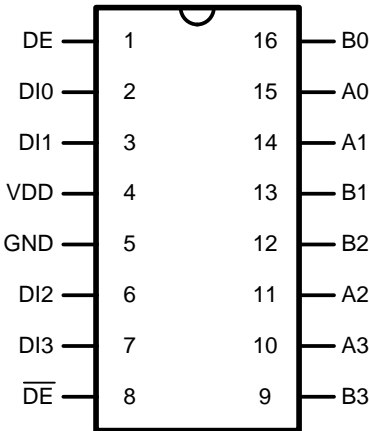
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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**Connection Diagrams**



**PIN DESCRIPTIONS**

Pin No.	Name	Description
2, 3, 6, 7	DI	Driver input pin, LVCMOS compatible.
10, 11, 14, 15	A	Non-inverting driver output pin, M-LVDS levels.
9, 12, 13, 16	B	Inverting driver output pin, M-LVDS levels.
1	DE	Driver enable pin: When DE is low, the driver is disabled. When DE is high and DE is low or open, the driver is enabled. If both DE and DE are open circuit, then the driver is disabled.
8	DE	Driver enable pin: When DE is high, the driver is disabled. When DE is low or open and DE is high, the driver is enabled. If both DE and DE are open circuit, then the driver is disabled.
4	V <sub>DD</sub>	Power supply pin, +3.3V ± 0.3V
5	GND	Ground pin

**TRUTH TABLE**

Enables		Input	Outputs	
DE	$\overline{DE}$	DI	A	B
H	L	L	L	H
		H	H	L
All other combinations of ENABLE inputs		X	Z	Z



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>

Power Supply Voltage		–0.3V to +4V
LVCMOS Input Voltage		–0.3V to ( $V_{DD} + 0.3V$ )
M-LVDS Output Voltage		–1.9V to +5.5V
M-LVDS Output Short Circuit Current Duration		Continuous
Junction Temperature		+140°C
Storage Temperature Range		–65°C to +150°C
Lead Temperature Range	Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation @ +25°C	D Package	2.21W
	Derate D Package	19.2 mW/°C above +25°C
Package Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	$\theta_{JA}$	+52°C/W
	$\theta_{JC}$	+19°C/W
ESD Susceptibility	HBM	≥8 kV
	MM	≥250V
	CDM	≥1250V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

## RECOMMENDED OPERATING CONDITIONS

	Min	Typ	Max	Units
Supply Voltage ( $V_{DD}$ )	+3.0	+3.3	+3.6	V
Voltage at Any Bus Terminal (Separate or Common-Mode)	–1.4		+3.8	V
High Level Input Voltage ( $V_{IH}$ )	2.0		$V_{DD}$	V
Low Level Input Voltage ( $V_{IL}$ )	0		0.8	V
Operating Free Air Temperature ( $T_A$ )	–40	+25	+85	°C

**DC ELECTRICAL CHARACTERISTICS**<sup>(1)(2)(3)(4)</sup>

Over supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>LVC MOS DC Specifications</b>						
$V_{IH}$	High-Level Input Voltage		2.0		$V_{DD}$	V
$V_{IL}$	Low-Level Input Voltage		GND		0.8	V
$I_{IH}$	High-Level Input Current	$V_{IH} = 3.6\text{V}$	-15	$\pm 1$	15	$\mu\text{A}$
$I_{IL}$	Low-Level Input Current	$V_{IL} = 0\text{V}$	-15	$\pm 1$	15	$\mu\text{A}$
$V_{CL}$	Input Clamp Voltage	$I_{IN} = -18\text{ mA}$	-1.5			V
<b>M-LVDS DC Specifications</b>						
$ V_{AB} $	Differential Output Voltage Magnitude	$R_L = 50\Omega$ , $C_L = 5\text{ pF}$ See <a href="#">Figure 1</a> and <a href="#">Figure 3</a>	480		650	mV
$\Delta V_{AB}$	Change in Differential Output Voltage Magnitude Between Logic States		-50		50	mV
$V_{OS(SS)}$	Steady-State Common-Mode Output Voltage	$R_L = 50\Omega$ See <a href="#">Figure 1</a> and <a href="#">Figure 2</a>	0.30	1.6	2.10	V
$ \Delta V_{OS(SS)} $	Change in Steady-State Common-Mode Output Voltage Between Logic States		0		50	mV
$V_{A(OC)}$	Maximum Steady-State Open-Circuit Output Voltage	See <a href="#">Figure 4</a>	0		2.4	V
$V_{B(OC)}$	Maximum Steady-State Open-Circuit Output Voltage		0		2.4	V
$V_{P(H)}$	Voltage Overshoot, Low-to-High Level Output <sup>(5)</sup>	$R_L = 50\Omega$ , $C_L = 5\text{ pF}$ $C_D = 0.5\text{ pF}$ , see <a href="#">Figure 6</a> and <a href="#">Figure 7</a>			$1.2V_{SS}$	V
$V_{P(L)}$	Voltage Overshoot, High-to-Low Level Output <sup>(5)</sup>		$-0.2V_{SS}$			V
$I_{OS}$	Output Short-Circuit Current <sup>(6)</sup>	See <a href="#">Figure 5</a>	-43		43	mA
$I_A$	Driver High-Impedance Output Current	$V_A = 3.8\text{V}$ , $V_B = 1.2\text{V}$	0		32	$\mu\text{A}$
		$V_A = 0\text{V}$ or $2.4\text{V}$ , $V_B = 1.2\text{V}$	-20		20	$\mu\text{A}$
		$V_A = -1.4\text{V}$ , $V_B = 1.2\text{V}$	-32		0	$\mu\text{A}$
$I_B$	Driver High-Impedance Output Current	$V_A = 3.8\text{V}$ , $V_B = 1.2\text{V}$	0		32	$\mu\text{A}$
		$V_A = 0\text{V}$ or $2.4\text{V}$ , $V_B = 1.2\text{V}$	-20		20	$\mu\text{A}$
		$V_A = -1.4\text{V}$ , $V_B = 1.2\text{V}$	-32		0	$\mu\text{A}$
$I_{AB}$	Driver High-Impedance Output Differential Current ( $I_A - I_B$ )	$V_A = V_B$ , $-1.4\text{V} \leq V \leq 3.8\text{V}$	-4		4	$\mu\text{A}$
$I_{A(OFF)}$	Driver High-Impedance Output Power-Off Current	$V_A = 3.8\text{V}$ , $V_B = 1.2\text{V}$ $DE = 0\text{V}$ $0\text{V} \leq V_{DD} \leq 1.5\text{V}$	0		32	$\mu\text{A}$
		$V_A = 0\text{V}$ or $2.4\text{V}$ , $V_B = 1.2\text{V}$ $DE = 0\text{V}$ $0\text{V} \leq V_{DD} \leq 1.5\text{V}$	-20		20	$\mu\text{A}$
		$V_A = -1.4\text{V}$ , $V_B = 1.2\text{V}$ $DE = 0\text{V}$ $0\text{V} \leq V_{DD} \leq 1.5\text{V}$	-32		0	$\mu\text{A}$
$I_{B(OFF)}$	Driver High-Impedance Output Power-Off Current	$V_A = 3.8\text{V}$ , $V_B = 1.2\text{V}$ $DE = 0\text{V}$ $0\text{V} \leq V_{DD} \leq 1.5\text{V}$	0		32	$\mu\text{A}$
		$V_A = 0\text{V}$ or $2.4\text{V}$ , $V_B = 1.2\text{V}$ $DE = 0\text{V}$ $0\text{V} \leq V_{DD} \leq 1.5\text{V}$	-20		20	$\mu\text{A}$
		$V_A = -1.4\text{V}$ , $V_B = 1.2\text{V}$ $DE = 0\text{V}$ $0\text{V} \leq V_{DD} \leq 1.5\text{V}$	-32		0	$\mu\text{A}$

- (1) The [Electrical Characteristics](#) tables list ensured specifications under the listed [Recommended Operating Conditions](#) except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except  $V_{OD}$  and  $\Delta V_{OD}$ .
- (3) Typical values represent most likely parametric norms for  $V_{DD} = +3.3\text{V}$  and  $T_A = +25^\circ\text{C}$ , and at the [Recommended Operating Conditions](#) at the time of product characterization and are not ensured.
- (4)  $C_L$  includes fixture capacitance and  $C_D$  includes probe capacitance.
- (5) Specification is specified by characterization and is not tested in production.
- (6) Output short circuit current ( $I_{OS}$ ) is specified as magnitude only, minus sign indicates direction only.

## DC ELECTRICAL CHARACTERISTICS<sup>(1)(2)(3)(4)</sup> (continued)

Over supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{AB(OFF)}$	Driver High-Impedance Output Power-Off Current ( $I_{A(OFF)} - I_{B(OFF)}$ )	$V_A = V_B$ , $-1.4V \leq V \leq 3.8V$ $DE = 0V$ $0V \leq V_{DD} \leq 1.5V$	-4		4	$\mu A$
$C_A$	Driver Output Capacitance	$V_{DD} = 0V$		7.8		pF
$C_B$	Driver Output Capacitance			7.8		pF
$C_{AB}$	Driver Output Differential Capacitance			3		pF
$C_{A/B}$	Driver Output Capacitance Balance ( $C_A/C_B$ )			1		
$I_{CC}$	Power Supply Current	$R_L = 50\Omega$ (All Outputs) $DI = V_{DD}$ or GND (All Inputs) $DE = V_{DD}$ , $\overline{DE} = GND$ $f = 125\text{ MHz}$		65	75	mA
$I_{CCZ}$	TRI-STATE Power Supply Current	$R_L = 50\Omega$ (All Outputs) $DI = V_{DD}$ or GND (All Inputs) $DE = GND$ , $\overline{DE} = V_{DD}$		19	24	mA

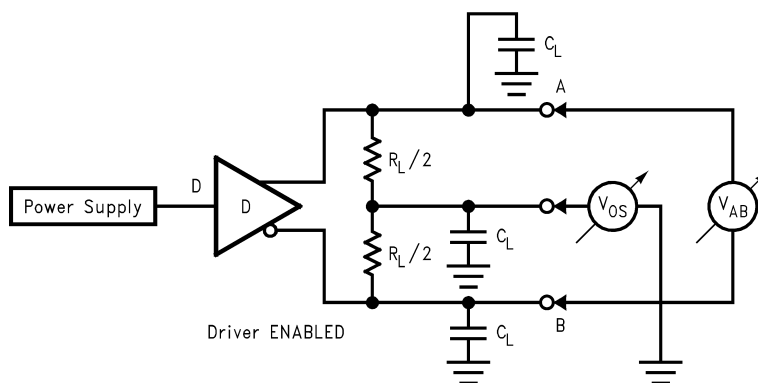
## SWITCHING CHARACTERISTICS<sup>(1)(2)(3)</sup>

Over supply voltage and operating temperature ranges, unless otherwise specified.

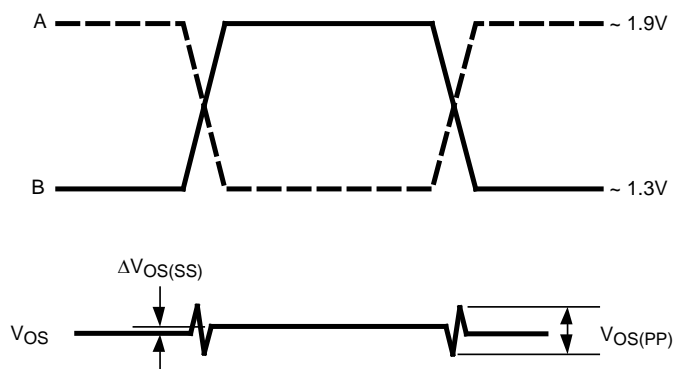
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PHL}$	Differential Propagation Delay High to Low	$R_L = 50\Omega$ $C_L = 5\text{ pF}$ , $C_D = 0.5\text{ pF}$ See <a href="#">Figure 6</a> and <a href="#">Figure 7</a>	1.5	3.1	5.0	ns
$t_{PLH}$	Differential Propagation Delay Low to High		1.5	3.1	5.0	ns
$t_{SKD1}$	Differential Pulse Skew $ t_{PHL} - t_{PLH} ^{(4)(5)}$		0	70	140	ps
$t_{SKD2}$	Channel-to-Channel Skew <sup>(4)(6)</sup>		0	70	200	ps
$t_{SKD3}$	Differential Part-to-Part Skew <sup>(4)(7)</sup> (Constant $T_A$ and $V_{DD}$ )		0	0.8	1.5	ns
$t_{SKD4}$	Differential Part-to-Part Skew <sup>(8)</sup>		0		3.5	ns
$t_{TLH}$	Rise Time <sup>(4)</sup>		1.1	2.0	3.0	ns
$t_{THL}$	Fall Time <sup>(4)</sup>		1.1	2.0	3.0	ns
$t_{PHZ}$	Disable Time High to Z	$R_L = 50\Omega$ $C_L = 5\text{ pF}$ , $C_D = 0.5\text{ pF}$ See <a href="#">Figure 8</a> and <a href="#">Figure 9</a>		7	12.5	ns
$t_{PLZ}$	Disable Time Low to Z			7	12.5	ns
$t_{PZH}$	Enable Time Z to High			7	12.5	ns
$t_{PZL}$	Enable Time Z to Low			7	12.5	ns
$f_{MAX}$	Maximum Operating Frequency	See <sup>(4)</sup>	125			MHz

- (1) The [Electrical Characteristics](#) list ensured specifications under the listed [Recommended Operating Conditions](#) except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Typical values represent most likely parametric norms for  $V_{DD} = +3.3V$  and  $T_A = +25^\circ C$ , and at the [Recommended Operating Conditions](#) at the time of product characterization and are not ensured.
- (3)  $C_L$  includes fixture capacitance and  $C_D$  includes probe capacitance.
- (4) Specification is specified by characterization and is not tested in production.
- (5)  $t_{SKD1}$ ,  $|t_{PLHD} - t_{PHLD}|$ , Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
- (6)  $t_{SKD2}$ , Channel-to-Channel Skew, is the difference in propagation delay ( $t_{PLHD}$  or  $t_{PHLD}$ ) among all output channels.
- (7)  $t_{SKD3}$ , Part-to-Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same  $V_{DD}$  and within  $5^\circ C$  of each other within the operating temperature range.
- (8)  $t_{SKD4}$ , Part-to-Part Skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution.  $t_{SKD4}$  is defined as  $|Max - Min|$  differential propagation delay.

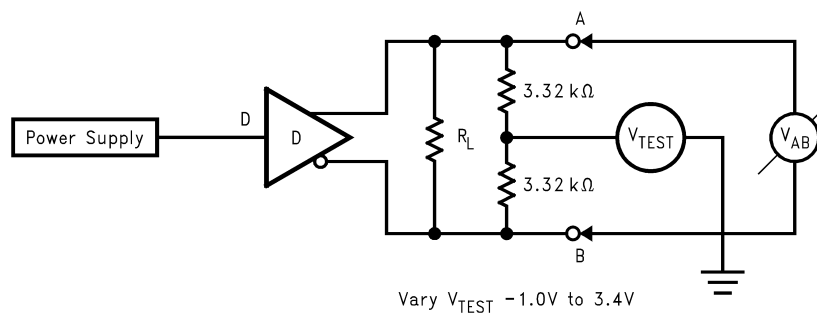
## PARAMETER MEASUREMENT INFORMATION



**Figure 1. Differential Driver Test Circuit**

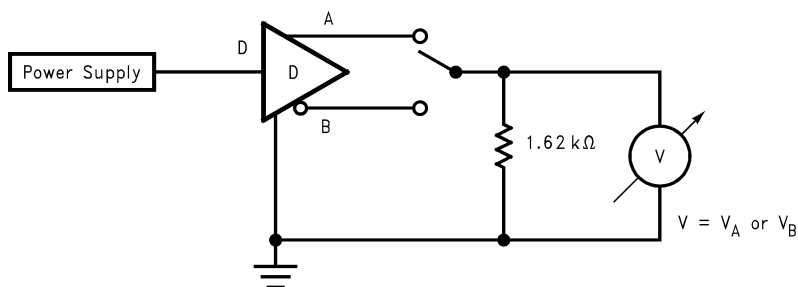


**Figure 2. Differential Driver Waveforms**

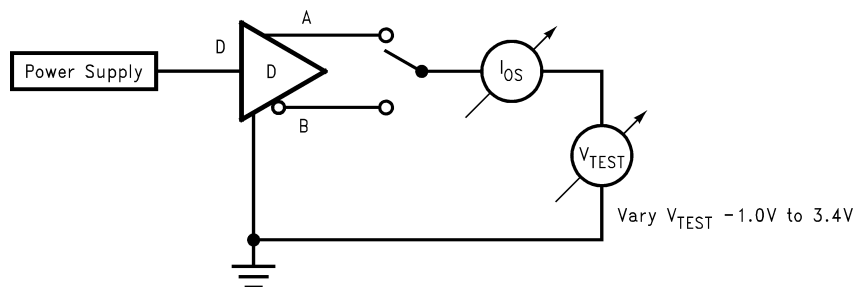


**Figure 3. Differential Driver Full Load Test Circuit**

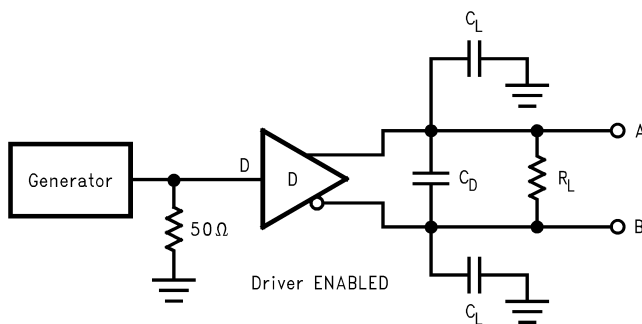
## PARAMETER MEASUREMENT INFORMATION (continued)



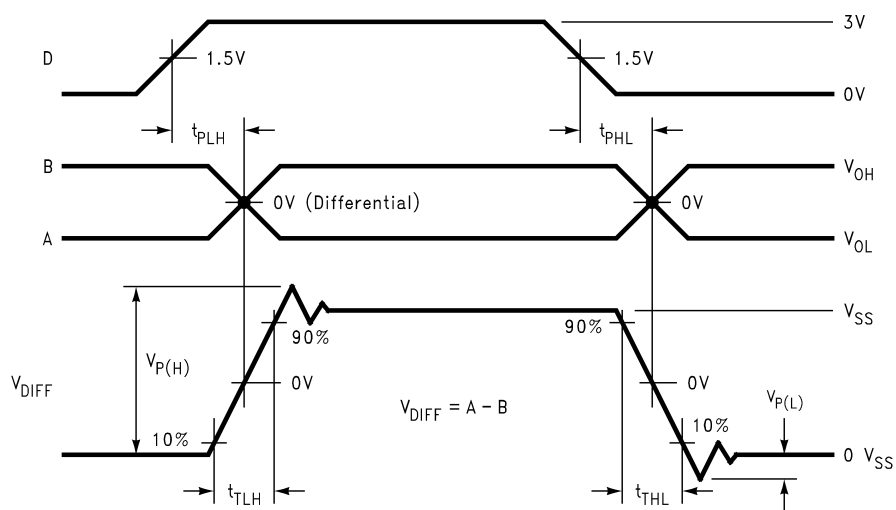
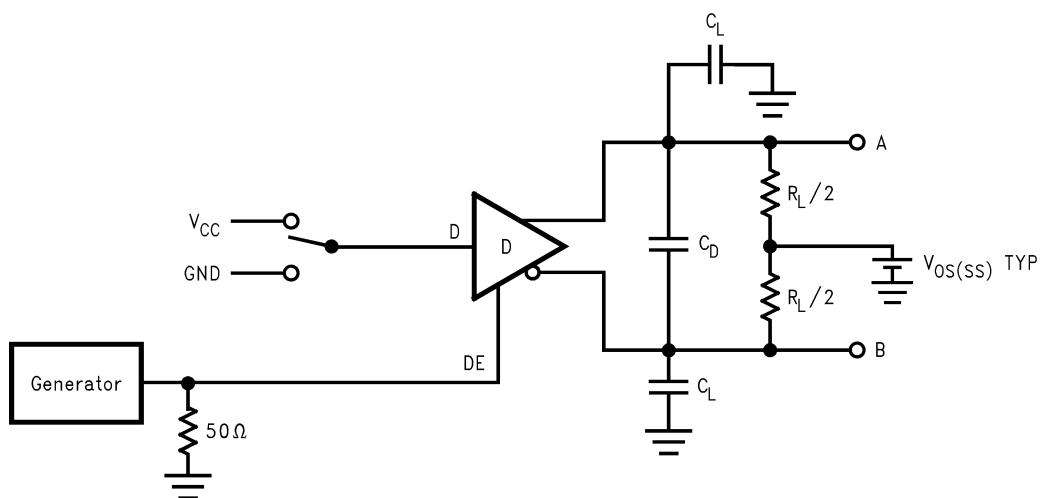
**Figure 4. Differential Driver DC Open Test Circuit**



**Figure 5. Differential Driver Short-Circuit Test Circuit**

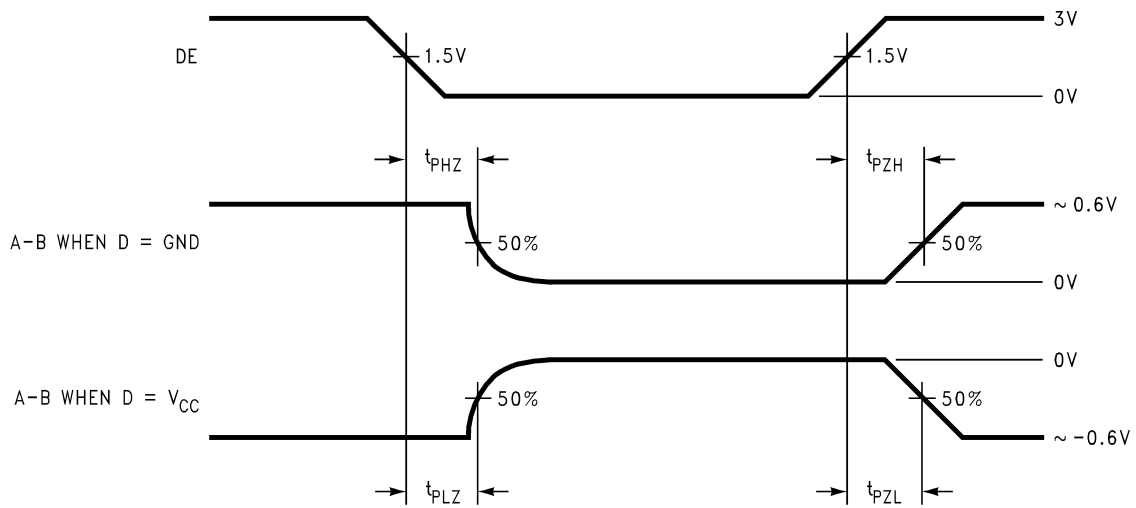


**Figure 6. Driver Propagation Delay and Transition Time Test Circuit**

**PARAMETER MEASUREMENT INFORMATION (continued)****Figure 7. Driver Propagation Delay and Transition Time Waveforms****Figure 8. Driver TRI-STATE Delay Test Circuit**



## PARAMETER MEASUREMENT INFORMATION (continued)



**Figure 9. Driver TRI-STATE Delay Waveforms**

## TYPICAL PERFORMANCE CHARACTERISTICS

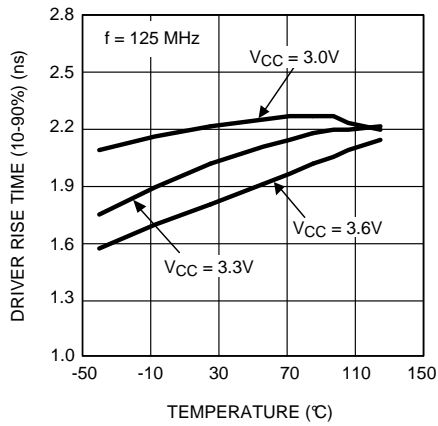


Figure 10. Driver Rise Time as a Function of Temperature

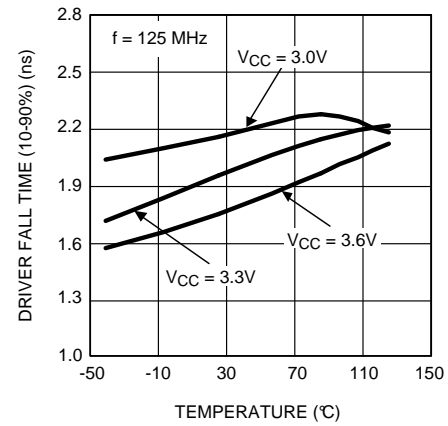


Figure 11. Driver Fall Time as a Function of Temperature

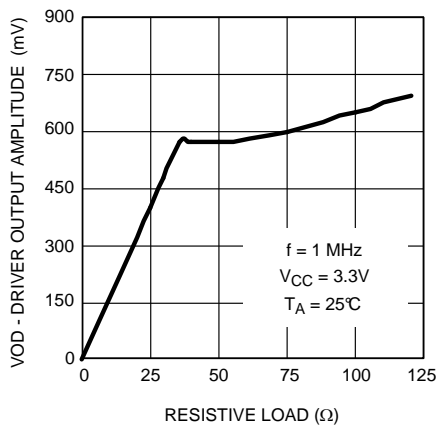


Figure 12. Driver Output Signal Amplitude as a Function of Resistive Load

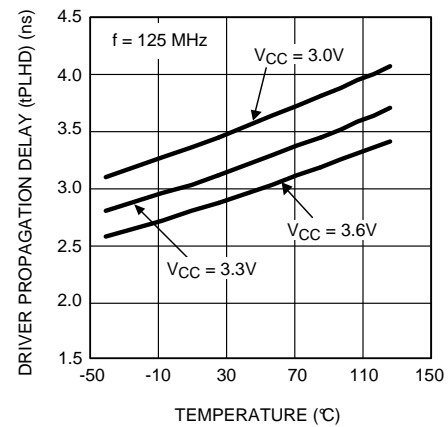


Figure 13. Driver Propagation Delay (tPLHD) as a Function of Temperature

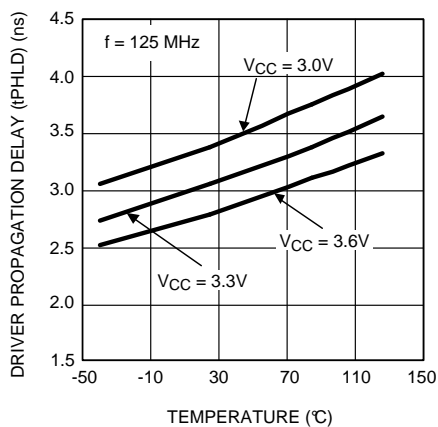


Figure 14. Driver Propagation Delay (tPLHD) as a Function of Temperature

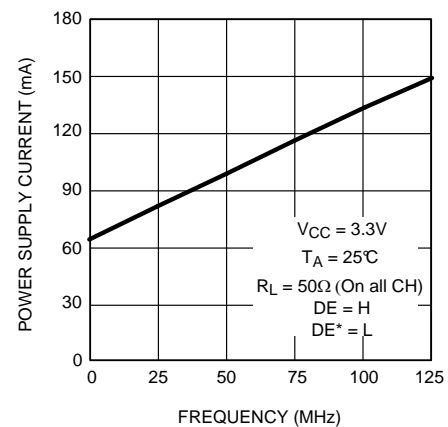


Figure 15. Driver Power Supply Current as a Function of Frequency

## REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">10</a>

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS91M047TMA/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS91M047 TMA	<a href="#">Samples</a>
DS91M047TMAX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS91M047 TMA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS91M047TMAX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS91M047TMAX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

## IMPORTANT NOTICE

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