

DLPS025B-AUGUST 2012-REVISED JULY 2013

# DLP<sup>®</sup> 0.95 1080p 2 x LVDS Type A DMD

Check for Samples: DLP9500

# **FEATURES**

- 0.95-Inch Micromirror Array Diagonal
  - 1920 × 1080 Array of Aluminum. **Micrometer-Sized Mirrors** (1080p Resolution)
  - 10.8-µm Micromirror Pitch
  - ±12° Micromirror Tilt Angle (Relative to Flat State)
  - Designed for Corner Illumination
- **Designed for Use With Broadband Visible** ٠ Light (400 nm-700 nm):
  - Window Transmission 97% (Single Pass, Through Two Window Surfaces)
  - Micromirror Reflectivity 88%
  - Array Diffraction Efficiency 86%
  - Array Fill Factor 92%
- Four 16-Bit, Low Voltage Differential Signaling (LVDS) Double Data Rate (DDR) input data buses
- Up to 400 MHz Input Data Clock Rate
- 42.2-mm by 42.2-mm by 7-mm Package Footprint
- **Hermetic Package**

# APPLICATIONS

- Industrial: •
  - **Direct Imaging Lithography** -
  - Laser Marking and Repair Systems
  - **Computer-to-Plate Printers**
  - **Rapid Prototyping Machines and 3D** Printers
  - **3D Scanners for Machine Vision and Quality Control**
- Medical:
  - Phototherapy Devices
  - Ophthalmology -
  - Vascular Imaging
  - Hyperspectral Imaging
  - 3D Scanners for Limb and Skin measurement
  - Confocal Microscopes
- Display: •
  - **3D Imaging Microscopes** \_
  - Intelligent and Adaptive Lighting
  - Augmented Reality and Information Overlay





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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

# DESCRIPTION

The 0.95 1080p Chipset is part of the DLP Discovery 4100 platform, which enables high resolution and high performance spatial light modulation. The DLP9500 is the digital micromirror device (DMD) at the heart of the 0.95 1080p chipset, and currently offers the highest resolution in the DLP catalog portfolio. The DLP Discovery 4100 platform also provides the highest level of individual micromirror control with the option for random row addressing. Combined with a hermetic package, the unique capability and value offered by DLP9500 makes it well suited to support a wide variety of industrial, medical, and advanced display applications.

The DLP9500 is the 0.95 1080p DMD, with a hermetic package, that is sold along with the following dedicated chipset (see Figure 1):

- 1 unit DLPC410 (DLP Discovery 4100 Digital Controller)
- 1 unit DLPR410 / DLPR4101 (DLP Discovery 4100 Configuration PROM)
- 2 units DLPA200 (DMD Micromirror Driver)

Reliable function and operation of the DLP9500 requires that it be used in conjunction with the other components of the chipset (see Figure 1). A dedicated chipset provides developers easier access to the DMD as well as high speed, independent micromirror control.

DLP9500 is a digitally controlled MOEMS (micro-opto-electromechanical system) spatial light modulator (SLM). When coupled to an appropriate optical system, the DLP9500 can be used to modulate the amplitude, direction, and/or phase of incoming light.

Electrically, the DLP9500 consists of a two-dimensional array of 1-bit CMOS memory cells, organized in a grid of 1920 memory cell columns by 1080 memory cell rows. The CMOS memory array is addressed on row-by-row basis, over four 16-bit Low Voltage Differential Signaling (LVDS) double data rate (DDR) buses. Addressing is handled via a serial control bus. The specific CMOS memory access protocol is handled by the DLPC410 digital controller.



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Figure 1. DLP410 and DLP9500 Functional Block Diagram

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Figure 2. DLP410 and DLP9500 Embedded Example Block Diagram

Optically, the DLP9500 consists of 2,073,600 highly reflective, digitally switchable, micrometer-sized mirrors ("micromirrors"), organized in a two-dimensional array of 1920 micromirror columns by 1080 micromirror rows (Figure 3). Each aluminum micromirror is approximately 10.8 microns in size (see the "Micromirror Pitch" in Figure 3), and is switchable between two discrete angular positions: -12° and +12°. The angular positions are measured relative to a 0° "flat state", which is parallel to the array plane (see Figure 4). The tilt direction is perpendicular to the hinge-axis which is positioned diagonally relative to the overall array. The "On State" landed position is directed towards "Row 0, Column 0" (upper left) corner of the device package (see the "Micromirror Hinge-Axis Orientation" in Figure 3). In the field of visual displays, the 1920 by 1080 "pixel" resolution is referred to as "1080p".

Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the mirror "clocking pulse" is applied. The angular position  $(-12^{\circ} \text{ or } +12^{\circ})$  of the individual micromirrors changes synchronously with a micromirror "clocking pulse", rather than being synchronous with the CMOS memory cell data update. Therefore, writing a logic 1 into a memory cell followed by a mirror "clocking pulse" will result in the corresponding micromirror switching to a  $+12^{\circ}$  position. Writing a logic 0 into a memory cell followed by a mirror "clocking pulse" will result in the corresponding micromirror switching to a  $-12^{\circ}$  position.

Updating the angular position of the micromirror array consists of two steps. First, updating the contents of the CMOS memory. Second, application of a Micromirror Clocking Pulse to all or a portion of the micromirror array (depending upon the configuration of the system). Micromirror Clocking Pulses are generated externally by two DLPA200s, with application of the pulses being coordinated by the DLPC410 controller.

Around the perimeter of the 1920 by 1080 array of micromirrors is a uniform band of "border" micromirrors. The border micromirrors are not user-addressable. The border micromirrors land in the  $-12^{\circ}$  position once power has been applied to the device. There are 10 border micromirrors on each side of the 1920 by 1080 active array.

Figure 2 shows a typical system application using the DLP Discovery 4100 chipset. The DLPC410 and DLPA200 control and coordinate the data loading and micromirror switching for reliable DLP9500 operation. The DLPR410 is the programmed PROM required to properly configure the DLPC410 controller. For more information on the chipset components, see DLP Discovery 4100 chipset data sheet.







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#### **Related Documents**

The following documents contain additional information related to the use of the DLP9500 device:

	Document	TI Literature Number
DLP® Discovery™ 4100 Chipset Datasheet		DLPU008
DLPC410 Digital Controller data sheet		DLPS024
DLPA200 DMD Micromirror Driver data sheet		DLPS015
DLPR410 / DLPR4101 EEPROM data sheet		DLPS027

#### **Table 1. Related Documentation**

## **Device Part Number Nomenclature**

Figure 5 provides a legend of reading the complete device name for any DLP device. DLP9500FLN is functionally equivalent to 1910N9145



Figure 5. Device Nomenclature

## **Device Marking**

The device marking consists of the fields shown in Figure 6.





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## **Device Terminals**

This section describes the input and output characteristics of signals that interface to the DLP9500, organized by functional groups. Table 2 includes I/O, Type, Internal Termination, Clock Domain, and Data Rate characteristics which are further described in subsequent sections.



Figure 7. Type A Package Pins (Device Bottom View)



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Table 2. Pin Characteristics										
PIN NAME	PIN See	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	Internal Trace Length (mils)	DATA RATE	DESCRIPTION		
Data Inputs				r				· · · · · · · · · · · · · · · · · · ·		
D_AN(0)	F2	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	512.01	DDR	_		
D_AN(1)	H8	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	158.79	DDR	_		
D_AN(2)	E5	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	471.24	DDR			
D_AN(3)	G9	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	159.33	DDR			
D_AN(4)	D2	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	585.41	DDR	_		
D_AN(5)	G3	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	551.17	DDR			
D_AN(6)	E11	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	229.41	DDR	_		
D_AN(7)	F8	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	300.54	DDR	_		
D_AN(8)	C9	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	346.35	DDR			
D_AN(9)	H2	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	782.27	DDR			
D_AN(10)	B10	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	451.52	DDR			
D_AN(11)	G15	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	74.39	DDR			
D_AN(12)	D14	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	194.26	DDR			
D_AN(13)	F14	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	148.29	DDR			
D_AN(14)	C17	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	244.9	DDR	Input data bus A (LVDS)		
D_AN(15)	H16	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	73.39	DDR			
D_AP(0)	F4	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	509.63	DDR			
D_AP(1)	H10	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	152.59	DDR			
D_AP(2)	E3	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	464.09	DDR	_		
D_AP(3)	G11	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	152.39	DDR	_		
D_AP(4)	D4	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	591.39	DDR			
D_AP(5)	G5	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	532.16	DDR	_		
D_AP(6)	E9	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	230.78	DDR	_		
D_AP(7)	F10	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	300.61	DDR			
D_AP(8)	C11	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	338.16	DDR			
D_AP(9)	H4	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	773.17	DDR			
D_AP(10)	B8	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	449.57	DDR			
D_AP(11)	H14	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	71.7	DDR			
D_AP(12)	D16	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	198.69	DDR			



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PIN NAME	PIN See	I/O/P	ТҮРЕ	INTERNAL TERMINATION	CLOCKED BY	Internal Trace Length (mils)	DATA RATE	DESCRIPTION
D_AP(13)	F16	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	143.72	DDR	
D_AP(14)	C15	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	240.14	DDR	Input data bus A (LVDS)
D_AP(15)	G17	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	74.05	DDR	
D_BN(0)	AH2	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	525.25	DDR	
D_BN(1)	AD8	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	190.59	DDR	
D_BN(2)	AJ5	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	525.25	DDR	
D_BN(3)	AE3	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	494.91	DDR	
D_BN(4)	AG9	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	222.67	DDR	
D_BN(5)	AE11	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	205.45	DDR	
D_BN(6)	AH10	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	309.05	DDR	
D_BN(7)	AF10	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	285.62	DDR	
D_BN(8)	AK8	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	483.58	DDR	
D_BN(9)	AG5	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	711.58	DDR	
D_BN(10)	AL11	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	462.21	DDR	
D_BN(11)	AE15	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	74.39	DDR	
D_BN(12)	AH14	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	194.26	DDR	Input data bus B (LVDS)
D_BN(13)	AF14	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	156	DDR	
D_BN(14)	AJ17	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	247.9	DDR	
D_BN(15)	AD16	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	111.52	DDR	
D_BP(0)	AH4	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	525.02	DDR	
D_BP(1)	AD10	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	190.61	DDR	
D_BP(2)	AJ3	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	524.22	DDR	
D_BP(3)	AE5	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	476.07	DDR	
D_BP(4)	AG11	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	222.8	DDR	
D_BP(5)	AE9	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	219.48	DDR	
D_BP(6)	AH8	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	306.55	DDR	
D_BP(7)	AF8	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	298.04	DDR	
D_BP(8)	AK10	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	480.31	DDR	



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Table 2	Pin	Characteristics	(continued)
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PIN NAME	PIN See	I/O/P	ТҮРЕ	INTERNAL TERMINATION	CLOCKED BY	Internal Trace Length (mils)	DATA RATE	DESCRIPTION
D_BP(9)	AG3	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	727.18	DDR	
D_BP(10)	AL9	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	461.02	DDR	
D_BP(11)	AD14	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	71.35	DDR	
D_BP(12)	AH16	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	197.69	DDR	Input data bus B (LVDS)
D_BP(13)	AF16	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	150.38	DDR	
D_BP(14)	AJ15	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	243.14	DDR	
D_BP(15)	AE17	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	113.36	DDR	
D_CN(0)	B14	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	459.04	DDR	
D_CN(1)	E15	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	342.79	DDR	
D_CN(2)	A17	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	456.22	DDR	
D_CN(3)	G21	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	68.24	DDR	
D_CN(4)	B20	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	362.61	DDR	
D_CN(5)	F20	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	163.07	DDR	
D_CN(6)	D22	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	204.16	DDR	
D_CN(7)	G23	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	105.59	DDR	
D_CN(8)	B26	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	450.51	DDR	
D_CN(9)	F28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	302.04	DDR	
D_CN(10)	C29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	429.8	DDR	Input data bus C
D_CN(11)	G27	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	317.1	DDR	(LVDS)
D_CN(12)	D26	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	276.76	DDR	
D_CN(13)	H28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	186.78	DDR	
D_CN(14)	E29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	311.3	DDR	
D_CN(15)	J29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	262.62	DDR	
D_CP(0)	B16	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	463.64	DDR	
D_CP(1)	E17	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	347.65	DDR	
D_CP(2)	A15	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	456.45	DDR	
D_CP(3)	H20	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	67.72	DDR	
D_CP(4)	B22	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	362.76	DDR	
D_CP(5)	F22	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	161.69	DDR	



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PIN NAME	PIN See	I/O/P	ТҮРЕ	INTERNAL TERMINATION	CLOCKED BY	, Internal Trace Length (mils)	DATA RATE	DESCRIPTION
D_CP(6)	D20	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	195.09	DDR	
D_CP(7)	H22	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	104.86	DDR	
D_CP(8)	B28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	451.41	DDR	
D_CP(9)	F26	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	294.22	DDR	
D_CP(10)	C27	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	429.68	DDR	Input data bus C
D_CP(11)	G29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	314.98	DDR	(LVDS)
D_CP(12)	D28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	276.04	DDR	
D_CP(13)	H26	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	186.25	DDR	
D_CP(14)	E27	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	312.07	DDR	-
D_CP(15)	J27	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	262.94	DDR	
D_DN(0)	AK14	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	492.53	DDR	
D_DN(1)	AG15	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	342.78	DDR	
D_DN(2)	AL17	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	491.83	DDR	
D_DN(3)	AE21	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	74.24	DDR	
D_DN(4)	AK20	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	356.23	DDR	
D_DN(5)	AF20	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	163.07	DDR	Input data bus D
D_DN(6)	AH22	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	204.16	DDR	(LVDS)
D_DN(7)	AE23	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	105.59	DDR	
D_DN(8)	AK26	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	450.51	DDR	
D_DN(9)	AF28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	302.04	DDR	
D_DN(10)	AJ29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	429.8	DDR	
D_DN(11)	AE27	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	298.87	DDR	

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PIN NAME	PIN See	I/O/P	ТҮРЕ	INTERNAL TERMINATION	CLOCKED BY	Internal Trace Length (mils)	DATA RATE	DESCRIPTION
D_DN(12)	AH26	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	276.76	DDR	
D_DN(13)	AD28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	186.78	DDR	
D_DN(14)	AG29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	311.3	DDR	
D_DN(15)	AC29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	262.62	DDR	
D_DP(0)	AK16	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	495.13	DDR	
D_DP(1)	AG17	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	342.47	DDR	
D_DP(2)	AL15	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	492.06	DDR	
D_DP(3)	AD20	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	67.72	DDR	
D_DP(4)	AK22	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	356.37	DDR	Input data bus D
D_DP(5)	AF22	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	161.98	DDR	
D_DP(6)	AH20	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	195.09	DDR	(LVDS)
D_DP(7)	AD22	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	102.86	DDR	
D_DP(8)	AK28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	451.41	DDR	
D_DP(9)	AF26	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	296.7	DDR	
D_DP(10)	AJ27	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	429.68	DDR	
D_DP(11)	AE29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	302.74	DDR	
D_DP(12)	AH28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	276.04	DDR	
D_DP(13)	AD26	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	186.25	DDR	
D_DP(14)	AG27	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	312.07	DDR	
D_DP(15)	AC27	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	262.94	DDR	

Product Folder Links: DLP9500





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PIN NAME	PIN See	I/O/P	ТҮРЕ	INTERNAL TERMINATION	CLOCKED BY	Internal Trace Length (mils)	DATA RATE	DESCRIPTION		
DCLK_AN	D10	Input	LVCMOS	Differential Terminated - 100 Ω	_	325.8	-	Input data bus A		
DCLK_AP	D8	Input	LVCMOS	Differential Terminated - 100 Ω	-	319.9	-	Clock (LVDS)		
DCLK_BN	AJ11	Input	LVCMOS	Differential Terminated - 100 Ω	-	318.92	-	Input data bus B Clock (LVDS)		
DCLK_BP	AJ9	Input	LVCMOS	Differential Terminated - 100 Ω	-	318.74	-			
DCLK_CN	C23	Input	LVCMOS	Differential Terminated - 100 Ω	-	252.01	-	Input data bus C		
DCLK_CP	C21	Input	LVCMOS	Differential Terminated - 100 Ω	_	241.18	-	Clock (LVDS)		
DCLK_DN	AJ23	Input	LVCMOS	Differential Terminated - 100 Ω	-	252.01	-	Input data bus D		
DCLK_DP	AJ21	Input	LVCMOS	Differential Terminated - 100 Ω	-	241.18	-	Clock (LVDS)		
Data Control Inputs										
SCTRL_AN	J3	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	608.14	DDR	Serial control for data bus A (LVDS)		
SCTRL_AP	J5	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	607.45	DDR			
SCTRL_BN	AF4	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	698.12	DDR	Serial control for		
SCTRL_BP	AF2	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	703.8	DDR	data bus B (LVDS)		
SCTRL_CN	E23	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	232.46	DDR	Serial control for		
SCTRL_CP	E21	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_C	235.21	DDR	data bus C (LVDS)		
SCTRL_DN	AG23	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_D	235.53	DDR	Serial control for		
SCTRL_DP	AG21	Input	LVCMOS	Differential Terminated - 100 $\Omega$	DCLK_D	235.66	DDR	data bus D (LVDS)		
Serial Communication	on and Configuration	n								
SCPCLK	AE1	Input	LVCMOS	pull-down	-	324.26	-	Serial port clock		
SCPDO	AC3	Output	LVCMOS	-	SCP_CLK	281.38	-	Serial port output		
SCPDI	AD2	Input	LVCMOS	pull-down	SCP_CLK	261.55	-	Serial port input		
SCPENZ	AD4	Input	LVCMOS	pull-down	SCP_CLK	184.86	-	Serial port enable		
PWRDNZ	B4	Input	LVCMOS	pull-down	-	458.78	-	Device reset		
MODE_A	J1	Input	LVCMOS	pull-down	-	471.57	-	Data bandwidth		
MODE_B	G1	Input	LVCMOS	pull-down	-	521.99	-	mode select		



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PIN NAME	PIN See	I/O/P	ТҮРЕ	INTERNAL TERMINATION	CLOCKED BY	Internal Trace Length (mils)	DATA RATE	DESCRIPTION
Micromirror Bias Res	set			I				
MBRST(0)	L5	Input	Analog	-	-	898.97	-	
MBRST(1)	M28	Input	Analog	-	-	621.98	-	
MBRST(2)	P4	Input	Analog	-	-	846.88	-	
MBRST(3)	P30	Input	Analog	-	-	784.18	-	
MBRST(4)	L3	Input	Analog	-	-	763.34	-	
MBRST(5)	P28	Input	Analog	-	-	749.61	-	
MBRST(6)	P2	Input	Analog	-	-	878.25	-	
MBRST(7)	T28	Input	Analog	-	-	783.83	-	
MBRST(8)	M4	Input	Analog	-	-	969.36	-	
MBRST(9)	L29	Input	Analog	-	-	621.24	-	
MBRST(10)	T4	Input	Analog	-	-	918.43	-	
MBRST(11)	N29	Input	Analog	-	-	685.14	-	
MBRST(12)	N3	Input	Analog	-	-	812.31	-	Micromirror Bias
MBRST(13)	L27	Input	Analog	-	_	591.89	_	Reset "MBRST"
MBRST(14)	R3	Input	Analog	-	_	878.5	_	signals "clock"
MBRST(15)	V28	Input	Analog	-	-	660.15	_	state of LVCMOS
MBRST(16)	V4	Input	Analog	-	_	848.64	_	memory cell associated with each
MBRST(17)	R29	Input	Analog	-	-	796.31	_	mirror.
MBRST(18)	Y4	Input	Analog	-	_	715	_	
MBRST(19)	AA27	Input	Analog	-	_	604.35	_	
MBRST(20)	W3	Input	Analog	-	-	832.39	-	
MBRST(21)	W27	Input	Analog	-	_	675.21	_	
MBRST(22)	AA3	Input	Analog	-	-	861.18	_	-
MBRST(23)	W29	Input	Analog	-	-	662.66	-	
MBRST(24)	U5	Input	Analog	-	-	850.06	-	-
MBRST(25)	U29	Input	Analog	-	-	726.56	-	
MBRST(26)	Y2	Input	Analog	-	-	861.48	-	
MBRST(27)	AA29	Input	Analog	-	-	683.83	-	-
MBRST(28)	U3	Input	Analog	-	_	878.5	_	-
MBRST(29)	Y30	Input	Analog	-	_	789.2	_	-
Power		-	_			1		
VCC	A3,A5,A7,A9,A11 ,A13,A21,A23,A2 5,A27,A29,B2,C1, C31,E31,G31,J31 ,K2,L31,N31,R31, U31,W31,AA31,A C1,AC31,AE31,A G1,AG31,AJ31,A K2,AK30,AL3,AL 5,AL7,AL19,AL21 ,AL23,AL25,AL27	Power	Analog	-	-	-	-	Power for LVCMOS Logic
VCC1	H6,H12,H18,H24, M6,M26,P6,P26, T6,T26,V6,V26,Y 6,Y26,AD6,AD12, AD18,AD24	Power	Analog	-	-	-	-	Power supply for LVDS Interface
VCC2	L1,N1,R1,U1,W1, AA1	Power	Analog	-	-	-	-	Power for High Voltage CMOS Logic



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PIN NAME	PIN See	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	Internal Trace Length (mils)	DATA RATE	DESCRIPTION
VSS	A1,B12,B18,B24, B30,C7,C13,C19, C25,D6,D12,D18, D24,D30,E1,E7,E 13,E19,E25,F6,F 12,F18,F24,F30, G7,G13,G19,G25, K4,K6,K26,K28, K30,M2,M30,N5, N27,R5,T2,T30,U 27,V2,V30,W5,Y2 8,AB2,AB4,AB6,A B26,AB28,AB30, AD30,AE7,AE13, AE19,AE25,AF6, AF12,AF18,AF24, AF30,AG7,AG13, AG19,AG25,AH6, AH12,AH18,AH2 4,AH30,AJ1,AJ7, AJ13,AJ19,AJ25, AK6,AK12,AK18, AL29	Power	Analog	_	_	_	_	Common return for all power inputs
<b>Reserved Signals (N</b>	ot for use in syster	n)						-
RESERVED_FC	J7	Input	LVCMOS	pull-down	-	-	-	
RESERVED_FD	J9	Input	LVCMOS	pull-down	-	-	-	
RESERVED_PFE	J11	Input	LVCMOS	pull-down	-	-	-	Pins should be connected to VSS
RESERVED_STM	AC7	Input	LVCMOS	pull-down	-	-	-	
RESERVED_AE	C3	Input	LVCMOS	pull-down	-	-	-	
NO_CONNECT	A19,B6,C5,H30,J 13,J15,J17,J19,J 21,J23,J25,R27,A A5,AC11,AC13,A C15,AC17,AC19, AC21,AC23,AC2 5,AC5,AC9,AK24, AK4,AL13	_	-	-	-	-	-	No connection (any connection to these terminals may result in undesirable effects)



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## **ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. The Absolute Maximum Ratings are stress ratings only, and functional performance of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

	PARAMETER	CONDITIONS	MIN	NOM MAX	UNIT
Electrica	ıl				
V <sub>CC</sub>	Voltage applied to V <sub>CC</sub> <sup>(1)(2)</sup>		-0.5	4	V
V <sub>CCI</sub>	Voltage applied to V <sub>CCI</sub> <sup>(1)(2)</sup>		-0.5	4	V
	Delta supply voltage $ V_{CC} - V_{CCI} ^{(3)}$			0.3	V
V <sub>ID</sub>	Maximum differential voltage, Damage can occur to internal termination resistor if exceeded, See Figure 11			700	mV
V <sub>CC2</sub>	Voltage applied to V <sub>VCC2</sub> <sup>(1)(2)(3)</sup>		-0.5	9	V
V <sub>MBRST</sub>	Clocking Pulse Waveforwm Voltage applied to MBRST[29:0] Input Pins (supplied by DLPA200s)		-28	28	V
	Voltage applied to all other input terminals <sup>(1)</sup>		-0.5	V <sub>CC</sub> + 0.3	V
	Current required from a high-level output	V <sub>OH</sub> = 2.4 V		-20	mA
	Current required from a low-level output	V <sub>OL</sub> = 0.4 V		15	mA
Environr	nental				
	Storage temperature range		-40	80	°C
	Storage humidity	Non-Condensing	0	95	% RH
	Electrostatic discharge immunity for LVCMOS pins <sup>(4)</sup>			2000	V
	Electrostatic discharge immunity for MBRST[29:0] pins			250	v

(1) All voltages referenced to V<sub>SS</sub> (ground).

(2)

Voltages  $V_{CC}$ ,  $V_{CCI}$ , and  $V_{CC2}$  are required for proper DMD operation. Exceeding the recommended allowable absolute voltage difference between  $V_{CC}$  and  $V_{CCI}$  may result in excess current draw. The (3) difference between  $V_{CC}$  and  $V_{CCI}$ ,  $|V_{CC} - V_{CCI}|$ , should be less than 0.3 V. Tested in accordance with JESD22-A114-B Electrostatic Discharge (ESD) sensitivity testing Human Body Model (HBM).

(4)



## **RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

(		0			•		1
	PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Electric	al						
V <sub>CC</sub>	LVCMOS interface supply voltage <sup>(1)(2</sup>		3.0	3.3	3.6	V	
V <sub>CCI</sub>	LVCMOS logic supply voltage <sup>(1)(2)</sup>			3.0	3.3	3.6	V
V <sub>CC2</sub>	Mirror electrode and HVCMOS supply	v voltage (1)(2)		8.25	8.5	8.75	V
V <sub>MBRST</sub>	Clocking Pulse Waveform Voltage ap Pins (supplied by DLPA200s)	plied to MBRST[29:0] Input		-27		26.5	V
Mechan	ical						
	Static load applied to electrical interfa				1334	Ν	
	Static load applied to the thermal inte	rface area, See <sup>(4)</sup> Figure 8				156	N
	Static load applied to Datum "A" inter				712	N	
Environ	imental			1			
			< 400 nm <sup>(7)</sup>			2	mW/c m <sup>2</sup>
	Illumination power density <sup>(5)(6)</sup>	400 to 700 nm <sup>(8)</sup>		see table notes	25	W/cm <sup>2</sup>	
			> 700 nm			10	mW/c m <sup>2</sup>
-		Thermal Test Points 1 and $2^{(9)}$	Operating Case	10	05.45	70 <sup>(9)</sup>	
1 <sub>C</sub>	Operating Case Temperature	Thermal Test Point 3 and Array <sup>(9)</sup>	Temperature <sup>(9)(10)</sup>	10	25-45 -	65 <sup>(9)</sup>	°C
	Operating Device Temperature Gradi	Gradient between any two points on the package <sup>(9)</sup>			10	°C	
	Operating Humidity <sup>(5)</sup>		Non-Condensing			95	%RH
	Operating Landed Duty Cycle <sup>(11)</sup>				25		%

(1) All voltages referenced to  $V_{SS}$  (ground).

(2) Voltages  $V_{CC}$ ,  $V_{CCI}$ , and  $V_{CC2}$ , are required for proper DMD operation.

(3) Load should be uniformly distributed across the entire Electrical Interface area number 1 and number 2.

(4) Load should be uniformly distributed across Thermal Interface Area. Refer to the for size and location of the datum-A surfaces.

(5) Optimal, long-term performance of the Digital Micromirror Device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty cycle, ambient temperature (both storage and operating), case temperature, and power on/off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle. Contact your local Texas Instruments representative for additional information related to optimizing the DMD performance.

(6) Total integrated illumination power density, above or below the indicated wavelength threshold.

(7) The maximum operating conditions for operating temperature and illumination power density for wavelengths < 400 nm shall not be implemented simultaneously.

(8) Also Limited by the resulting micromirror array temperature .Refer to Thermal Characteristics for information related to calculating the micromirror array temperature.

(9) See the for Thermal Test Point Locations, Package Thermal Resistance, and Device Temperature Calculation.

(10) In some applications, the total DMD heat load can be dominated by the amount of incident light energy absorbed. Se the Thermal Characteristics for further details.

(11) "Landed Duty-Cycle" refers to the percentage of time an individual micromirror spends landed in one state (+12° or -12°) versus the other state (-12° or +12°).



Figure 8. System Interface Loads

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# **ELECTRICAL CHARACTERISTICS**

Over the range of recommended supply voltage and recommended case operating temperature (unless otherwise noted)

PARAMETERS (Under RECOMMENDED OPERATING CONDITIONS)		TEST CO	MIN	NOM	МАХ	UNIT	
V <sub>OH</sub>	High-level output voltage <sup>(1)</sup> , See Figure 9	V <sub>CC</sub> = 3.0 V,	I <sub>OH</sub> = -20 mA	2.4			V
V <sub>OL</sub>	Low-level output voltage <sup>(1)</sup> , See Figure 9	V <sub>CC</sub> = 3.6 V,	I <sub>OH</sub> = 15 mA			0.4	V
V <sub>MBRS</sub> T	Clocking Pulse Waveform applied to MBRST[29:0] Input Pins (supplied by DLPA200s)			-27		26.5	V
I <sub>OZ</sub>	High impedance output current <sup>(1)</sup>	V <sub>CC</sub> = 3.6 V				10	μA
	High lovel output current <sup>(1)</sup>	$V_{OH} = 2.4 \text{ V}, V_{CC} \geq 3 \text{ V}$				-20	<b>m</b> 1
ЮН	High-level output current W	$V_{OH} = 1.7 \text{ V}, V_{CC} \ge 2.25$	V			-15	ma
I <sub>OL</sub>		$V_{OL} = 0.4 \text{ V}, V_{CC} \ge 3 \text{ V}$				15	m۸
		$V_{OL} = 0.4 \text{ V}, V_{CC} \ge 2.25$			14	ША	
VIH	High-level input voltage <sup>(1)</sup>			1.7		VCC + .3	V
VIL	Low-level input voltage <sup>(1)</sup>			-0.3		0.7	V
IIL	Low-level input current <sup>(1)</sup>	V <sub>CC</sub> = 3.6 V,	$V_I = 0 V$			-60	μA
I <sub>IH</sub>	High-level input current <sup>(1)</sup>	V <sub>CC</sub> = 3.6 V,	$V_I = V_{CC}$			60	μA
I <sub>CC</sub>	Current into V <sub>CC</sub> pin	V <sub>CC</sub> = 3.6 V,				2990	mA
I <sub>CCI</sub>	Current into $V_{OFFSET}$ pin <sup>(2)</sup>	V <sub>CCI</sub> = 3.6 V				910	mA
I <sub>CC2</sub>	Current into V <sub>CC2</sub> pin	V <sub>CC2</sub> = 8.75V				25	mA
Z <sub>IN</sub>	Internal Differential Impedance			95		105	Ohms
Z <sub>LINE</sub>	Line Differential Impedance (PWB, Trace)			90	100	110	Ohms
CI	Input capacitance (1)	f = 1 MHz				10	pF
Co	Output capacitance (1)	f = 1 MHz				10	pF
C <sub>IM</sub>	Input capacitance for MBRST[29:0] pins	f = 1 MHz		270		355	pF

(1) Applies to LVCMOS pins only.

(2) Exceeding the maximum allowable absolute voltage difference between V<sub>CC</sub> and V<sub>CCI</sub> may result in excess current draw. (See the Absolute Maximum Ratings for details)

## **Measurement Conditions**

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. Figure 9 shows an equivalent test load circuit for the output under test. The load capacitance value stated is only for characterization and measurement of ac timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving. All rise and fall transition timing parameters are referenced to  $V_{IL}$  MAX and  $V_{IH}$  MIN for input clocks,  $V_{OL}$  MAX and  $V_{OH}$  MIN for output clocks.







## SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

	LVDS TIMING PARAMETERS See Figure 10	MIN	NOM	МАХ	UNIT
f <sub>DCLK_*</sub>	DCLK_* clock frequency {where * = [A, B, C, or D]}	200		400	MHz
t <sub>c</sub>	Clock Cycle - DLCK_*	2.5			ns
tw	Pulse Width - DLCK_*		1.25		ns
t <sub>s</sub>	Setup Time - D_*[15:0] & SCTRL_* before DCLK_*	.35			ns
t <sub>h</sub>	Hold Time, D_*[15:0] & SCTRL_* after DCLK_*	.35			ns
t <sub>skew</sub>	Skew between any two buses [A ,B, C, and D]	-1.25		1.25	ns





# SWITCHING CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

	LVDS Waveform Requirements SeeFigure 11	MIN	NOM	МАХ	UNIT
V <sub>ID</sub>	Input Differential Voltage (absolute difference)	100	400	600	mV
V <sub>CM</sub>	Common Mode Voltage		1200		mV
V <sub>LVDS</sub>	LVDS Voltage	0		2000	mV
t <sub>r</sub>	Rise Time (20% to 80%)	100		400	ps
t <sub>r</sub>	Fall Time (80% to 20%)	100		400	ps



Figure 11. LVDS Waveform Requirements



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## SWITCHING CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

	Serial Control Bus Timing Parameters See and	MIN	NOM MAX	UNIT
f <sub>SCP_CLK</sub>	SCP Clock Frequency	50	500	KHz
t <sub>SCP_SKEW</sub>	Time between valid SCP_DI and rising edge of SCP_CLK	-300	300	ns
t <sub>SCP_DELAY</sub>	Time between valid SCP_DO and rising edge of SCP_CLK		960	ns
t <sub>SCP_ENZ</sub>	Time between falling edge of SCP_ENZ and the first rising edge of SCP_CLK	30		ns
t_SCP	Rise time for SCP signals		200	ns
t <sub>f_SCP</sub>	Fall time for SCP signals		200	ns



Figure 12. Serial Communications Bus Timing Parameters



#### **DMD Power-Up and Power-Down Procedures**

Repeated failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. The DLP9500 power-up and power-down procedures are defined by the DLPC410 data sheet (TI Literature number DLPS024) and the DLP Discovery Chipset Data sheet (TI Literature number DLPU008). These procedures must be followed to ensure reliable operation of the device.



## **Micromirror Array Physical Characteristics**

Physical characteristics of the micromirror array are provided in . Additional details are provided in the **Package Mechanical Characteristics** section at the end of this document.

#### **Table 3. Micromirror Array Physical Characteristics**

PARAMETER	VALUE	UNITS
Number of active micromirror columns <sup>(1)</sup>	1920	micromirrors
Number of active micromirror rows <sup>(1)</sup>	1080	micromirrors
Micromirror pitch <sup>(1)</sup>	10.8	microns
Micromitror active array beight (1)	1080	micromirrors
	11.664	millimeters
Micromitror active array width (1)	1920	micromirrors
	20.736	millimeters
Micromirror array border <sup>(2)</sup>	10	micromirrors/side

(1) See Figure 3

(2) The mirrors that form the array border are hard-wired to tilt in the -12° ("Off") direction once power is applied to the DMD (see Figure 3 and Figure 4).

## **Micromirror Array Optical Characteristics**

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-off's between numerous component and system design parameters. See the related application reports (listed in Related Documents) for guidleines.

	DADAMETER	CONDITIONS	MIN	NOM	ΜΛΥ		
		DMD "parked" state <sup>(1)(2)(3)</sup> , See <sup>Figure 4</sup>		0	MIAA	UNIT	
α	Micromirror tilt angle	DMD "landed" state <sup>(1)(4)(5)</sup> See <sup>Figure 4</sup>	12			degrees	
β	Micromirror tilt angle variation (1)(4)(6)(7)(8)	See Figure 4	-1		1	degrees	
	Micromirror Cross Over Time <sup>(9)</sup>			16	22	us	
	Micromirror Switching Time <sup>(10)</sup>			140		us	
	No. 0	Non-adjacent micromirrors			10		
	Non Operating micromirrors	adjacent micromirrors			0	microminors	
	Orientation of the micromirror axis-of-rotation <sup>(12)</sup>	See Figure 3	44	45	46	degrees	
	Micromirror array optical efficiency <sup>(13)(14)</sup>	400 nm to 700 nm, with all micromirrors in the ON state		68%			
	Window material		Cor	ning 7056			
	Window refractive index	at 545 nm		1.487			
	Window flatness <sup>(15)</sup>	Per 25 mm			4	fringes	
	Window Artifact Size	Within the Window Aperture <sup>(16)</sup>			400	um	
	Window aperture			See (16)			

#### **Table 4. Micromirror Array Optical Characteristics**

(1) Measured relative to the plane formed by the overall micromirror array

(2) "Parking" the micromirror array returns all of the micromirrors to an essentially flat (0°) state (as measured relative to the plane formed by the overall micromirror array).

(3) When the micromirror array is "parked", the tilt angle of each individual micromirror is uncontrolled.

(4) Additional variation exists between the micromirror array and the package datums, as shown in the Package Mechanical Characteristics section at the end of this document.

(5) When the micromirror array is "landed", the tilt angle of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of "1" will result in a micromirror "landing" in an nominal angular position of "+12 degrees". A binary value of 0 results in a micromirror "landing" in an nominal angular position of "-12 degrees".

(6) Represents the "landed" tilt angle variation relative to the Nominal "landed" tilt angle.

(7) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different

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devices

- (8) For some applications, it is critical to account for the micromirror tilt angle variation in the overall System Optical Design. With some System Optical Designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some System Optical Designs, the micromirror tilt angle variation between devices may result in colorimetry variations and/or system contrast vacation.
- (9) Micromirror Cross Over time is primarily a function of the natural response time of the micromirrors.
- (10) Micromirror switching is controlled and coordinated by the DLPC410 (TI Literature number DLPS024) AND DLPA200 (TI Literature number DLPS015). Nominal Switching time depends on the system implementation and represents the time for the entire micromirror array to be refreshed.
- (11) Non-operating micromirror is defined as a micromirror that is unable to transition nominally from the -12 degree position to +12 degree or vice versa.
- (12) Measured relative to the package datums "B" and "C", shown in the Package Mechanical Characteristics section at the end of this document.
- (13) The minimum or maximum DMD optical efficiency observed in a specific application depends on numerous application-specific design variables, such as:
  - Illumination wavelength, bandwidth/line-width, degree of coherence
  - Illumination angle, plus angle tolerance
  - Illumination and projection aperture size, and location in the system optical path
  - Illumination overfill of the DMD micromirror array
  - Aberrations present in the illumination source and/or path
  - Aberrations present in the projection path
  - Etc.

The specified nominal DMD optical efficiency is based on the following use conditions:

- Visible illumination (400 nm 700 nm)
- Input illumination optical axis oriented at 24° relative to the window normal
- Projection optical axis oriented at 0° relative to the window normal
- f/3.0 illumination aperture
- f/2.4 projection aperture

Based on these use conditions, the nominal DMD optical efficiency results from the following four components:

- Micromirror array fill factor: nominally 92%
- Micromirror array diffraction efficiency: nominally 86%
- Micromirror surface reflectivity: nominally 88%
- Window transmission: nominally 97% (single pass, through two surface transitions)
- (14) Does not account for the effect of micromirror switching duty cycle, which is application dependant. Micromirror switching duty cycle represents the percentage of time that the micromirror is actually reflecting light from the optical illumination path to the optical projection path. This duty cycle depends on the illumination aperture size, the projection aperture size, and the micromirror array update rate.
- (15) At a wavelength of 632.8nm.
- (16) See the Package Mechanical Characteristics section at the end of this document for details regarding the size and location of the window aperture.
- (17) Refers only to non-cleanable artifacts. see the DMD S4xx Glass Cleaning Procedure (TI Literature number DLPA025) and DMD S4xx Handling Specifications (TI Literature number DLPA014) for recommend handling and cleaning processes.



## Thermal Characteristics

Achieving optimal DMD performance requires proper management of the maximum DMD case temperature, the maximum temperature of any individual micromirror in the active array, the maximum temperature of the window aperture, and the temperature gradient between case temperature and the predicted micromirror array temperature. (see Figure 14).

See the **RECOMMEND OPERATING CONDITIONS** for applicable temperature limits.

#### Package Thermal Resistance

The DMD is designed to conduct absorbed and dissipated heat to the back of the Type A package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the specified operational temperatures, refer to Figure 14. The total heat load on the DMD is typically driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.

Package Thermal Resistance						
	Min	Nom	Max	Units		
Active Micromirror Array resistance to TC2			0.5	°C/W		

#### **Case Temperature**

The temperature of the DMD case can be measured directly. For consistency, a Thermal Test Point locations TC1 and TC2 are defined, as shown in Figure 14.



Figure 14. Thermal Test Point Location



(1) (2)

#### **Micromirror Array Temperature Calculation**

Micromirror array temperature cannot be measured directly; therefore, it must be computed analytically from measurement points (Figure 14), the package thermal resistance, the electrical power, and the illumination heat load. The relationship between micromirror array temperature and the case temperature are provided by Equation 1 and Equation 2:

$$T_{Array} = T_{Ceramic} + (Q_{Array} \times R_{Array-To-Ceramic})$$

$$Q_{Array} = Q_{ELE} + Q_{ILL}$$

Where the following elements are defined as:

T<sub>Array</sub> = computed micromirror array temperature (°C)

 $T_{Ceramic}$  = Ceramic temperature (°C) (TC2 Location Figure 14)

Q<sub>Arrav</sub> = Total DMD array power (electrical + absorbed) (measured in Watts)

R<sub>Array-To-Ceramic</sub> = thermal resistance of DMD package from array to TC2 (°C/Watt) (see Package Thermal Resistance)

Q<sub>ELE</sub> = Nominal electrical power (Watts)

Q<sub>ILL</sub> = Absorbed illumination energy (Watts)

An example calculation is provided below based on a traditional DLP Video projection system. The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. The nominal electrical power dissipation to be used in the calculation is 4.4 Watts. Thus,  $Q_{ELE} = 4.4$  Watts. The absorbed power from the illumination source is variable and depends on the operating state of the mirrors and the intensity of the light source. Based on modeling and measured data from DLP projection system  $Q_{ILL} = C_{L2W} \times SL$ .

Where:

C<sub>L2W</sub> is a Lumens to Watts constant, and can be estimated at 0.00274 Watt/Lumen

SL = Screen Lumens nominally measured to be 2000 lumens

Qarray = 4.4 + (0.00274 x 2000) = 9.88 watts, Estimated total power on micromirror Array

 $T_{Ceramic} = 55^{\circ}C$ , assumed system measurement

Finally,  $T_{Array}$  (micromirror active array temperature) is

**T**<sub>Arrav</sub>= 55°C + (9.88 watts x 0.5°C/watt) = **59.9°C** 

## **REVISION HISTORY**

C	hanges from Original (August 2012) to Revision A Page
•	Changed the device From: Product Preview To: Production 1
C	hanges from Revision A (September 2012) to Revision B Page
•	Added / DLPR4101 Enhanced PROM to DLPR410 in chipset list 2
•	Added / DLPR4101 Enhanced PROM to DLPR410 in Related Documentation Table



2-May-2013

# PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing		Qty	(2)		(3)		(4)	
DLP9500FLN	ACTIVE	LCCC	FLN	355	3	Green (RoHS & no Sb/Br)	W NIAU	N / A for Pkg Type			Samples

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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