

300 MHz, 2.5 Ω , Dual SPDT Analog Switches

DESCRIPTION

The DG3516, DG3517 are dual SPDT analog switches which operate from 1.8 V to 5.5 V single rail power supply. They are design for audio, video, and USB switching applications.

The devices have 2.5 Ω on-resistance and 300 MHz 3dB bandwidth. 0.2 Ω on-resistance matching and 1 Ω flatness make the device high linearity. The devices are 1.6 V logic compatible within the full operation voltage range.

These switches are built on a sub-micron high density process that brings low power consumption and low voltage performance.

The switches are packaged in MICRO FOOT chip scale package of 4 mm x 3 mm bump array.

As a committed partner to the community and environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For MICRO FOOT analog switch products manufactured with tin/silver/copper (SnAgCu) device termination, the lead (Pb)-free "E1" suffix is being used as a designator.

FEATURES

- **Halogen-free according to IEC 61249-2-21 Definition**
- 1.8 V to 5.5 V operation
- 2.5 Ω at 2.7 V R_{ON}
- 300 MHz - 3 dB bandwidth
- ESD method 3015.7 > 2 kV
- Latch-up current 200 mA (JESD 78)
- 1.6 V logic compatible
- **Compliant to RoHS Directive 2002/95/EC**

BENEFITS

- Space Saving MICRO FOOT® Package
- High Linearity
- Low Power Consumption
- High Bandwidth
- Full Rail Signal Swing Range

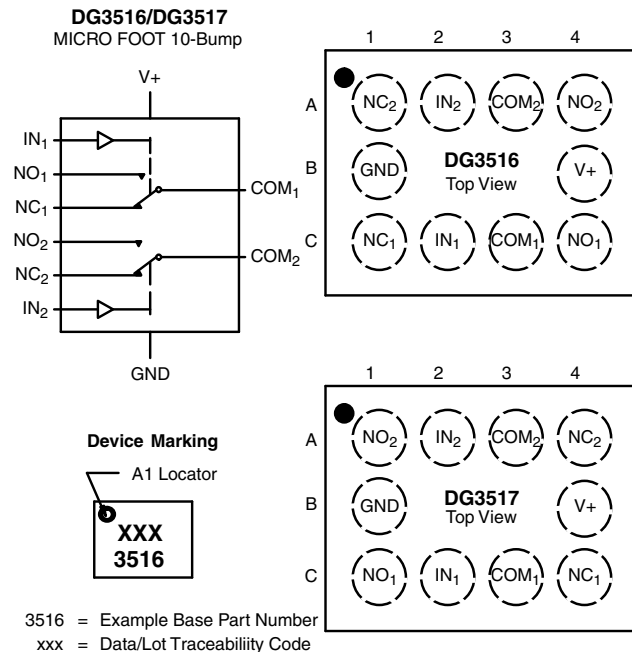
APPLICATIONS

- Cellular Phones
- MP3
- Media Players
- Modems
- Hard Drives
- PCMCIA



RoHS
COMPLIANT
HALOGEN
FREE

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE

| Logic | NC1 and NC2 | NO1 and NO2 |
|-------|-------------|-------------|
| 0 | ON | OFF |
| 1 | OFF | ON |

ORDERING INFORMATION

| Temp. Range | Package | Part Number |
|------------------|--|----------------------------------|
| - 40 °C to 85 °C | MICRO FOOT: 10 Bump (4 x 3, 0.5 mm Pitch, 238 μ m Bump Height) | DG3516DB-T5-E1 DG3517DB-T5-E1 |

ABSOLUTE MAXIMUM RATINGS

| Parameter | Limit | Unit |
|--|--|------|
| Reference V+ to GND | - 0.3 to + 6 | V |
| IN, COM, NC, NO ^a | - 0.3 to (V+ + 0.3) | |
| Continuous Current (NO, NC, COM) | ± 100 | mA |
| Peak Current (Pulsed at 1 ms, 10 % duty cycle) | ± 200 | |
| Storage Temperature | (D Suffix) | °C |
| Package Solder Reflow Conditions ^b | IR/Convection | |
| ESD per Method 3015.7 | > 2 | kV |
| Power Dissipation (Packages) ^c | MICRO FOOT: 10 Bump (4 mm x 3 mm) ^d | mW |

Notes:

- a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. Refer to IPC/JEDEC (J-STD-020B).
c. All bumps welded or soldered to PC board.
d. Derate 5.7 mW/°C above 70 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 3 V)

| Parameter | Symbol | Test Conditions Otherwise Unless Specified V+ = 2.7 V to 3.6 V, VIN = 0.5 V or 1.4 V ^e | | Temp. ^a | Limits - 40 °C to 85 °C | | | Unit |
|--|---|---|--------------------------------|--------------------|----------------------------|-------------------|-------------------|------|
| | | | | | Min. ^b | Typ. ^c | Max. ^b | |
| Analog Switch | | | | | | | | |
| Analog Signal Range ^d | V _{NO} , V _{NC} , V _{COM} | | | Full | 0 | | V+ | V |
| On-Resistance ^d | R _{ON} | V+ = 2.7 V I _{NO} , I _{NC} = 10 mA | V _{COM} = 1.5 V | Room Full | | 2.5 | 3.5 3.8 | Ω |
| R _{ON} Flatness ^d | R _{ON} Flatness | | V _{COM} = 1, 1.5, 2 V | Room | | 0.52 | 1 | |
| On-Resistance Match Between Channels ^d | ΔR _{DS(on)} | | V _{COM} = 1.5 V | Room | | | 0.25 | |
| Switch Off Leakage Current | I _{NO(off)} I _{NC(off)} | V+ = 3.3 V, V _{NO} , V _{NC} = 0.3 V/3 V, V _{COM} = 3 V/0.3 V | | Room Full | - 2 - 20 | | 2 20 | nA |
| | I _{COM(off)} | | | Room Full | - 2 - 20 | | 2 20 | |
| Channel-On Leakage Current | I _{COM(on)} | V+ = 3.3 V, V _{NO} , V _{NC} = V _{COM} = 0.3 V/3 V | | Room Full | - 2 - 20 | | 2 20 | |
| Digital Control | | | | | | | | |
| Input High Voltage ^d | V _{INH} | | | Full | 1.4 | | | V |
| Input Low Voltage | V _{INL} | | | Full | | | 0.5 | |
| Input Capacitance | C _{in} | | | Full | | 5 | | pF |
| Input Current | I _{INL} or I _{INH} | VIN = 0 V or V+ | | Full | 1 | | 1 | μA |

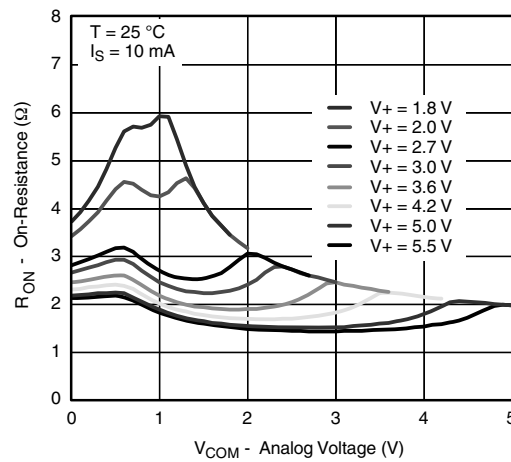
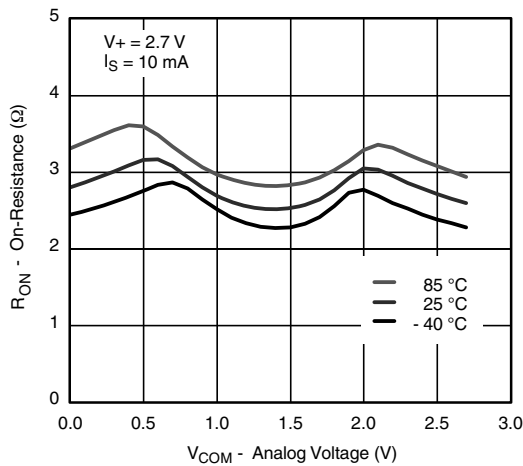
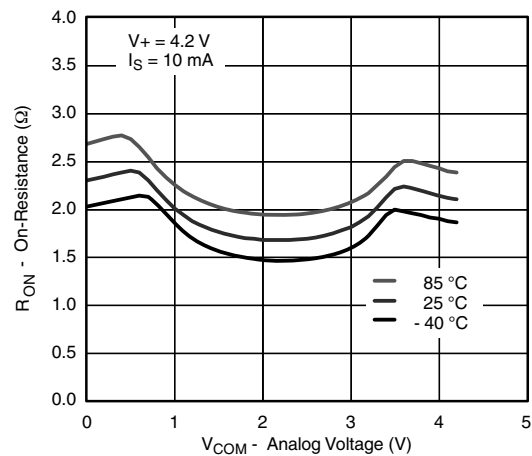
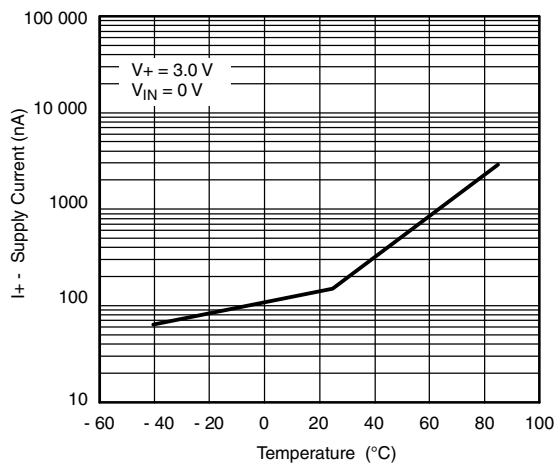
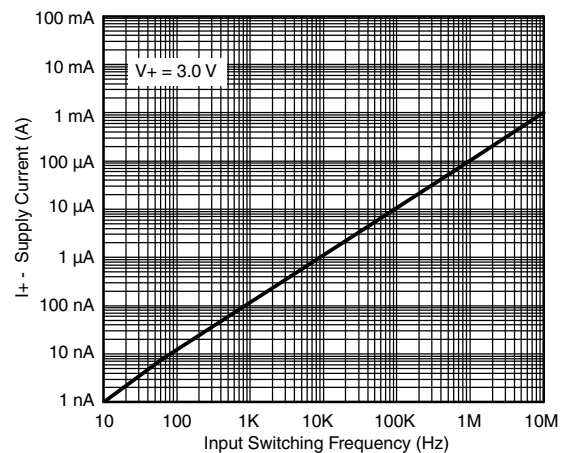


| SPECIFICATIONS (V+ = 3 V) | | | | | | | | |
|-------------------------------------|----------|---|------------|--------------------|----------------------------|-------------------|-------------------|------|
| Parameter | Symbol | Test Conditions Otherwise Unless Specified V+ = 2.7 V to 3.6 V, VIN = 0.5 V or 1.4 V ^e | | Temp. ^a | Limits - 40 °C to 85 °C | | | Unit |
| | | | | | Min. ^b | Typ. ^c | Max. ^b | |
| Dynamic Characteristics | | | | | | | | |
| Turn-On Time | tON | V+ = 2.7 V, VNO or VNC = 1.5 V RL = 300 Ω, CL = 35 pF | | Room Full | | 21 | 51 52 | ns |
| Turn-Off Time | tOFF | | | Room Full | | 15 | 45 46 | |
| Break-Before-Make Time | td | | | Full | 1 | | | |
| Charge Injection ^d | QINJ | CL = 1 nF, VGEN = 2 V, RGEN = 0 Ω | | Room | | 1 | | pC |
| Off-Isolation ^d | OIRR | RL = 50 Ω, CL = 5 pF | f = 1 MHz | Room | | - 74 | | dB |
| | | | f = 10 MHz | Room | | - 54 | | |
| Crosstalk ^d | XTALK | | f = 1 MHz | Room | | - 76 | | |
| | | | f = 10 MHz | Room | | - 56 | | |
| NO, NC Off Capacitance ^d | CNO(off) | VIN = 0 or V+, f = 1 MHz | | Room | | 12 | | pF |
| | CNC(off) | | | Room | | 12 | | |
| Channel-On Capacitance ^d | CNO(on) | | | Room | | 40 | | |
| | CNC(on) | | | Room | | 40 | | |
| Power Supply | | | | | | | | |
| Power Supply Current | I+ | VIN = 0 V or V+ | | Room Full | | | 1 1 | μA |

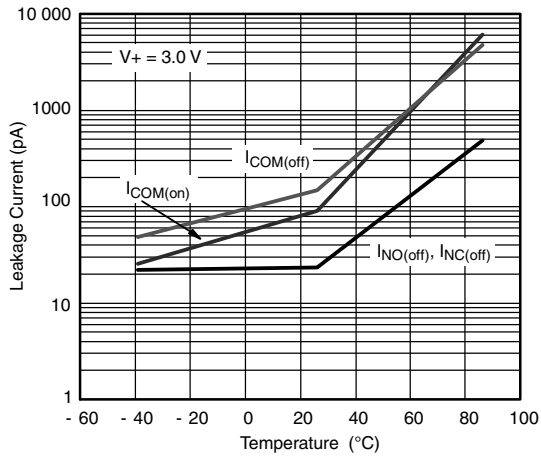
| SPECIFICATIONS (V+ = 5 V) | | | | | | | | |
|--|----------------------|---|--------------------|--------------------|----------------------------|-------------------|-------------------|------|
| Parameter | Symbol | Test Conditions Otherwise Unless Specified V+ = 4.2 V to 5.5 V, VIN = 0.8 V or 2 V ^e | | Temp. ^a | Limits - 40 °C to 85 °C | | | Unit |
| | | | | | Min. ^b | Typ. ^c | Max. ^b | |
| Analog Switch | | | | | | | | |
| Analog Signal Range ^d | VNO, VNC, VCOM | | | Full | 0 | | V+ | V |
| On-Resistance ^d | RON | V+ = 4.2 V INO, INC = 10 mA | VCOM = 3.5 V | Room Full | | 2.2 | 2.9 3.1 | Ω |
| RON Flatness ^d | RON Flatness | | VCOM = 1, 2, 3.5 V | Room | | 0.53 | 1 | |
| On-Resistance Match Between Channels ^d | ΔRDS(on) | | VCOM = 3.5 V | Room | | | 0.25 | |
| Switch Off Leakage Current | INO(off) INC(off) | V+ = 5.5 V, VNO, VNC = 1 V/4.5 V, VCOM = 4.5 V/1 V | | Room Full | - 2 - 20 | | 2 20 | nA |
| | ICOM(off) | | | Room Full | - 2 - 20 | | 2 20 | |
| Channel-On Leakage Current | ICOM(on) | V+ = 5.5 V, VNO, VNC = VCOM = 1 V/4.5 V | | Room Full | - 2 - 20 | | 2 20 | |
| Digital Control | | | | | | | | |
| Input High Voltage ^d | VINH | | | Full | 2 | | | V |
| Input Low Voltage | VINL | | | Full | | | 0.8 | |
| Input Capacitance | Cin | | | Full | | 5 | | pF |
| Input Current | IINL or IINH | VIN = 0 or V+ | | Full | 1 | | 1 | μA |
| Dynamic Characteristics | | | | | | | | |
| Turn-On Time | tON | V+ = 4.2 V, VNO or VNC = 3 V RL = 300 Ω, CL = 35 pF | | Room Full | | 15 | 45 46 | ns |
| Turn-Off Time | tOFF | | | Room Full | | 12 | 42 43 | |
| Break-Before-Make Time | td | | | Full | 1 | | | |
| Charge Injection ^d | QINJ | CL = 1 nF, VGEN = 2 V, RGEN = 0 Ω | | Room | | 1 | | pC |
| Off-Isolation ^d | OIRR | RL = 50 Ω, CL = 5 pF | f = 1 MHz | Room | | - 74 | | dB |
| Crosstalk ^d | XTALK | | f = 10 MHz | Room | | - 54 | | |
| | | | f = 1 MHz | Room | | - 78 | | |
| | | | f = 10 MHz | Room | | - 56 | | |
| NO, NC Off Capacitance ^d | CNO(off) | VIN = 0 or V+, f = 1 MHz | | Room | | 12 | | pF |
| | CNC(off) | | | Room | | 12 | | |
| Channel-On Capacitance ^d | CNO(on) | | | Room | | 40 | | |
| | CNC(on) | | | Room | | 40 | | |
| Power Supply | | | | | | | | |
| Power Supply Current | I+ | VIN = 0 V or V+ | | Room Full | | | 1 1 | μA |

Notes:

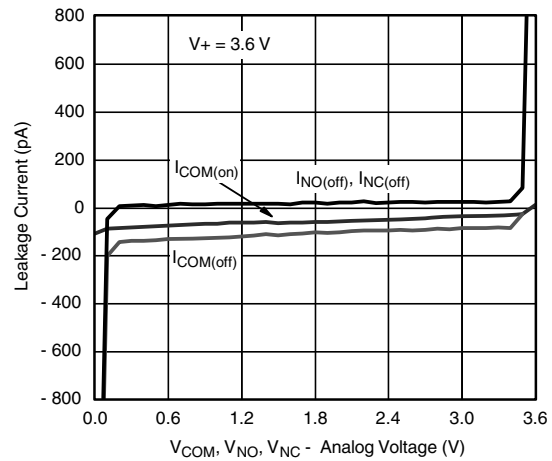
- Room = 25 °C, Full = as determined by the operating suffix.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.
- Guaranteed by 5 V testing, not production tested.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

 R_{ON} vs. V_{COM} and Single Supply Voltage

 R_{ON} vs. Analog Voltage and Temperature

 R_{ON} vs. Analog Voltage and Temperature

Supply Current vs. Temperature

Supply Current vs. Input Switching Frequency

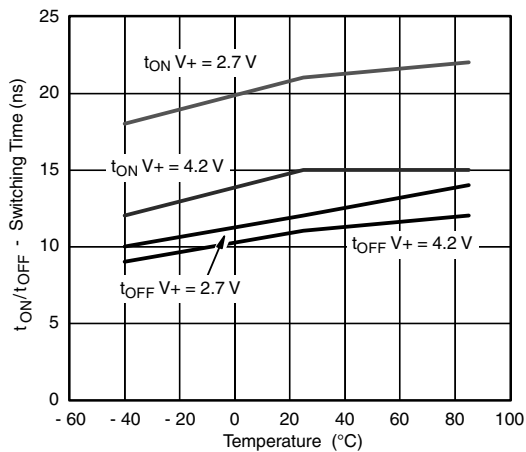
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



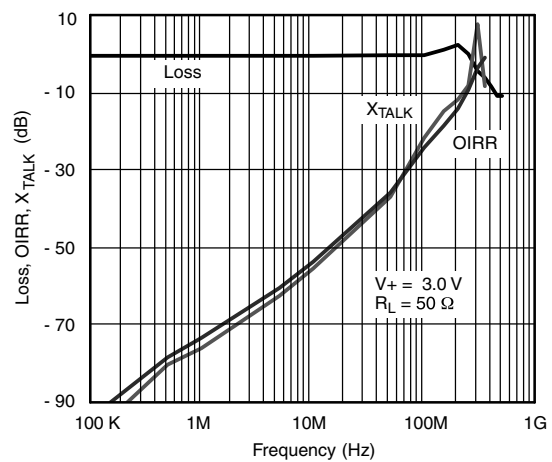
Leakage Current vs. Temperature



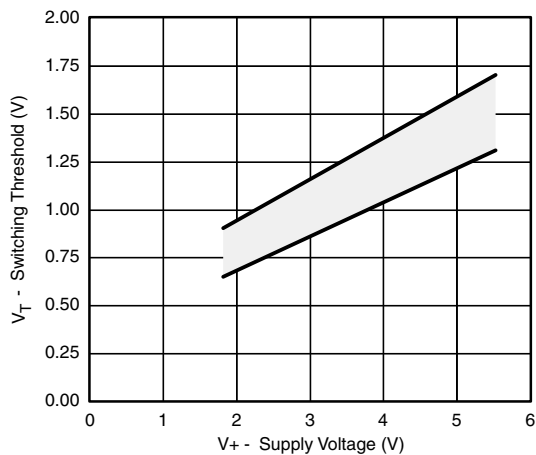
Leakage vs. Analog Voltage



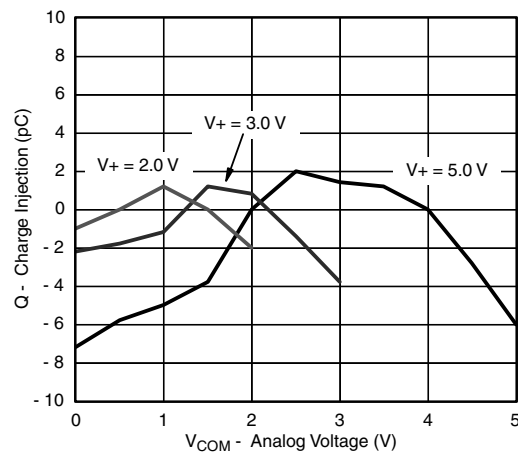
Switching Time vs. Temperature



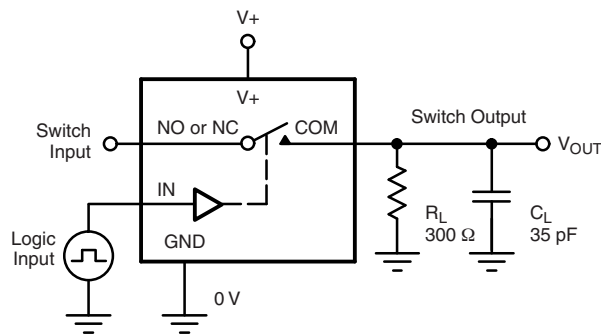
Insertion Loss, Off-Isolation Crosstalk vs. Frequency



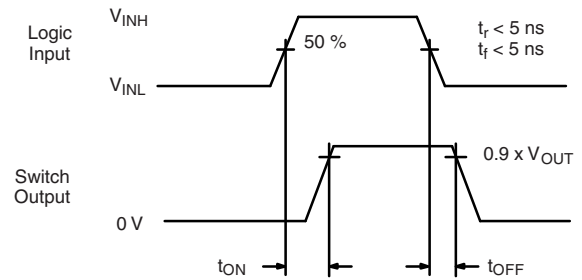
Switching Threshold vs. Supply Voltage



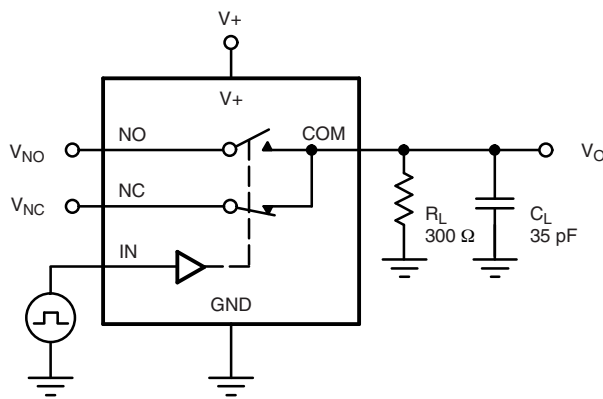
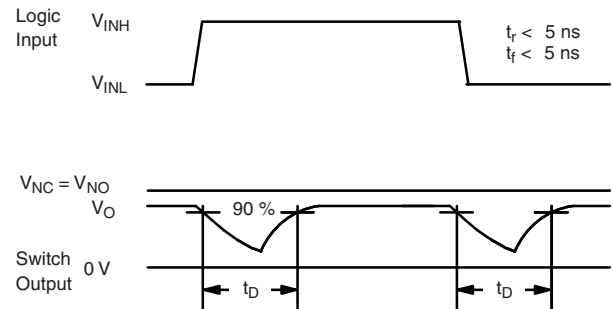
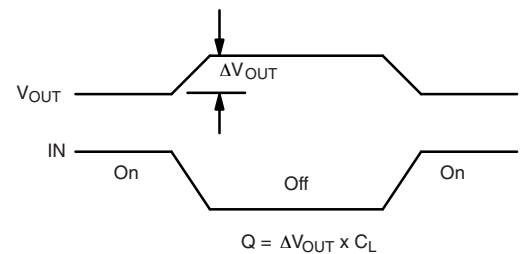
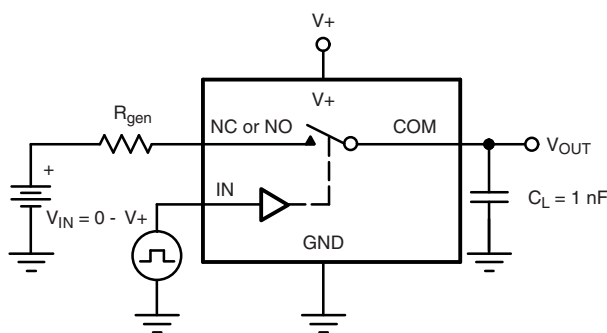
Charge Injection vs. Analog Voltage

TEST CIRCUITS

 C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

 C_L (includes fixture and stray capacitance)

Figure 2. Break-Before-Make Interval


IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

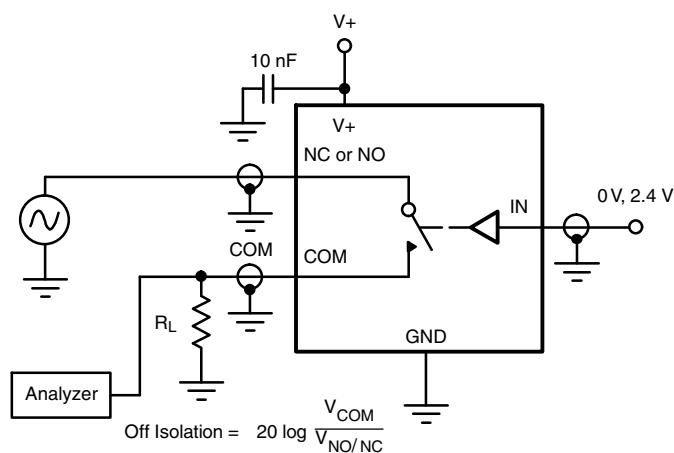


Figure 4. Off-Isolation

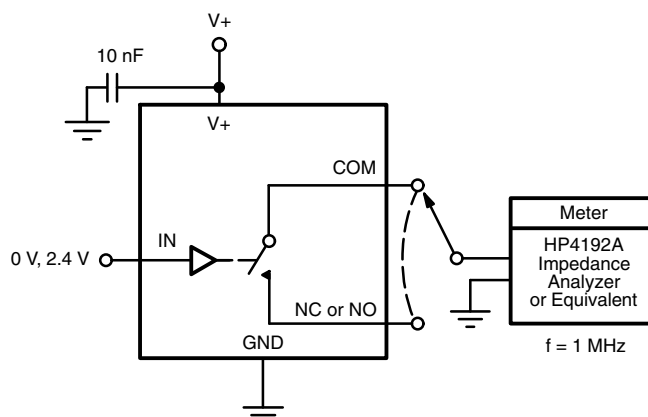
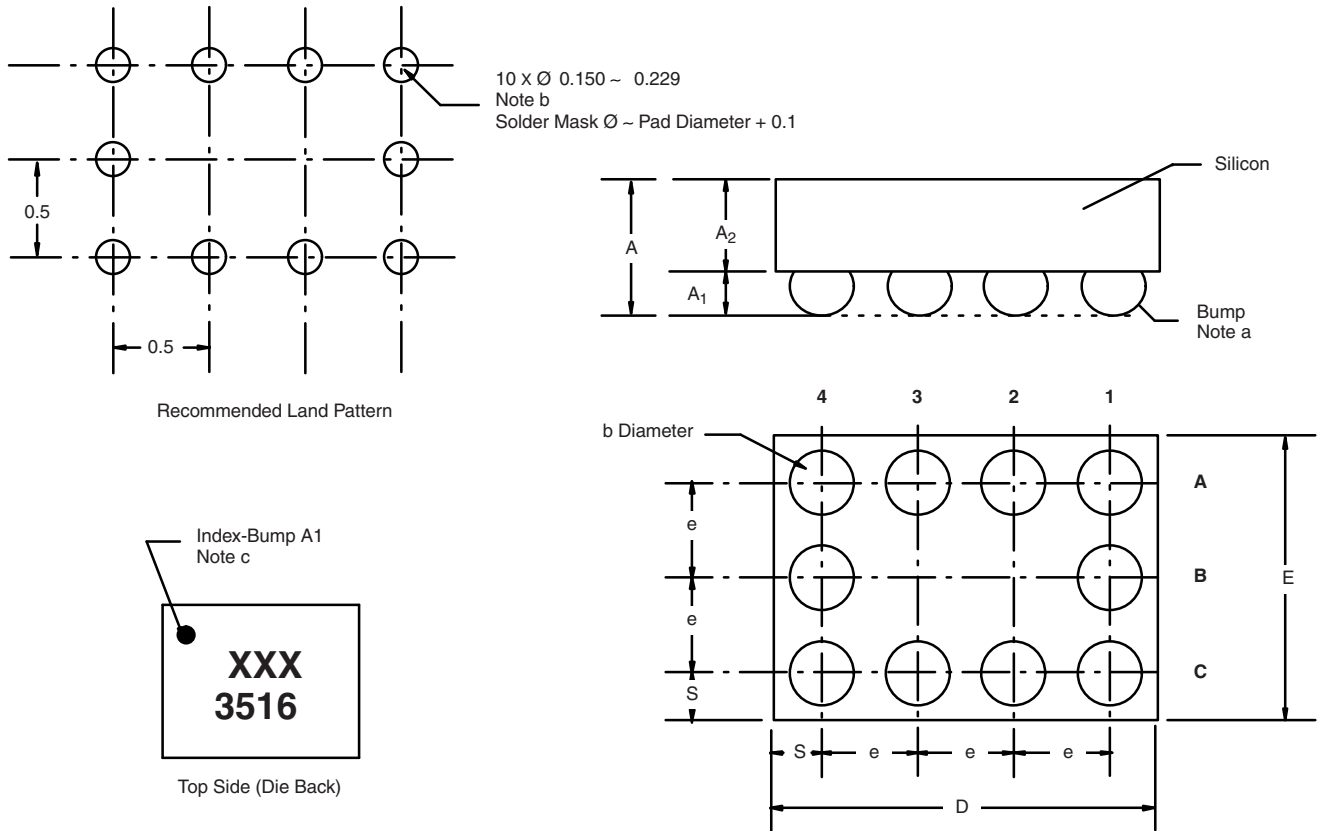


Figure 5. Channel Off/On Capacitance

PACKAGE OUTLINE
MICRO FOOT: 10 BUMP (4 mm x 3 mm, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)


Notes (Unless Otherwise Specified):

- a. Bump is Lead (Pb)-free Sn/Ag/Cu.
- b. Non-solder mask defined copper landing pad.
- c. Laser Mark on silicon die back; back-lapped, no coating. Shown is not actual marking; sample only.

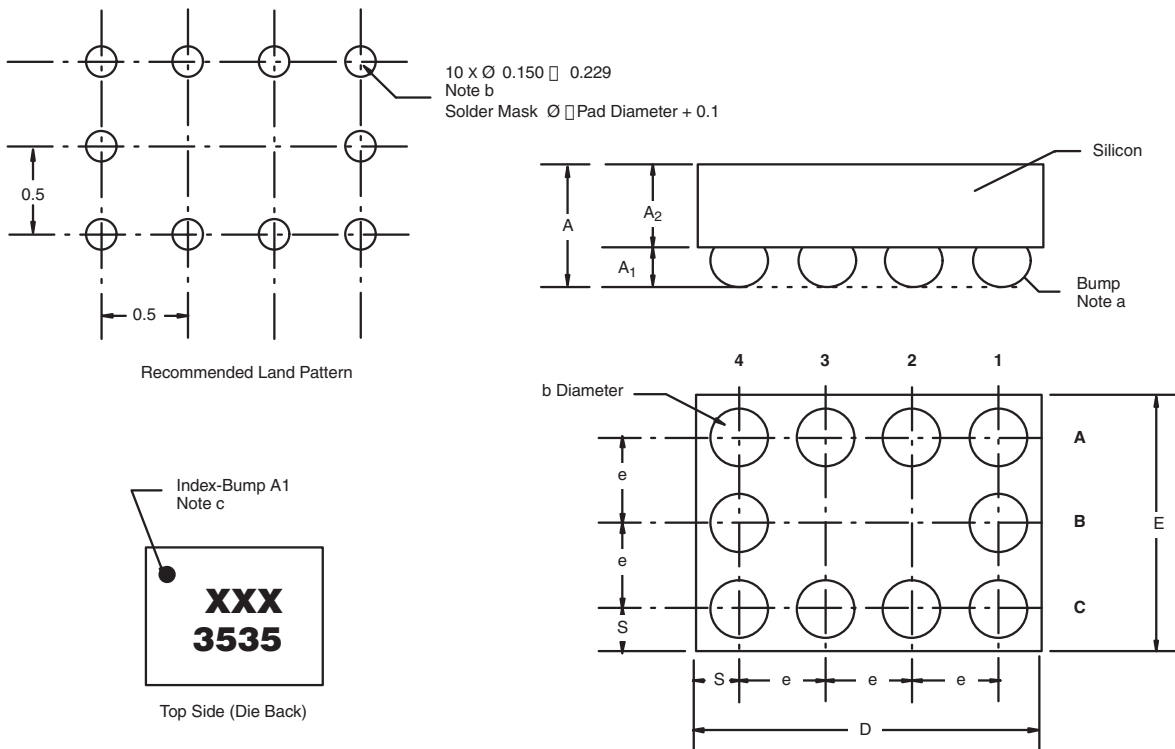
| Dim. | Millimeters ^a | | Inches | |
|----------------------|--------------------------|-------|--------------|--------|
| | Min. | Max. | Min. | Max. |
| A | 0.688 | 0.753 | 0.0271 | 0.0296 |
| A₁ | 0.218 | 0.258 | 0.0086 | 0.0102 |
| A₂ | 0.470 | 0.495 | 0.0185 | 0.0195 |
| b | 0.306 | 0.346 | 0.0120 | 0.0136 |
| D | 1.980 | 2.020 | 0.0780 | 0.0795 |
| E | 1.480 | 1.520 | 0.0583 | 0.0598 |
| e | 0.5 BASIC | | 0.0197 BASIC | |
| S | 0.230 | 0.270 | 0.0091 | 0.0106 |

Notes:

- a. Use millimeters as the primary measurement.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73404.

MICRO FOOT: 10-BUMP (4 mm x 3 mm, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)



Notes

(unless otherwise specified)

- Bump is lead (Pb)-free Sn/Ag/Cu.
- Non-solder mask defined copper landing pad.
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Note

- Use millimeters as the primary measurement.

ECN: S11-1065-Rev. A, 13-Jun-11
DWG: 6001



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