

LM6132/LM6134 Dual and Quad Low Power 10 MHz Rail-to-Rail I/O Operational Amplifiers

Check for Samples: [LM6132](#)

FEATURES

- (For 5V Supply, Typ Unless Noted)
- Rail-to-Rail Input CMVR -0.25V to 5.25V
- Rail-to-Rail Output Swing 0.01V to 4.99V
- High Gain-Bandwidth, 10 MHz at 20 kHz
- Slew Rate 12 V/ μs
- Low Supply Current 360 $\mu\text{A}/\text{Amp}$
- Wide Supply Range 2.7V to over 24V
- CMRR 100 dB
- Gain 100 dB with $R_L = 10\text{k}$
- PSRR 82 dB

APPLICATIONS

- Battery Operated Instrumentation
- Instrumentation Amplifiers
- Portable Scanners
- Wireless Communications
- Flat Panel Display Driver

Connection Diagram

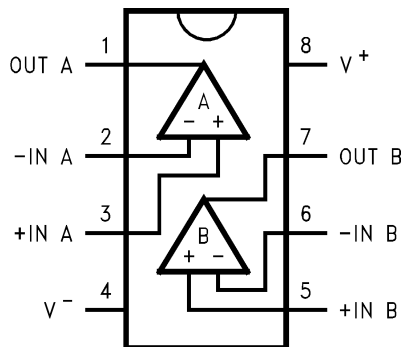


Figure 1. 8-Pin SOIC/PDIP (Top View)
See Package Number D and P

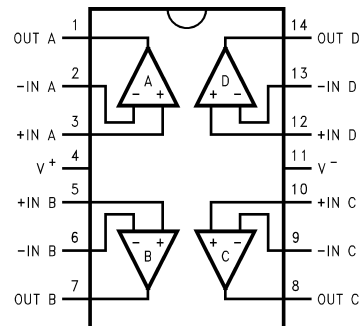


Figure 2. 14-Pin SOIC/PDIP (Top View)
See Package Number D and NFF0014A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



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Absolute Maximum Ratings⁽¹⁾⁽²⁾

ESD Tolerance ⁽³⁾	2500V
Differential Input Voltage	15V
Voltage at Input/Output Pin	(V ⁺)+0.3V, (V ⁻)-0.3V
Supply Voltage (V ⁺ -V ⁻)	35V
Current at Input Pin	±10 mA
Current at Output Pin ⁽⁴⁾	±25 mA
Current at Power Supply Pin	50 mA
Lead Temp. (soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature ⁽⁵⁾	150°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) Human body model, 1.5 kΩ in series with 100 pF.
- (4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
- (5) The maximum power dissipation is a function of T_{J(MAX)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A)/θ_{JA}. All numbers apply for packages soldered directly into a PC board.

Operating Ratings⁽¹⁾

Supply Voltage		1.8V ≤ V ⁺ ≤ 24V
Junction Temperature Range	LM6132, LM6134	-40°C ≤ T _J ≤ +85°C
Thermal resistance (θ _{JA})	P Package, 8-pin PDIP	115°C/W
	D Package, 8-pin SOIC	193°C/W
	NFF0014A Package, 14-pin PDIP	81°C/W
	D Package, 14-pin SOIC	126°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.

5.0V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5.0\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{M}\Omega$ to $V^+/2$.

Boldface limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (1)	LM6134AI LM6132AI Limit (2)	LM6134BI LM6132BI Limit (2)	Units
V_{OS}	Input Offset Voltage		0.25	2 4	6 8	mV max
TCV_{OS}	Input Offset Voltage Average Drift		5			$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$0\text{V} \leq V_{CM} \leq 5\text{V}$	110	140 300	180 350	nA max
I_{OS}	Input Offset Current		3.4	30 50	30 50	nA max
R_{IN}	Input Resistance, CM		104			$\text{M}\Omega$
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 4\text{V}$	100	75 70	75 70	dB min
		$0\text{V} \leq V_{CM} \leq 5\text{V}$	80	60 55	60 55	
PSRR	Power Supply Rejection Ratio	$\pm 2.5\text{V} \leq V^+ \leq \pm 12\text{V}$	82	78 75	78 75	dB min
V_{CM}	Input Common-Mode Voltage Range		-0.25 5.25	0 5.0	0 5.0	V
A_V	Large Signal Voltage Gain	$R_L = 10\text{k}$	100	25 8	15 6	V/mV min
V_O	Output Swing	100k Load	4.992	4.98 4.93	4.98 4.93	V min
			0.007	0.017 0.019	0.017 0.019	V max
		10k Load	4.952	4.94 4.85	4.94 4.85	V min
			0.032	0.07 0.09	0.07 0.09	V max
		5k Load	4.923	4.90 4.85	4.90 4.85	V min
			0.051	0.095 0.12	0.095 0.12	V max
I_{SC}	Output Short Circuit Current LM6132	Sourcing	4	2 2	2 1	mA min
		Sinking	3.5	1.8 1.8	1.8 1	mA min
I_{SC}	Output Short Circuit Current LM6134	Sourcing	3	2 1.6	2 1	mA min
		Sinking	3.5	1.8 1.3	1.8 1	mA min
I_S	Supply Current	Per Amplifier	360	400 450	400 450	μA max

(1) Typical Values represent the most likely parametric normal.

(2) All limits are guaranteed by testing or statistical analysis.

5.0V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5.0\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$ to $V^+/2$.

Boldface limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (1)	LM6134AI LM6132AI Limit (2)	LM6134BI LM6132BI Limit (2)	Units
SR	Slew Rate	$\pm 4\text{V}$ @ $V_S = \pm 6\text{V}$ $R_S < 1\text{ k}\Omega$	14	8 7	8 7	V/ μs min
GBW	Gain-Bandwidth Product	$f = 20\text{ kHz}$	10	7.4 7	7.4 7	MHz min
θ_m	Phase Margin	$R_L = 10\text{k}$	33			deg
G_m	Gain Margin	$R_L = 10\text{k}$	10			dB
e_n	Input Referred Voltage Noise	$f = 1\text{ kHz}$	27			nV/ $\sqrt{\text{Hz}}$
i_n	Input Referred Current Noise	$f = 1\text{ kHz}$	0.18			pA/ $\sqrt{\text{Hz}}$

(1) Typical Values represent the most likely parametric normal.

(2) All limits are guaranteed by testing or statistical analysis.

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$ to $V^+/2$.

Boldface limits apply at the temperature extreme

Symbol	Parameter	Conditions	Typ (1)	LM6134AI LM6132AI Limit (2)	LM6134BI LM6132BI Limit (2)	Units
V_{OS}	Input Offset Voltage		0.12	2 8	6 12	mV max
I_B	Input Bias Current	$0\text{V} \leq V_{\text{CM}} \leq 2.7\text{V}$	90			nA
I_{OS}	Input Offset Current		2.8			nA
R_{IN}	Input Resistance		134			M Ω
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 2.7\text{V}$	82			dB
PSRR	Power Supply Rejection Ratio	$\pm 1.35\text{V} \leq V^+ \leq \pm 12\text{V}$	80			dB
V_{CM}	Input Common-Mode Voltage Range			2.7 0	2.7 0	V
A_V	Large Signal Voltage Gain	$R_L = 10\text{k}$	100			V/mV
V_O	Output Swing	$R_L = 100\text{k}$	0.03	0.08 0.112	0.08 0.112	V max
			2.66	2.65 2.25	2.65 2.25	V min
I_S	Supply Current	Per Amplifier	330			μA

(1) Typical Values represent the most likely parametric normal.

(2) All limits are guaranteed by testing or statistical analysis.

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$ to $V^+/2$.

Symbol	Parameter	Conditions	Typ (1)	LM6134AI LM6132AI Limit (2)	LM6134BI LM6132BI Limit (2)	Units
GBW	Gain-Bandwidth Product	$R_L = 10\text{k}$, $f = 20\text{ kHz}$	7			MHz
θ_m	Phase Margin	$R_L = 10\text{k}$	23			deg
G_m	Gain Margin		12			dB

(1) Typical Values represent the most likely parametric normal.

(2) All limits are guaranteed by testing or statistical analysis.

24V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 24\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$ to $V^+/2$.

Boldface limits apply at the temperature extreme

Symbol	Parameter	Conditions	Typ (1)	LM6134AI LM6132AI Limit (2)	LM6134BI LM6132BI Limit (2)	Units
V_{OS}	Input Offset Voltage		1.7	3 5	7 9	mV max
I_B	Input Bias Current	$0\text{V} \leq V_{CM} \leq 24\text{V}$	125			nA
I_{OS}	Input Offset Current		4.8			nA
R_{IN}	Input Resistance		210			M Ω
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 24\text{V}$	80			dB
PSRR	Power Supply Rejection Ratio	$2.7\text{V} \leq V^+ \leq 24\text{V}$	82			dB
V_{CM}	Input Common-Mode Voltage Range		-0.25 24.25	0 24	0 24	V min V max
A_V	Large Signal Voltage Gain	$R_L = 10\text{k}$	102			V/mV
V_O	Output Swing	$R_L = 10\text{k}$	0.075 23.86	0.15 23.8	0.15 23.8	V max
						V min
I_S	Supply Current	Per Amplifier	390	450 490	450 490	μA max

(1) Typical Values represent the most likely parametric normal.

(2) All limits are guaranteed by testing or statistical analysis.

24V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 24\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$ to $V^+/2$.

Symbol	Parameter	Conditions	Typ (1)	LM6134AI LM6132AI Limit (2)	LM6134BI LM6132BI Limit (2)	Units
GBW	Gain-Bandwidth Product	$R_L = 10\text{k}$, $f = 20\text{ kHz}$	11			MHz
θ_m	Phase Margin	$R_L = 10\text{k}$	23			deg
G_m	Gain Margin	$R_L = 10\text{k}$	12			dB
THD + N	Total Harmonic Distortion and Noise	$A_V = +1$, $V_O = 20V_{P-P}$ $f = 10\text{ kHz}$	0.0015			%

(1) Typical Values represent the most likely parametric normal.

(2) All limits are guaranteed by testing or statistical analysis.

Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ unless otherwise specified

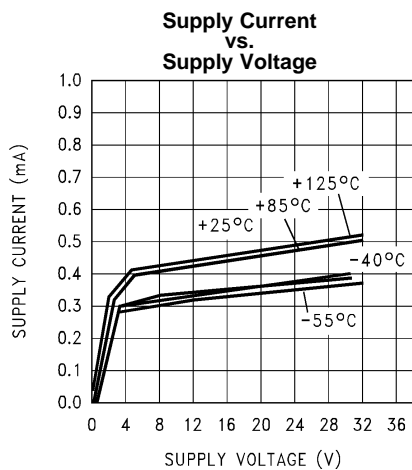


Figure 3.

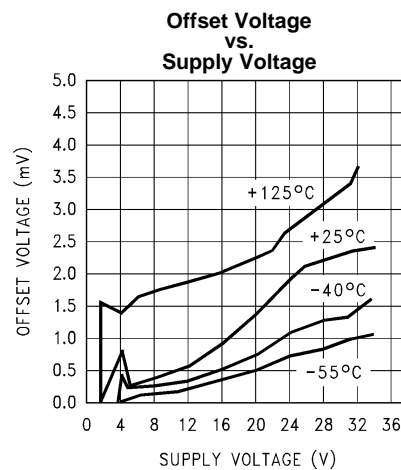


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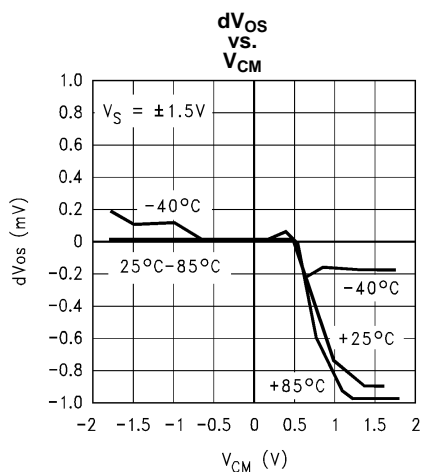


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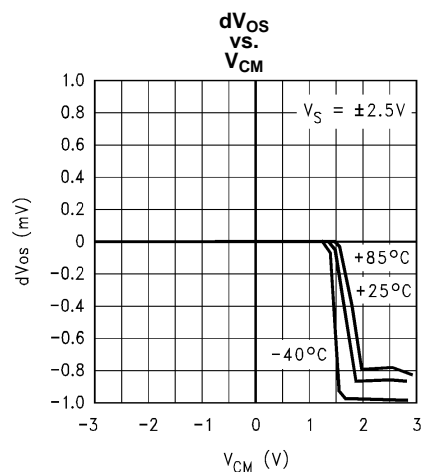


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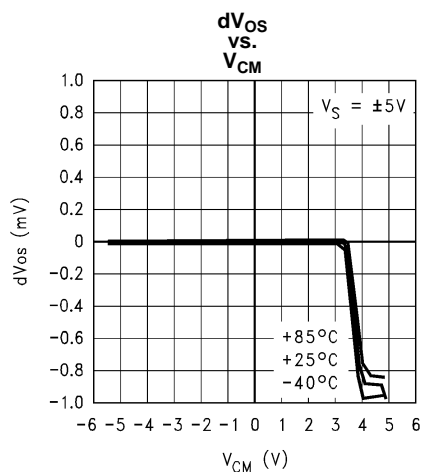


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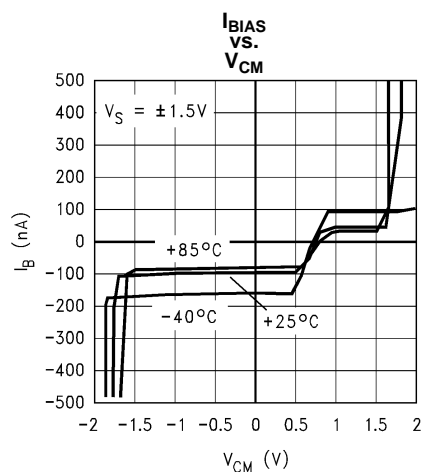


Figure 8.

Typical Performance Characteristics (continued)

$T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ unless otherwise specified

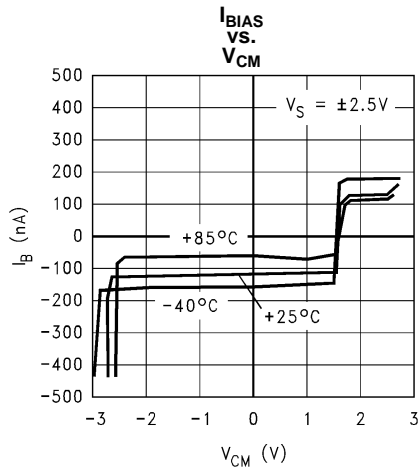


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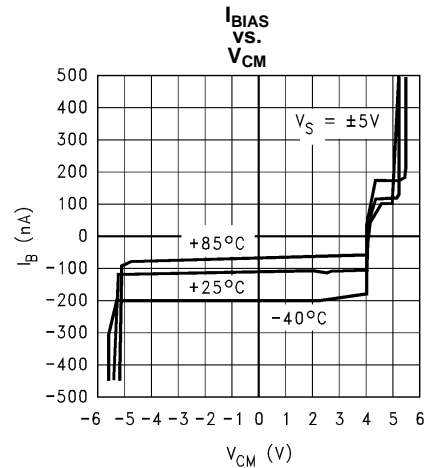


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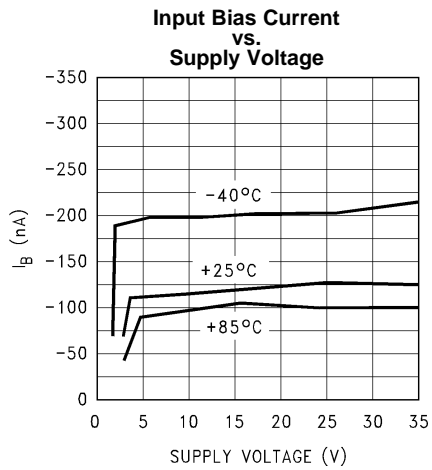


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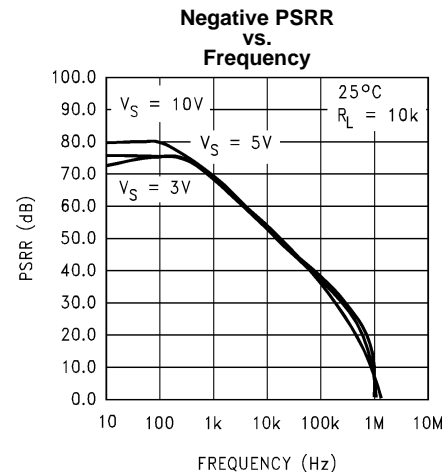


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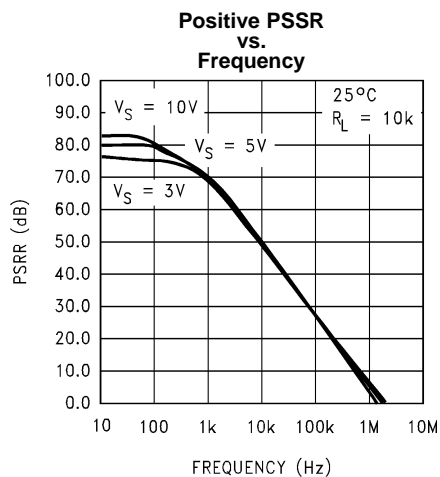


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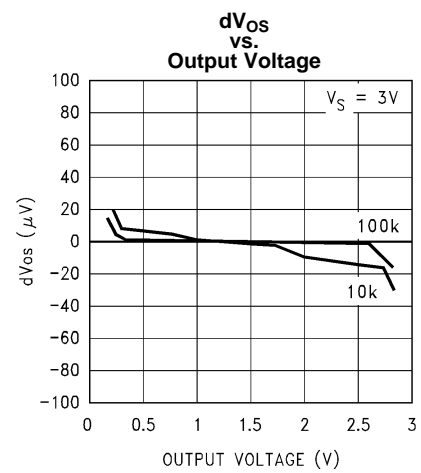


Figure 14.

Typical Performance Characteristics (continued)

$T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ unless otherwise specified

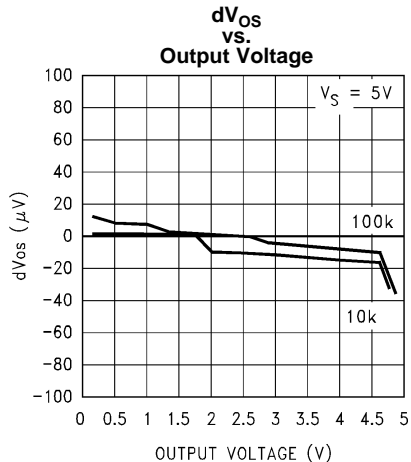


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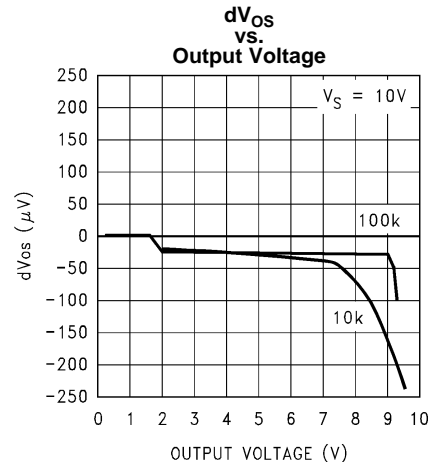


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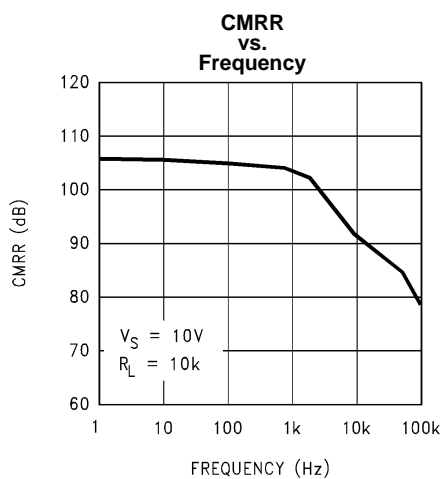


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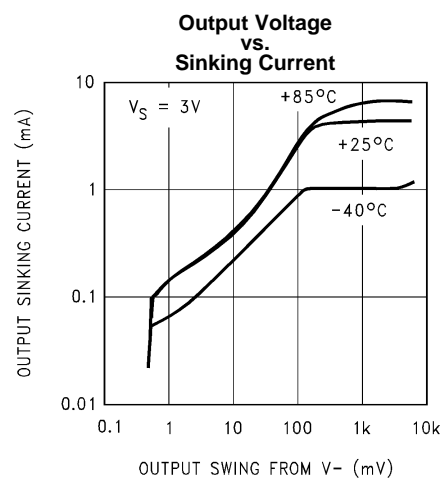


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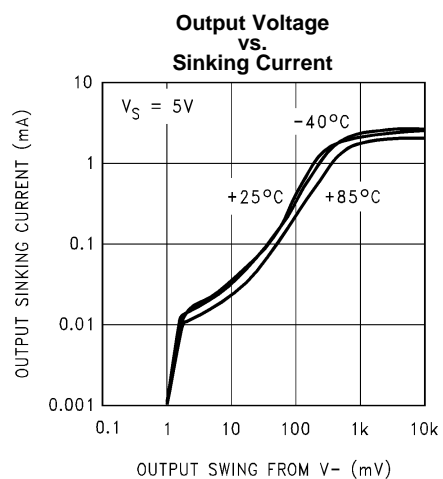


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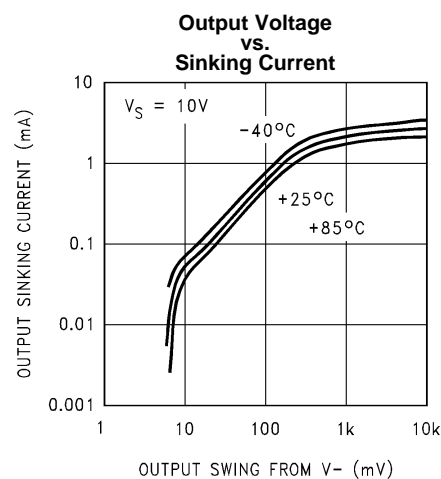


Figure 20.

Typical Performance Characteristics (continued)

$T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ unless otherwise specified

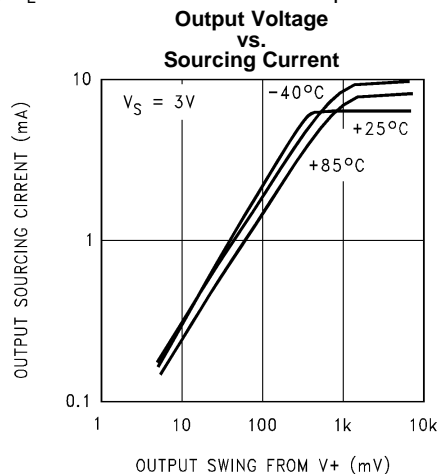


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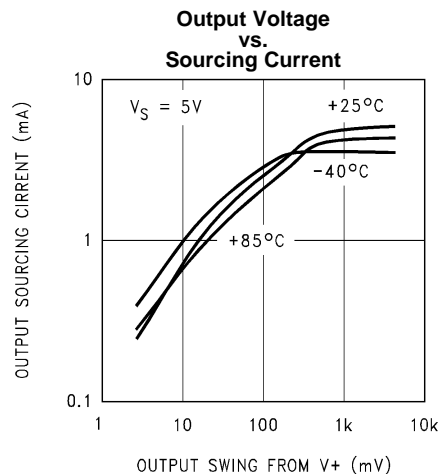


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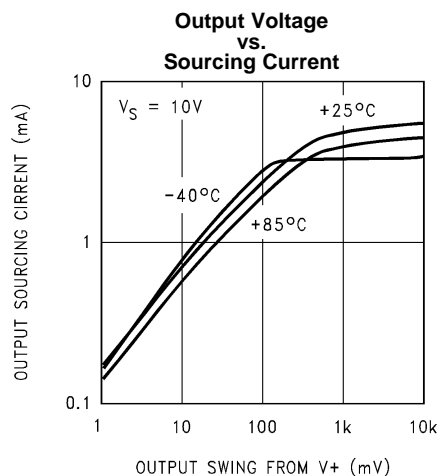


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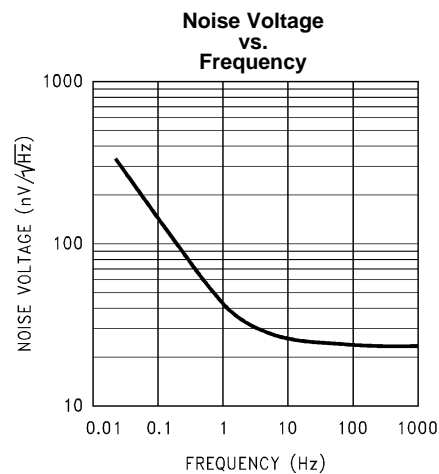


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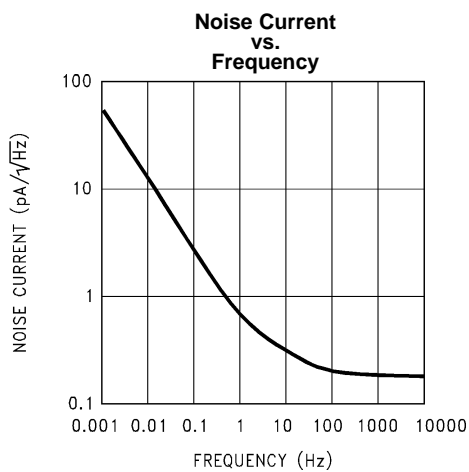


Figure 25.

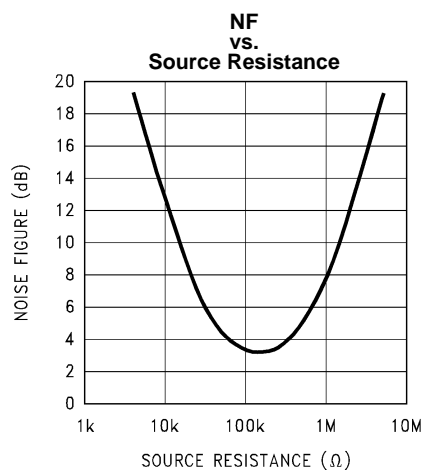
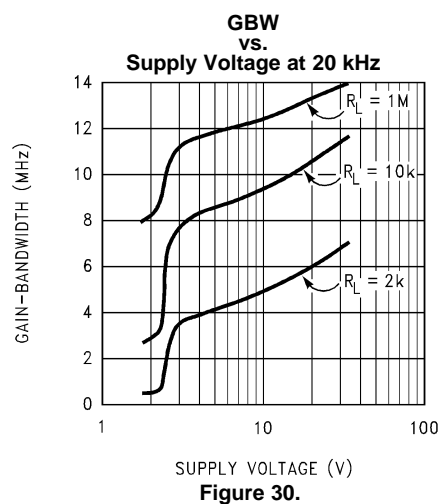
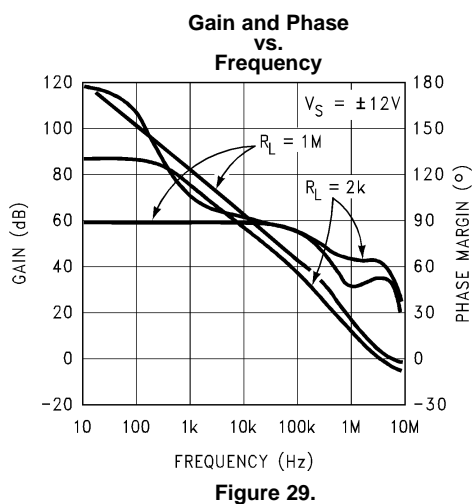
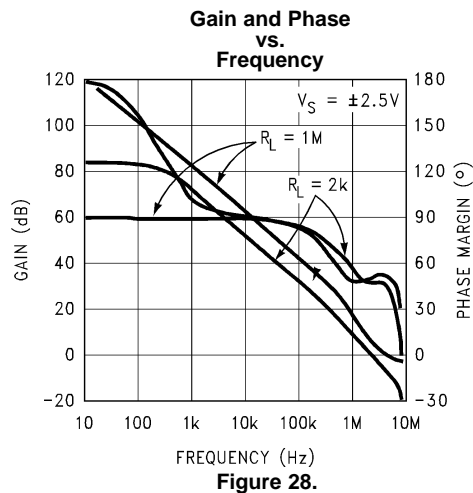
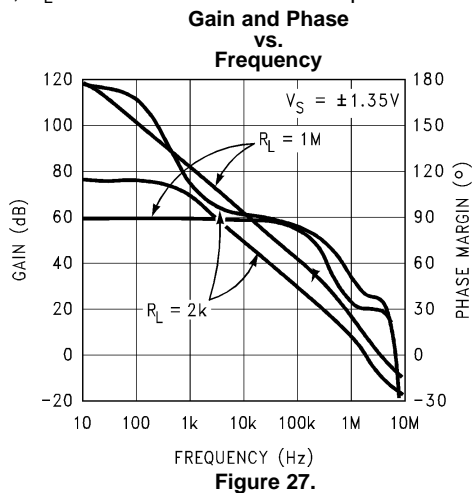


Figure 26.

Typical Performance Characteristics (continued)

$T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ unless otherwise specified



LM6132/34 APPLICATION INFORMATION

The LM6132 brings a new level of ease of use to op amp system design.

With greater than rail-to-rail input voltage range concern over exceeding the common-mode voltage range is eliminated.

Rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The high gain-bandwidth with low supply current opens new battery powered applications, where high power consumption, previously reduced battery life to unacceptable levels.

To take advantage of these features, some ideas should be kept in mind.

ENHANCED SLEW RATE

Unlike most bipolar op amps, the unique phase reversal prevention/speed-up circuit in the input stage eliminates phase reversal and allows the slew rate to be very much a function of the input signal amplitude.

Figure 32 shows how excess input signal is routed around the input collector-base junctions directly to the current mirrors.

The LM6132/34 input stage converts the input voltage change to a current change. This current change drives the current mirrors through the collectors of Q1–Q2, Q3–Q4 when the input levels are normal.

If the input signal exceeds the slew rate of the input stage and the differential input voltage rises above a diode drop, the excess signal bypasses the normal input transistors, (Q1–Q4), and is routed in correct phase through the two additional transistors, (Q5, Q6), directly into the current mirrors.

This rerouting of excess signal allows the slew-rate to increase by a factor of 10 to 1 or more. (See Figure 31).

As the overdrive increases, the op amp reacts better than a conventional op amp. Large fast pulses will raise the slew- rate to around 25V to 30 V/ μ s.

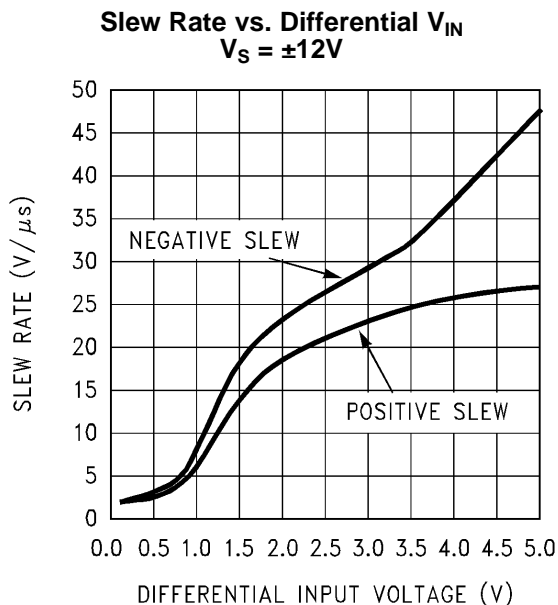


Figure 31.

This effect is most noticeable at higher supply voltages and lower gains where incoming signals are likely to be large.

This speed-up action adds stability to the system when driving large capacitive loads.

DRIVING CAPACITIVE LOADS

Capacitive loads decrease the phase margin of all op amps. This is caused by the output resistance of the amplifier and the load capacitance forming an R-C phase lag network. This can lead to overshoot, ringing and oscillation. Slew rate limiting can also cause additional lag. Most op amps with a fixed maximum slew-rate will lag further and further behind when driving capacitive loads even though the differential input voltage raises. With the LM6132, the lag causes the slew rate to raise. The increased slew-rate keeps the output following the input much better. This effectively reduces phase lag. After the output has caught up with the input, the differential input voltage drops down and the amplifier settles rapidly.

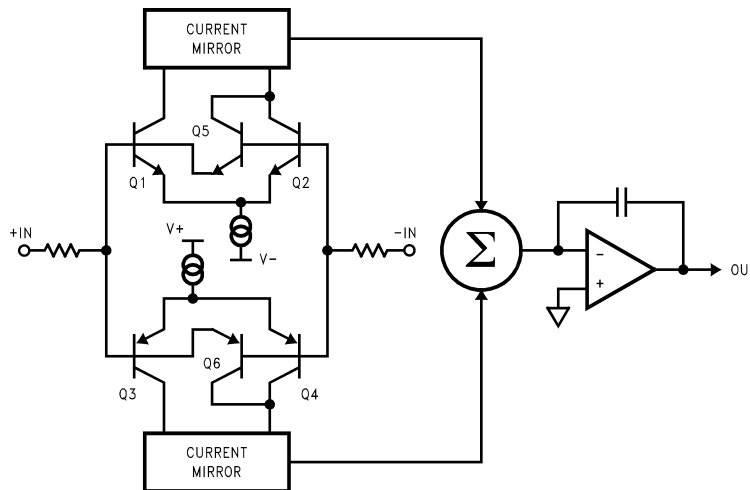


Figure 32.

These features allow the LM6132 to drive capacitive loads as large as 500 pF at unity gain and not oscillate. The scope photos (Figure 33 and Figure 34) above show the LM6132 driving a 500 pF load. In Figure 33, the lower trace is with no capacitive load and the upper trace is with a 500 pF load. Here we are operating on $\pm 12\text{V}$ supplies with a 20 V_{PP} pulse. Excellent response is obtained with a C_f of 39 pF. In Figure 34, the supplies have been reduced to $\pm 2.5\text{V}$, the pulse is 4 V_{PP} and C_F is 39 pF. The best value for the compensation capacitor should be established after the board layout is finished because the value is dependent on board stray capacity, the value of the feedback resistor, the closed loop gain and, to some extent, the supply voltage.

Another effect that is common to all op amps is the phase shift caused by the feedback resistor and the input capacitance. This phase shift also reduces phase margin. This effect is taken care of at the same time as the effect of the capacitive load when the capacitor is placed across the feedback resistor.

The circuit shown in Figure 35 was used for these scope photos.

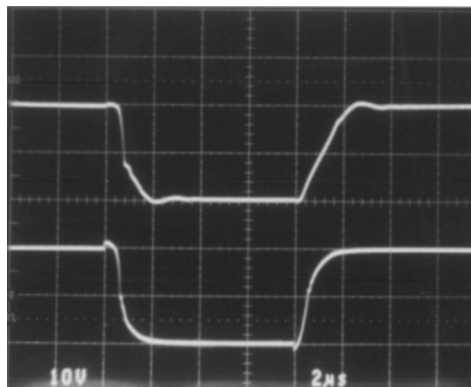


Figure 33.

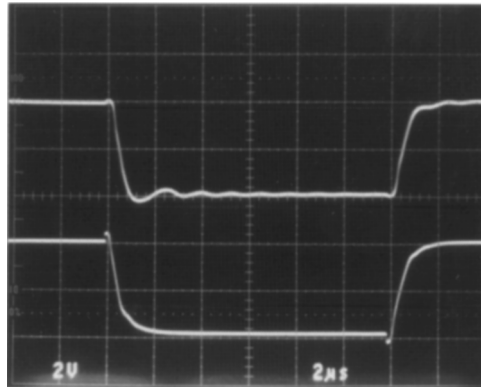


Figure 34.

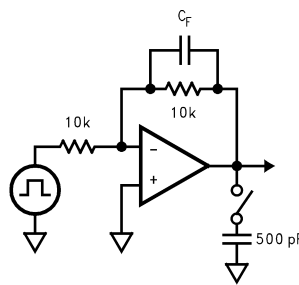


Figure 35.

Figure 36 shows a method for compensating for load capacitance (C_O) effects by adding both an isolation resistor R_O at the output and a feedback capacitor C_F directly between the output and the inverting input pin. Feedback capacitor C_F compensates for the pole introduced by R_O and C_O , minimizing ringing in the output waveform while the feedback resistor R_F compensates for dc inaccuracies introduced by R_O . Depending on the size of the load capacitance, the value of R_O is typically chosen to be between 100Ω to 1 kΩ.

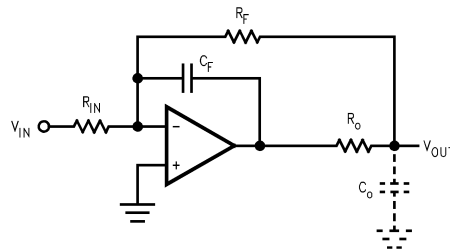


Figure 36.

Typical Applications

3 OP AMP INSTRUMENTATION AMP WITH RAIL-TO-RAIL INPUT AND OUTPUT

Using the LM6134, a 3 op amp instrumentation amplifier with rail-to-rail inputs and rail to rail output can be made. These features make these instrumentation amplifiers ideal for single supply systems.

Some manufacturers use a precision voltage divider array of 5 resistors to divide the common-mode voltage to get an input range of rail-to-rail or greater. The problem with this method is that it also divides the signal, so to even get unity gain, the amplifier must be run at high closed loop gains. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMR as well. Using the LM6134, all of these problems are eliminated.

In this example, amplifiers A and B act as buffers to the differential stage (Figure 37). These buffers assure that the input impedance is over 100 M Ω and they eliminate the requirement for precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMR set by the matching of R1–R2 with R3–R4.

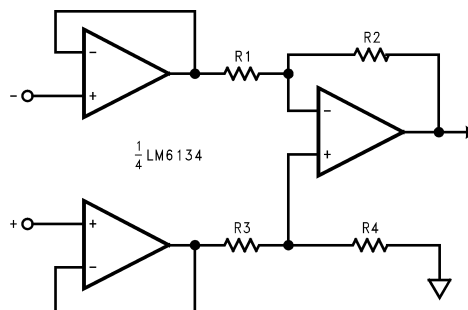


Figure 37.

FLAT PANEL DISPLAY BUFFERING

Three features of the LM6132/34 make it a superb choice for TFT LCD applications. First, its low current draw (360 μ A per amplifier @ 5V) makes it an ideal choice for battery powered applications such as in laptop computers. Second, since the device operates down to 2.7V, it is a natural choice for next generation 3V TFT panels. Last, but not least, the large capacitive drive capability of the LM6132 comes in very handy in driving highly capacitive loads that are characteristic of LCD display drivers.

The large capacitive drive capability of the LM6132/34 allows it to be used as buffers for the gamma correction reference voltage inputs of resistor-DAC type column (Source) drivers in TFT LCD panels. This amplifier is also useful for buffering only the center reference voltage input of Capacitor-DAC type column (Source) drivers such as the LMC750X series.

Since for VGA and SVGA displays, the buffered voltages must settle within approximately 4 μ s, the well known technique of using a small isolation resistor in series with the amplifier's output very effectively dampens the ringing at the output.

With its wide supply voltage range of 2.7V to 24V, the LM6132/34 can be used for a diverse range of applications. The system designer is thus able to choose a single device type that serves many sub-circuits in the system, eliminating the need to specify multiple devices in the bill of materials. Along with its sister parts, the LM6142 and LM6152 that have the same wide supply voltage capability, choice of the LM6132 in a design eliminates the need to search for multiple sources for new designs.

REVISION HISTORY

Changes from Revision C (February 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM6132AIM	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LM61 32AIM	Samples
LM6132AIM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM61 32AIM	Samples
LM6132AIMX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LM61 32AIM	Samples
LM6132AIMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM61 32AIM	Samples
LM6132BIM	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LM61 32BIM	Samples
LM6132BIM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM61 32BIM	Samples
LM6132BIMX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LM61 32BIM	Samples
LM6132BIMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM61 32BIM	Samples
LM6132BIN	ACTIVE	PDIP	P	8	40	TBD	Call TI	Call TI	-40 to 85	LM6132 BIN	Samples
LM6132BIN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	LM6132 BIN	Samples
LM6134AIM	ACTIVE	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85	LM6134AIM	Samples
LM6134AIM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM6134AIM	Samples
LM6134AIMX	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85	LM6134AIM	Samples
LM6134AIMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM6134AIM	Samples
LM6134BIM	ACTIVE	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85	LM6134BIM	Samples
LM6134BIM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM6134BIM	Samples
LM6134BIMX	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85	LM6134BIM	Samples
LM6134BIMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM6134BIM	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM6134BIN	ACTIVE	PDIP	NFF	14	25	TBD	Call TI	Call TI	-40 to 85	LM6134BIN	Samples
LM6134BIN/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 85	LM6134BIN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6132AIMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6132AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6132BIMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6132BIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6134AIMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM6134AIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM6134BIMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM6134BIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6132AIMX	SOIC	D	8	2500	367.0	367.0	35.0
LM6132AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM6132BIMX	SOIC	D	8	2500	367.0	367.0	35.0
LM6132BIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM6134AIMX	SOIC	D	14	2500	367.0	367.0	35.0
LM6134AIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LM6134BIMX	SOIC	D	14	2500	367.0	367.0	35.0
LM6134BIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

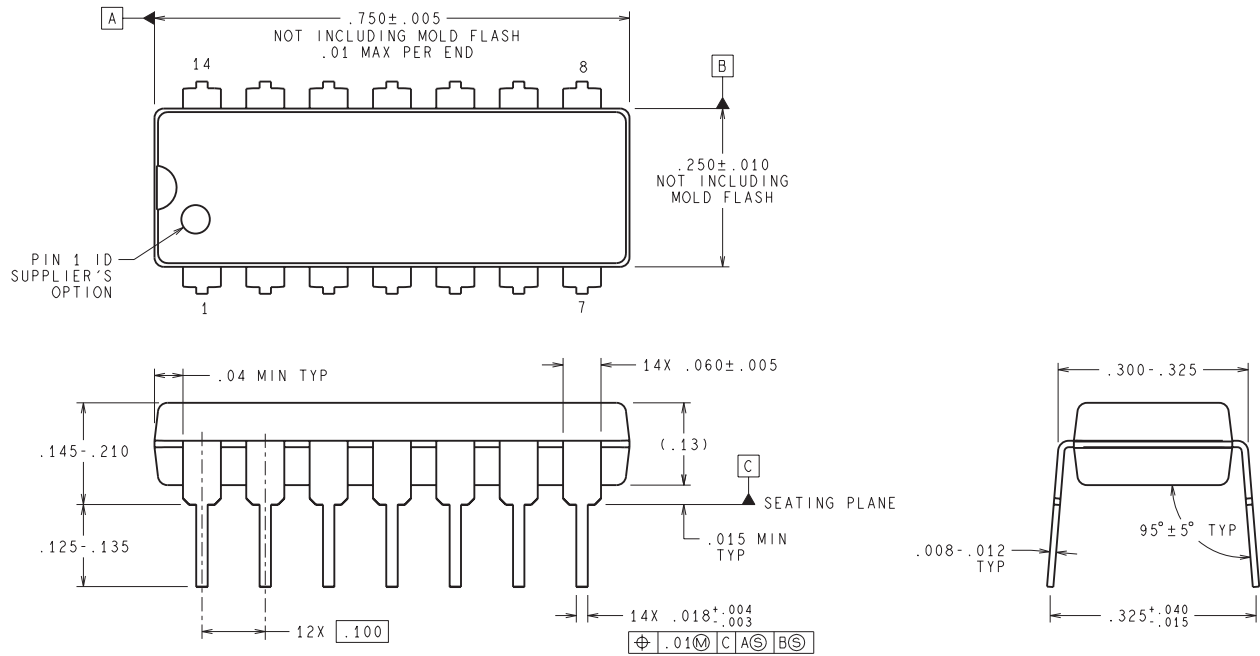
P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

NFF0014A



DIMENSIONS ARE IN INCHES
DIMENSIONS IN () FOR REFERENCE ONLY

N14A (Rev G)

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
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- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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