

16-BIT, 1.0 GSPS 2x-4x INTERPOLATING DIGITAL-TO-ANALOG CONVERTER (DAC)

Check for Samples: [DAC5681Z](#)

FEATURES

- **16-Bit Digital-to-Analog Converter (DAC)**
- **1.0 GSPS Update Rate**
- **16-Bit Wideband Input LVDS Data Bus**
 - **8 Sample Input FIFO**
- **High Performance**
 - **73 dBc ACLR WCDMA TM1 at 180 MHz**
- **2x-32x Clock Multiplying PLL/VCO**
- **2x or 4x Interpolation Filters**
 - **Stopband Transition 0.4–0.6 Fdata**
 - **Filters Configurable in Either Low-Pass or High-Pass Mode**
 - **Allows Selection of Higher Order Image**
- **On Chip 1.2 V Reference**
- **Differential Scalable Output: 2 to 20 mA**
- **Package: 64-Pin 9 × 9 mm QFN**

APPLICATIONS

- **Cellular Base Stations**
- **Broadband Wireless Access (BWA)**
- **WiMAX 802.16**
- **Fixed Wireless Backhaul**
- **Cable Modem Termination System (CMTS)**

DESCRIPTION

The DAC5681Z is a 16-bit 1.0 GSPS digital-to-analog converter (DAC) with wideband LVDS data input, integrated 2x/4x interpolation filters, on-board clock multiplier and internal voltage reference. The DAC5681Z offers superior linearity, noise, crosstalk and PLL phase noise performance.

The DAC5681Z integrates a wideband LVDS port with on-chip termination. Full-rate input data can be transferred to a single DAC channel, or half-rate and 1/4-rate input data can be interpolated by on-board 2x or 4x FIR filters. Each interpolation FIR is configurable in either Low-Pass or High-Pass mode, allowing selection of a higher order output spectral image. An on-chip delay lock loop (DLL) simplifies LVDS interfacing by providing skew control for the LVDS input data clock.

The DAC5681Z is characterized for operation over the industrial temperature range of –40°C to 85°C and is available in a 64-pin QFN package. Other members of the family include the dual-channel, interpolating DAC5682Z and the single-channel, non-interpolating DAC5681.

ORDERING INFORMATION

T _A	ORDER CODE	PACKAGE DRAWING/TYPE ⁽¹⁾ (2) (3)	TRANSPORT MEDIA	QUANTITY
–40°C to 85°C	DAC5681ZIRGCT	RGC / 64QFN Quad Flatpack No-Lead	Tape and Reel	250
	DAC5681ZIRGCR		Tape and Reel	2000

(1) Thermal Pad Size: 7,4 mm × 7,4 mm

(2) MSL Peak Temperature: Level-3-260C-168 HR

(3) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

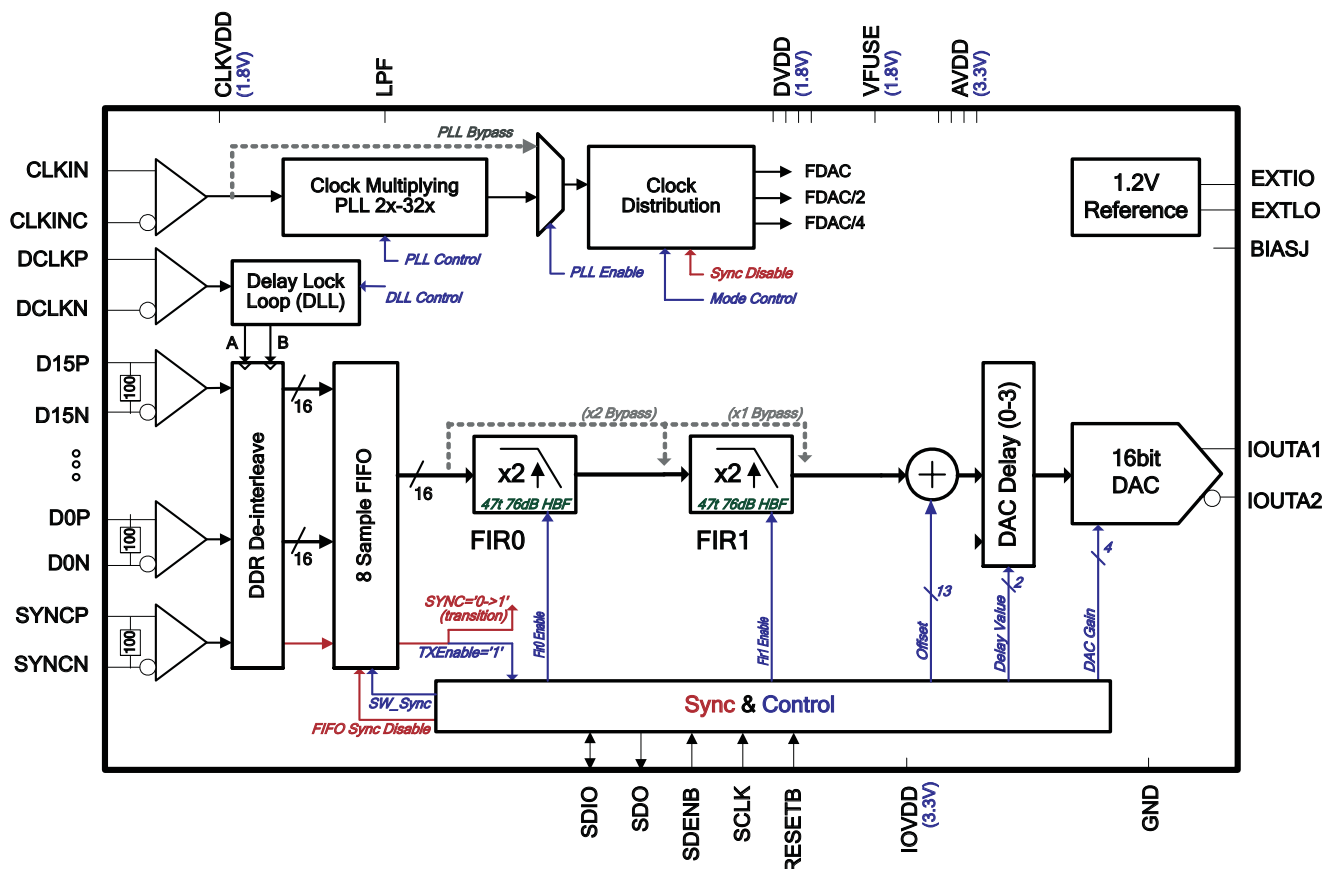


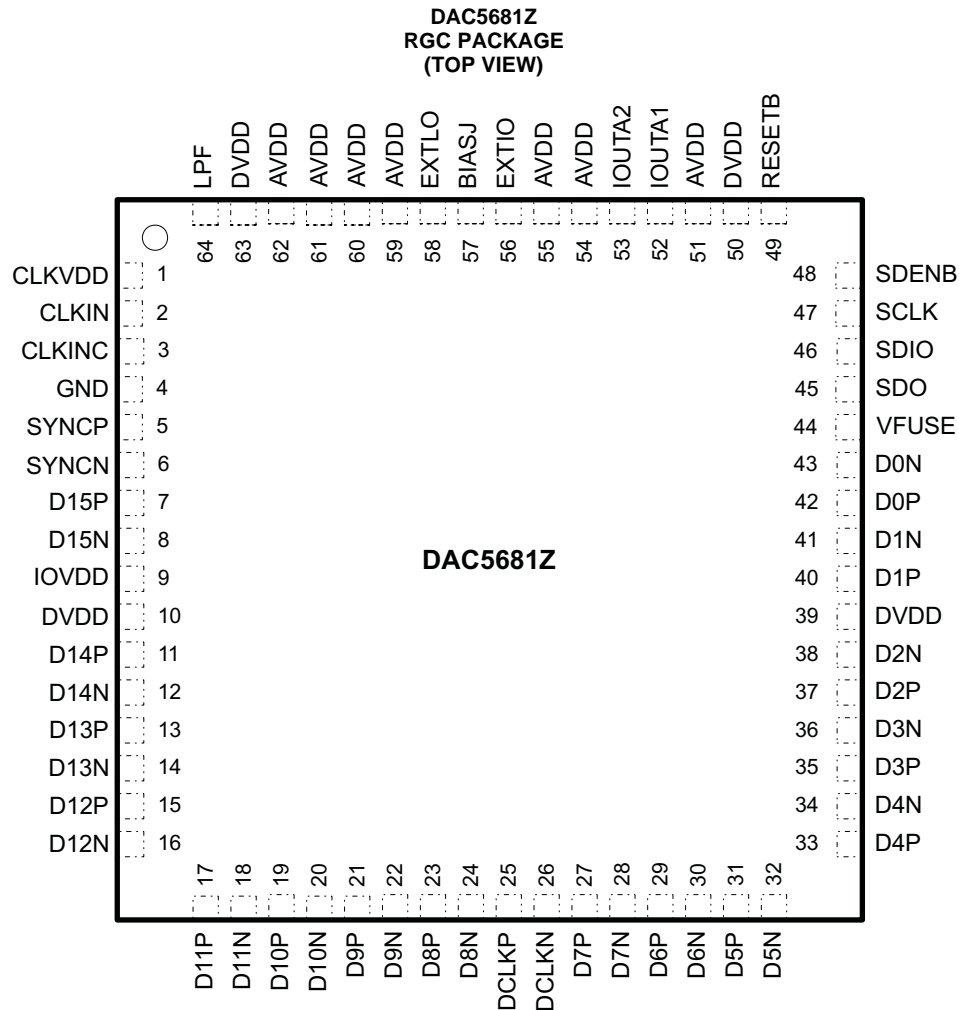
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM





TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AVDD	51, 54, 55, 59–62	I	Analog supply voltage. (3.3V)
BIASJ	57	O	Full-scale output current bias. For 20mA full-scale output current, connect a 960 Ω resistor to GND.
CLKIN	2	I	Positive external clock input with a self-bias of approximately CLKVDD/2. With the clock multiplier PLL enabled, CLKIN provides lower frequency reference clock. If the PLL is disabled, CLKIN directly provides clock for DAC up to 1GHz.
CLKINC	3	I	Complementary external clock input. (See the CLKIN description)
CLKVDD	1	I	Internal clock buffer supply voltage. (1.8 V)
D[15..0]P	7, 11, 13, 15, 17, 19, 21, 23, 27, 29, 31, 33, 35, 37, 40, 42	I	LVDS positive input data bits 0 through 15. Each positive/negative LVDS pair has an internal 100 Ω termination resistor. Order of bus can be reversed via rev_bus bit in CONFIG5 register. Data format relative to DCLKP/N clock is Double Data Rate (DDR) with two data samples input per DCLKP/N clock. In dual-channel mode, data for the A-channel is input while DCLKP is high. D15P is most significant data bit (MSB) – pin 7 D0P is least significant data bit (LSB) – pin 42
D[15..0]N	8, 12, 14, 16, 18, 20, 22, 24, 28, 30, 32, 34, 36, 38, 41, 43	I	LVDS negative input data bits 0 through 15. (See D[15:0]P description above) D15N is most significant data bit (MSB) – pin 8 D0N is least significant data bit (LSB) – pin 43

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DCLKP	25	I	LVDS positive input clock. Unlike the other LVDS inputs, the DCLKP/N pair is self-biased to approximately DVDD/2 and does not have an internal termination resistor in order to optimize operation of the DLL circuit. See the "DLL Operation" section. For proper external termination, connect a 100 Ω resistor across LVDS clock source lines followed by series 0.01 μ F capacitors connected to each of DCLKP and DCLKN pins (see Figure 26). For best performance, the resistor and capacitors should be placed as close as possible to these pins.
DCLKN	26	I	LVDS negative input clock. (See the DCLKP description)
DVDD	10, 39, 50, 63	I	Digital supply voltage. (1.8 V)
EXTIO	56	I/O	Used as external reference input when internal reference is disabled (i.e., EXTLO connected to AVDD). Used as 1.2V internal reference output when EXTLO = GND, requires a 0.1 μ F decoupling capacitor to AGND when used as reference output.
EXTLO	58	O	Connect to GND for internal reference, or AVDD for external reference.
GND	4, Thermal Pad	I	Pin 4 and the Thermal Pad located on the bottom of the QFN package is ground for AVDD, DVDD and IOVDD supplies.
IOUTA1	52	O	DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full scale current sink and the least positive voltage on the IOUTA1 pin. Similarly, a 0xFFFF data input results in a 0 mA current sink and the most positive voltage on the IOUTA1 pin.
IOUTA2	53	O	DAC complementary current output. The IOUTA2 has the opposite behavior of the IOUTA1 described above. An input data value of 0x0000 results in a 0mA sink and the most positive voltage on the IOUTA2 pin.
IOVDD	9	I	Digital I/O supply voltage (3.3V) for pins RESETB, SCLK, SDENB, SDIO, SDO.
LPF	64	I	PLL loop filter connection. If not using the clock multiplying PLL, the LPF pin may be left open. Set both PLL_bypass and PLL_sleep control bits for reduced power dissipation.
RESETB	49	I	Resets the chip when low. Internal pull-up.
SCLK	47	I	Serial interface clock. Internal pull-down.
SDENB	48	I	Active low serial data enable, always an input to the DAC5681Z. Internal pull-up.
SDIO	46	I/O	Bi-directional serial interface data in 3-pin mode (default). In 4-pin interface mode (CONFIG5 sif4), the SDIO pin is an input only. Internal pull-down.
SDO	45	O	Uni-directional serial interface data in 4-pin mode (CONFIG5 sif4). The SDO pin is in high-impedance state in 3-pin interface mode (default), but can optionally be used as a status output pin via CONFIG14 SDO_func_sel(2:0) . Internal pull-down.
SYNCP	5	I	LVDS SYNC positive input data. The SYNCP/N LVDS pair has an internal 100 Ω termination resistor. By default, the SYNCP/N input must be logic '1' to enable a DAC analog output . See the <i>LVDS SYNCP/N Operation</i> paragraph for a detailed description.
SYNCN	6	I	LVDS SYNC negative input data.
VFUSE	44	I	Digital supply voltage. (1.8V) Connect to DVDD pins for normal operation . This supply pin is also used for factory fuse programming.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		VALUE	UNIT
Supply voltage range	DVDD ⁽²⁾	–0.5 to 2.3	V
	VFUSE ⁽²⁾	–0.5 to 2.3	V
	CLKVDD ⁽²⁾	–0.5 to 2.3	V
	AVDD ⁽²⁾	–0.5 to 4	V
	IOVDD ⁽²⁾	–0.5 to 4	V
Terminal voltage range	AVDD to DVDD	–2 to 2.6	V
	CLKVDD to DVDD	–0.5 to 0.5	V
	IOVDD to AVDD	–0.5 to 0.5	V
	D[15..0]P ,D[15..0]N, SYNCN, SYNCN ⁽²⁾	–0.5 to DVDD + 0.5	V
	DCLKP, DCLKN ⁽²⁾	–0.3 to 2.1	V
	CLKIN, CLKINC ⁽²⁾	–0.5 to CLKVDD + 0.5	V
	SDO, SDIO, SCLK, SDENB, RESETB ⁽²⁾	–0.5 to IOVDD + 0.5	V
	IOUTA1, IOUTA2 ⁽²⁾	–0.5 to AVDD + 0.5	V
LPF, EXTIO, EXTLO, BIASJ ⁽²⁾		–0.5 to AVDD + 0.5	V
Peak input current (any input)		20	mA
Peak total input current (all inputs)		–30	mA
Operating free-air temperature range, T _A : DAC5681Z		–40 To 85	°C
Storage temperature range		–65 To 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Measured with respect to GND.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

THERMAL CONDUCTIVITY		64ld QFN	UNIT
T _J	Maximum junction temperature ⁽¹⁾ ⁽²⁾	125	°C
θ _{JA}	Theta junction-to-ambient (still air)	22	°C/W
	Theta junction-to-ambient (200 lfm)	15	
Ψ _{JT}	Psi junction-to-top of package	0.2	°C/W
θ _{JB}	Theta junction-to-board	3.5	°C/W

(1) Air flow or heat sinking reduces θ_{JA} and may be required for sustained operation at 85° under maximum operating conditions.

(2) It is strongly recommended to solder the device thermal pad to the board ground plane.

ELECTRICAL CHARACTERISTICS — DC SPECIFICATION

over operating free-air temperature range , AVDD = 3.3 V, CLKVDD = 1.8 V, IOVDD = 3.3 V, DVDD = 1.8 V, Iout_{FS} = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION			16			Bits
DC ACCURACY ⁽¹⁾						
INL	Integral nonlinearity	1 LSB = IOUTFS/2 ¹⁶	±4			LSB
DNL	Differential nonlinearity		±2			
ANALOG OUTPUT						
Coarse gain linearity			±0.04			LSB
Offset error		Mid code offset	0.01			%FSR
Gain error		With external reference	1			%FSR
Gain error		With internal reference	0.7			%FSR
	Minimum full scale output current ⁽²⁾		2			mA
	Maximum full scale output current ⁽²⁾		20			
Output Compliance range ⁽³⁾		IOUTFS = 20 mA	AVDD –0.5V		AVDD + 0.5V	V
Output resistance			300			kΩ
Output capacitance			5			pF
REFERENCE OUTPUT						
V _{ref}	Reference voltage		1.14	1.2	1.26	V
Reference output current ⁽⁴⁾			100			nA
REFERENCE INPUT						
V _{EXTIO}	Input voltage range		0.1		1.25	V
Input resistance			1			MΩ
Small signal bandwidth		CONFIG6: BiasLPF_A = 0	95			kHz
		CONFIG6: BiasLPF_A = 1	472			
Input capacitance			100			pF
TEMPERATURE COEFFICIENTS						
Offset drift			±1			ppm of FSR/°C
Gain drift		With external reference	±15			ppm of FSR/°C
		With internal reference	±30			
Reference voltage drift			±8			ppm/°C
POWER SUPPLY						
Analog supply voltage, AVDD			3.0	3.3	3.6	V
Digital supply voltage, DVDD			1.7	1.8	1.9	V
Clock supply voltage, CLKVDD			1.7	1.8	1.9	V
I/O supply voltage, IOVDD			3.0	3.3	3.6	V
I _(AVDD)	Analog supply current	Mode 4 (below)	68			mA
I _(DVDD)	Digital supply current		271			mA
I _(CLKVDD)	Clock supply current		41			mA
I _(IOVDD)	IO supply current		13			mA

(1) Measured differential across IOUTA1 and IOUTA2 with 25 Ω each to AVDD.

(2) Nominal full-scale current, IoutFS, equals 16 × IBIAS current.

(3) The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5681Z device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.

(4) Use an external buffer amplifier with high impedance input to drive any external load.

ELECTRICAL CHARACTERISTICS — DC SPECIFICATION (continued)

over operating free-air temperature range , AVDD = 3.3 V, CLKVDD = 1.8 V, IOVDD = 3.3 V, DVDD = 1.8 V, Iout_{FS} = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _(AVDD)	Sleep mode, AVDD supply current	Mode 6 (below)		1		mA
I _(DVDD)	Sleep mode, DVDD supply current			4		mA
I _(CLKVDD)	Sleep mode, CLKVDD supply current			2		mA
I _(IOVDD)	Sleep mode, IOVDD supply current			2		mA
P	AVDD + IOVDD current, 3.3V	Mode 1: 1X2, PLL = OFF, CLKIN = 983.04 MHz FDAC = 983.04MHz, IF = 184.32 MHz 4 carrier WCDMA		71		mA
	DVDD + CLKVDD current, 1.8V			267		mA
	Power Dissipation			715		mW
	AVDD + IOVDD current, 3.3V	Mode 2: 1X2, PLL = ON (8X), CLKIN = 122.88 MHz FDAC = 983.04MHz, IF = 184.32 MHz 4 carrier WCDMA		81		mA
	DVDD + CLKVDD current, 1.8V			292		mA
	Power Dissipation			790		mW
	AVDD + IOVDD current, 3.3V	Mode 3: 1X4, HP/HP, PLL = OFF, CLKIN = 983.04 MHz, FDAC = 983.04MHz, IF = 215.04 MHz 4 carrier WCDMA		71		mA
	DVDD + CLKVDD current, 1.8V			278		mA
	Power Dissipation			735		mW
	AVDD + IOVDD current, 3.3V	Mode 4: 1X4, HP/HP, PLL = ON (8X), CLKIN = 122.88 MHz FDAC = 983.04MHz, IF = 215.04 MHz DACA on, 4 carrier WCDMA		81		mA
	DVDD + CLKVDD current, 1.8V			312		mA
	Power Dissipation			830	910	mW
	AVDD + IOVDD current, 3.3V	Mode 5: PLL = OFF, CLKIN = 983.04 MHz, FDAC = 983.04MHz, Digital Logic Disabled, DAC on SLEEP, Static Data Pattern		3		mA
	DVDD + CLKVDD current, 1.8V			117		mA
	Power Dissipation			220		mW
	AVDD + IOVDD current, 3.3V	Mode 6: PLL = OFF, CLKIN = OFF FDAC = OFF, Digital Logic Disabled DAC on SLEEP, Static Data Pattern		3		mA
	DVDD + CLKVDD current, 1.8V			6		mA
	Power Dissipation			20	30	mW
PSRR	Power supply rejection ratio	DC tested	–0.2		0.2	%FSR/V
T	Operating range		–40		85	°C
ANALOG OUTPUT						
f _{CLK}	Maximum output update rate		1000			MSPS
t _{s(DAC)}	Output settling time to 0.1%	Transition: Code 0x0000 to 0xFFFF		10.4		ns
t _{pd}	Output propagation delay	DAC output is updated on falling edge of DAC clock. Does not include Digital Latency (see below).		2.5		ns
t _{r(IOUT)}	Output rise time 10% to 90%			220		ps
t _{f(IOUT)}	Output fall time 90% to 10%			220		ps
Digital Latency		No interpolation, PLL Off		76		DAC clock cycles
		x2 interpolation, PLL Off		158		
		x4 interpolation, PLL Off		289		
Power-up Time	DAC Wake-up Time	IOUT current settling to 1% of IOUT _{FS} . Measured from SDENB; Register 0x06, toggle Bit 4 from 1 to 0.		80		μs
	DAC Sleep Time	IOUT current settling to less than 1% of IOUT _{FS} . Measured from SDENB; Register 0x06, toggle Bit 4 from 0 to 1.		80		μs

ELECTRICAL CHARACTERISTICS — AC SPECIFICATION⁽¹⁾

Over recommended operating free-air temperature range, AVDD, IOVDD = 3.3 V, CLKVDD, DVDD = 1.8 V, IOUT_{FS} = 20 mA, 4:1 transformer output termination, 50Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SFDR	Spurious free dynamic range	1X1, PLL off, CLKIN = 500 MHz, IF = 5.1 MHz, First Nyquist Zone < f _{DATA} /2		81		dBc
		1X2, PLL off, CLKIN = 1000 MHz, IF = 5.1 MHz, First Nyquist Zone < f _{DATA} /2		80		
		1X2, PLL off, CLKIN = 1000 MHz, IF = 20.1 MHz, First Nyquist Zone < f _{DATA} /2		77		
SNR	Signal-to-noise ratio	1X2, PLL off, CLKIN = 500 MHz, Single tone, 0 dBFS, IF = 20.1 MHz		75		dBc
		1X2, PLL off, CLKIN = 1000 MHz, Single tone, 0 dBFS, IF = 20.1 MHz		70		
		1X2, PLL off, CLKIN = 1000 MHz, Single tone, 0 dBFS, IF = 70.1 MHz		66		
		1X4, PLL off, CLKIN = 1000 MHz, Single tone, 0 dBFS, IF = 180 MHz		60		
		1X2, PLL off, CLKIN = 1000 MHz, Single tone, 0 dBFS, IF = 300.2 MHz		60		
		1X2, PLL off, CLKIN = 1000 MHz, Four tone, each -12 dBFS, IF = 24.7, 24.9, 25.1 and 25.3 MHz		73		
IMD3	Third-order two-tone intermodulation (each tone at -6 dBFS)	1X2, PLL off, CLKIN = 1000 MHz, IF = 20.1 and 21.1 MHz		88		dBc
		1X2, PLL off, CLKIN = 1000 MHz, IF = 70.1 and 71.1 MHz		75		
		1X2, PLL off, CLKIN = 1000 MHz, IF = 150.1 and 151.1 MHz		67		
IMD	Four-tone intermodulation (each tone at -12 dBFS)	1X2, PLL off, CLKIN = 1000 MHz, IF = 298.4, 299.2, 300.8 and 301.6 MHz		64		dBc
ACLR ⁽²⁾	Adjacent channel leakage ratio	Single carrier, baseband, 1X2, PLL off, CLKIN = 983.04 MHz	80	83		dBc
		Single carrier, IF = 180 MHz, 1X2, PLL off, CLKIN = 983.04 MHz		73		
		Four carrier, IF = 180 MHz, 1X2, PLL off, CLKIN = 983.04 MHz		68		
		Four carrier, IF = 275 MHz, 1X2, PLL off, CLKIN = 983.04 MHz		66		
	Noise floor ⁽³⁾	50-MHz offset, 1-MHz BW, Single Carrier, baseband, 1X2, PLL off, CLKIN = 983.04		93		dBc
		50-MHz offset, 1-MHz BW, Four Carrier, baseband, 1X2, PLL off, CLKIN = 983.04		85		

(1) Measured single-ended into 50 Ω load.

(2) W-CDMA with 3.84 MHz BW, 5-MHz spacing, centered at IF. TESTMODEL 1, 10 ms

(3) Carrier power measured in 3.84 MHz BW.

ELECTRICAL CHARACTERISTICS (DIGITAL SPECIFICATIONS)

over recommended operating free-air temperature range, AVDD, IOVDD = 3.3V, CLKVDD, DVDD = 1.8V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVDS INTERFACE: D[15:0]P/N, SYNC/N, DCLKP/N ⁽¹⁾							
V _{A,B+}	Logic high differential input voltage threshold			175			mV
V _{A,B-}	Logic low differential input voltage threshold			-175			mV
V _{COM1}	Input Common Mode	SYNCP/N, D[15:0]P/N only		1.0			V
V _{COM2}	Input Common Mode	DCLKP/N only		DVDD ÷2			V
Z _T	Internal termination	SYNCP/N, D[15:0]P/N only		85	110	135	Ω
C _L	LVDS Input capacitance			2			pF
t _S , t _H	DCLK to Data	DCLKP/N: 0 to 125MHz (see Figure 32) DLL Disabled, CONFIG5 DLL_bypass = 1, CONFIG10 = '00000000'	Setup_min	1100			ps
			Hold_min	-600			
t _{SKEW(A)} , t _{SKEW(B)}	DCLK to Data Skew ⁽²⁾	DLL Enabled, CONFIG5 DLL_bypass = 0, DDR format	DCLKP/N = 150 MHz	Positive	1000		ps
				Negative	-1800		
			DCLKP/N = 200 MHz	Positive	800		
				Negative	-1300		
			DCLKP/N = 250 MHz	Positive	600		
				Negative	-1000		
			DCLKP/N = 300 MHz	Positive	450		
				Negative	-800		
			DCLKP/N = 350 MHz	Positive	400		
				Negative	-700		
			DCLKP/N = 400 MHz	Positive	300		
				Negative	-600		
			DCLKP/N = 450 MHz	Positive	300		
				Negative	-500		
			DCLKP/N = 500 MHz	Positive	350		
				Negative	-300		
f _{DATA}	Input data rate supported	DLL Disabled, CONFIG5 DLL_bypass = 1, DDR format, DCLKP frequency: <125 MHz		250		MSPS	
		DLL Enabled, CONFIG5 DLL_bypass = 0, DDR format, DCLKP frequency: 125 to 500 MHz		250	1000		
DLL Operating Frequency (DCLKP/N Frequency)	DLL Enabled, CONFIG5 DLL_bypass = 0, DDR format	CONFIG10 = '11001101' = 0xCD	125-150		MHz		
		CONFIG10 = '11001110' = 0xCE	150-175				
		CONFIG10 = '11001111' = 0xCF	175-200				
		CONFIG10 = '11001000' = 0xC8	200-325				
		CONFIG10 = '11000000' = 0xC0	325-500				

(1) See LVDS INPUTS section for terminology.

(2) Positive skew: Clock ahead of data.

Negative skew: Data ahead of clock.

ELECTRICAL CHARACTERISTICS (DIGITAL SPECIFICATIONS) (continued)

over recommended operating free-air temperature range, AVDD, IOVDD = 3.3V, CLKVDD, DVDD = 1.8V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS INTERFACE: SDO, SDIO, SCLK, SDENB, RESETB						
V _{IH}	High-level input voltage		2	3		V
V _{IL}	Low-level input voltage		0	0	0.8	V
I _{IH}	High-level input current			±20		µA
I _{IL}	Low-level input current			±20		µA
CI	CMOS Input capacitance			5		pF
V _{OH}	SDO, SDIO	I _{load} = -100 µA	IOVDD -0.2			V
		I _{load} = -2mA	0.8 x IOVDD			V
V _{OL}	SDO, SDIO	I _{load} = 100 µA			0.2	V
		I _{load} = 2 mA			0.5	V
t _{s(SDENB)}	Setup time, SDENB to rising edge of SCLK		20			ns
t _{s(SDIO)}	Setup time, SDIO valid to rising edge of SCLK		10			ns
t _{h(SDIO)}	Hold time, SDIO valid to rising edge of SCLK		5			ns
t _(SCLK)	Period of SCLK		100			ns
t _(SCLKH)	High time of SCLK		40			ns
t _(SCLKL)	Low time of SCLK		40			ns
t _{d(Data)}	Data output delay after falling edge of SCLK			10		ns
t _{RESET}	Minimum RESETB pulse width			25		ns
CLOCK INPUT (CLKIN/CLKINC)						
	Duty cycle			50%		
	Differential voltage ⁽³⁾		0.4	1		V
	CLKIN/CLKINC input common mode			CLKVDD ÷2		V

(3) Driving the clock input with a differential voltage lower than 1V will result in degraded performance.

ELECTRICAL CHARACTERISTICS (DIGITAL SPECIFICATIONS) (continued)

over recommended operating free-air temperature range, AVDD, IOVDD = 3.3V, CLKVDD, DVDD = 1.8V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PHASE LOCKED LOOP					
Phase noise	DAC output at 600 kHz offset, 100 MHz, 0-dBFS tone, 1X4, f _{DATA} = 250 MSPS, CLKIN/C = 250 MHz, PLL_m = '00111', PLL_n = '001', VCO_div2 = 0, PLL_range = '1111', PLL_gain = '00'		-125		dBc/ Hz
	DAC output at 6 MHz offset, 100 MHz, 0-dBFS tone, 1X4, f _{DATA} = 250 MSPS, CLKIN/C = 250 MHz, PLL_m = '00111', PLL_n = '001', VCO_div2 = 0, PLL_range = '1111', PLL_gain = '00'		-146		
PLL/VCO Operating Frequency, Typical VCO Gain	PLL_gain = '00', PLL_range = '0000' (0)	160		290	MHz
			220		MHz/V
	PLL_gain = '01', PLL_range = '0001' (1)	290		460	MHz
			300		MHz/V
	PLL_gain = '01', PLL_range = '0010' (2)	400		520	MHz
			260		MHz/V
	PLL_gain = '01', PLL_range = '0011' (3)	480		570	MHz
			240		MHz/V
	PLL_gain = '01', PLL_range = '0100' (4)	560		620	MHz
			210		MHz/V
	PLL_gain = '10', PLL_range = '0101' (5)	620		740	MHz
			270		MHz/V
	PLL_gain = '10', PLL_range = '0110' (6)	690		780	MHz
			250		MHz/V
	PLL_gain = '10', PLL_range = '0111' (7)	740		820	MHz
			240		MHz/V
	PLL_gain = '10', PLL_range = '1000' (8)	790		850	MHz
			220		MHz/V
	PLL_gain = '10', PLL_range = '1001' (9)	840		880	MHz
			210		MHz/V
	PLL_gain = '11', PLL_range = '1010' (A)	880		940	MHz
			250		MHz/V
	PLL_gain = '11', PLL_range = '1011' (B)	920		990	MHz
			230		MHz/V
	PLL_gain = '11', PLL_range = '1100' (C)	960		1000	MHz
			220		MHz/V
PFD Maximum Frequency			160		MHz

TYPICAL CHARACTERISTICS

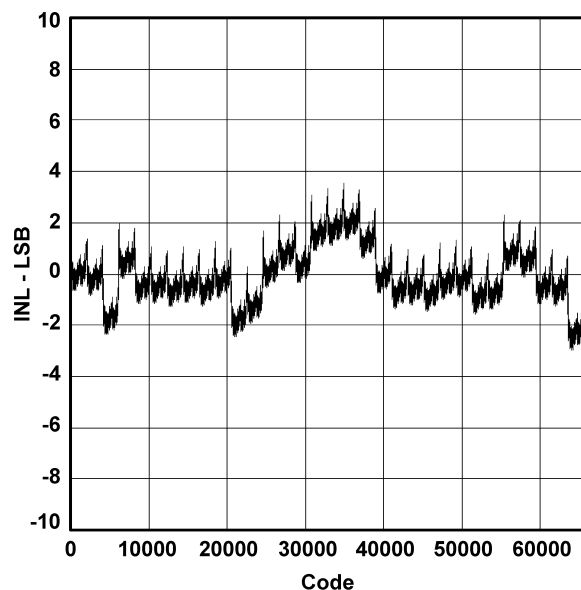


Figure 1. Integral Nonlinearity

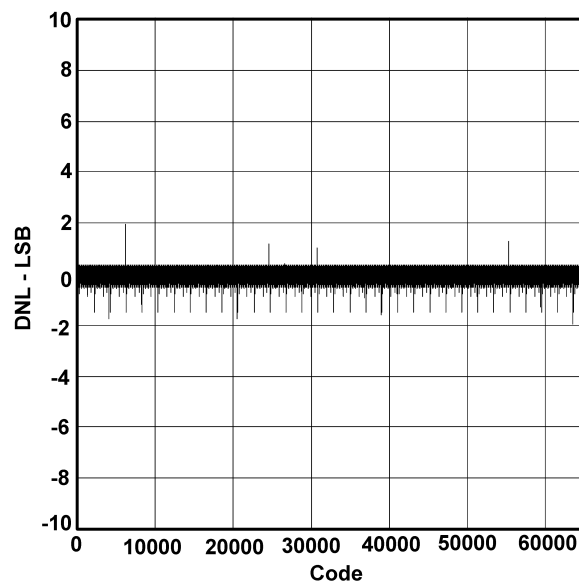


Figure 2. Differential Nonlinearity

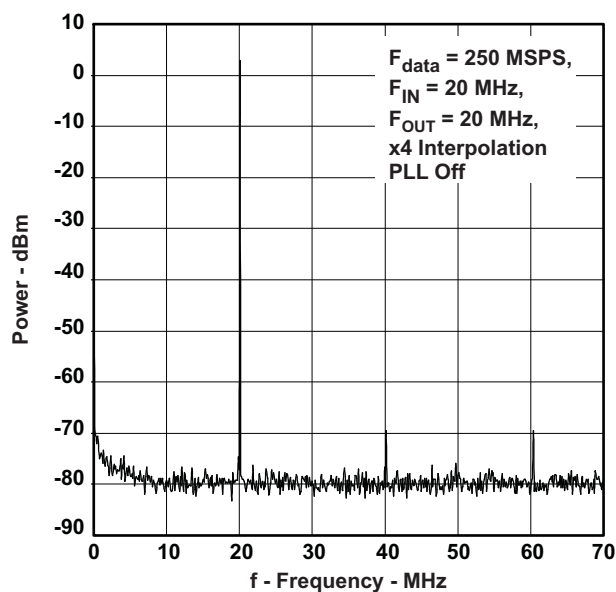


Figure 3. Single-Tone Spectral Plot

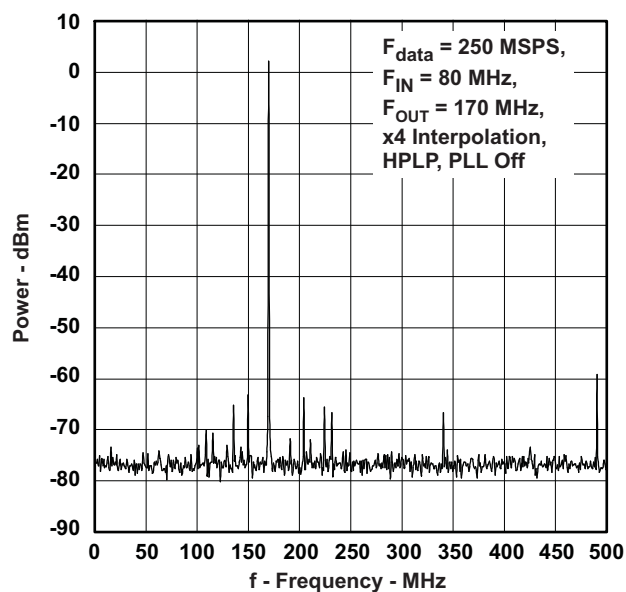


Figure 4. Single-Tone Spectral Plot

TYPICAL CHARACTERISTICS (continued)

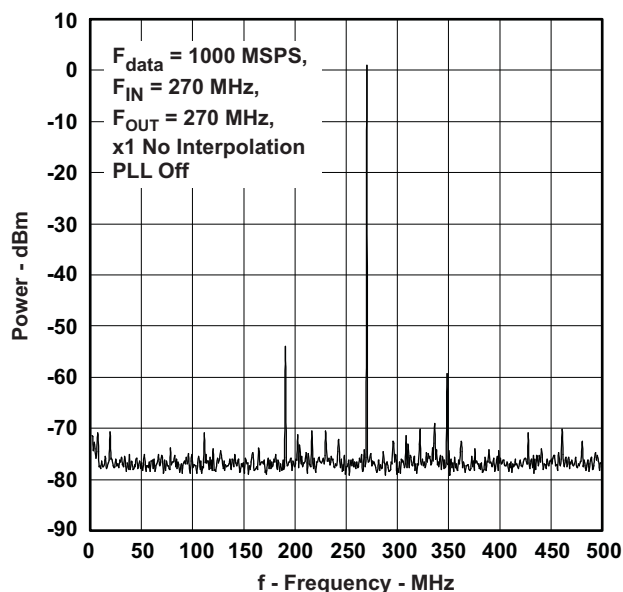


Figure 5. Single-Tone Spectral Plot

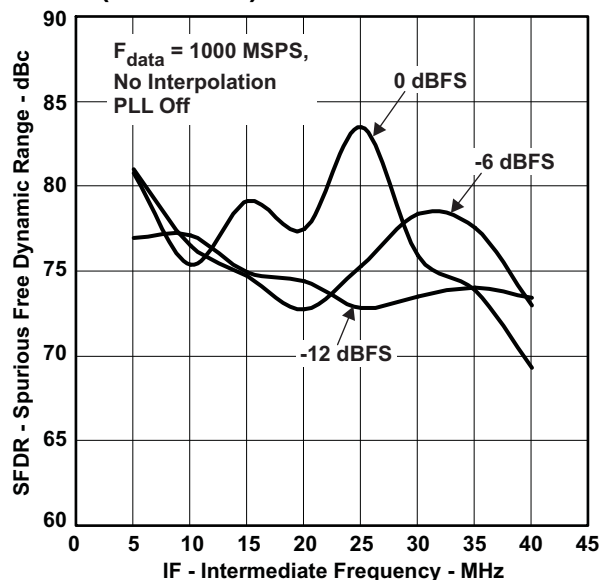


Figure 6. In-Band SFDR vs IF

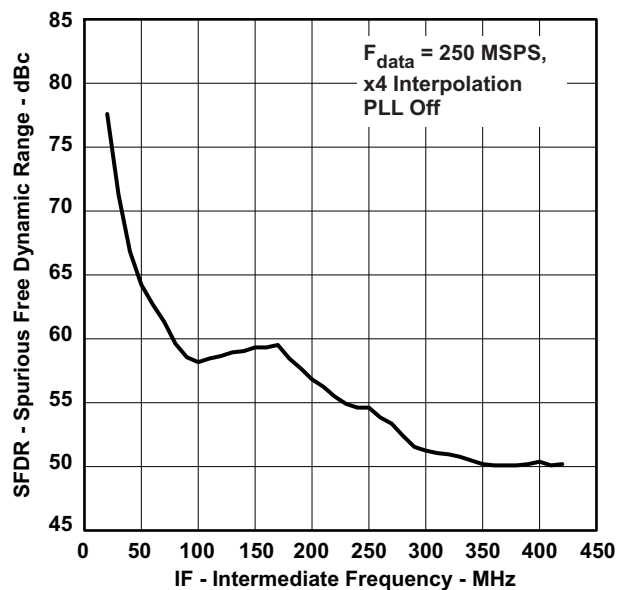


Figure 7. Out-Of-Band SFDR vs IF

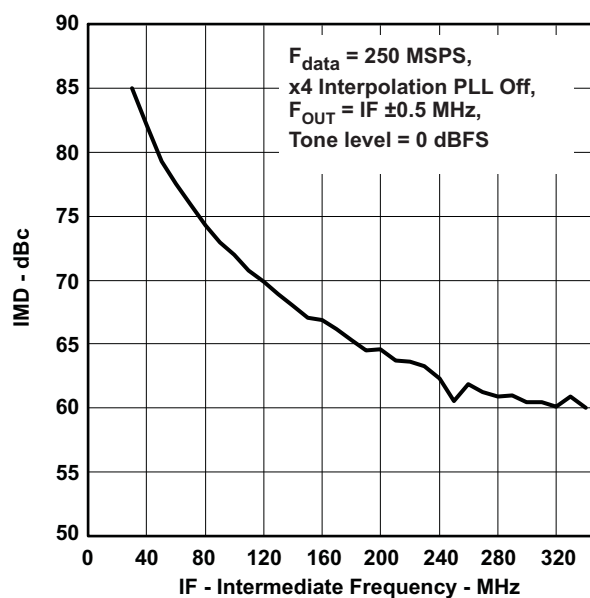


Figure 8. Two Tone IMD vs Output Frequency

TYPICAL CHARACTERISTICS (continued)

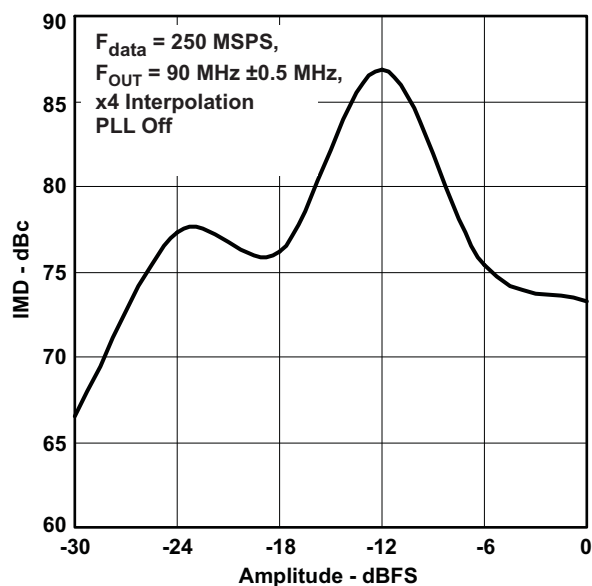


Figure 9. Two Tone IMD vs Amplitude

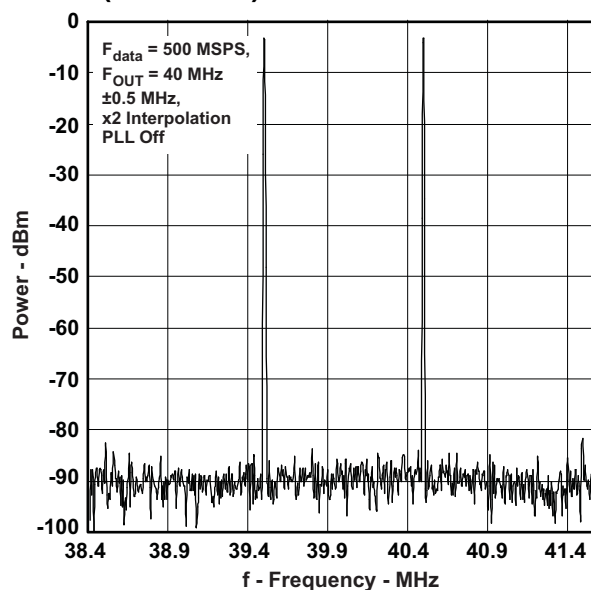


Figure 10. Two-Tone IMD Spectral Plot

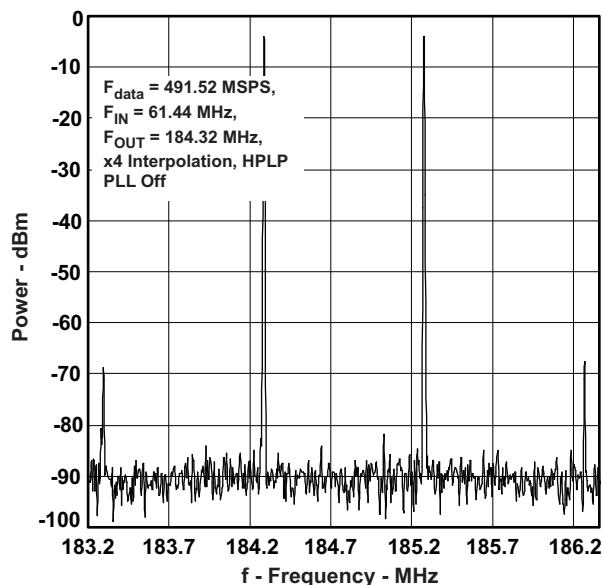


Figure 11. Two-Tone IMD Spectral Plot

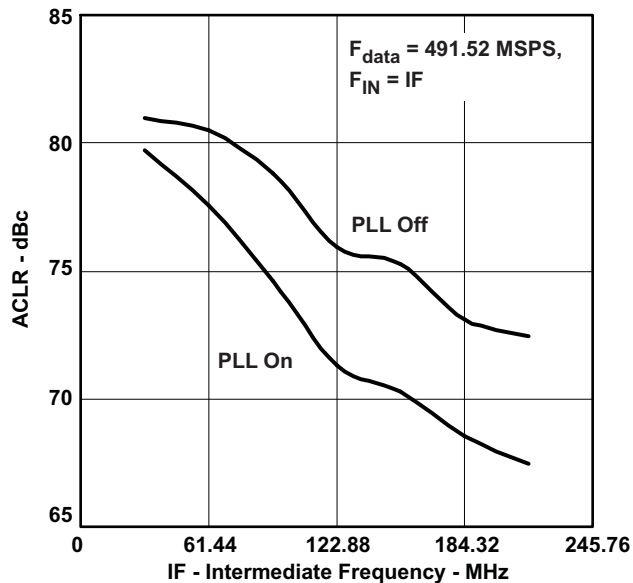


Figure 12. Single Carrier W-CDMA Test Model 1

TYPICAL CHARACTERISTICS (continued)

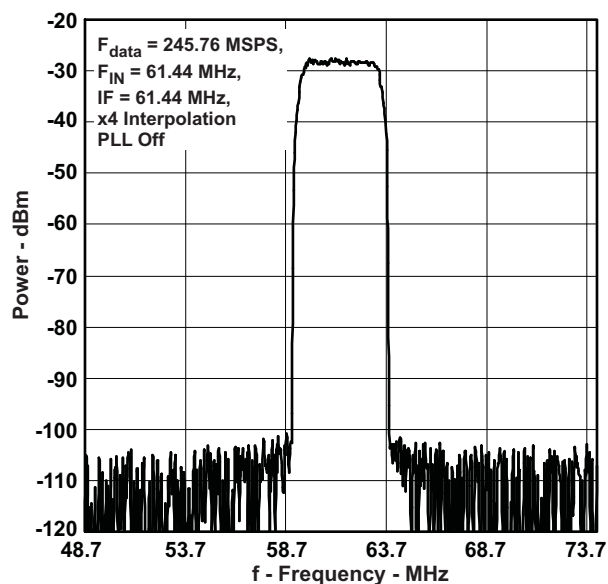


Figure 13. Single Carrier W-CDMA Test Model 1
Carrier Power: -7.8 dBm, ACLR: 79.3 dB

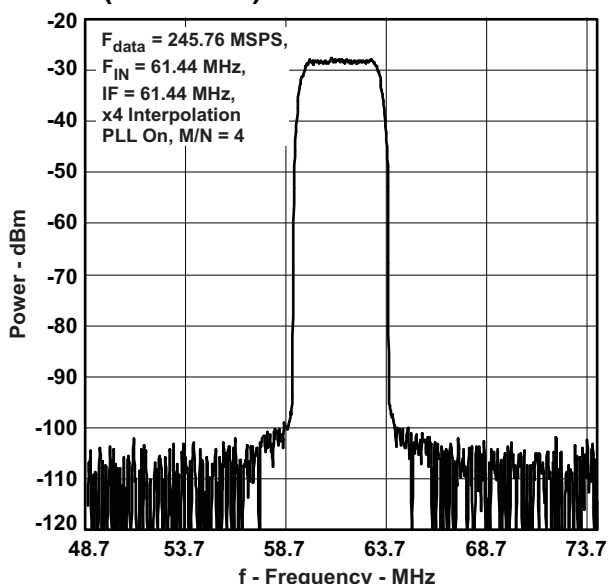


Figure 14. Single Carrier W-CDMA Test Model 1
Carrier Power: -7.8 dBm, ACLR: 76.9 dB

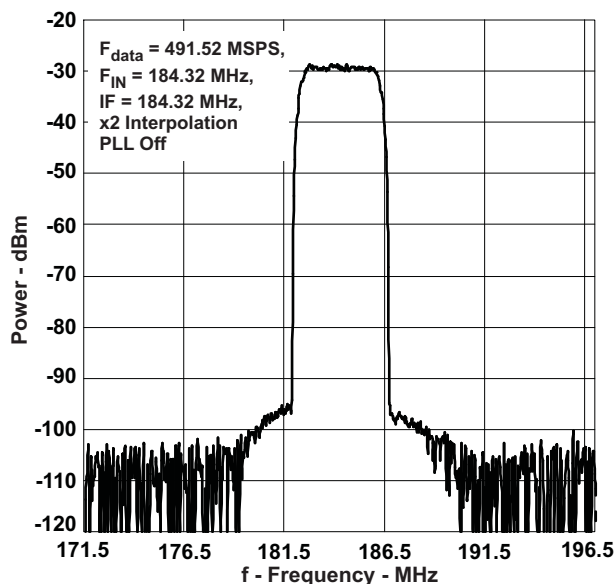


Figure 15. Single Carrier W-CDMA Test Model 1
Carrier Power: -8.9 dBm, ACLR: 72 dB

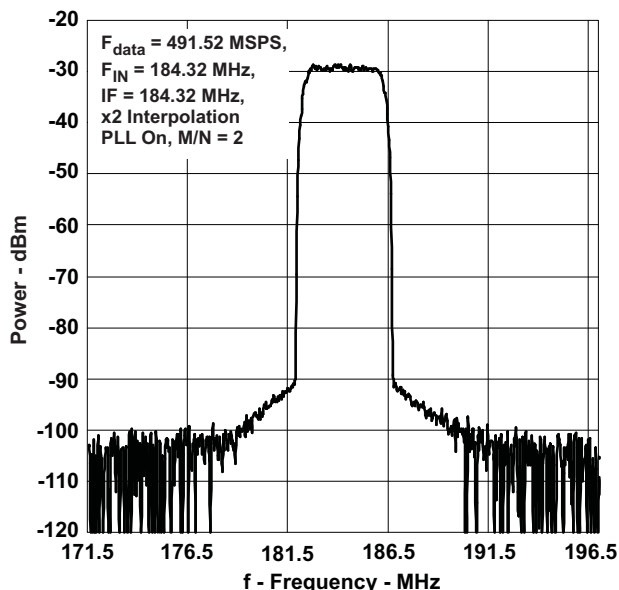
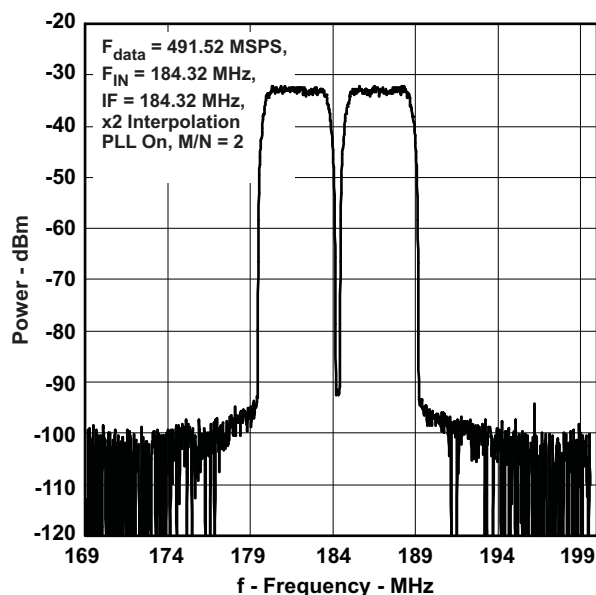
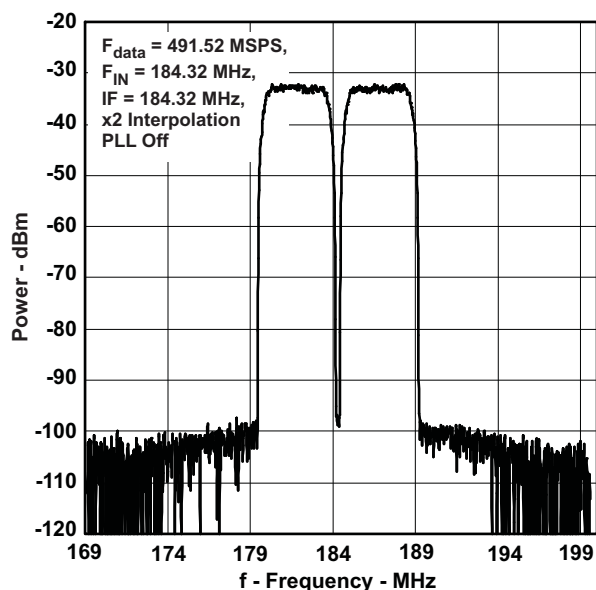
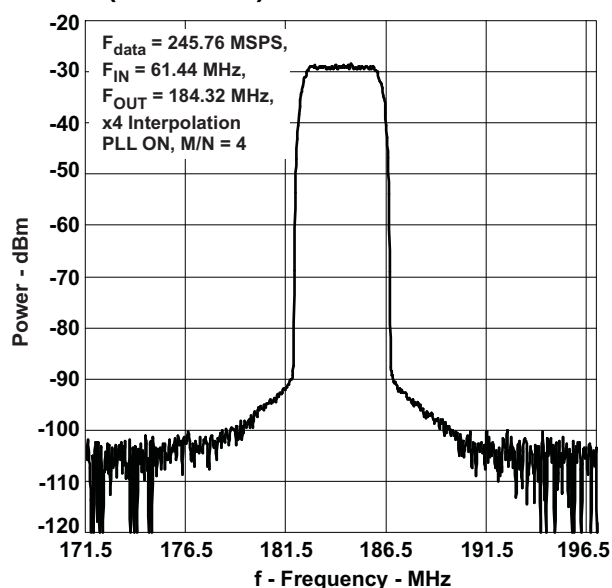
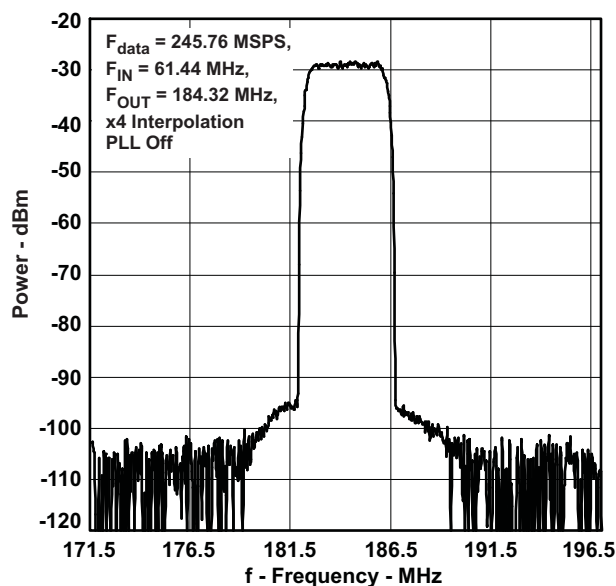


Figure 16. Single Carrier W-CDMA Test Model 1
Carrier Power: -8.9 dBm, ACLR: 68 dB

TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)

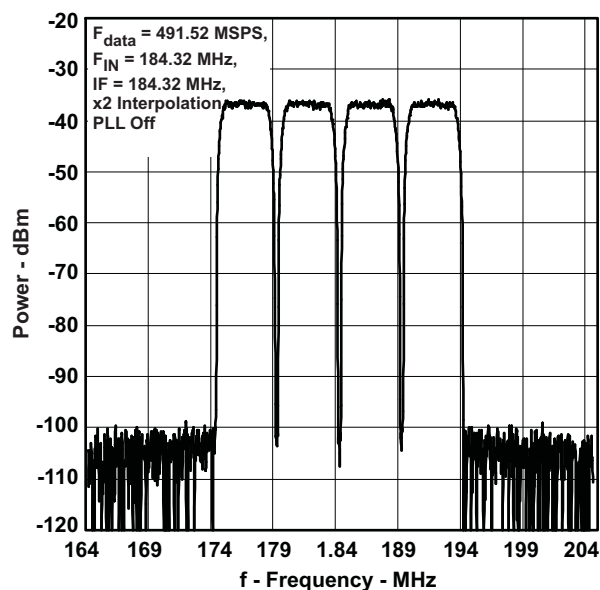


Figure 21. Four Carrier W-CDMA Test Model 1
Carrier Power: -16.3 dBm, ACLR: 66.7 dB

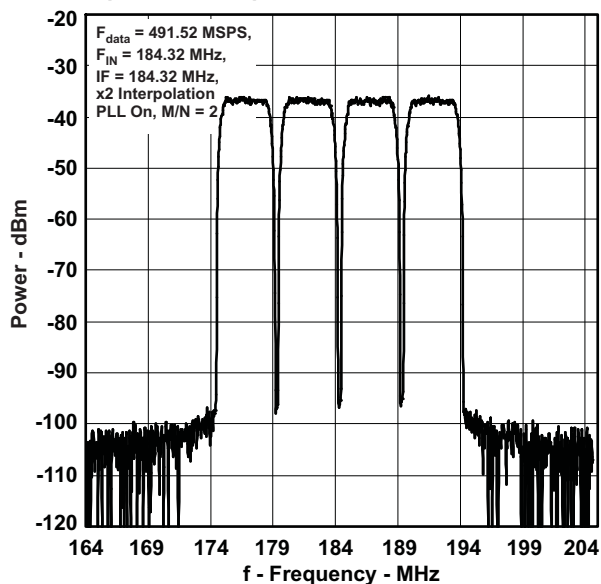


Figure 22. Four Carrier W-CDMA Test Model 1
Carrier Power: -16.3 dBm, ACLR: 64.5 dB

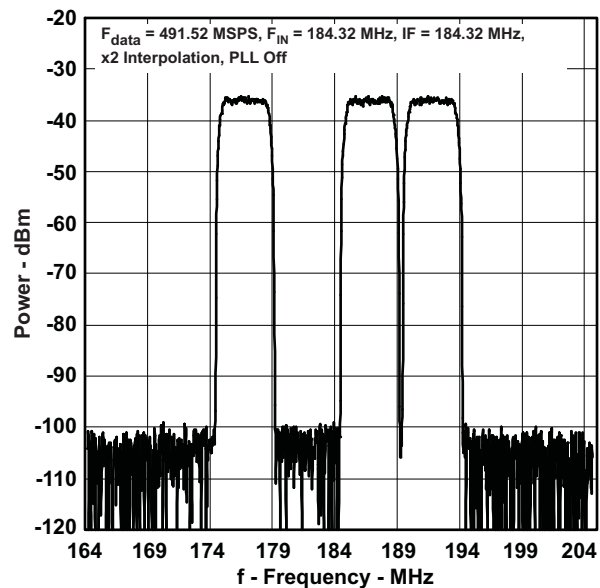


Figure 23. Three Carrier W-CDMA Test Model 1 with Gap
Carrier Power: -15.7 dBm, ACLR: 67.5 dB

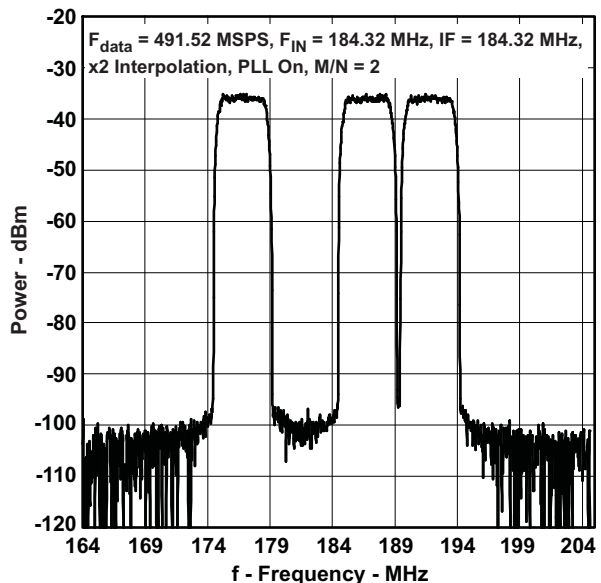


Figure 24. Three Carrier W-CDMA Test Model 1 with Gap
Carrier Power: -15.7 dBm, ACLR: 65.9 dB

TEST METHODOLOGY

Typical AC specifications were characterized with the DAC5681ZEVM using the test configuration shown in Figure 25. A sinusoidal master clock frequency is generated by an HP8665B signal generator and into a splitter. One output drives an Agilent 8133A pulse generator, and the other drives the CDCM7005 clock driver. The 8133A converts the sinusoidal frequency into a square wave output clock and drives an Agilent ParBERT 81250A pattern-generator clock. On the EVM, the DAC5681Z CLKIN/C input clock is driven by an CDCM7005 clock distribution chip that is configured to simply buffer the external 8665B clock or divide it down for PLL test configurations.

The DAC5681Z output is characterized with a Rohde and Schwarz FSU spectrum analyzer. For WCDMA signal characterization, it is important to use a spectrum analyzer with high IP3 and noise subtraction capability so that the spectrum analyzer does not limit the ACPR measurement.

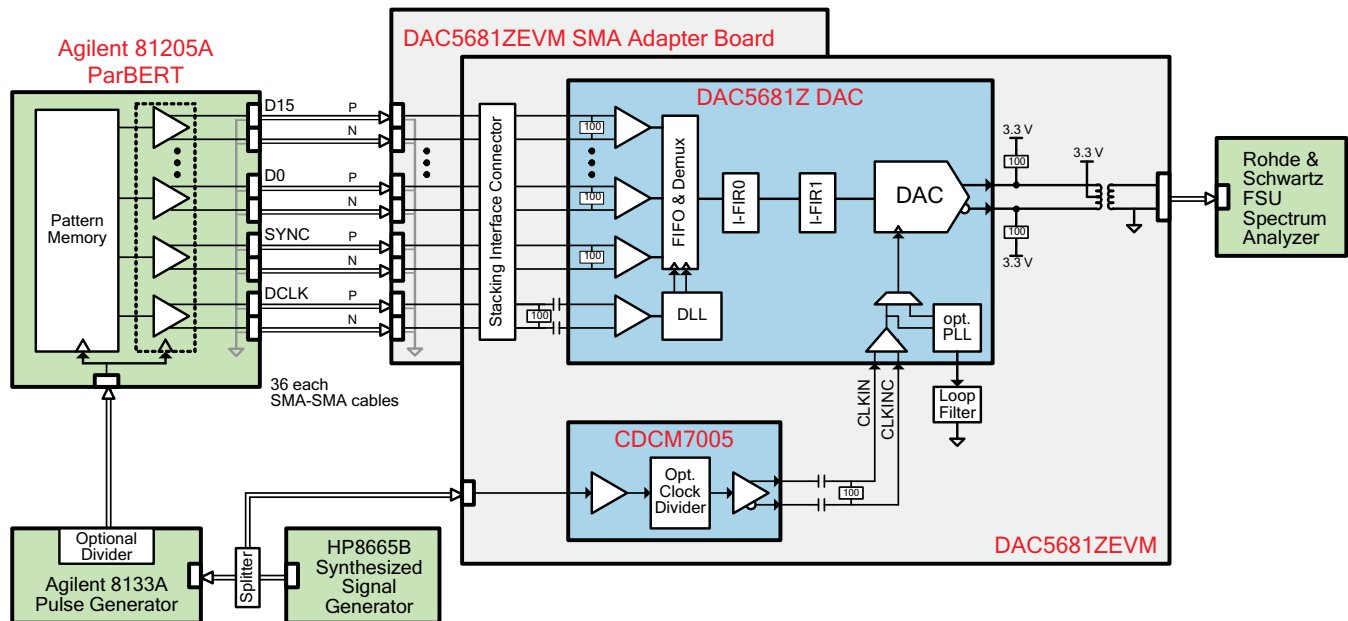


Figure 25. DAC5681Z Test Configuration for Normal Clock Mode

DEFINITION OF SPECIFICATIONS

Adjacent Carrier Leakage Ratio (ACLR): Defined for a 3.84Mcps 3GPP W-CDMA input signal measured in a 3.84MHz bandwidth at a 5MHz offset from the carrier with a 12dB peak-to-average ratio.

Analog and Digital Power Supply Rejection Ratio (APSSR, DPSSR): Defined as the percentage error in the ratio of the delta IOUT and delta supply voltage normalized with respect to the ideal IOUT current.

Differential Nonlinearity (DNL): Defined as the variation in analog output associated with an ideal 1 LSB change in the digital input code.

Gain Drift: Defined as the maximum change in gain, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Gain Error: Defined as the percentage error (in FSR%) for the ratio between the measured full-scale output current and the ideal full-scale output current.

Integral Nonlinearity (INL): Defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Intermodulation Distortion (IMD3, IMD): The two-tone IMD3 or four-tone IMD is defined as the ratio (in dBc) of the worst 3rd-order (or higher) intermodulation distortion product to either fundamental output tone.

Offset Drift: Defined as the maximum change in DC offset, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Offset Error: Defined as the percentage error (in FSR%) for the ratio of the differential output current (IOUT1–IOUT2) and the mid-scale output current.

Output Compliance Range: Defined as the minimum and maximum allowable voltage at the output of the current-output DAC. Exceeding this limit may result reduced reliability of the device or adversely affecting distortion performance.

Reference Voltage Drift: Defined as the maximum change of the reference voltage in ppm per degree Celsius from value at ambient (25°C) to values over the full operating temperature range.

Spurious Free Dynamic Range (SFDR): Defined as the difference (in dBc) between the peak amplitude of the output signal and the peak spurious signal.

Signal to Noise Ratio (SNR): Defined as the ratio of the RMS value of the fundamental output signal to the RMS sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and dc.

- ### Figure 26. Schematic

DETAILED DESCRIPTION

The primary modes of operation, listed in [Table 1](#), are selected by registers CONFIG1, CONFIG2 and CONFIG3.

Table 1. DAC5681Z Modes of Operation

Mode Name	No. of DACs Out	Interp. Factor	FIR0, CMIX0 Mode	FIR1, CMIX1 Mode	Device Config.	LVDS Input Data Mode	Max CLKIN Freq (MHz) ⁽¹⁾	Max DCLK Freq [DDR] (MHz)	Max Total Input Bus Rate (MSPS)	Max Input Data Rate Per Chan (#Ch @ MSPS)	Max Signal BW Per DAC (MHz) ⁽²⁾
1X1 (Bypass)	1	X1	–	–	Single Real	A	1000	500	1000	1 at 1000	500
1X2	1	X2	–	LP	Single Real	A	1000	250	500	1 at 500	200
1X2 HP	1	X2	–	HP	Single Real	A	1000	250	500	1 at 500	200
1X4	1	X4	LP	LP	Single Real	A	1000	125	250	1 at 250	100
1X4 LP/HP	1	X4	LP	HP	Single Real	A	1000	125	250	1 at 250	100
1X4 HP/LP	1	X4	HP	LP	Single Real	A	1000	125	250	1 at 250	50
1X4 HP/HP	1	X4	HP	HP	Single Real	A	1000	125	250	1 at 250	50

(1) Also the final DAC sample rate in MSPS.

(2) Assumes a 40% passband for FIR0 and/or FIR1 filters in all modes except 1X1 and 2X1 where simple Nyquist frequency is listed. Slightly wider bandwidths may be achievable depending on filtering requirements. Refer to *FIR Filters* section for more detail on filter characteristics. Also refer to Table 7 for IF placement and upconversion considerations.

Table 2. Register Map

Name	Address	Default	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0
STATUS0	0x00	0x0B	PLL_lock	DLL_lock	Unused	device_ID(2:0)			version(1:0)	
CONFIG1	0x01	0x10	DAC_delay(1:0)		Unused	fir_ena	SLFTST_ena	FIFO_offset(2:0)		
CONFIG2	0x02	0xC0	Twos_comp	Reserved	FIR2x4x	Unused	Reserved	FIR1_HP	Reserved	FIR0_HP
CONFIG3	0x03	0x70	DAC_offset_ena	SLFTST_err_mask	FIFO_err_mask	Pattern_err_mask	Reserved	Reserved	SW_sync	SW_sync_sel
STATUS4	0x04	0x00	Unused	SLFTST_err	FIFO_err	Pattern_err	Unused	Unused	Unused	Unused
CONFIG5	0x05	0x00	SIF4	rev_bus	clkdiv_sync_dis	Reserved	Reserved	DLL_bypass	PLL_bypass	Reserved
CONFIG6	0x06	0x0C	Reserved	Unused	Reserved	Sleep_A	BiasLPF_A	Reserved	PLL_sleep	DLL_sleep
CONFIG7	0x07	0xFF	DACA_gain(3:0)				Reserved			
CONFIG8	0x08	0x00	Reserved					DLL_restart	Reserved	
CONFIG9	0x09	0x00	PLL_m(4:0)				PLL_n(2:0)			
CONFIG10	0x0A	0x00	DLL_delay(3:0)			DLL_invclk	DLL_ifixed(2:0)			
CONFIG11	0x0B	0x00	PLL_LPF_reset	VCO_div2	PLL_gain(1:0)		PLL_range(3:0)			
CONFIG12	0x0C	0x00	Reserved		Offset_sync	OffsetA(12:8)				
CONFIG13	0x0D	0x00	OffsetA(7:0)							
CONFIG14	0x0E	0x00	SDO_func_sel(2:0)			Reserved				
CONFIG15	0x0F	0x00	Reserved							

Register name: STATUS0 – Address: 0x00, Default = 0x0B

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL_lock	DLL_lock	Unused	device_ID(2:0)		version(1:0)		
0	0	0	0	1	0	1	1

PLL_lock: Asserted when the internal PLL is locked. **(Read Only)**

DLL_lock: Asserted when the internal DLL is locked. Once the DLL is locked, this bit should remain a '1' unless the DCLK input clock is removed or abruptly changes frequency causing the DLL to fall out of lock. **(Read Only)**

device_ID(2:0): Returns '010' for DAC5681Z Device_ID code. **(ReadOnly)**

version(1:0): A hardwired register that contains the register set version of the chip. **(ReadOnly)**

version (1:0)	Identification
'01'	PG1.0 Initial Register Set
'10'	PG1.1 Register Set
'11'	Production Register Set

Register name: CONFIG1 – Address: 0x01, Default = 0x10

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAC_delay(1:0)		Unused	FIR_ena	SLFTST_ena	FIFO_offset(2:0)		
0	0	0	1	0	0	0	0

DAC_delay(1:0): DAC data delay adjustment. (0–3 periods of the DAC clock) This can be used to adjust system level output timing. The same delay is applied to DACA data paths.

FIR_ena: When set, the interpolation filters are enabled.

SLFTST_ena: When set, a Digital Self Test (SLFTST) of the core logic is enabled. Refer to *Digital Self Test Mode* section for details on SLFTST operation.

FIFO_offset(2:0): Programs the FIFO's output pointer location, allowing the input pointer to be shifted –4 to +3 positions upon SYNC. Default offset is 0 and is updated upon each sync event. **The recommended setting is 001.**

FIFO_offset(2:0)	Offset
011	+3
010	+2
001	+1
000	0
111	–1
110	–2
101	–3
100	–4

Register name: CONFIG2 – Address: 0x02, Default = 0xC0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Twos_comp	Reserved	FIR2x4x	Unused	Reserved	FIR1_HP	Reserved	FIR0_HP
1	1	0	0	0	0	0	0

Twos_comp: When set (default) the input data format is expected to be 2s complement, otherwise offset binary format is expected.

Reserved (Bit 6): Set to '1' for proper operation.

FIR2x4x: When set, 4X interpolation of the input data is performed, otherwise 2X interpolation.

FIR1_HP: When set, the FIR1 functions in High Pass (HP) mode; otherwise, the Low Pass (LP) filter mode is used. In 1X4 mode, the cascaded combination of HP and LP modes of FIR0 and FIR1 can be used to perform real upconversion. See Section DUAL-CHANNEL REAL UPCONVERSION.

FIR0_HP: When set, the FIR0 functions in High Pass (HP) mode; otherwise, the Low Pass (LP) filter mode is used. In 1X4 mode, the cascaded combination of HP and LP modes of FIR0 and FIR1 can be used to perform real upconversion. See Section DUAL-CHANNEL REAL UPCONVERSION.

Register name: CONFIG3 – Address: 0x03, Default = 0x70

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAC_offset_ena	SLFTST_err_mask	FIFO_err_mask	Pattern_err_mask	Reserved	Reserved	SW_sync	SW_sync_sel
0	1	1	1	0	0	0	0

DAC_offset_ena: When set, the values of **OffsetA(12:0)** in CONFIG12 through CONFIG13 registers are summed into the DAC-A data path. This provides a system-level offset adjustment capability that is independent of the input data.

SLFTST_err_mask: When set, masks out the **SLFTST_err** bit in STATUS4 register. Refer to *Digital Self Test Mode* section for details on SLFTST operation.

FIFO_err_mask: When set, masks out the **FIFO_err** bit in STATUS4 register.

Pattern_err_mask: When set, masks out the **Pattern err** bit in STATUS4 register.

Reserved (Bit 3): Set to '0' for proper operation.

Reserved (Bit 2): Set to '0' for proper operation.

SW_sync: This bit can be used as a substitute for the LVDS external SYNC input pins for both synchronization and transmit enable control.

SW_sync_sel: When set, the SW_sync bit is used as the only synchronization input and the LVDS external SYNC input pins are ignored.

Register name: STATUS4 – Address: 0x04, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused	SLFTST_err	FIFO_err	Pattern_err	Unused	Unused	Unused	Unused
0	0	0	0	0	0	0	0

SLFTST_err: Asserted when the Digital Self Test (SLFTST) fails. To clear the error, write a '0' to this register bit. This bit is also output on the SDO pin when the Self Test is enabled via **SLFTST_ena** control bit in CONFIG1. Refer to *Digital Self Test Mode* section for details on SLFTST operation.

FIFO_err: Asserted when the FIFO pointers over run each other causing a sample to be missed. To clear the error, write a '0' to this register bit.

Pattern_err: A digital checkerboard pattern compare function is provided for board level confidence testing and DLL limit checks. If the **Pattern_err_mask** bit via CONFIG3 is cleared, logic is enabled to continuously monitor input FIFO data. Any received data pattern other than 0xAAAA or 0x5555 causes this bit to be set. To clear the error, flush out the previous pattern error by inputting at least 8 samples of the 0xAAAA and/or 0x5555, then write a '0' to this register bit.

Register name: CONFIG5 – Address: 0x05, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIF4	rev_bus	clkdiv_sync_dis	Reserved	Reserved	DLL_bypass	PLL_bypass	Reserved
0	0	0	0	0	0	0	0

SIF4: When set, the serial interface is in 4 pin mode, otherwise it is in 3 pin mode. Refer to **SDO_func_sel (2:0)** bits in CONFIG14 register for options available to output status indicator data on the SDO pin.

rev_bus: Reverses the LVDS input data bus so that the MSB to LSB order is swapped. This function is provided to ease board level layout and avoid wire crossovers in case the LVDS data source output bus is mirrored with respect to the DAC's input data bus.

clkdiv_sync_dis: Disables the clock divider sync when this bit is set.

Reserved (Bit 4): Set to '0' for proper operation.

Reserved (Bit 3): Set to '0' for proper operation.

DLL_bypass: When set, the DLL is bypassed and the LVDS data source is responsible for providing correct setup and hold timing.

PLL_bypass: When set, the PLL is bypassed.

Reserved (Bit 0): Set to '0' for proper operation.

Register name: CONFIG6 – Address: 0x06, Default = 0x0C

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Unused	Reserved	Sleep_A	BiasLPF_A	Reserved	PLL_sleep	DLL_sleep
0	0	0	0	1	1	0	0

Reserved (Bit 7): Reserved (Bit 7): Set to 0 for proper operation.

Reserved (Bit 5): Set to '0' for proper operation.

Sleep_A: When set, DACA is put into sleep mode.

BiasLPF_A: Enables a 95 kHz low pass filter corner on the DACA current source bias when cleared. If this bit is set, a 472 kHz filter corner is used.

Reserved (Bit 2): Set to '1' for proper operation.

PLL_sleep: When set, the PLL is put into sleep mode.

DLL_sleep: When set, the DLL is put into sleep mode.

Register name: CONFIG7 – Address: 0x07, Default = 0xFF

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DACA_gain(3:0)				Reserved			
1	1	1	1	1	1	1	1

DACA_gain(3:0): Scales DACA output current in 16 equal steps.

$$\frac{V_{EXTIO}}{R_{bias}} \times (DACA_gain + 1)$$

Reserved (3:0): Set to '1111' for proper operation.

Register name: CONFIG8 – Address: 0x08, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					DLL_restart	Reserved	
0	0	0	0	0	0	0	0

Reserved (7:3): Set to '00000' for proper operation.

DLL_restart: This bit is used to restart the DLL. When this bit is set, the internal DLL loop filter is reset to zero volts, and the DLL delay line is held at the center of its bias range. When cleared, the DLL will acquire lock to the DCLK signal. A DLL restart is accomplished by setting this bit with a serial interface write, and then clearing this bit with another serial interface write. Any interruption in the DCLK signal or changes to the DLL programming in the CONFIG10 register must be followed by this DLL restart sequence. Also, when this bit is set, the **DLL_lock** indicator in the STATUS0 register is cleared.

Reserved (1:0): Set to '00' for proper operation

Register name: CONFIG9 – Address: 0x09, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL_m(4:0)					PLL_n(2:0)		
0	0	0	0	0	0	0	0

PLL_m: M portion of the M/N divider of the PLL thermometer encoded:

PLL_m(4:0)	M value
00000	1
00001	2
00011	4
00111	8
01111	16
11111	32
All other values	Invalid

PLL_n: N portion of the M/N divider of the PLL thermometer encoded. If supplying a high rate CLKIN frequency, the PLL_n value should be used to divide down the input CLKIN to maintain a maximum PFD operating of 160 MHz.

PLL_n(2:0)	N value
000	1
001	2
011	4
111	8
All other values	Invalid

PLL Function:

$$f_{\text{VCO}} = \left[\frac{(M)}{(N)} \right] \times f_{\text{ref}}$$

where f_{ref} is the frequency of the external DAC clock input on the CLKIN/CLKINC pins.

Register name: CONFIG10 – Address: 0x0A, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLL_delay(3:0)				DLL_invclk	DLL_ifixed(2:0)		
0	0	0	0	0	0	0	0

DLL_delay(3:0): The DCLKP/N LVDS input data clock has a DLL to automatically skew the clock to LVDS data timing relationship, providing proper setup and hold times. **DLL_delay(3:0)** is used to manually adjust the DLL delay \pm from the fixed delay set by **DLL_ifixed(2:0)**. Adjustment amounts are approximate.

DLL_delay(3:0)	Delay Adjust (degrees)
1000	50°
1001	55°
1010	60°
1011	65°
1100	70°
1101	75°
1110	80°
1111	85°
0000	90° (Default)
0001	95°
0010	100°
0011	105°
0100	110°
0101	115°
0110	120°
0111	125°

DLL_invclk: When set, used to invert an internal DLL clock to force convergence to a different solution. This can be used in the case where the DLL delay adjustment has exceeded the limits of its range.

DLL_ifixed(2:0): Adjusts the DLL delay line bias current. Refer to the Electrical Characteristics table. Used in conjunction with the DLL_invclk bit to select appropriate delay range for a given DCLK frequency:

'011' – maximum bias current and minimum delay range

'000' – mid scale bias current

'101' – minimum bias current and maximum delay range

'100' – do not use.

Register name: CONFIG11 – Address: 0x0B, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL_LPF_reset	VCO_div2	PLL_gain(1:0)		PLL_range(3:0)			
0	0	0	0	0	0	0	0

PLL_LPF_reset: When a logic high, the PLL loop filter (LPF) is pulled down to 0V. Toggle from '1' to '0' to restart the PLL if an over-speed lock-up occurs. Over-speed can happen when the process is fast, the supplies are higher than nominal, etc., resulting in the feedback dividers missing a clock.

VCO_div2: When set, the PLL CLOCK output is 1/2 the PLL VCO frequency. Used to run the VCO at 2X the needed clock frequency to reduce phase noise for lower input clock rates.

PLL_gain(1:0): Used to adjust the PLL's Voltage Controlled Oscillator (VCO) gain, K_{VCO} . Refer to the Electrical Characteristics table. By increasing the **PLL_gain**, the VCO can cover a broader range of frequencies; however, the higher gain also increases the phase noise of the PLL. In general, lower **PLL_gain** settings result in lower phase noise. The K_{VCO} of the VCO can also affect the PLL stability and is used to determine the loop filter components. See section on determining the PLL filter components for more detail.

PLL_range(3:0): Programs the PLL VCO fixed bias current. Refer to the Electrical Characteristics table. This setting, in conjunction with the PLL_gain(1:0), sets the achievable frequency range of the PLL VCO:
 '000' – minimum bias current and lowest VCO frequency range
 '111' – maximum bias current and highest VCO frequency range

Register name: CONFIG12 – Address: 0x0C, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Offset_sync	OffsetA(12:8)				
0	0	0	0	0	0	0	0

Reserved (1:0): Set to '00' for proper operation.

Offset_sync: On a change from '0' to '1' the values of the OffsetA(12:0) and OffsetB(12:0) control registers are transferred to the registers used in the DAC-A and DAC-B offset calculations. This double buffering allows complete control by the user as to when the change in the offset value occurs. This bit does not auto-clear. Prior to updating new offset values, it is recommended that the user clear this bit.

OffsetA(12:8): Upper 5 bits of the offset adjustment value for the A data path. (**SYNCED via Offset_sync**)

Register name: CONFIG13 – Address: 0x0D, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OffsetA(7:0)							
0	0	0	0	0	0	0	0

OffsetA(7:0): Lower 8 bits of the offset adjustment value for the A data path. (**SYNCED via Offset_sync**)

Register name: CONFIG14 – Address: 0x0E, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SDO_func_sel(2:0)			Reserved				
0	0	0	0	0	0	0	0

SDO_func_sel(2:0): Selects the signal for output on the SDO pin. When using the 3 pin serial interface mode, this allows the user to multiplex several status indicators onto the SDO pin. In 4 pin serial interface mode, programming this register to view one of the 5 available status indicators will override normal SDO serial interface operation.

SDO_func_sel (2:0)	Output to SDO
000, 110, 111	Normal SDO function
001	PLL_lock
010	DLL_lock
011	Pattern_err
100	FIFO_err
101	SLFTST_err

Reserved (4:0): Set to '00000' for proper operation.

Register name: CONFIG15 – Address: 0x0F, Default = 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							
0	0	0	0	0	0	0	0

Reserved (7:0): Set to '0x00' for proper operation.

SERIAL INTERFACE

The serial port of the DAC5681Z is a flexible serial interface which communicates with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of DAC5681Z. It is compatible with most synchronous transfer formats and can be configured as a 3 or 4 pin interface by **SIF4** in register **CONFIG5**. In both configurations, **SCLK** is the serial interface input clock and **SDENB** is serial interface enable. For 3 pin configuration, **SDIO** is a bidirectional pin for both data in and data out. For 4 pin configuration, **SDIO** is data in only and **SDO** is data out only. Data is input into the device with the rising edge of **SCLK**. Data is output from the device on the falling edge of **SCLK**.

Each read/write operation is framed by signal **SDENB** (Serial Data Enable Bar) asserted low for 2 to 5 bytes, depending on the data length to be transferred (1–4 bytes). The first frame byte is the instruction cycle which identifies the following data transfer cycle as read or write, how many bytes to transfer, and what address to transfer the data. [Table 3](#) indicates the function of each bit in the instruction cycle and is followed by a detailed description of each bit. Frame bytes 2 to 5 comprise the data transfer cycle.

Table 3. Instruction Byte of the Serial Interface

	MSB				LSB			
Bit	7	6	5	4	3	2	1	0
Description	R/W	N1	N0	A4	A3	A2	A1	A0

R/W Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from DAC5681Z and a low indicates a write operation to DAC5681Z.

[N1 : N0] Identifies the number of data bytes to be transferred per [Table 5](#) below. Data is transferred MSB first.

Table 4. Number of Transferred Bytes Within One Communication Frame

N1	N0	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

[A4 : A0] Identifies the address of the register to be accessed during the read or write operation. For multi-byte transfers, this address is the starting address. Note that the address is written to the DAC5681Z MSB first and counts down for each byte.

[Figure 27](#) shows the serial interface timing diagram for a DAC5681Z write operation. **SCLK** is the serial interface clock input to DAC5681Z. Serial data enable **SDENB** is an active low input to DAC5681Z. **SDIO** is serial data in. Input data to DAC5681Z is clocked on the rising edges of **SCLK**.

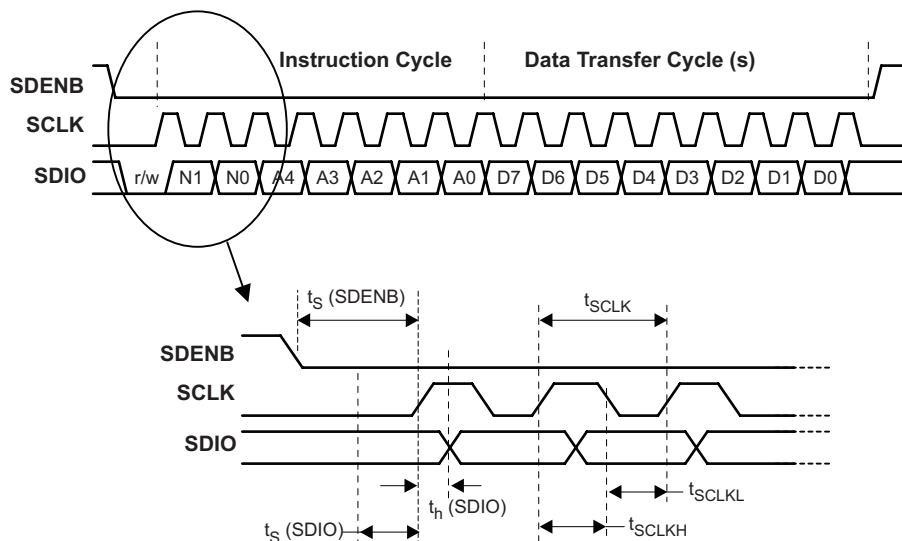


Figure 27. Serial Interface Write Timing Diagram

Figure 28 shows the serial interface timing diagram for a DAC5681Z read operation. **SCLK** is the serial interface clock input to DAC5681Z. Serial data enable **SDENB** is an active low input to DAC5681Z. **SDIO** is serial data in during the instruction cycle. In 3 pin configuration, **SDIO** is data out from DAC5681Z during the data transfer cycle(s), while **SDO** is in a high-impedance state. In 4 pin configuration, **SDO** is data out from DAC5681Z during the data transfer cycle(s). At the end of the data transfer, SDO will output low on the final falling edge of SCLK until the rising edge of SDENB when it will 3-state.

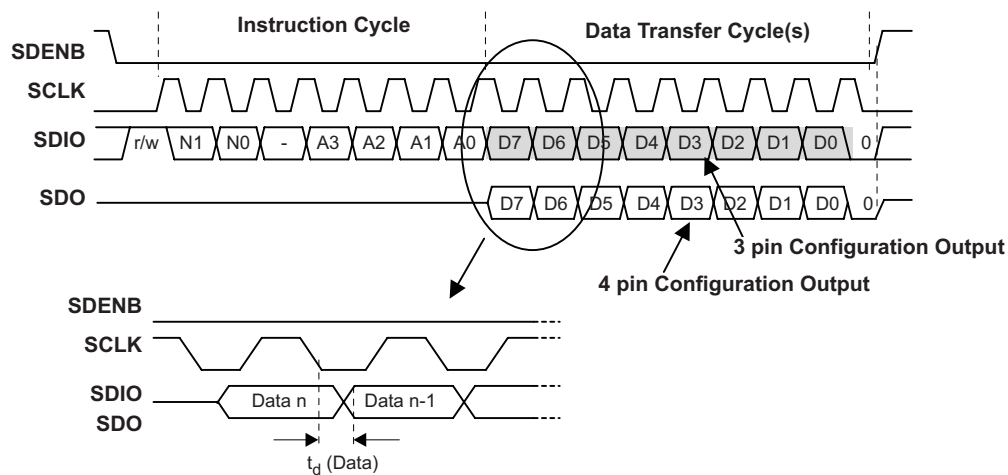


Figure 28. Serial Interface Read Timing Diagram

FIR FILTERS

Figure 29 shows the magnitude spectrum response for the identical 47-tap FIR0 and FIR1 filters. The transition band is from 0.4 to $0.6 \times F_{IN}$ (the input data rate for the FIR filter) with <0.002 dB of pass-band ripple and approximately 76dB of stop-band attenuation. Figure 30 shows the region from 0.35 to $0.45 \times F_{IN}$ – up to $0.44 \times F_{IN}$ there is less than 0.4 dB attenuation. The composite spectrum for x4 interpolation mode, the cascaded response of FIR0 and FIR1, is shown in Figure 31. The filter taps for both FIR0 and FIR1 are listed in Table 5.

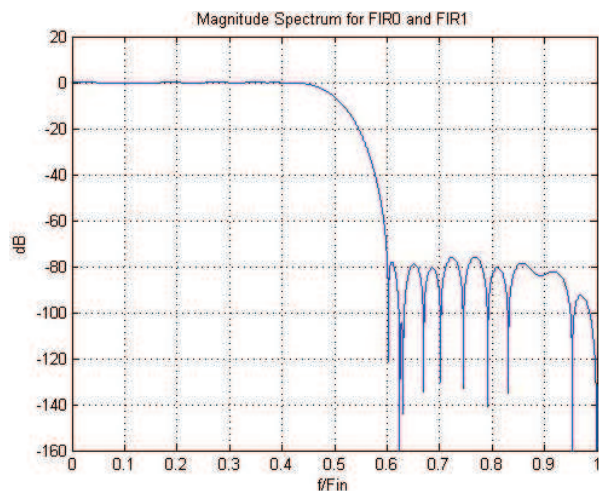


Figure 29. Magnitude Spectrum for FIR0 and FIR1

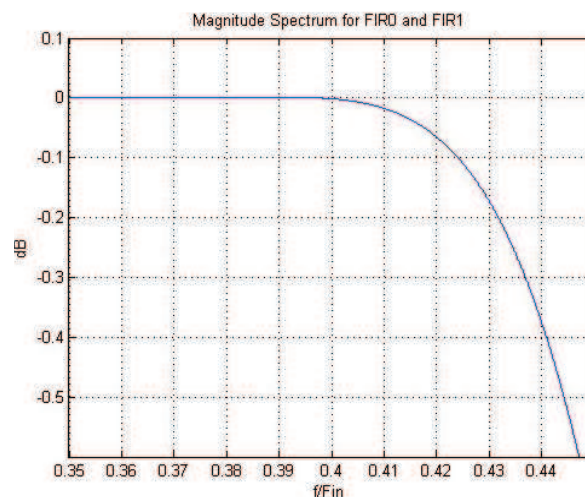


Figure 30. FIR0 and FIR1 Transition Band

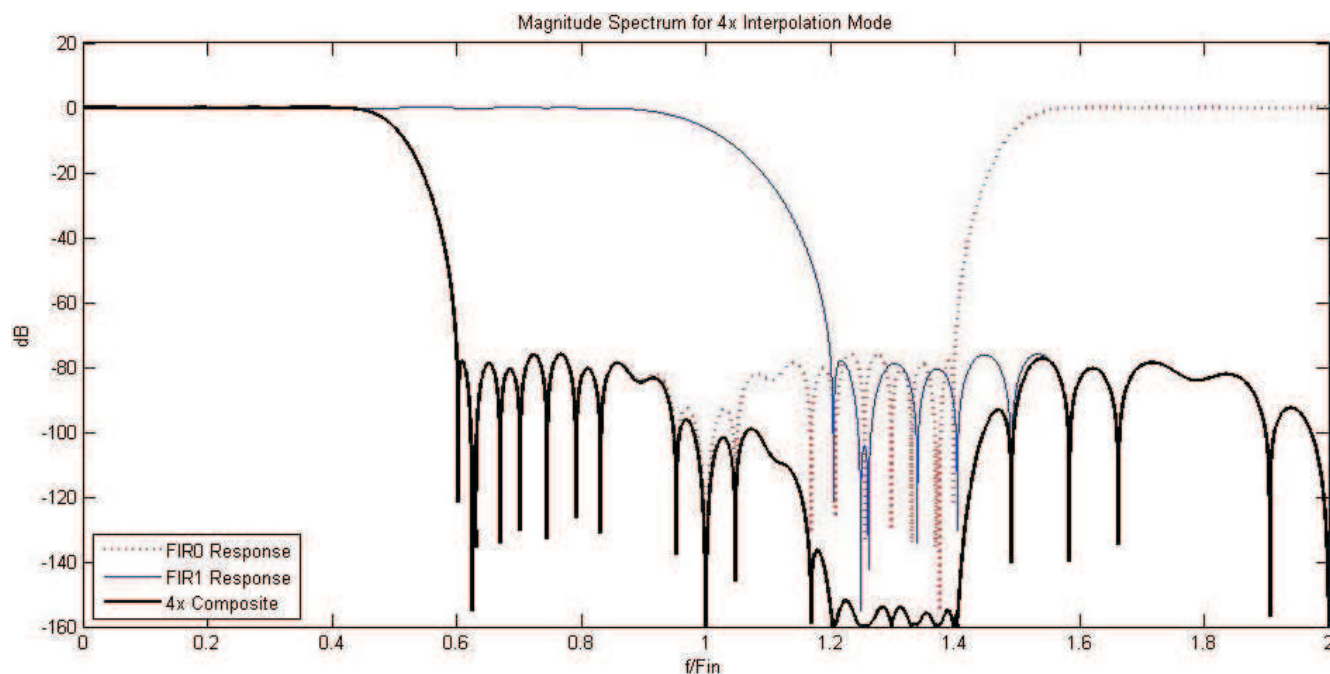


Figure 31. Magnitude Composite Spectrum for 4x Interpolation Mode

Table 5. FIR0 and FIR1 Digital Filter Taps

TAP#	COEFF	TAP#	COEFF
1, 47	–5	2, 46	0
3, 45	18	4, 44	0
5, 43	–42	6, 42	0
7, 41	85	8, 40	0
9, 39	–158	10, 38	0
11, 37	272	12, 36	0
13, 35	–444	14, 34	0
15, 33	704	16, 32	0
17, 31	–1106	18, 30	0
19, 29	1795	20, 28	0
21, 27	–3295	22, 26	0
23, 25	10368	—	—
24	16384	—	—

DUAL-CHANNEL REAL UPCONVERSION

Each DAC5681Z digital filter has a normal Low Pass (LP) characteristic, but can be configured to perform a High Pass (HP) function by mixing a 1 –1....sequence at the output of the FIR to invert the spectrum. The mixing mode for each filter is controlled by FIR0_HP and FIR1_HP bits in register CONFIG2. With 1X4 interpolation and cascaded combinations of HP and LP filter modes, the output frequency response will be digitally shifted or upconverted. The wide bandwidths of both FIR0 and FIR1 (40% bandpass) provide options for setting six different frequency ranges, listed in [Table 6](#). With the High Pass (1X2 HP mode), High Pass/Low Pass (1X4 HP/LP mode) and Low Pass/High Pass (1X4 LP/HP mode) settings, the upconverted signal is spectrally inverted.

Table 6. Dual-Channel Real Upconversion Options

MODE NAME	INTERP. FACTOR	FIR0, CMIX0 MODE	FIR1, CMIX1 MODE	INPUT FREQUENCY	OUTPUT FREQUENCY	SIGNAL BANDWIDTH	SPECTRUM INVERTED?
1X2	X2	--	LP	0.0 to $0.4 \times f_{\text{DATA}}$	0.0 to $0.4 \times f_{\text{DATA}}$	$0.4 \times f_{\text{DATA}}$	No
1X2 HP	X2	--	HP	0.0 to $0.4 \times f_{\text{DATA}}$	0.6 to $1.0 \times f_{\text{DATA}}$	$0.4 \times f_{\text{DATA}}$	Yes
1X4	X4	LP	LP	0.0 to $0.4 \times f_{\text{DATA}}$	0.0 to $0.4 \times f_{\text{DATA}}$	$0.4 \times f_{\text{DATA}}$	No
1X4 HP/LP	X4	HP	LP	0.2 to $0.4 \times f_{\text{DATA}}$	0.6 to $0.8 \times f_{\text{DATA}}$	$0.2 \times f_{\text{DATA}}$	Yes
1X4 HP/HP	X4	HP	HP	0.2 to $0.4 \times f_{\text{DATA}}$	1.2 to $1.4 \times f_{\text{DATA}}$	$0.2 \times f_{\text{DATA}}$	No
1X4 LP/HP	X4	LP	HP	0.0 to $0.4 \times f_{\text{DATA}}$	1.6 to $2.0 \times f_{\text{DATA}}$	$0.4 \times f_{\text{DATA}}$	Yes

CLOCK AND DATA MODES

There are two modes of operation to drive the internal clocks on the DAC5681Z. Timing diagrams for both modes are shown in [Figure 32](#). EXTERNAL CLOCK MODE accepts an external full-rate clock input on the CLKIN/CLKINC pins to drive the DACs and final logic stages while distributing an internally divided down clock for lower speed logic such as the interpolating FIRs. PLL CLOCK MODE uses an internal clock multiplying PLL to derive the full-rate clock from an external lower rate reference frequency on the CLKIN/CLKINC pins. In both modes, an LVDS half-rate data clock (DCLKP/DCLKN) is provided by the user and is typically generated by a *toggleing data bit* to maintain LVDS data to DCLK timing alignment. LVDS data relative to DCLK is input using Double Data Rate (DDR) switching using both rising and falling edges as shown in the both figures below. The CONFIG10 register contains user controlled settings for the DLL to adjust for the DCLK input frequency and various t_{SKEW} timing offsets between the LVDS data and DCLK. The CDCM7005 and CDCE62005 from Texas Instruments are recommended for providing phase aligned clocks at different frequencies for device-to-device clock distribution and multiple DAC synchronization.

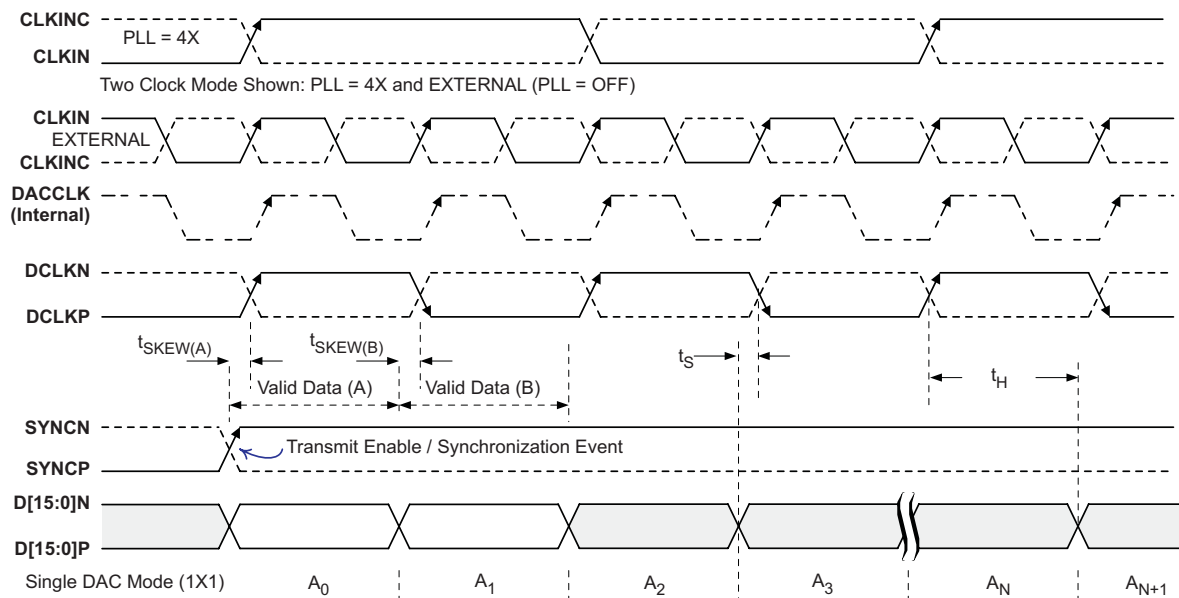


Figure 32. Clock and Data Timing Diagram

In PLL Clock Mode, the user provides an external reference clock to the CLKIN/C input pins. Refer to [Figure 33](#). An internal clock multiplying PLL uses the lower-rate reference clock to generate a high-rate clock for the DAC. This function is very useful when a high-rate clock is not already available at the system level; however, the internal VCO phase noise in PLL Clock Mode may degrade the quality of the DAC output signal when compared to an external low jitter clock source.

The input reference clock N-Divider is selected by CONFIG9 **PLL_n(2:0)** for values of $\div 1$, $\div 2$, $\div 4$ or $\div 8$. The VCO feedback clock M-Divider is selected by CONFIG9 **PLL_m(4:0)** for values of $\div 1$, $\div 2$, $\div 4$, $\div 8$, $\div 16$ or $\div 32$. The combination of M-Divider and N-Divider form the clock multiplying ratio of M/N. If the reference clock frequency is greater than 160 MHz, use a N-Divider of $\div 2$, $\div 4$ or $\div 8$ to avoid exceeding the maximum PFD operating frequency.

The diagram illustrates the internal structure of the PLL (Phase-Locked Loop) circuit. It shows the following components and signals:

- Inputs:**
 - CLKIN** and **CLKINC** (Clock Input and Increment) are connected to the **N-Divider**.
 - CLKVDD** (1.8V, Pin 1) and **IOVDD** (3.3V, Pin 9) are power supply pins.
 - LPF** (Pin 64) is the Loop Filter Pin.
- PLL Sleep:** A control signal (CONFIG 6) that can put the PLL into a sleep state.
- PLL LPF reset:** A control signal (CONFIG 11) that resets the loop filter.
- PLL m (4:0) (CONFIG 9):** The M-Divider value, which can be 1, 2, 4, 8, 16, or 32.
- PLL n (2:0) (CONFIG 9):** The N-Divider value, which can be 1, 2, 4, or 8.
- PLL range (3:0) (CONFIG 11):** The PLL gain, which can be 1, 2, 4, or 8.
- VCO div2 (CONFIG 11):** A control signal that divides the VCO output by 2.
- PLL bypass via CONFIG 5:** A control signal that bypasses the PLL and uses the external loop filter.

The internal components of the PLL are:

- N-Divider (1, 2, 4, 8):** Divides the input clock by N.
- PFD (Phase-Frequency Detector):** Compares the divided input clock with the feedback clock.
- Charge Pump:** Generates the error signal for the VCO.
- VCO (Voltage-Controlled Oscillator):** Generates the output clock based on the error signal.
- M-Divider (1, 2, 4, 8, 16, 32):** Divides the VCO output by M.

The output of the PLL is **F_{PLL}**, which is connected to the **To internal DAC clock distribution** block. The external loop filter is shown as a dashed box containing a capacitor and a resistor.

Figure 33. Functional Block Diagram for PLL

CLOCK INPUTS

Figure 34 shows an equivalent circuit for the LVDS data input clock (DCLKP/N).

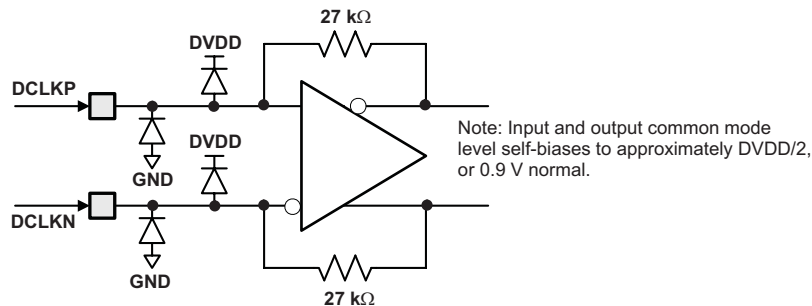


Figure 34. DCLKP/N Equivalent Input Circuit

Figure 35 shows an equivalent circuit for the DAC input clock (CLKIN/C).

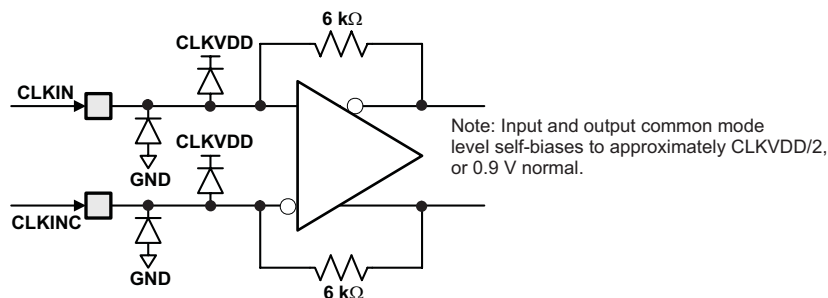


Figure 35. CLKIN/C Equivalent Input Circuit

Figure 36 shows the preferred configuration for driving the CLKIN/CLKINC input clock with a differential ECL/PECL source.

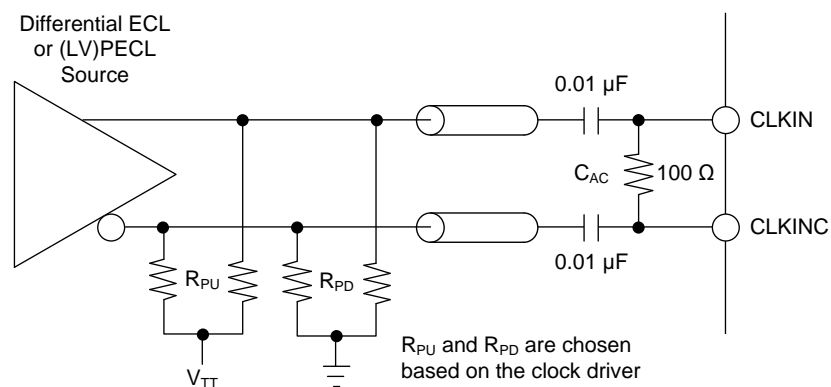


Figure 36. Preferred Clock Input Configuration With a Differential ECL/PECL Clock Source

LVDS DATA INTERFACING

Interfacing very high-speed LVDS data and clocks presents a big challenge to system designers as they have unique constraints and are often implemented with specialized circuits to increase bandwidth. One such specialized LVDS circuit used in many FPGAs and ASICs is a Serializer-DESerializer (SERDES) block. For interfacing to the DAC5681Z, only the Serializer functionality of the SERDES block is required. SERDES drivers accept lower rate parallel input data and output a serial stream using a shift register at a frequency multiple of the data bit width. For example, a 4-bit SERDES block can accept parallel 4-bit input data at 250 MSPS and output serial data 1000 MSPS.

External clock distribution for FPGA and ASIC SERDES drivers often have a chip-to-chip system constraint of a limited input clock frequency compared to the desired LVDS data rate. In this case, an internal clock multiplying PLL is often used in the FPGA or ASIC to drive the high-rate SERDES outputs. Due to this possible system clocking constraint, the DAC5681Z accommodates a scheme where a toggling LVDS SERDES data bit can provide a “data driven” half-rate clock (DCLK) from the data source. A DLL on-board the DAC is used to shift the DCLK edges relative to LVDS data to maintain internal setup and hold timing.

To increase bandwidth of a single 16-bit input bus, the DAC5681Z assumes Double Data Rate (DDR) style interfacing of data relative to the half-rate DCLK. Refer to [Figure 37](#) and [Figure 38](#) providing an example implementation using FPGA-based LVDS data and clock interfaces to drive the DAC5681Z. In this example, an assumed system constraint is that the FPGA can only receive a 250 MHz maximum input clock while the desired DAC clock is 1000 MHz. A clock distribution chip such as the CDCM7005 or the CDCE62005 is useful in this case to provide frequency and phase locked clocks at 250 MHz and 1000 MHz.

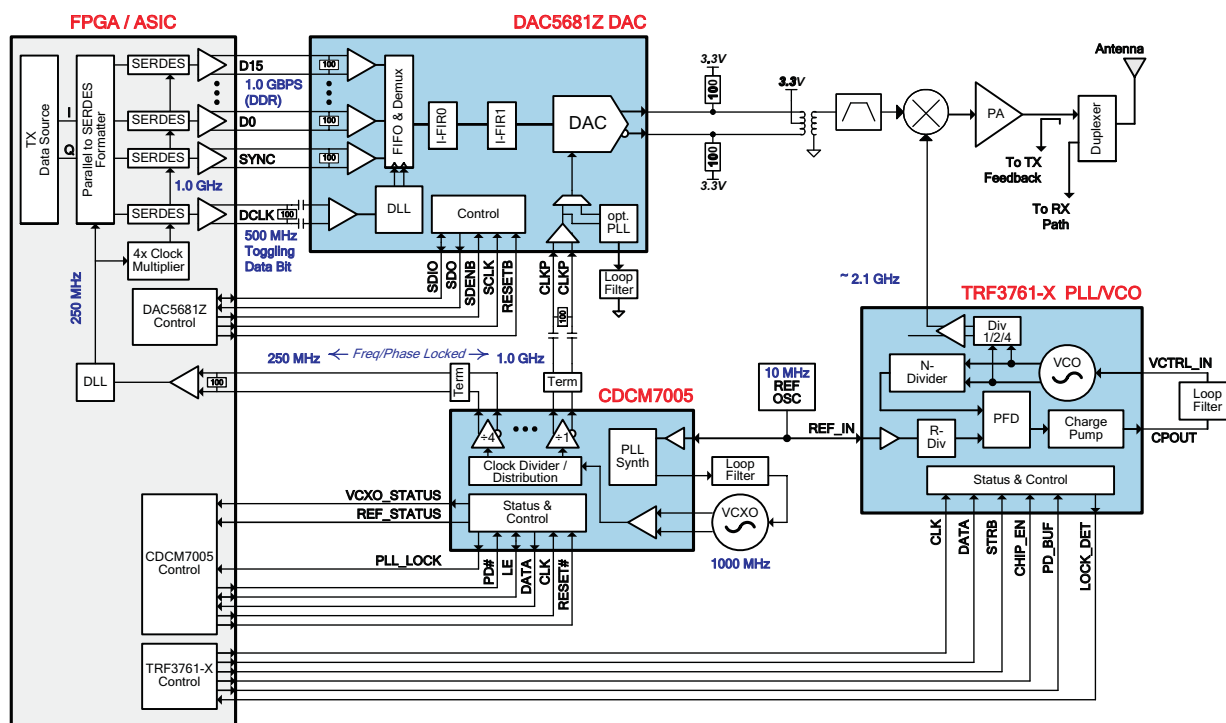


Figure 37. Example Real IF System Diagram

From the example provided by [Figure 38](#), driving LVDS data into the DAC using SERDES blocks requires a parallel load of 4 consecutive data samples to shift registers. Color is used in the figure to indicate how data and clocks flow from the FPGA to the DAC5681Z. The figure also shows the use of the SYNC/P/N input, which along with DCLK, requires 18 individual SERDES data blocks to drive the DAC's input data FIFO that provides an elastic buffer to the DAC5681Z digital processing chain.

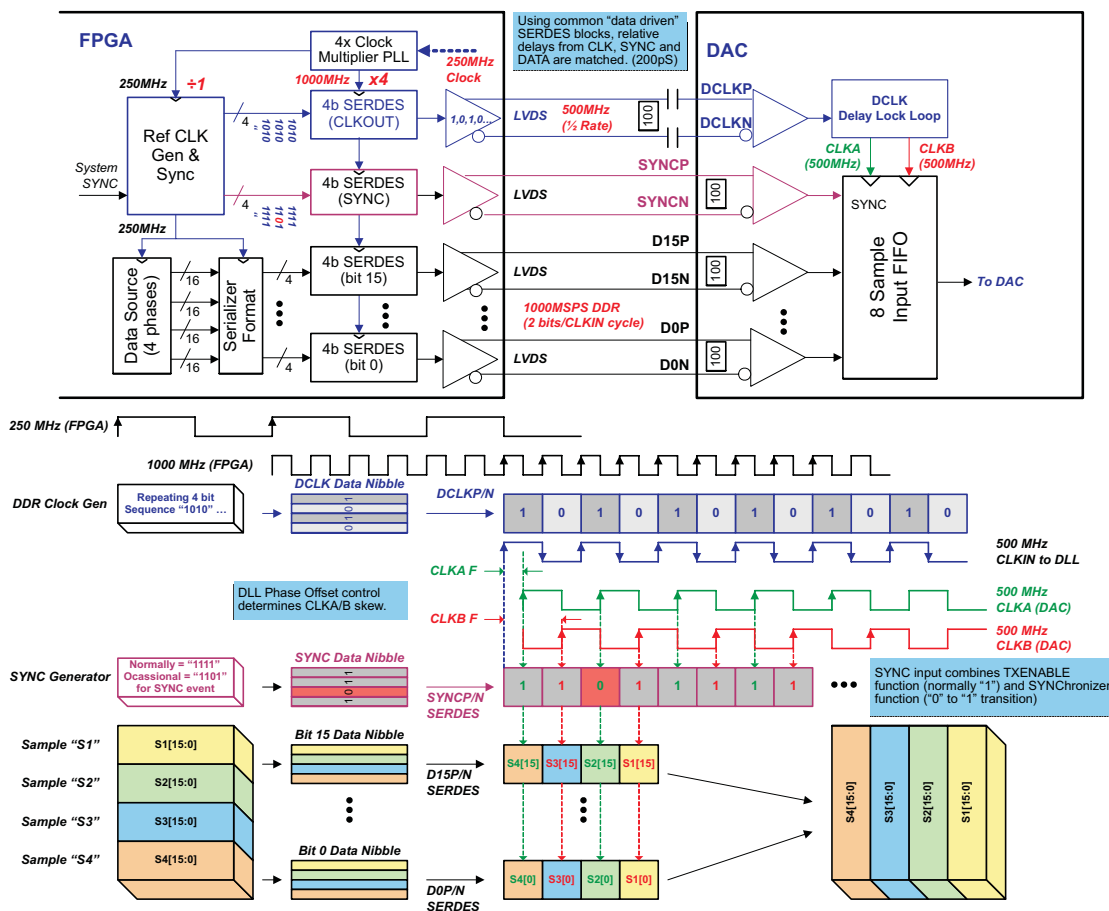


Figure 38. Example FPGA-Based LVDS Data Flow to DAC

LVDS INPUTS

The D[15:0]P/N and SYNC P/N LVDS pairs have the input configuration shown in Figure 39. Figure 40 shows the typical input levels and common-mode voltage used to drive these inputs.

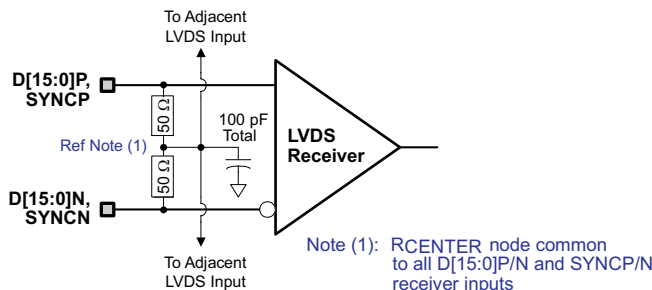


Figure 39. D[15:0]P/N and SYNC P/N LVDS Input Configuration

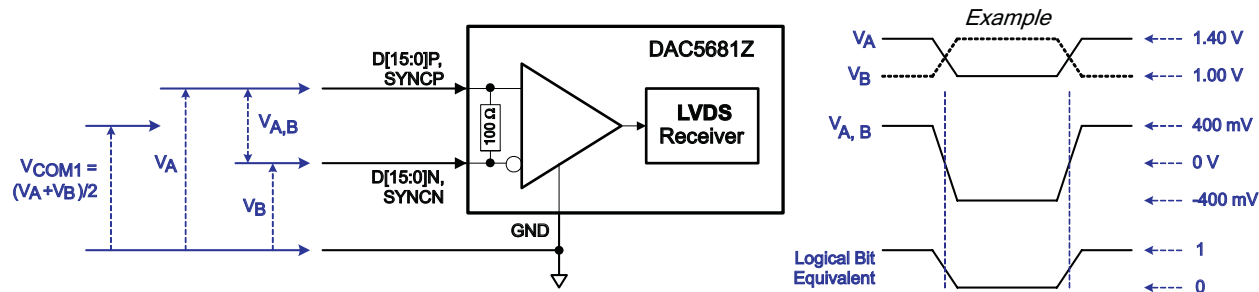


Figure 40. LVDS Data (D[15:0]P/N, SYNCN/P Pairs) Input Levels

Table 7. Example LVDS Data Input Levels

APPLIED VOLTAGES		RESULTING DEFERENTIAL VOLTAGE	RESULTING COMMON- MODE VOLTAGE	LOGICAL BIT BINARY EQUIVALENT
V_A	V_B	$V_{A,B}$	V_{COM1}	
1.4 V	1.0 V	400 mV	1.2 V	1
1.0 V	1.4 V	–400 mV		0
1.2 V	0.8 V	400 mV	1.0 V	1
0.8 V	1.2 V	–400 mV		0

Figure 41 shows the DCLKP/N LVDS clock input levels. Unlike the D[15:0]P/N and SYNCN/P LVDS pairs, the DCLKP/N pair does not have an internal resistor and the common-mode voltage is self-biased to approximately DVDD/2 in order to optimize the operation of the DLL circuit. For proper external termination a 100 Ω resistor needs to be connected across the LVDS clock source lines followed by series 0.01 μF capacitors connected to each of the DCLKP and DCLKN pairs. For best performance, the resistor and capacitors should be placed as close as possible to these pins.

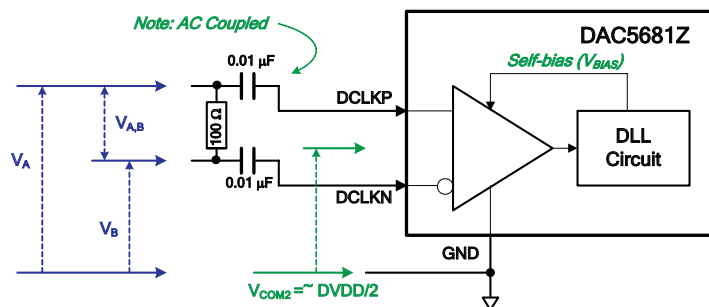


Figure 41. LVDS Clock (DCLKP/N) Input Levels

LVDS SYNCN/P Operation

The SYNCN/P LVDS input control functions as a combination of Transmit Enable (TXENABLE) and Synchronization trigger. If SYNCN is low, the transmit chain is disabled so input data from the FIFO is ignored while zeros are inserted into the data path. If SYNCN is raised from low to high, a synchronization event occurs with behavior defined by individual control bits in registers CONFIG1 and CONFIG5. The SYNCN/P control is sampled and input into the FIFO along with the other LVDS data to maintain timing alignment with the data bus. See Figure 38.

The **software_sync_sel** and **software_sync** controls in CONFIG3 provide a substitute for external SYNCN/P control; however, since the serial interface is used no timing control is provided with respect to the DAC clock.

DLL OPERATION

The DAC5681Z provides a digital Delay Lock Loop (DLL) to skew the LVDS data clock (DCLK) relative to the data bits, D[15:0] and SYNC, in order to maintain proper setup and hold timing. Since the DLL operates closed-loop, it requires a stable DCLK to maintain delay lock. Refer to the description of **DLL_ifixed(2:0)** and **DLL_delay(3:0)** control bits in the CONFIG10 register. Prior to initializing the DLL, the **DLL_ifixed** value should be programmed to match the expected DCLK frequency range. To initialize the DLL, refer to the **DLL_Restart** programming bit in the CONFIG8 register. After initialization, the status of the DLL can be verified by reading the **DLL_Lock** bit from STATUS0. See *Startup Sequence* below.

RECOMMENDED STARTUP SEQUENCE

The following startup sequence is recommended to initialize the DAC5681Z:

1. Supply all 1.8V (CLKVDD, DVDD, VFUSE) voltages simultaneously followed by all 3.3V (AVDD and IOVDD) voltages.
2. Provide stable CLKIN/C clock.
3. Toggle RESETB pin for a minimum 25 nSec active low pulse width.
4. Program all desired SIF registers. Set **DLL_Restart** bit during this write cycle. The CONFIG10 register value should match the corresponding DCLKP/N frequency range in the Electrical Characteristics table.
5. Provide stable DCLKP/N clock. (This can also be provided earlier in the sequence)
6. Clear the **DLL_Restart** bit when the DCLKP/N clock is expected to be stable.
7. Verify the status of **DLL_Lock** and repeat until set to '1'. **DLL_Lock** can be monitored by reading the STATUS0 register or by monitoring the SDO pin in 3-wire SIF mode. (See description for CONFIG14 **SDO_func_sel**.)
8. Enable transmit of data by asserting the LVDS SYNC/N input or setting CONFIG3 **SW_sync** bit. (See description for CONFIG3 **SW_sync** and **SW_sync_sel**) The SYNC source must be held at a logic '1' to enable data flow through the DAC. If multiple DAC devices require synchronization, refer to the "Recommended Multi-DAC Synchronization Procedure" below.
9. Provide data flow to LVDS D[15:0]P/N pins. If using the LVDS SYNC/N input, data can be input simultaneous with the logic '1' transition of SYNC/N.

RECOMMENDED MULTI-DAC SYNCHRONIZATION PROCEDURE

The DAC5681Z provides a mechanism to synchronize multiple DAC devices in a system. The procedure has two steps involving control of the CONFIG5 **clkdiv_sync_dis** bits as well as external control of the LVDS SYNC/N input. (All DACs involved need to be configured to accept the external SYNC/N input and not "software" sync mode).

1. Synchronize Clock Dividers (for each DAC):
 - (a) Set CONFIG5 **clkdiv_sync_dis** = 0.
 - (b) Toggle SYNC/N input to all DACs simultaneously (same input to all DACs).
2. Synchronize FIFO pointers (for each DAC):
 - (a) Set CONFIG5 **clkdiv_sync_dis** = 1 (Disable clock divider re-sync).
 - (b) Wait a minimum of 50 CLKIN cycles from previous SYNC/N toggle. In practice, the time required to write the above register value will typically occupy more than 50 cycles.
 - (c) Assert SYNC/N input and hold at '1' to all DACs simultaneously. Holding this at '1' is effectively the TXENABLE for the chip so data will be output on the analog pins.
3. After the normal pipeline delay of the device, the outputs of all DACs will be synchronized to within ± 1 DAC clock cycle.

CMOS DIGITAL INPUTS

Figure 42 shows a schematic of the equivalent CMOS digital inputs of the DAC5681Z. SDIO and SCLK have pull-down resistors while RESETB and SDENB have pull-up resistors internal the DAC5681Z. See the specification table for logic thresholds. The pull-up and pull-down circuitry is approximately equivalent to 100kΩ.

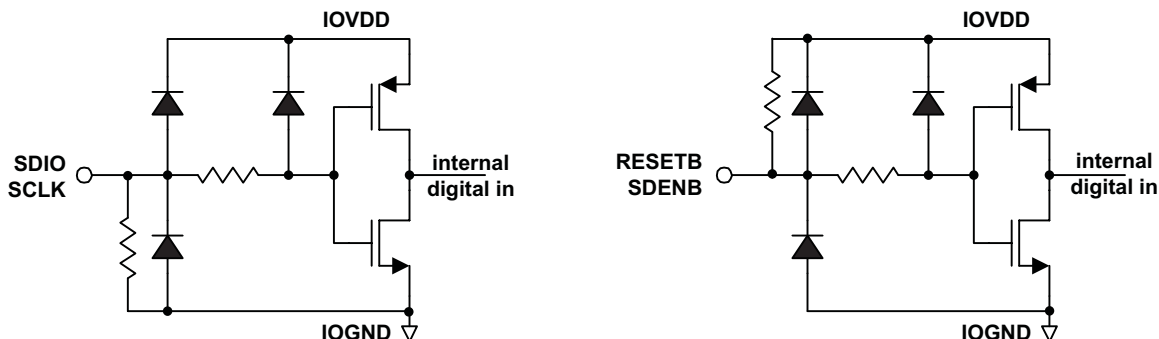


Figure 42. CMOS/TTL Digital Equivalent Input

DIGITAL SELF TEST MODE

The DAC5681Z has a Digital Self Test (SLFTST) mode to designed to enable board level testing without requiring specific input data test patterns. The SLFTST mode is enabled via the CONFIG1 **SLFTST_ena** bit and results are only valid when CONFIG3 **SLFTST_err_mask** bit is cleared. An internal Linear Feedback Shift Register (LFSR) is used to generate the input test patterns for the full test cycle while a checksum result is computed on the digital signal chain outputs. The LVDS input data bus is ignored in SLFTST mode. After the test cycle completes, if the checksum result does not match a hardwired comparison value, the STATUS4 **SLFTST_err** bit is set and will remain set until cleared by writing a '0' to the **SLFTST_err** bit. A full self test cycle requires no more than 400,000 CLKIN/C clock cycles to complete and will automatically repeat until the **SLFTEST_ena** bit is cleared.

To initiate a the Digital Self Test:

1. Provide a normal CLKIN/C input clock. (The PLL is not used in SLFTST mode)
2. Provide a RESETB pulse to perform a hardware reset on device.
3. Program the registers with the values shown in [Table 8](#). These register values contain the settings to properly configure the SLFTST including **SLFTST_ena** and **SLFTST_err_mask** bits
4. Provide a '1' on the SYNCP/N input to initiate TXENABLE.
5. Wait at a minimum of 400,000 CLKIN/C cycles for the SLFTST to complete. Example: If CLKIN = 1GHz, then the wait period is $400,000 \times 1 / 1\text{GHz} = 400 \mu\text{Sec}$.
6. Read STATUS4 **SLFTST_err** bit. If set, a self test error has occurred. The **SLFTST_err** status may optionally be programmed to output on the SDO pin if using the 3-bit SIF interface. See [Table 8](#) Note (1).
7. (Optional) The SLFTST function automatically repeats until **SLFTST_ena** bit is cleared. To the loop the test, write a '0' to STATUS4 **SLFTST_err** to clear previous errors and continue at step 5 above.
8. To continue normal operating mode, provide another RESETB pulse and reprogram registers to the desired normal settings.

Table 8. Digital Self Test (SLFTST) Register Values

REGISTER	ADDRESS (hex)	VALUE (Binary)	VALUE (Hex)
CONFIG1	01	00011000	18
CONFIG2	02	11101010	EA
CONFIG3	03	10110000	B0
STATUS4	04	00000000	00
CONFIG5	05	00000110	06
CONFIG6	06	00001111	0F
CONFIG12	0C	00001010	0A
CONFIG13	0D	01010101	55
CONFIG14 ⁽¹⁾	0E	00001010	0A
CONFIG15	0F	10101010	AA
All others	–	Default	Default

(1) If using a 3-bit SIF interface, the SDO pin can be programmed to report **SLFTST_err** status via the **SDO_fun_sel(2:0)** bits. In this case, set CONFIG14 = '10101010' or AA hex.

REFERENCE OPERATION

The DAC5681Z uses a bandgap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS} to pin BIASJ. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip bandgap reference voltage and control amplifier. The default full-scale output current equals 16 times this bias current and can thus be expressed as:

$$I_{OUT_{FS}} = 16 \times I_{BIAS} = 16 \times V_{EXTIO} / R_{BIAS}$$

The DAC has a 4-bit coarse gain control via **DACA_gain(3:0)** in the CONFIG7 register so the $I_{OUT_{FS}}$ can be expressed as:

$$I_{OUT_{FS}} = (DACA_gain + 1) \times I_{BIAS} = (DACA_gain + 1) \times V_{EXTIO} / R_{BIAS}$$

where V_{EXTIO} is the voltage at terminal EXTIO. The bandgap reference voltage delivers an accurate voltage of 1.2 V. This reference is active when terminal EXTLO is connected to AGND. An external decoupling capacitor C_{EXT} of 0.1 μF should be connected externally to terminal EXTIO for compensation. The bandgap reference can additionally be used for external reference operation. In that case, an external buffer with high impedance input should be applied in order to limit the bandgap load current to a maximum of 100 nA. The internal reference can be disabled and overridden by an external reference by connecting EXTLO to AVDD. Capacitor C_{EXT} may hence be omitted. Terminal EXTIO thus serves as either input or output node.

The full-scale output current can be adjusted from 20 mA down to 2 mA by varying resistor R_{BIAS} or changing the externally applied reference voltage. The internal control amplifier has a wide input range, supporting the full-scale output current range of 20 dB.

DAC TRANSFER FUNCTION

The CMOS DAC's consist of a segmented array of NMOS current sinks, capable of sinking a full-scale output current up to 20 mA. Differential current switches direct the current to either one of the complementary output nodes IOUT1 or IOUT2. Complementary output currents enable differential operation, thus canceling out common mode noise sources (digital feed-through, on-chip and PCB noise), dc offsets, even order distortion components, and increasing signal output power by a factor of two.

The full-scale output current is set using external resistor R_{BIAS} in combination with an on-chip bandgap voltage reference source (+1.2 V) and control amplifier. Current I_{BIAS} through resistor R_{BIAS} is mirrored internally to provide a maximum full-scale output current equal to 16 times I_{BIAS} .

The relation between IOUT1 and IOUT2 can be expressed as:

$$IOUT1 = -IOUT_{FS} - IOUT2$$

We will denote current flowing into a node as – current and current flowing out of a node as + current. Since the output stage is a current sink the current can only flow from AVDD into the IOUT1 and IOUT2 pins. The output current flow in each pin driving a resistive load can be expressed as:

$$IOUT1 = IOUT_{FS} \times (65535 - CODE) / 65536$$

$$IOUT2 = IOUT_{FS} \times CODE / 65536$$

where CODE is the decimal representation of the DAC data input word.

For the case where IOUT1 and IOUT2 drive resistor loads R_L directly, this translates into single ended voltages at IOUT1 and IOUT2:

$$VOUT1 = AVDD - |IOUT1| \times R_L$$

$$VOUT2 = AVDD - |IOUT2| \times R_L$$

Assuming that the data is full scale (65536 in offset binary notation) and the R_L is 25 Ω , the differential voltage between pins IOUT1 and IOUT2 can be expressed as:

$$VOUT1 = AVDD - |-0 \text{ mA}| \times 25 \Omega = 3.3 \text{ V}$$

$$VOUT2 = AVDD - |-20 \text{ mA}| \times 25 \Omega = 2.8 \text{ V}$$

$$V_{DIFF} = VOUT1 - VOUT2 = 0.5 \text{ V}$$

Note that care should be taken not to exceed the compliance voltages at node IOUT1 and IOUT2, which would lead to increased signal distortion.

DAC OUTPUT SINC RESPONSE

Due to the sampled nature of a high-speed DAC, the well known $\sin(x)/x$ (or SINC) response can significantly attenuate higher frequency output signals. Figure 43 shows the unitized SINC attenuation roll-off with respect to the final DAC sample rate in 4 Nyquist zones. For example, if the final DAC sample rate $F_s = 1.0$ GSPS, then a tone at 440MHz is attenuated by 3.0dB. Although the SINC response can create challenges in frequency planning, one side benefit is the natural attenuation of Nyquist images. The increased over-sampling ratio of the input data provided by the 2x and 4x digital interpolation modes of the DAC5681Z improves the SINC roll-off (droop) within the original signal's band of interest.

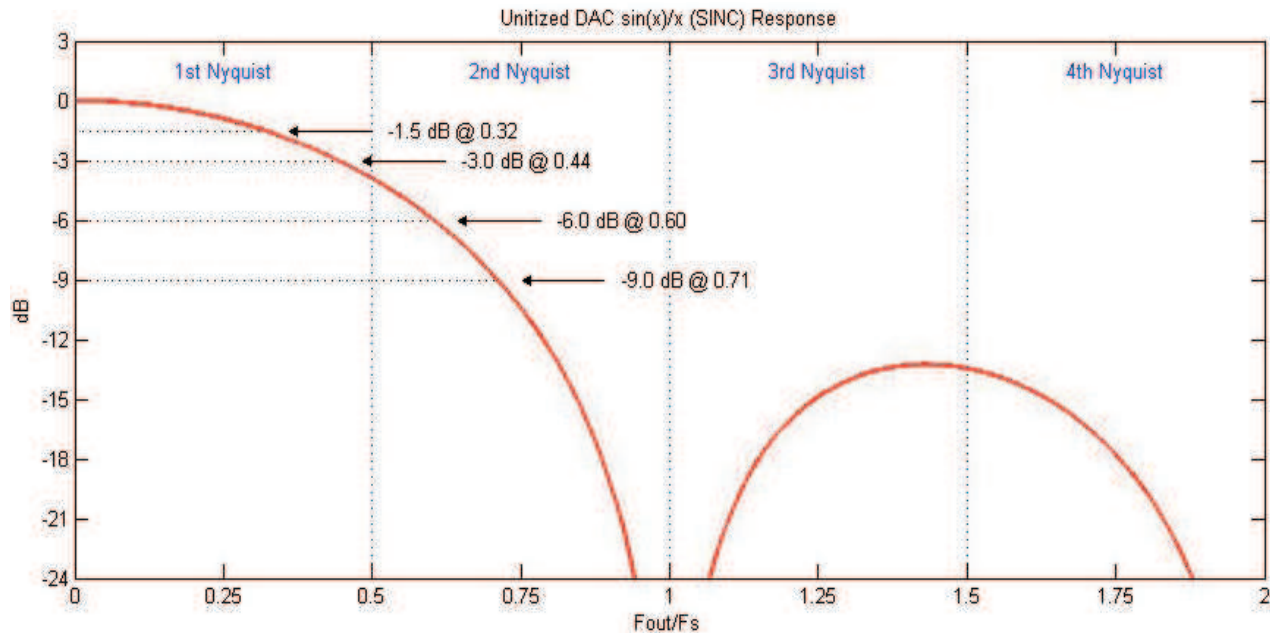


Figure 43. Unitized DAC $\sin(x)/x$ (SINC) Response

ANALOG CURRENT OUTPUTS

Figure 44 shows a simplified schematic of the current source array output with corresponding switches in a current sink configuration. Differential switches direct the current into either the positive output node, IOUT1, or its complement, IOUT2, then through the individual NMOS current sources. The output impedance is determined by the stack of the current sources and differential switches, and is typically $>300\text{ k}\Omega$ in parallel with an output capacitance of 5 pF .

The external output resistors are referenced to an external ground. The minimum output compliance at nodes IOUT1 and IOUT2 is limited to $AVDD - 0.5\text{ V}$, determined by the CMOS process. Beyond this value, transistor breakdown may occur resulting in reduced reliability of the DAC5681Z device. The maximum output compliance voltage at nodes IOUT1 and IOUT2 equals $AVDD + 0.5\text{ V}$. Exceeding the minimum output compliance voltage adversely affects distortion performance and integral non-linearity. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at IOUT1 and IOUT2 does not exceed 0.5 V .

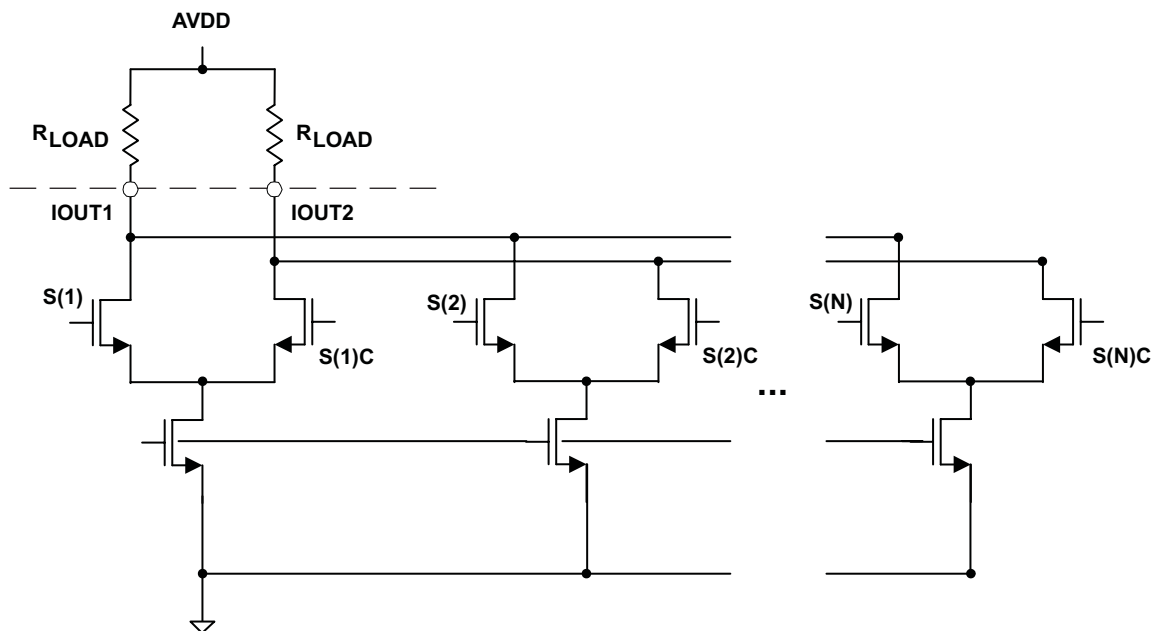


Figure 44. Equivalent Analog Current Output

The DAC5681Z can be easily configured to drive a doubly terminated 50Ω cable using a properly selected RF transformer. Figure 45 and Figure 46 show the 50Ω doubly terminated transformer configuration with 1:1 and 4:1 impedance ratio, respectively. Note that the center tap of the primary input of the transformer has to be connected to AVDD to enable a dc current flow. Applying a 20 mA full-scale output current would lead to a 0.5 V_{PP} for a 1:1 transformer, and a 1 V_{PP} output for a 4:1 transformer. The low dc-impedance between IOUT1 or IOUT2 and the transformer center tap sets the center of the ac-signal at AVDD, so the 1 V_{PP} output for the 4:1 transformer results in an output between $AVDD + 0.5\text{ V}$ and $AVDD - 0.5\text{ V}$.

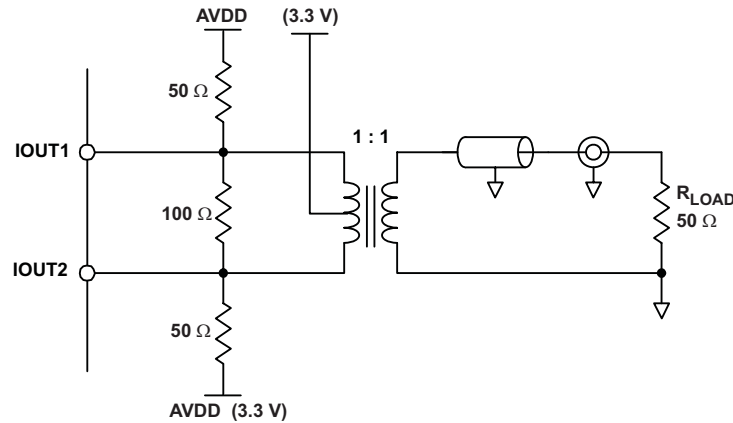


Figure 45. Driving a Doubly-Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

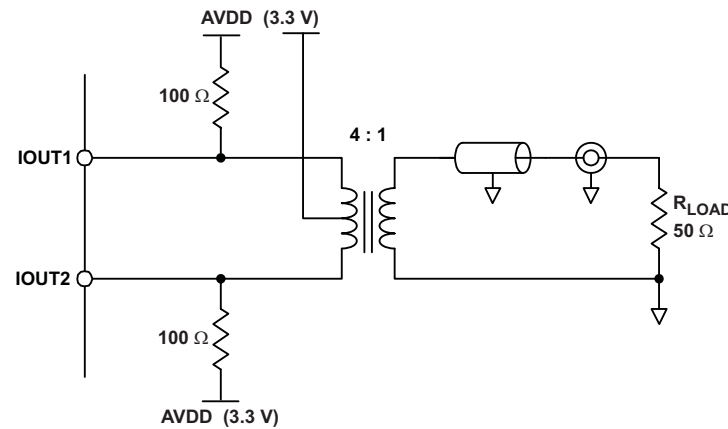


Figure 46. Driving a Doubly-Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

DESIGNING THE PLL LOOP FILTER

To minimize phase noise given for a given fDAC and M/N, the values of **PLL_gain** and **PLL_range** are selected so that G_{VCO} is minimized and within the MIN and MAX frequency for a given setting.

The external loop filter components C1, C2, and R1 are set by the G_{VCO} , M/N, the loop phase margin ϕ_d and the loop bandwidth ω_d . Except for applications where abrupt clock frequency changes require a fast PLL lock time, it is suggested that ϕ_d be set to at least 80 degrees for stable locking and suppression of the phase noise side lobes. Phase margins of 60 degrees or less can be sensitive to board layout and decoupling details.

See [Figure 47](#), the recommend external loop filter topology. C1, C2, and R1 are calculated by the following equations:

$$C1 = \tau1 \left(1 - \frac{\tau2}{\tau3} \right) \quad C2 = \frac{\tau1 \times \tau2}{\tau3} \quad R1 = \frac{\tau3^2}{\tau1(\tau3 - \tau2)} \quad (1)$$

where,

$$\tau_1 = \frac{K_d K_{VCO}}{\omega_d^2} (\tan \Phi_d + \sec \Phi_d) \quad \tau_2 = \frac{1}{\omega_d (\tan \Phi_d + \sec \Phi_d)} \quad \tau_3 = \frac{\tan \Phi_d + \sec \Phi_d}{\omega_d} \quad (2)$$

charge pump current: $i_{qp} = 1 \text{ mA}$

vco gain: $K_{VCO} = 2\pi \times G_{VCO} \text{ rad/V}$

PFD Frequency: $\omega_d \leq 160 \text{ MHz}$

phase detector gain: $K_d = i_{qp} \div (2 \times \pi \times M) \text{ A/rad}$

An Excel spreadsheet is available from Texas Instruments for automatically calculating the values for C1, R1 and C2.

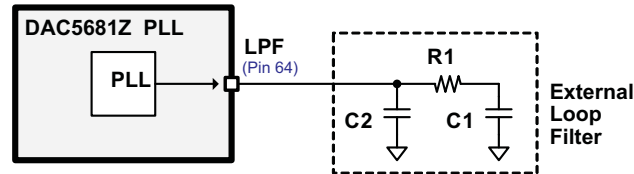


Figure 47. Recommended External Loop Filter Topology

APPLICATIONS EXAMPLES

DIGITAL INTERFACE AND CLOCKING CONSIDERATIONS FOR APPLICATION EXAMPLES

The DAC5681Z's LVDS digital input bus can be driven by an FPGA or digital ASIC. This input signal can be generated directly by the FPGA, or fed by a Texas Instruments Digital Up Converter (DUC) such as the GC5016 or GC5316. Optionally, a GC1115 Crest Factor Reduction (CFR) or Digital Pre-Distortion (DPD) processor may be inserted in the digital signal chain for improving the efficiency of high-power RF amplifiers. For the details on the DAC's high-rate digital interface, refer to the [LVDS Data Interfacing](#) section.

A low phase noise clock for the DAC at the final sample rate can be generated by a VCXO and a Clock Synchronizer/PLL such as the Texas Instruments CDCM7005 or CDCE62005, which can also provide other system clocks. An optional system clocking solution can use the DAC in clock multiplying PLL mode in order to avoid distributing a high-frequency clock at the DAC sample rate; however, the internal VCO phase noise of the DAC in PLL mode may degrade the quality of the DAC output signal.

DIGITAL IF OUTPUT RADIO

Refer to [Figure 48](#) for an example Digital IF Output Radio. The DAC5681Z receives a real digital input data stream and increases the sample rate through interpolation by a factor of 2 or 4. By performing digital interpolation on the input data, undesired images of the original signal can be pushed out of the band of interest and more easily suppressed with analog filters. Real mixing is available at each stage of interpolation using the LP/HP filter modes to upconvert the signal. (See Digital Real Upconversion section) The DAC output signal would typically be terminated with a transformer (see the [Analog Current Outputs](#) section). An IF filter, either LC or SAW, is used to suppress the DAC Nyquist zone images and other spurious signals before being mixed to RF with a mixer. The TRF3671 Frequency Synthesizer, with integrated VCO, may be used to drive a common LO input of the mixers for frequencies between 375 and 2380 MHz.

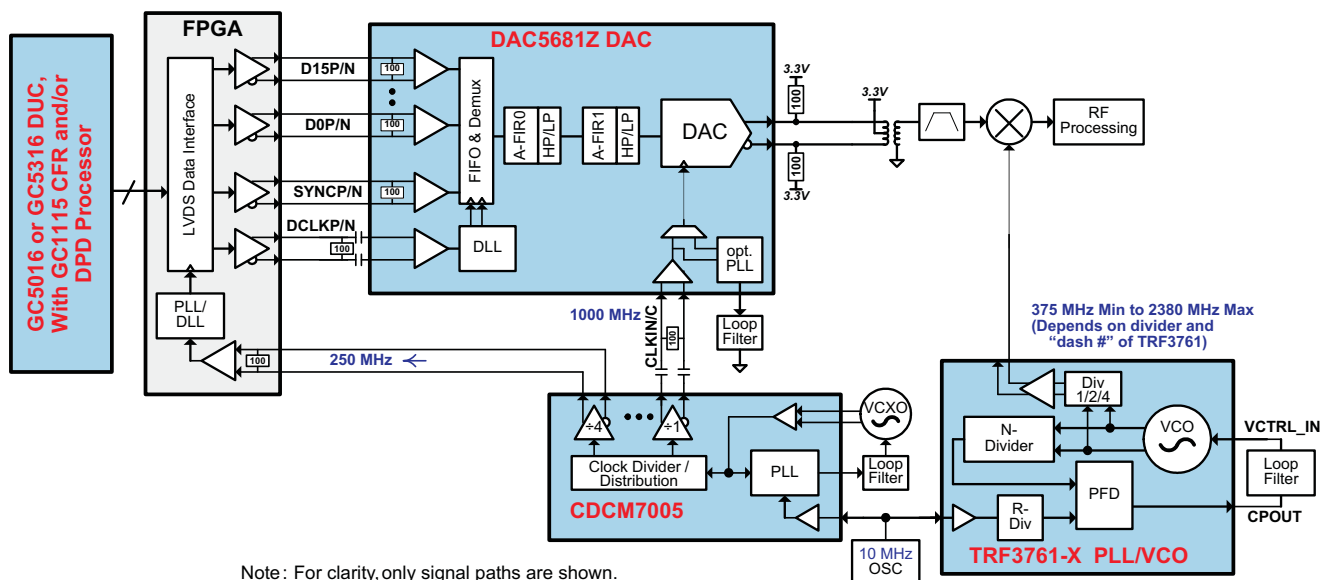


Figure 48. System Diagram of a Digital IF Output Radio

APPLICATIONS EXAMPLES (continued)

CMTS/VOD TRANSMITTER

The exceptional SNR of the DAC5681Z enables a cable modem termination system (CMTS) or video on demand (VOD) QAM transmitter in excess of the stringent DOCSIS specification, with >74 dBc and 75 dBc in the adjacent and alternate channels.

See [Figure 48](#) for an example IF Output Radio – this signal chain is nearly identical to a typical system using the DAC5681Z for a cost optimized two QAM transmitter. A GC5016 would accept two separate symbol rate inputs and provide pulse shaping and interpolation to ~ 128 MSPS. The two QAM carriers would be combined into two groups of two QAM carriers with intermediate frequencies of approximately 30 MHz to 40 MHz. The GC5016 would output data to the DAC5681Z through an FPGA for CMOS to LVDS translation. The DAC5681Z would provide 2x or 4x interpolation to increase the frequency of the 2nd Nyquist zone image. The signal is then output through a transformer and to an RF upconverter.

HIGH-SPEED ARBITRARY WAVEFORM GENERATOR

The 1GSPS bandwidth input data bus combined with the 16-bit DAC resolution of the DAC5681Z allows wideband signal generation for test and measurement applications. In this case, interpolation is not desired by the FPGA-based waveform generator as it can make use of the full Nyquist bandwidth of up to 500MHz.

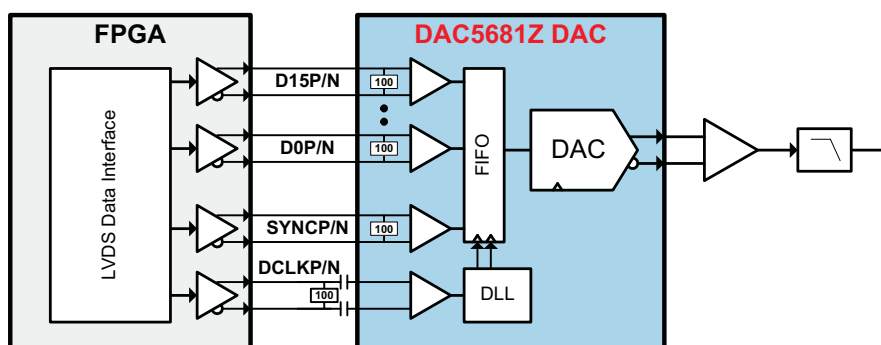


Figure 49. System Diagram of Arbitrary Waveform Generator

REVISION HISTORY

Changes from Revision D (September 2009) to Revision E	Page
• Changed defined by registers CONFIG1, CONFIG5 and CONFIG6 to defined byregisters CONFIG1 and CONFIG5.	39
• Changed in RECOMMENDED...PROCEDURE section, second sentence from "clkdiv_sync_dis and FIFO_sync_dis bits as wellinput." to "clkdiv_sync_dis as well.....input."	40
• Deleted "CONFIG5 FIFO_sync_dis = 0" from first and second ordered lists under RECMENDED.....PROCEDURE section.	40
<hr/>	
Changes from Revision E (March 2011) to Revision F	Page
• Changed the Revision to F, August 2012	1
• Changed graphic entity of Figure 36 for clarification.	36
• Changed the first paragraph of ANALOG CURRENT OUTPUTS section for clarification.	45

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
DAC5681ZIRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC5681ZIRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC5681ZIRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
DAC5681ZIRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



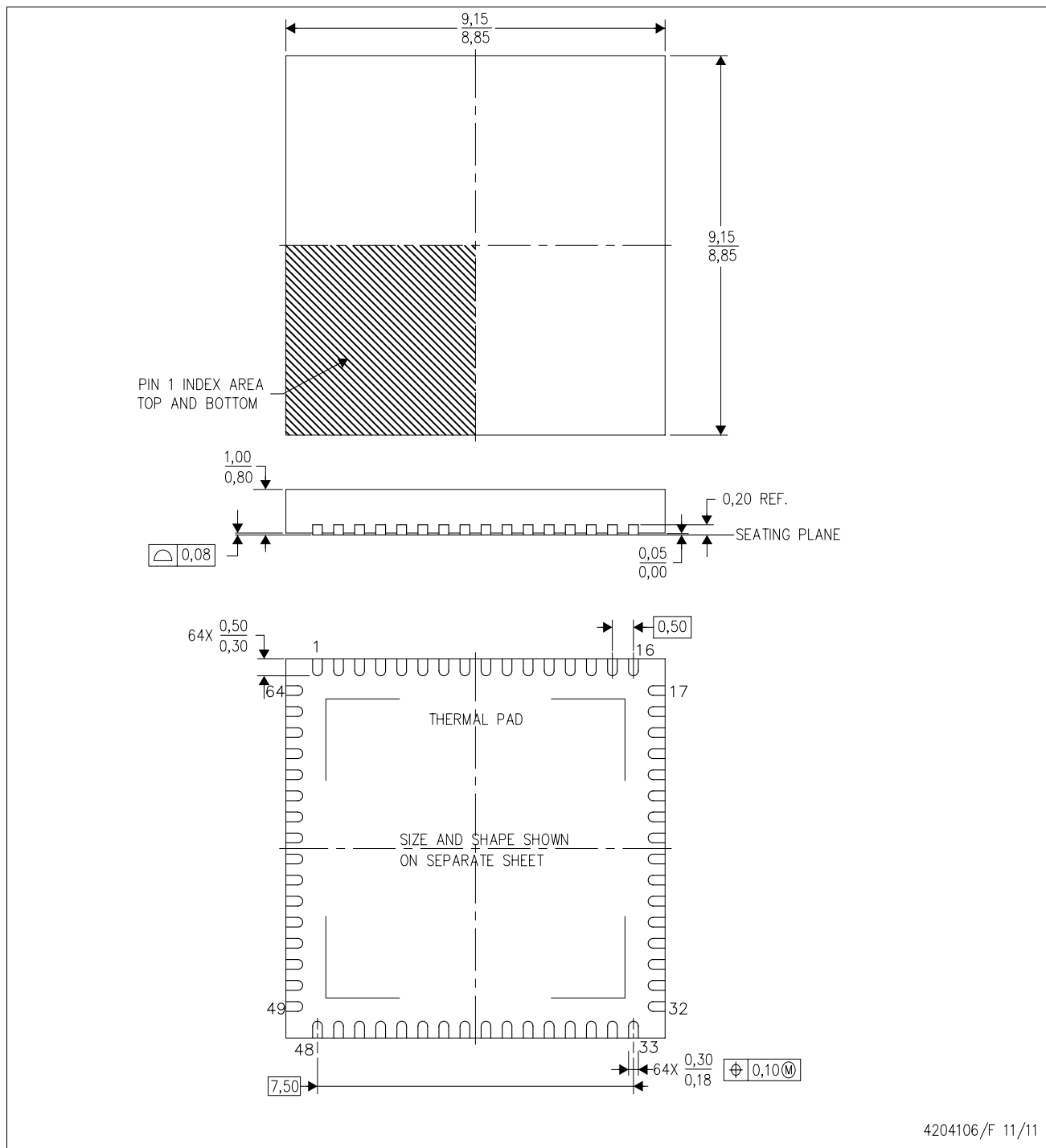
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC5681ZIRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
DAC5681ZIRGCT	VQFN	RGC	64	250	336.6	336.6	28.6

RGC(S-PVQFN-N64)

CUSTOM DEVICE

PLASTIC QUAD FLATPACK NO-LEAD



4204106/F 11/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RGC (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD

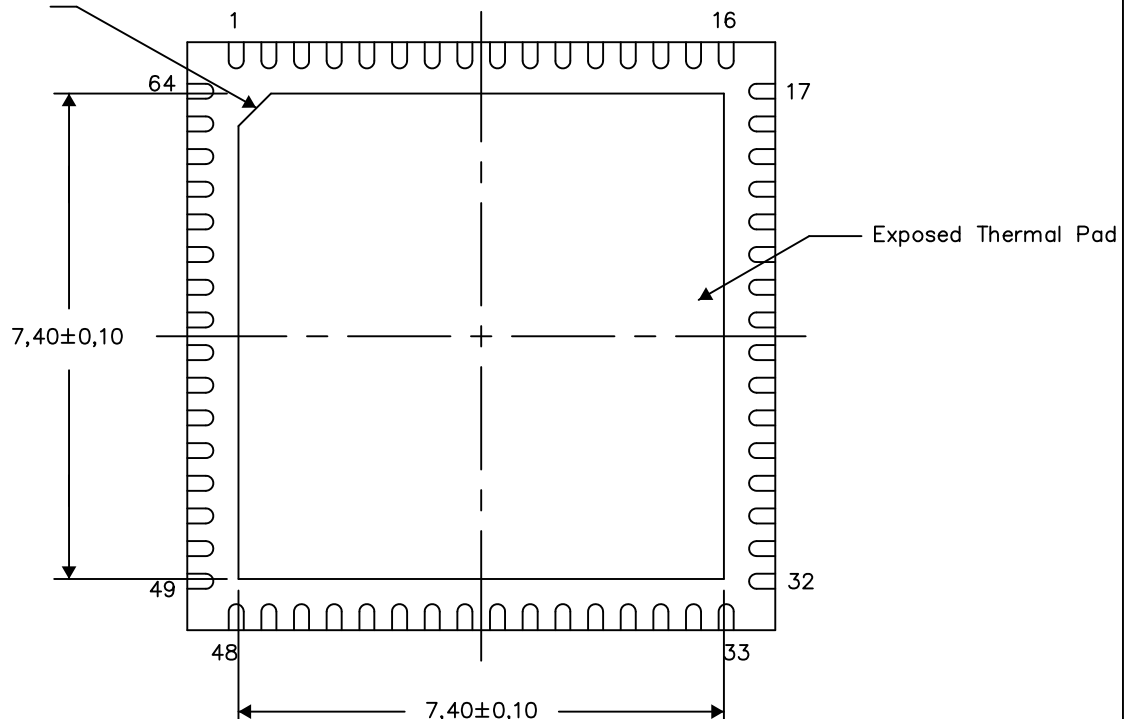
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR
CO,35

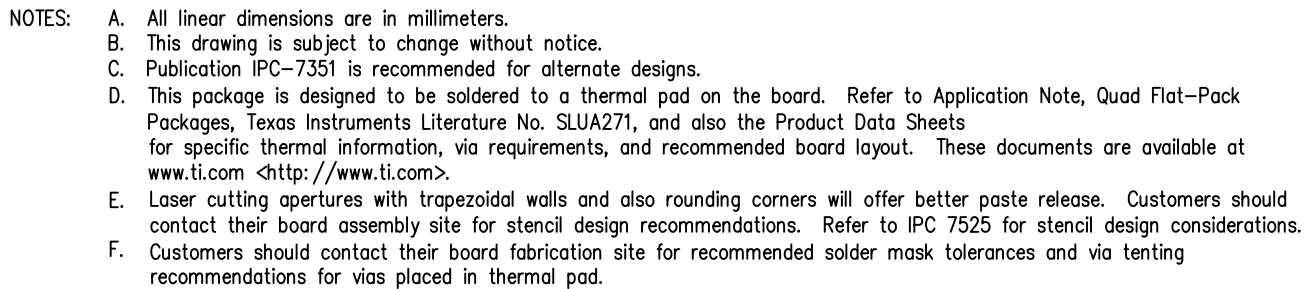


Bottom View

Exposed Thermal Pad Dimensions

4206192-4/U 08/12

NOTE: A. All linear dimensions are in millimeters



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