

60-V N-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD18563Q5A](#)

FEATURES

- Ultra Low Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- Logic Level
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

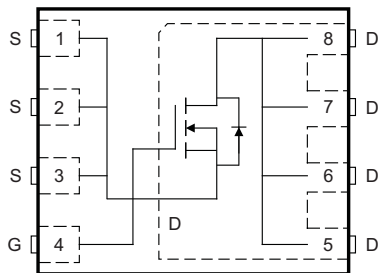
APPLICATIONS

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Motor Control

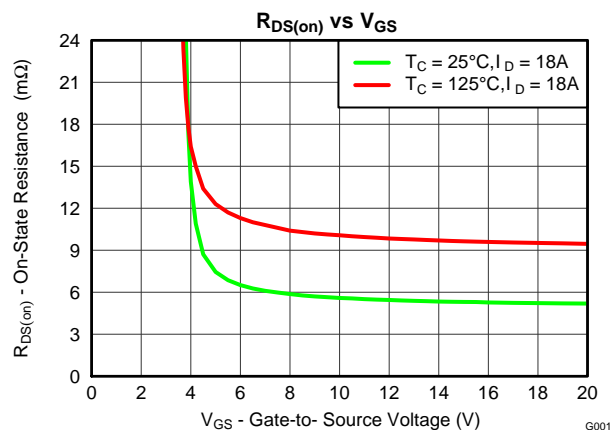
DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

Top View



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T _A = 25°C		TYPICAL VALUE		UNIT
V _{DS}	Drain to Source Voltage	60		V
Q _g	Gate Charge Total (10V)	15.0		nC
Q _{gd}	Gate Charge Gate to Drain	2.9		nC
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 4.5V	8.6	mΩ
		V _{GS} = 10V	5.7	mΩ
V _{GS(th)}	Threshold Voltage	2.0		V

ORDERING INFORMATION

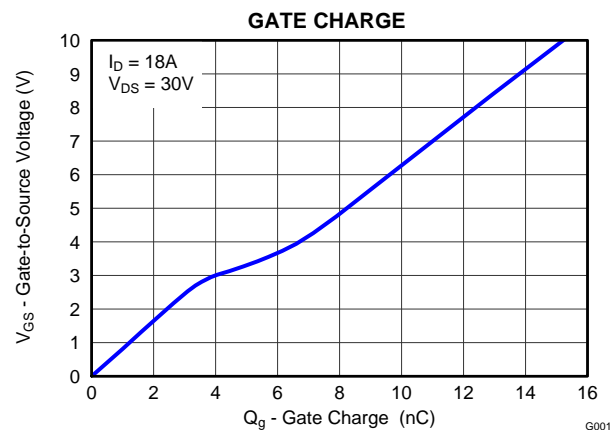
Device	Package	Media	Qty	Ship
CSD18563Q5A	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

T _A = 25°C		VALUE	UNIT
V _{DS}	Drain to Source Voltage	60	V
V _{GS}	Gate to Source Voltage	±20	V
I _D	Continuous Drain Current (Package limited), T _C = 25°C	100	A
	Continuous Drain Current (Silicon limited), T _C = 25°C	91	
	Continuous Drain Current, T _A = 25°C ⁽¹⁾	15	
I _{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	96	A
P _D	Power Dissipation ⁽¹⁾	3.2	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E _{AS}	Avalanche Energy, single pulse I _D = 54A, L = 0.1mH, R _G = 25Ω	146	mJ

(1) Typical R_{θJA} = 40°C/W on a 1-inch², 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Pulse duration ≤300μs, duty cycle ≤2%



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

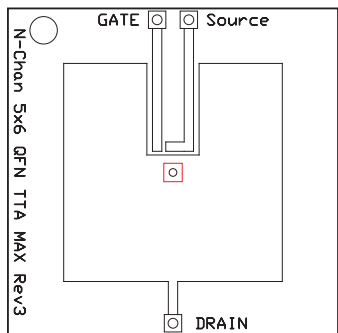
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
B _V DSS	Drain to Source Voltage	V _{GS} = 0V, I _D = 250μA	60			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 48V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = 20V			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1.7	2.0	2.4	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 4.5V, I _D = 18A		8.6	10.8	mΩ
		V _{GS} = 10V, I _D = 18A		5.7	6.8	mΩ
g _{fs}	Transconductance	V _{DS} = 30V, I _D = 18A		60		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 30V, f = 1MHz		1150	1500	pF
C _{oss}	Output Capacitance			280	364	pF
C _{rss}	Reverse Transfer Capacitance			3.9	5.1	pF
R _G	Series Gate Resistance			1.5	3.0	Ω
Q _g	Gate Charge Total (4.5V)	V _{DS} = 30V, I _D = 18A		7.3	9.5	nC
Q _g	Gate Charge Total (10V)			15	20	
Q _{gd}	Gate Charge Gate to Drain			2.9		nC
Q _{gs}	Gate Charge Gate to Source			3.3		nC
Q _{g(th)}	Gate Charge at V _{th}			2.3		nC
Q _{oss}	Output Charge	V _{DS} = 30V, V _{GS} = 0V		36		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 30V, V _{GS} = 10V, I _{DS} = 18A, R _G = 0Ω		3.2		ns
t _r	Rise Time			6.3		ns
t _{d(off)}	Turn Off Delay Time			11.4		ns
t _f	Fall Time			1.7		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{SD} = 18A, V _{GS} = 0V		0.8	1	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 30V, I _F = 18A, di/dt = 300A/μs		63		nC
t _{rr}	Reverse Recovery Time			49		ns

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

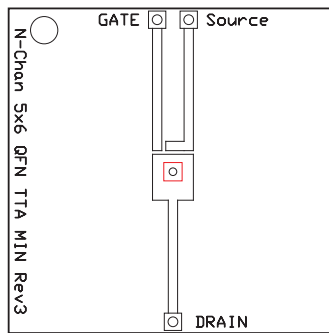
PARAMETER		MIN	TYP	MAX	UNIT
R _{θJC}	Thermal Resistance Junction to Case ⁽¹⁾			1.3	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			50	°C/W

- (1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



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Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of 2-
oz. (0.071-mm thick)
Cu.

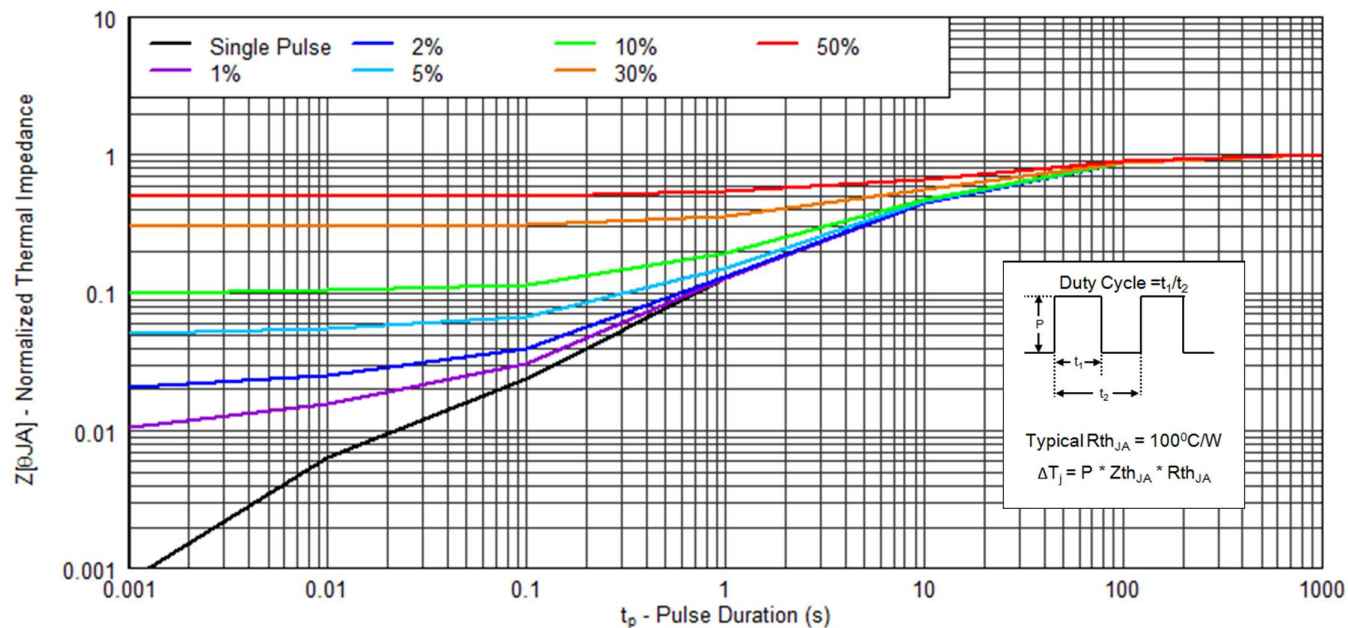


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Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



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Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

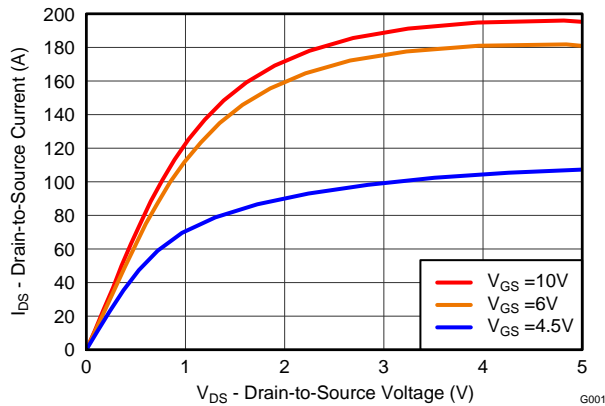


Figure 2. Saturation Characteristics

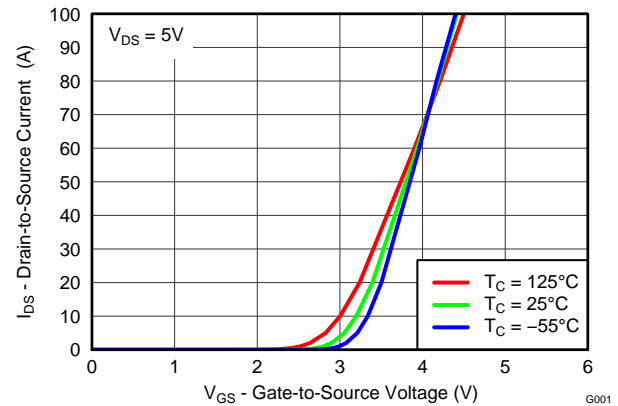


Figure 3. Transfer Characteristics

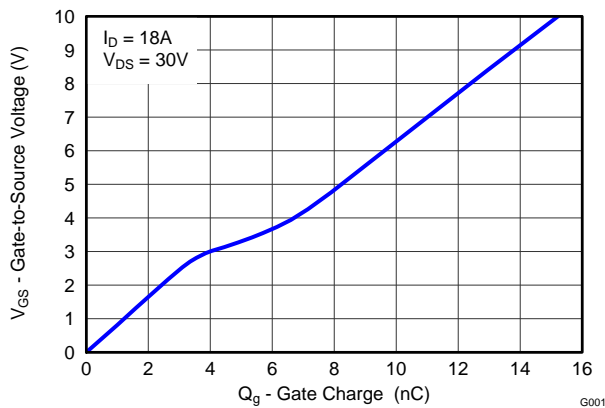


Figure 4. Gate Charge

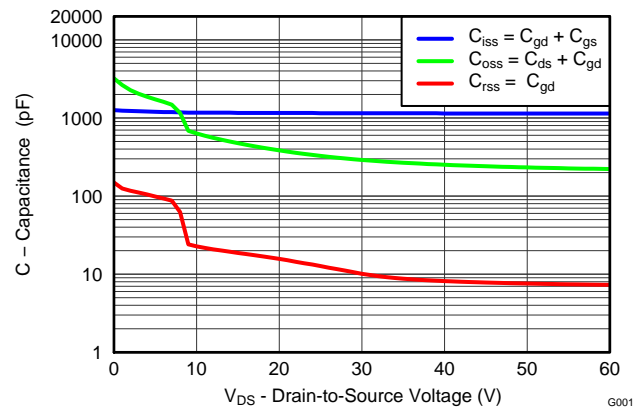


Figure 5. Capacitance

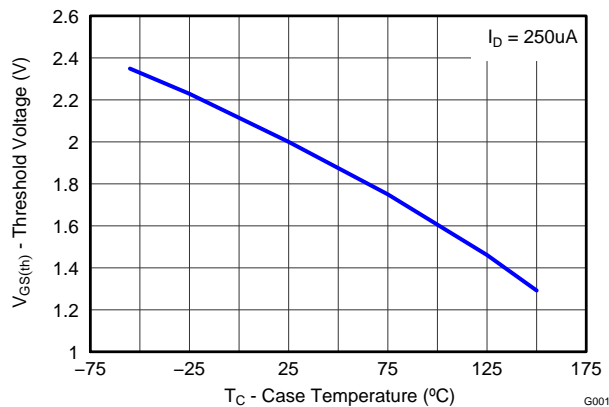


Figure 6. Threshold Voltage vs. Temperature

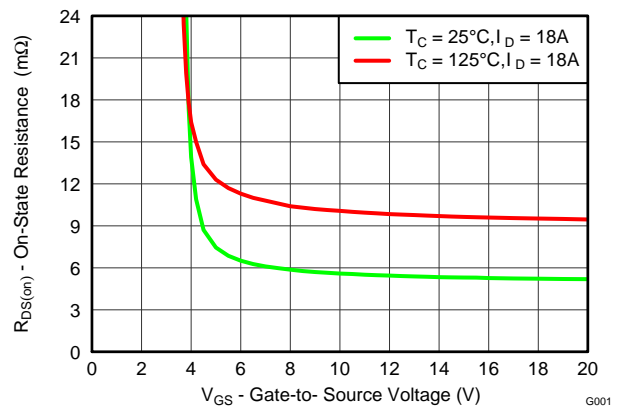


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

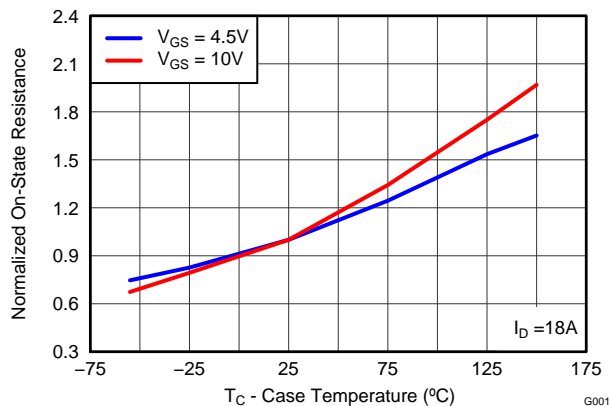


Figure 8. Normalized On-State Resistance vs. Temperature

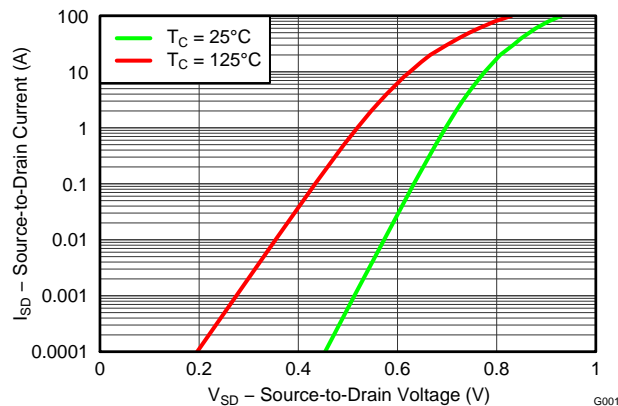


Figure 9. Typical Diode Forward Voltage

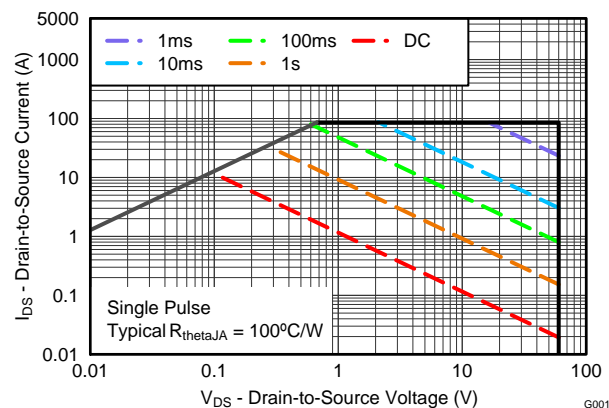


Figure 10. Maximum Safe Operating Area

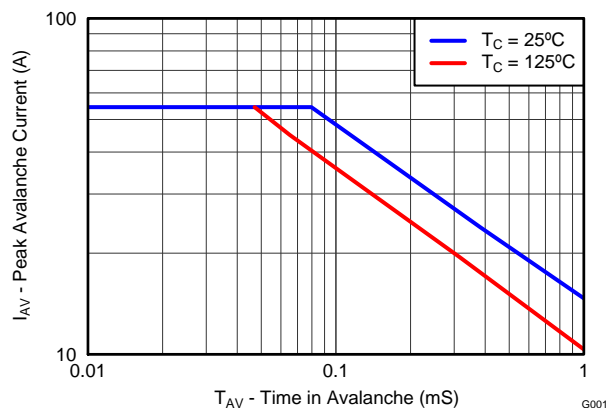


Figure 11. Single Pulse Unclamped Inductive Switching

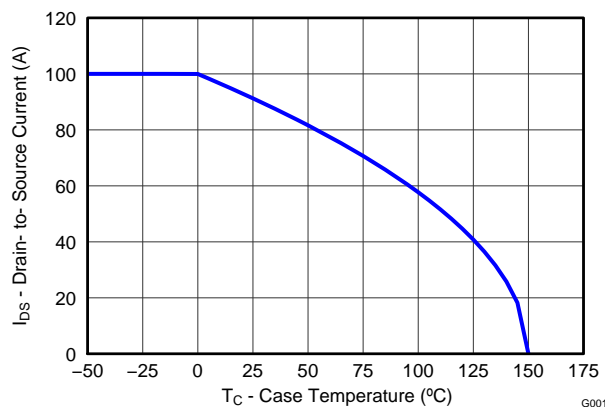
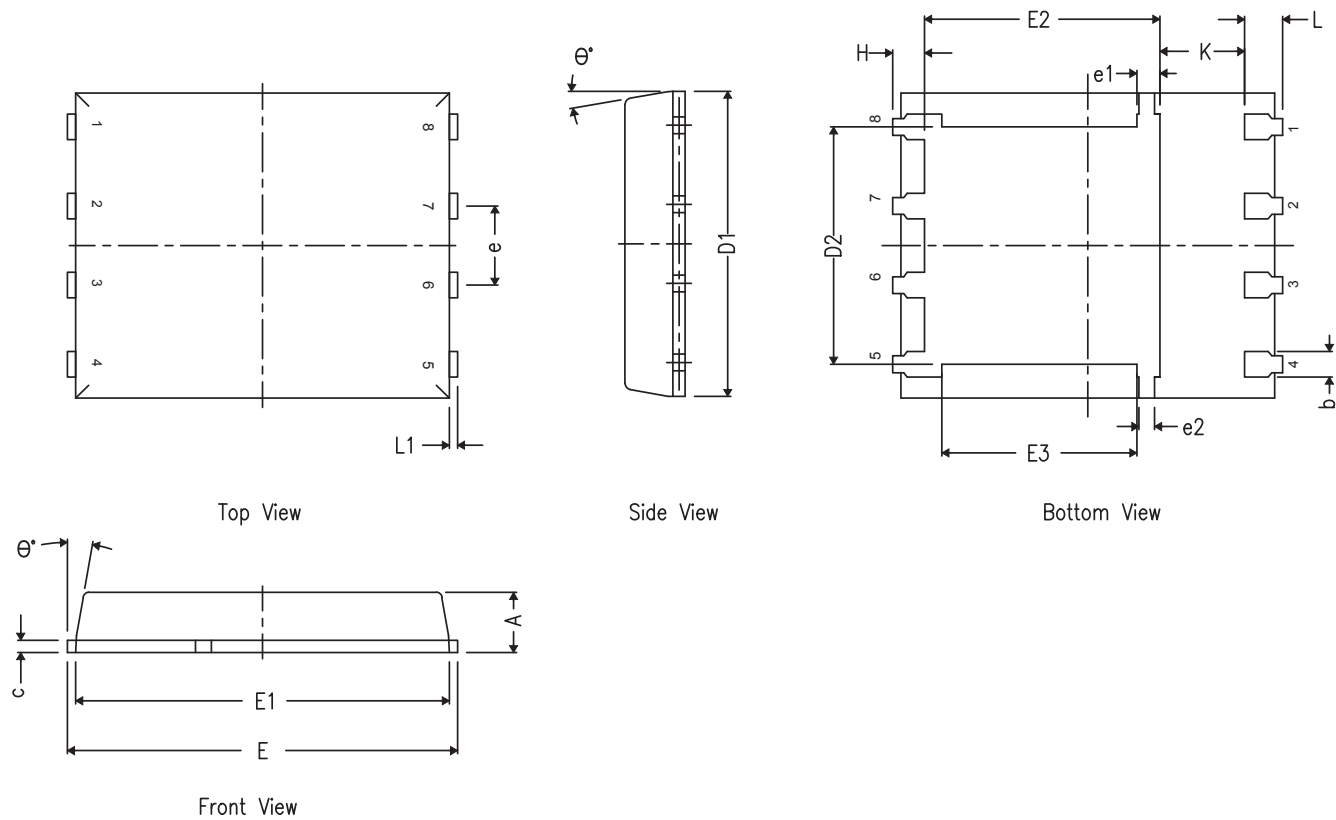


Figure 12. Maximum Drain Current vs. Temperature

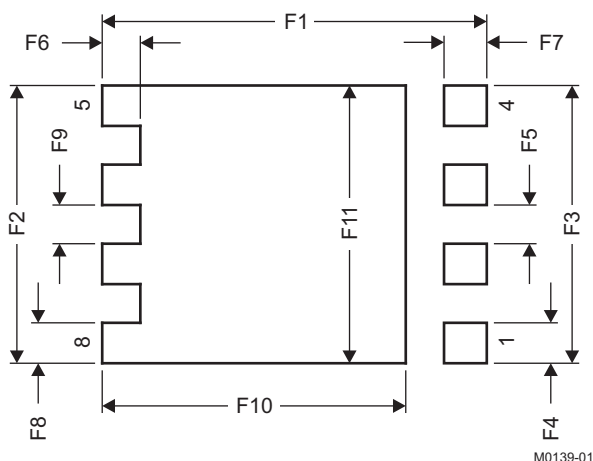
MECHANICAL DATA

Q5A Package Dimensions



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
E3	3.03	3.13	3.23
e	1.17	1.27	1.37
e1	0.27	0.37	0.47
e2	0.15	0.25	0.35
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°

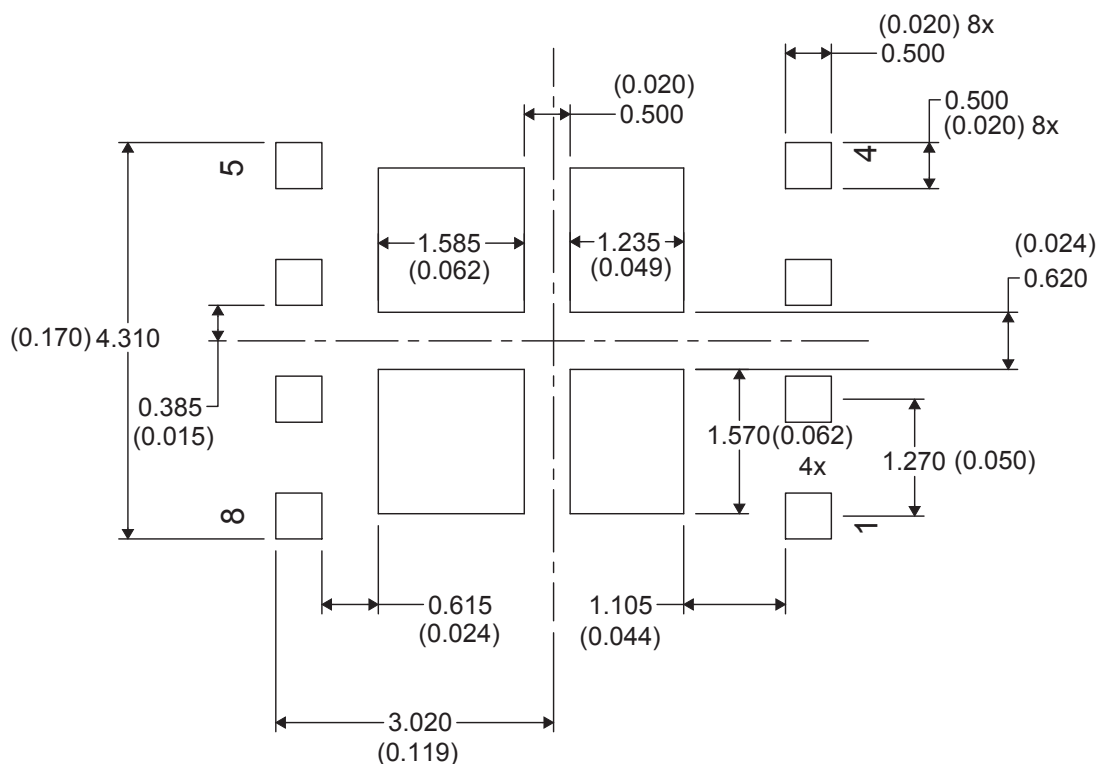
Recommended PCB Pattern



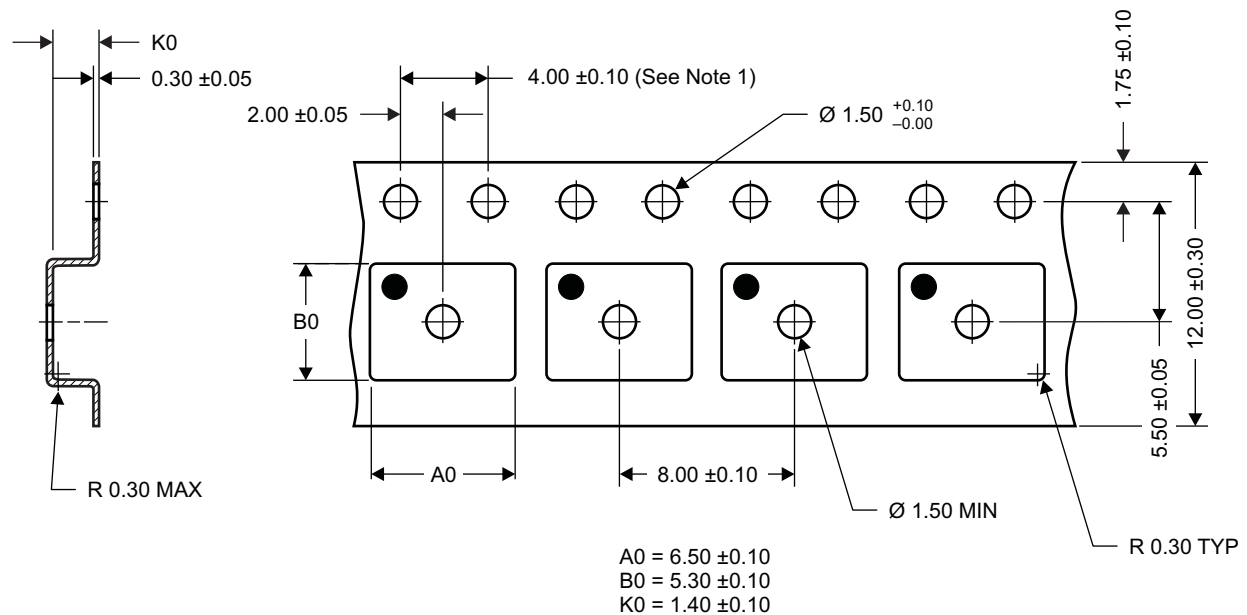
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Recommended Stencil Opening



Q5A Tape and Reel Information



M0138-01

Notes:

- 10-sprocket hole-pitch cumulative tolerance ± 0.2
- Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm (unless otherwise specified)
- $A0$ and $B0$ measured on a plane 0.3mm above the bottom of the pocket

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18563Q5A	ACTIVE	SON	DQJ	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD18563	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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