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SLPS321B -JUNE 2012-REVISED OCTOBER 2012

60V N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD18531Q5A

FEATURES

- Ultra Low Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- Logic Level
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

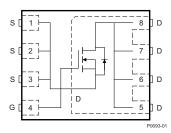
APPLICATIONS

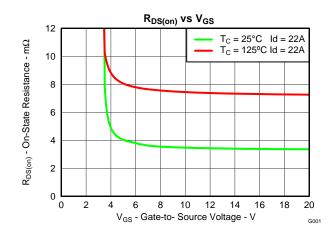
- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Battery Motor Control

DESCRIPTION

The NexFET[™] power MOSFET has been designed to minimize losses in power conversion applications.

Figure 1. Top View





PRODUCT SUMMARY

	/alues at 25°C therwise stated	TYPICAL VA	UNIT		
V _{DS}	Drain to Source Voltage	60		V	
Qg	Gate Charge Total (4.5V)	tal (4.5V) 18			
Q _{gd}	Gate Charge Gate to Drain	5.9	nC		
Р	Drain to Source On Resistance	$V_{GS} = 4.5V$	4.4	mΩ	
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 10V 3.5		mΩ	
V _{GS(th)}	Threshold Voltage	1.8	V		

ORDERING INFORMATION

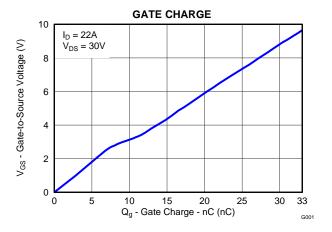
Device Package		Media	Qty	Ship		
CSD18531Q5A	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel		

ABSOLUTE MAXIMUM RATINGS

$T_A = 2$	5°C unless otherwise stated	VALUE	UNIT
V_{DS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	±20	V
	Continuous Drain Current (Package limited), $T_{C} = 25^{\circ}C$	100	
I _D	Continuous Drain Current (Silicon limited), $T_{C} = 25^{\circ}C$	134	A
	Continuous Drain Current, $T_A = 25^{\circ}C^{(1)}$	19	
I _{DM}	Pulsed Drain Current, $T_A = 25^{\circ}C^{(2)}$	122	А
PD	Power Dissipation ⁽¹⁾	3.1	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E _{AS}	Avalanche Energy, single pulse I_D = 67A, L = 0.1mH, R_G = 25 Ω	224	mJ

(1) Typical $R_{\theta JA}$ = 40°C/W on a 1-inch², 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Pulse duration \leq 300µs, duty cycle \leq 2%



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

$(T_A = 25^{\circ}C \text{ unless otherwise stated})$

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
Static Cl	haracteristics				
BV _{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	60		V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 48V		1	μA
I _{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = 20V$		100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.5 1.8	2.3	V
		V _{GS} = 4.5V, I _D = 22A	4.4	5.8	mΩ
R _{DS(on)}	Drain to Source On Resistance	$V_{GS} = 10V, I_D = 22A$	3.5	4.6	mΩ
9 _{fs}	Transconductance	V _{DS} = 30V, I _D = 22A	128		S
Dynamic	Characteristics	· ·		4	
C _{iss}	Input Capacitance		3200	3840	pF
C _{oss}	Output Capacitance	$V_{GS} = 0V, V_{DS} = 30V, f = 1MHz$	380	456	pF
C _{rss}	Reverse Transfer Capacitance		11	14	pF
R _G	Series Gate Resistance		1.2	2.4	Ω
Qg	Gate Charge Total (4.5V)		18	22	
Qg	Gate Charge Total (10V)		36	43	nC
Q _{gd}	Gate Charge Gate to Drain	$V_{DS} = 30V, I_D = 22A$	5.9		nC
Q _{gs}	Gate Charge Gate to Source		6.9		nC
Q _{g(th)}	Gate Charge at Vth		5.2		nC
Q _{oss}	Output Charge	$V_{DS} = 30V, V_{GS} = 0V$	32		nC
t _{d(on)}	Turn On Delay Time		4.4		ns
t _r	Rise Time	$V_{DS} = 30V, V_{GS} = 10V,$	7.8		ns
t _{d(off)}	Turn Off Delay Time	$I_{DS} = 22A, R_G = 0\Omega$	20		ns
t _f	Fall Time		2.7		ns
Diode C	haracteristics				
V _{SD}	Diode Forward Voltage	$I_{SD} = 22A, V_{GS} = 0V$	0.8	1	V
Q _{rr}	Reverse Recovery Charge	V_{DS} = 30V, I _F = 22A,	100		nC
t _{rr}	Reverse Recovery Time	di/dt = 300A/µs	40		ns

THERMAL CHARACTERISTICS

($T_A = 25^{\circ}C$ unless otherwise stated)

	PARAMETER	MIN	TYP	MAX	UNIT
$R_{ extsf{ heta}JC}$	Thermal Resistance Junction to Case ⁽¹⁾			1	°C/W
R_{\thetaJA}	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			50	°C/W

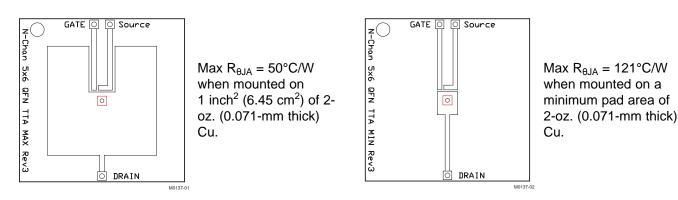
(1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



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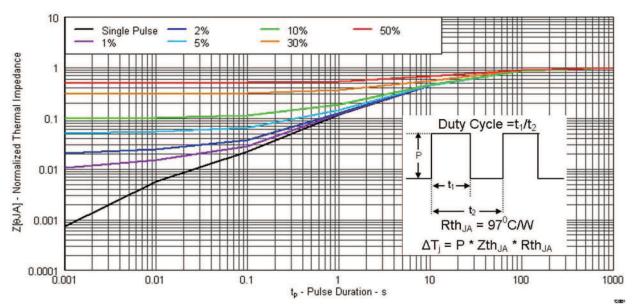
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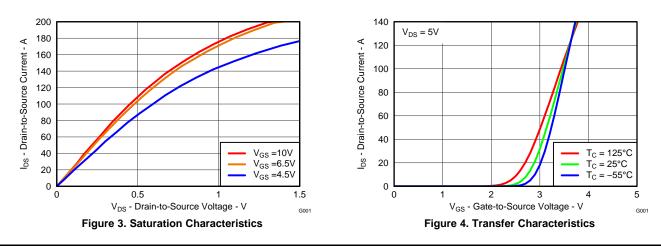


TYPICAL MOSFET CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$







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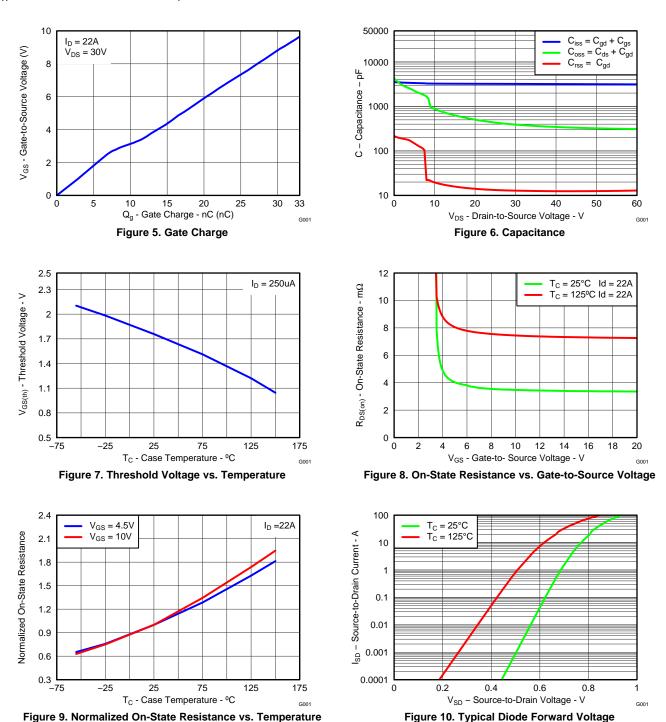
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NSTRUMENTS

FEXAS

TYPICAL MOSFET CHARACTERISTICS (continued)

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$





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TYPICAL MOSFET CHARACTERISTICS (continued)

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

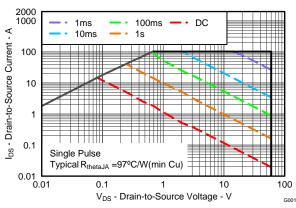
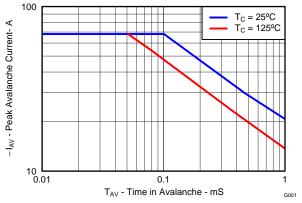


Figure 11. Maximum Safe Operating Area





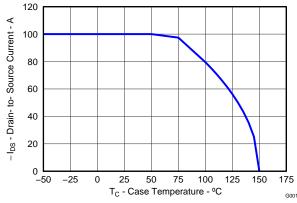


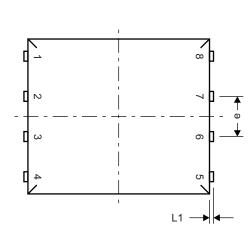
Figure 13. Maximum Drain Current vs. Temperature

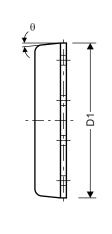
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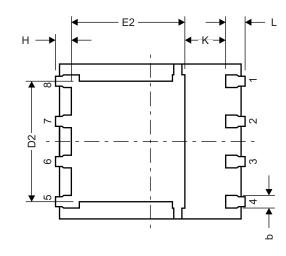
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MECHANICAL DATA

Q5A Package Dimensions



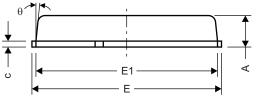




Top View

Side View

Bottom View



Front View

M0135-01

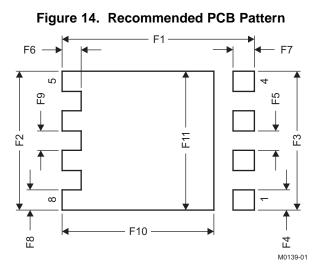
DIM		MILLIMETERS	
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
С	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
е	1.17	1.27	1.37
Н	0.41	0.56	0.71
К	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°



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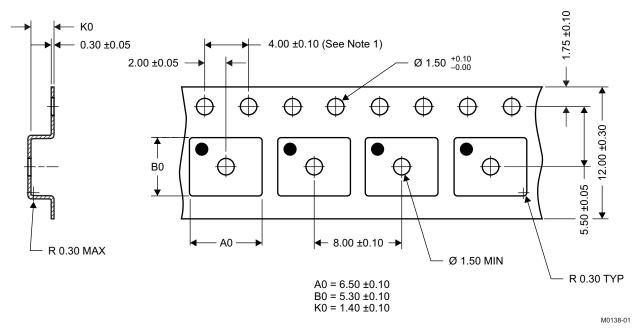
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DIM	MILLIM	ETERS	INCHES				
DIN	MIN	MAX	MIN	MAX			
F1	6.205	6.305	0.244	0.248			
F2	4.46	4.56	0.176	0.18			
F3	4.46	4.56	0.176	0.18			
F4	0.65	0.7	0.026	0.028			
F5	0.62	0.67	0.024	0.026			
F6	0.63	0.68	0.025	0.027			
F7	0.7	0.8	0.028	0.031			
F8	0.65	0.7	0.026	0.028			
F9	0.62	0.67	0.024	0.026			
F10	4.9	5	0.193	0.197			
F11	4.46	4.56	0.176	0.18			

For recommended circuit layout for PCB designs, see application note SLPA005 – Reducing Ringing Through PCB Layout Techniques.

Q5A Tape and Reel Information



Notes:

- 1. 10-sprocket hole-pitch cumulative tolerance ±0.2
- 2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- 3. Material: black static-dissipative polystyrene
- 4. All dimensions are in mm (unless otherwise specified)
- 5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

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REVISION HISTORY



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13-Jun-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)		(3)		(4/5)	
CSD18531Q5A	ACTIVE	SON	DQJ	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD18531	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18531Q5A	SON	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

15-Sep-2012



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18531Q5A	SON	DQJ	8	2500	340.0	340.0	38.0

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