

30-V, N-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD17551Q3A](#)

FEATURES

- Ultra Low Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3-mm × 3.3-mm Plastic Package

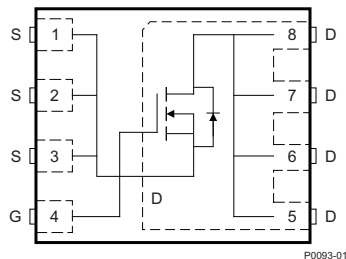
APPLICATIONS

- Point of load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Control FET Applications

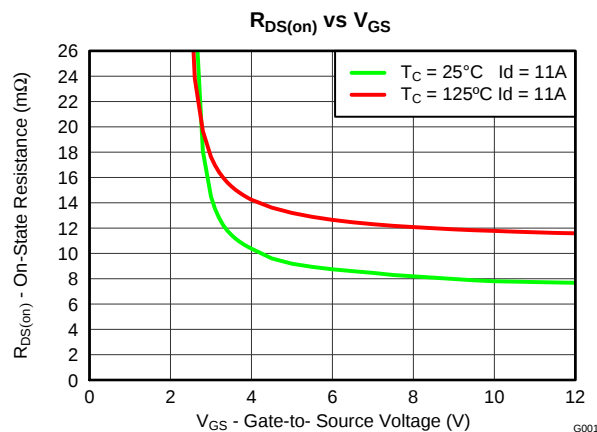
DESCRIPTION

The NexFET power MOSFET has been designed to minimize losses in power conversion applications.

Figure 1. Top View



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PRODUCT SUMMARY

V _{DS}	Drain to Source Voltage	30	V
Q _g	Gate Charge Total (4.5V)	6.0	nC
Q _{gd}	Gate Charge Gate to Drain	1.5	nC
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 4.5V	9.6 mΩ
		V _{GS} = 10V	7.8 mΩ
V _{GS(th)}	Threshold Voltage	1.6	V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD17551Q3A	SON 3.3-mm × 3.3-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

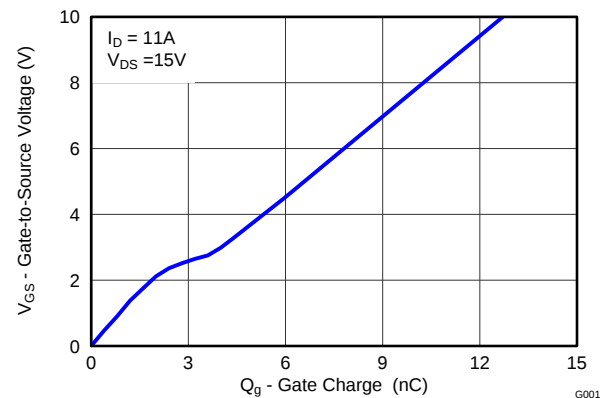
ABSOLUTE MAXIMUM RATINGS

T _A = 25°C unless otherwise stated		VALUE	UNIT
V _{DS}	Drain to Source Voltage	30	V
V _{GS}	Gate to Source Voltage	±20	V
I _D	Continuous Drain Current, T _C = 25°C	48	A
	Continuous Drain Current, Silicon Limited	48	A
	Continuous Drain Current, T _A = 25°C ⁽¹⁾	12	A
I _{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	71	A
P _D	Power Dissipation ⁽¹⁾	2.6	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E _{AS}	Avalanche Energy, single pulse I _D = 25A, L = 0.1mH, R _G = 25Ω	31	mJ

(1) Typical R_{θJA} = 48°C/W on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤300μs, duty cycle ≤2%

GATE CHARGE



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Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

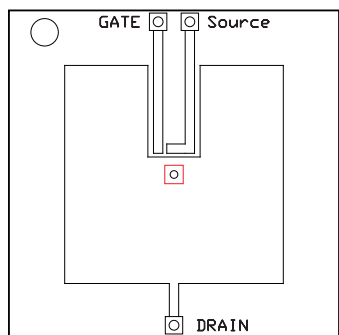
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _D = 250μA	30			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 24V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = 20V			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1.1	1.6	2.1	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 4.5V, I _D = 11A		9.6	11.8	mΩ
		V _{GS} = 10V, I _D = 11A		7.8	9.0	mΩ
g _{fs}	Transconductance	V _{DS} = 15V, I _D = 11A		101		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		1050	1370	pF
C _{oss}	Output Capacitance			244	317	pF
C _{rss}	Reverse Transfer Capacitance			24	31	pF
R _G	Series Gate Resistance			1.5	3.0	Ω
Q _g	Gate Charge Total (4.5V)	V _{DS} = 15V, I _D = 11A		6.0	7.8	nC
Q _{gd}	Gate Charge Gate to Drain			1.5		nC
Q _{gs}	Gate Charge Gate to Source			2.3		nC
Q _{g(th)}	Gate Charge at V _{th}			1.4		nC
Q _{oss}	Output Charge	V _{DS} = 15V, V _{GS} = 0V		7.4		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 15V, V _{GS} = 4.5V, I _{DS} = 11A, R _G = 2Ω		8.0		ns
t _r	Rise Time			24		ns
t _{d(off)}	Turn Off Delay Time			12		ns
t _f	Fall Time			3.4		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{SD} = 11A, V _{GS} = 0V		0.8	1	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 13.5V, I _F = 11A, di/dt = 300A/μs		13		nC
t _{rr}	Reverse Recovery Time			14		ns

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

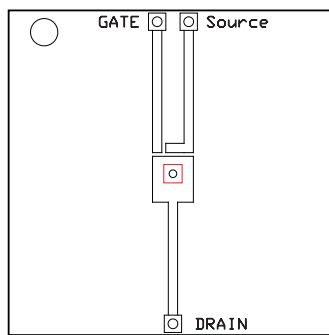
PARAMETER		MIN	TYP	MAX	UNIT
R _{θJC}	Thermal Resistance Junction to Case ⁽¹⁾			3.9	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			60	°C/W

- (1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



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Max $R_{\theta JA} = 60^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of 2-
oz. (0.071-mm thick)
Cu.

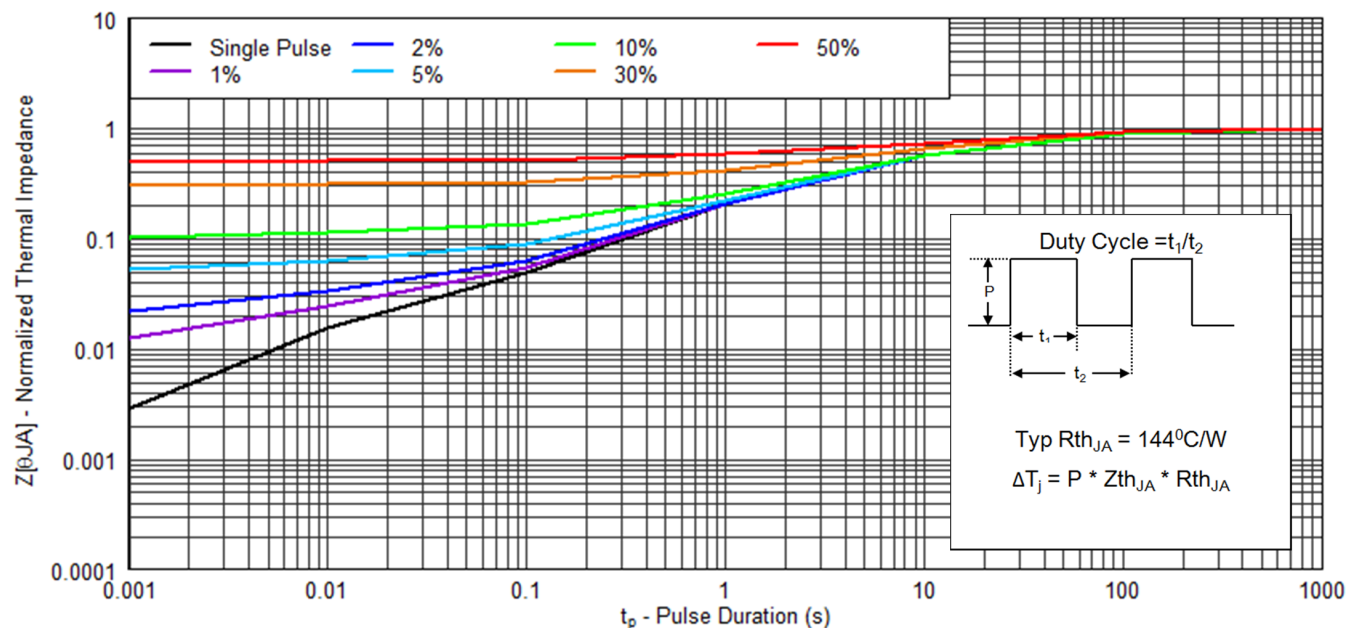


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Max $R_{\theta JA} = 144^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



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Figure 2. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

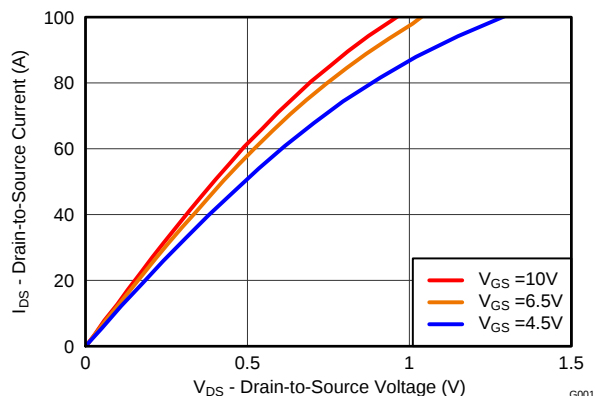


Figure 3. Saturation Characteristics

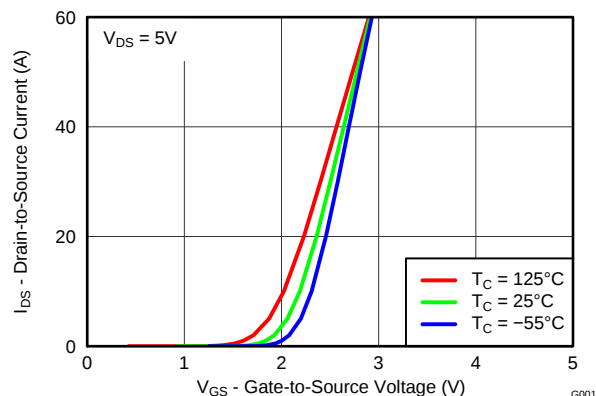


Figure 4. Transfer Characteristics

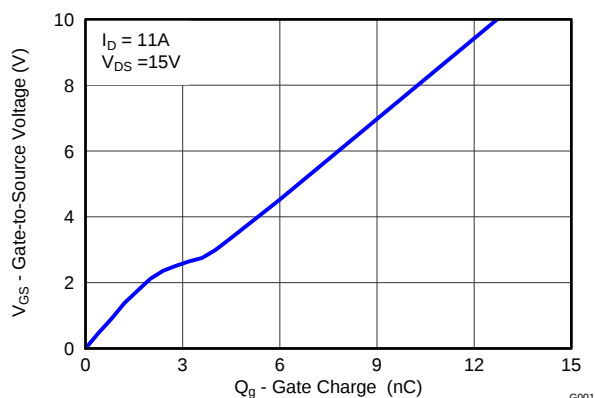


Figure 5. Gate Charge

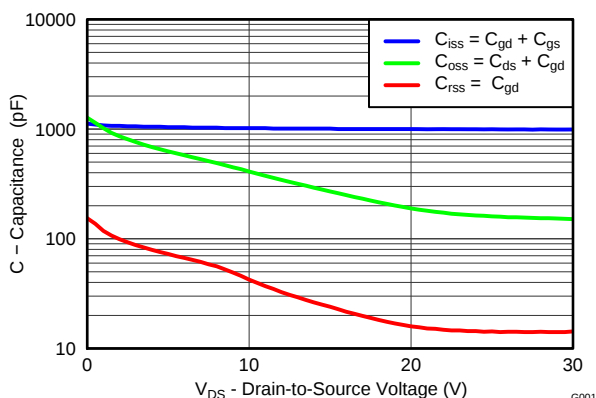


Figure 6. Capacitance

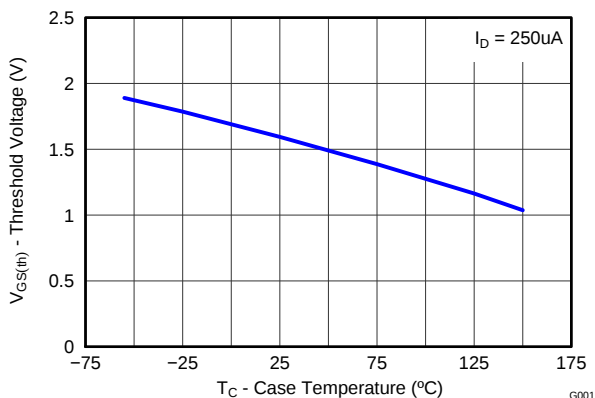


Figure 7. Threshold Voltage vs. Temperature

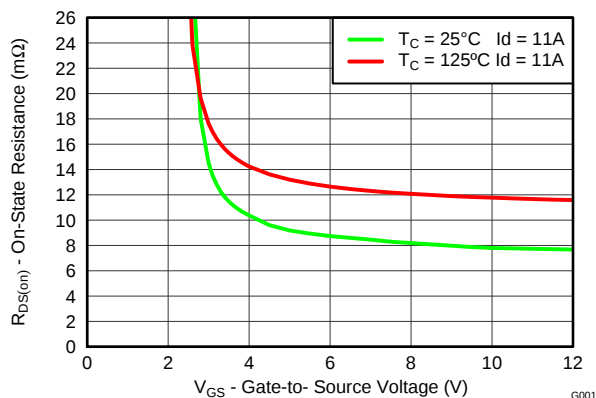


Figure 8. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

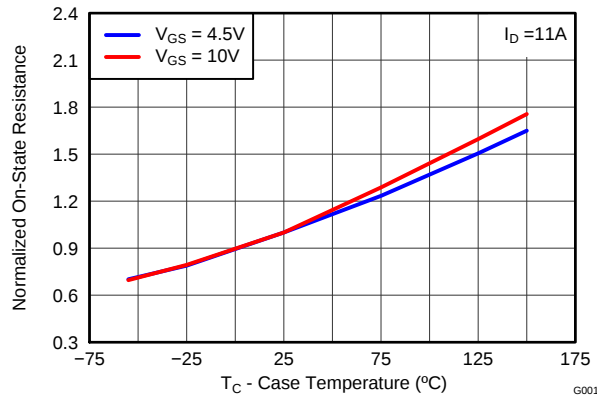


Figure 9. Normalized On-State Resistance vs. Temperature

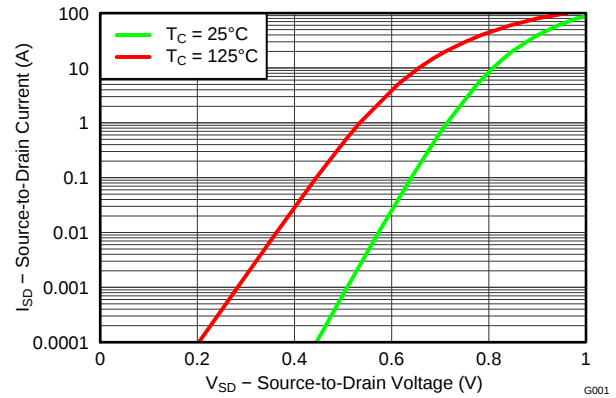


Figure 10. Typical Diode Forward Voltage

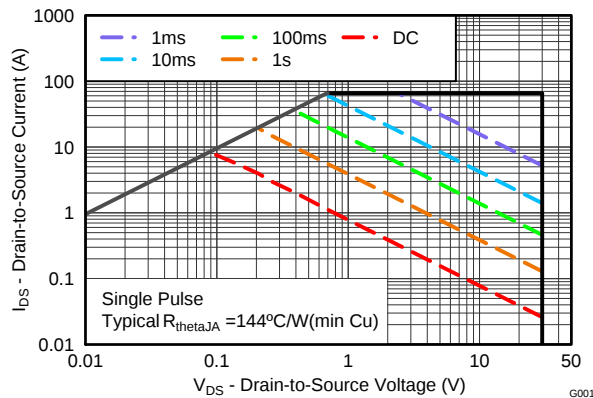


Figure 11. Maximum Safe Operating Area

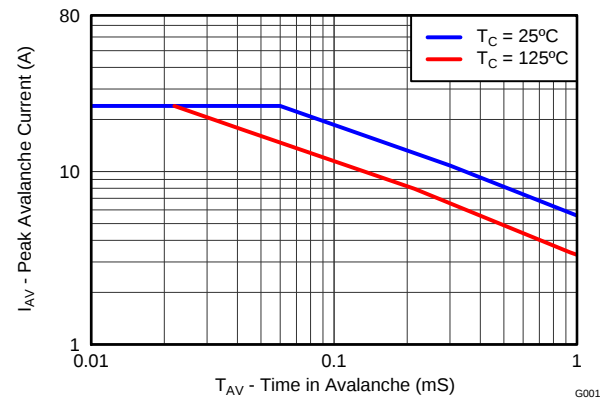


Figure 12. Single Pulse Unclamped Inductive Switching

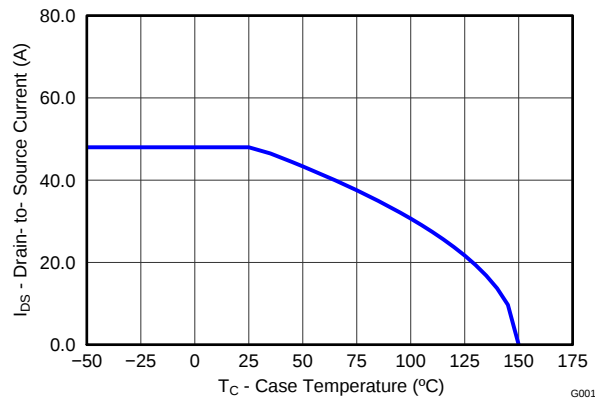
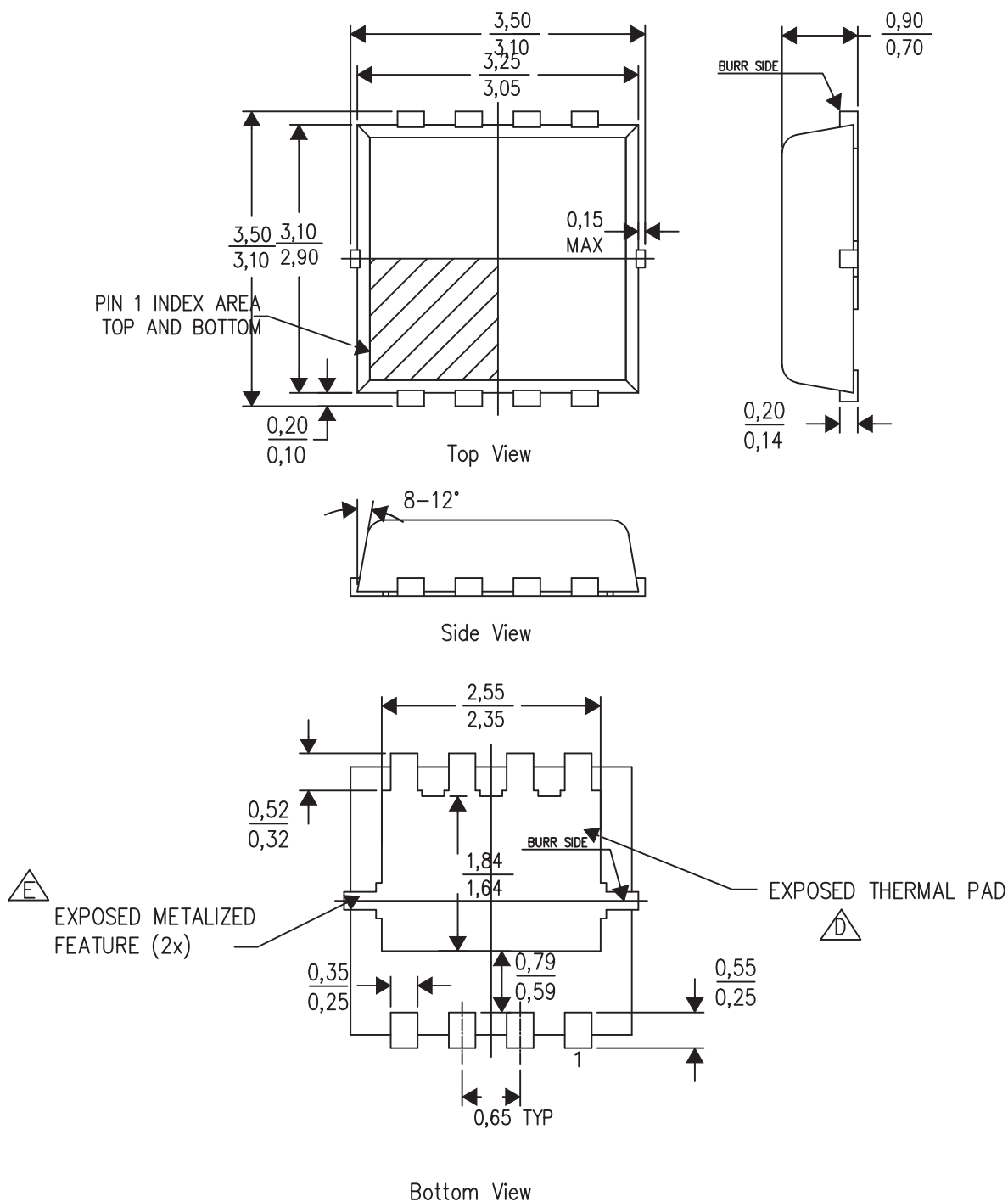


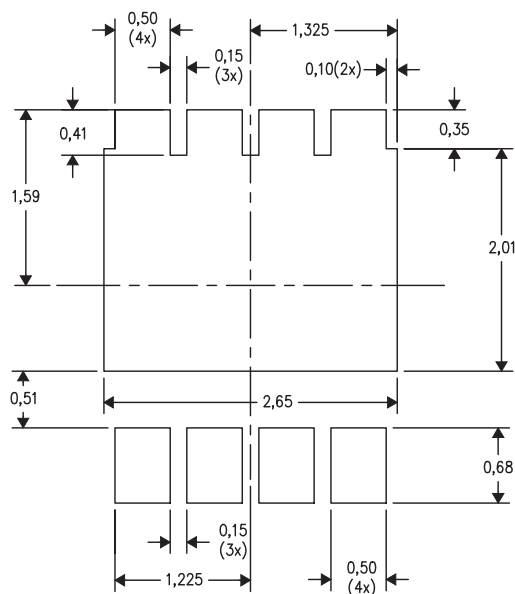
Figure 13. Maximum Drain Current vs. Temperature

MECHANICAL DATA

Q3A Package Dimensions

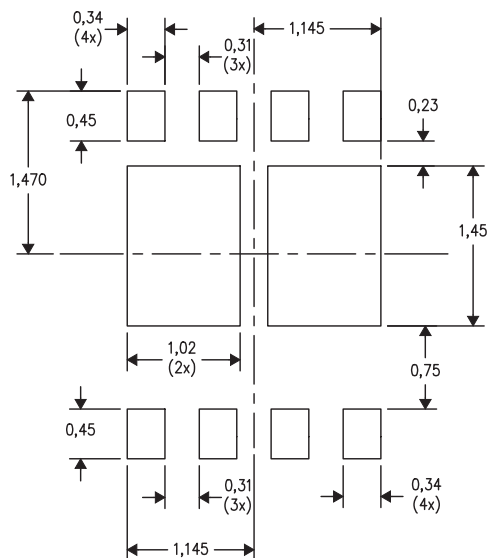


Q3A Recommended PCB Pattern

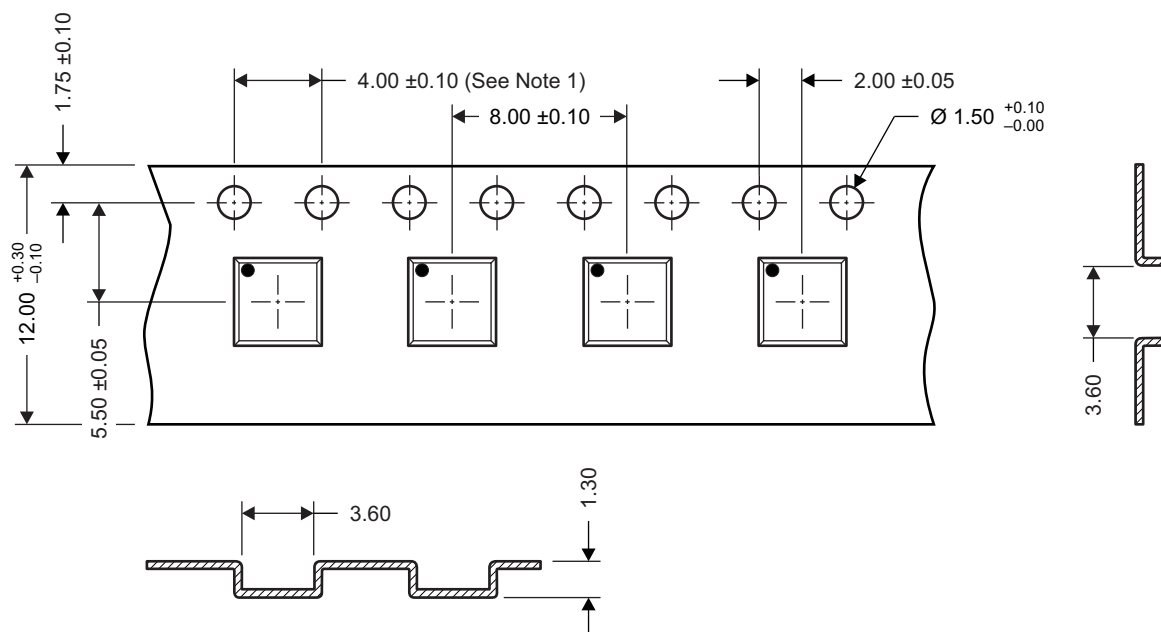


For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

Q3A Recommended Stencil Pattern



Q3A Tape and Reel Information



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- Notes:
1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
 2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
 3. Material: black static-dissipative polystyrene
 4. All dimensions are in mm, unless otherwise specified.
 5. Thickness: 0.30 ± 0.05 mm
 6. MSL1 260°C (IR and convection) PbF reflow compatible

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CSD17551Q3A	ACTIVE	VSON	DNH	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

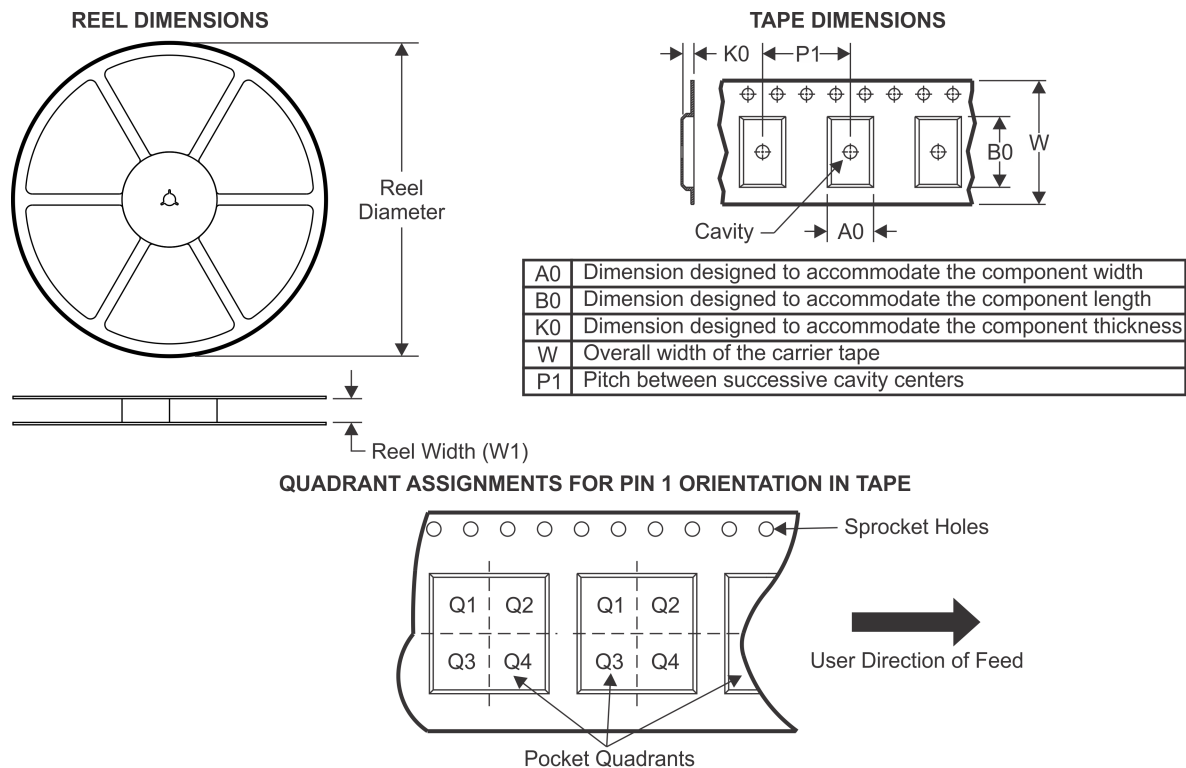
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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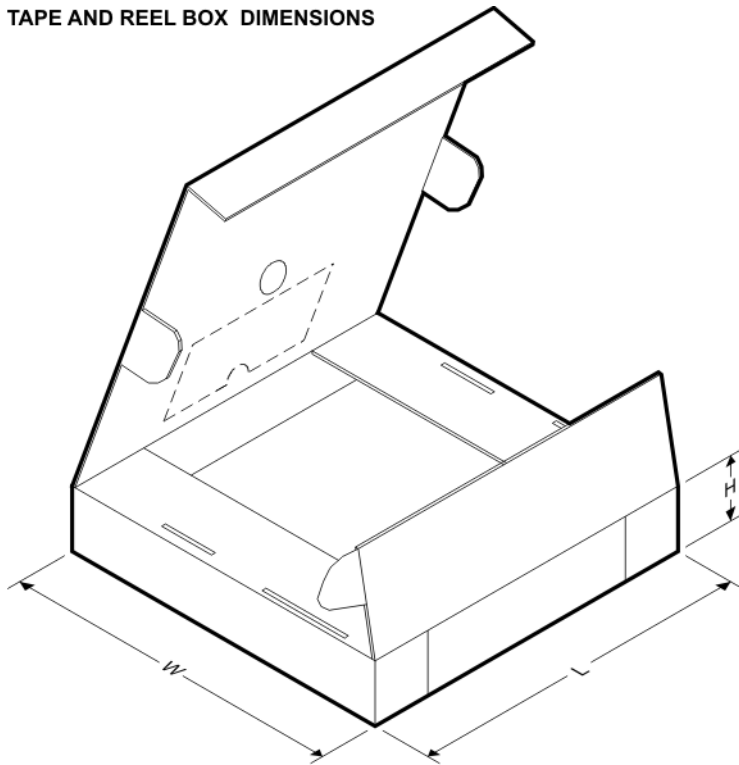
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17551Q3A	VSON	DNH	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17551Q3A	VSON	DNH	8	2500	340.0	340.0	38.0

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