

30V, N-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD17327Q5A](#)

FEATURES

- **Ultralow Q_g and Q_{gd}**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 5-mm × 6-mm Plastic Package**

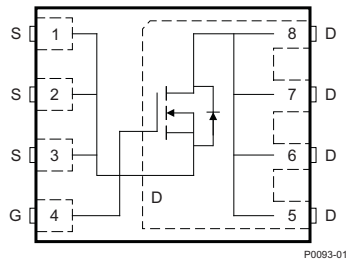
APPLICATIONS

- **Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems**
- **Optimized for Control FET Applications**

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

Top View



P0093-01

PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	30	V
Q_g	Gate Charge Total (4.5V)	2.8	nC
Q_{gd}	Gate Charge Gate to Drain	0.8	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V$	12.5 mΩ
		$V_{GS} = 8V$	9.9 mΩ
$V_{GS(th)}$	Threshold Voltage	1.6	V

ORDERING INFORMATION

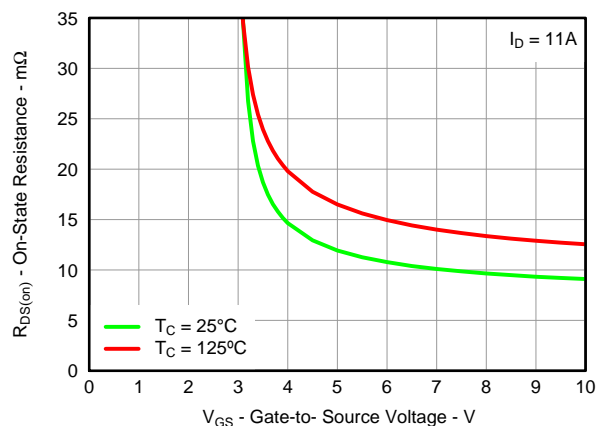
Device	Package	Media	Qty	Ship
CSD17327Q5A	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

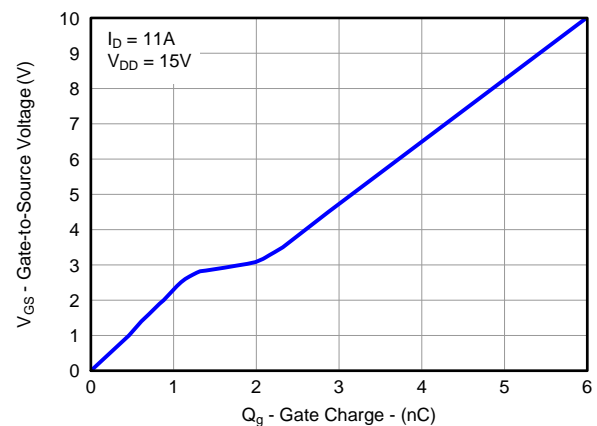
$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	+10 / -10	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	65	A
	Continuous Drain Current ⁽¹⁾	13	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	85	A
P_D	Power Dissipation ⁽¹⁾	3	W
T_J , T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E_{AS}	Avalanche Energy, single pulse $I_D = 30A$, $L = 0.1mH$, $R_G = 25\Omega$	45	mJ

(1) Typical $R_{\theta JA} = 44^\circ\text{C/W}$ on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

 $R_{DS(on)}$ vs V_{GS}


GATE CHARGE



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

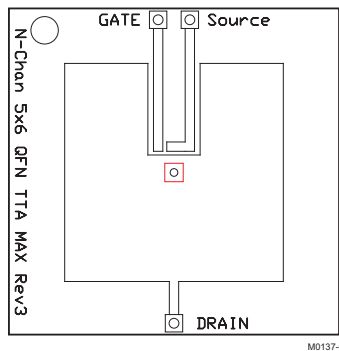
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
B _V D _{SS}	Drain to Source Voltage	V _{GS} = 0V, I _{DS} = 250μA	30			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 24V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = +10/-10V			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = 250μA	1.1	1.6	2.0	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 4.5V, I _{DS} = 11A		12.5	15.5	mΩ
		V _{GS} = 8V, I _{DS} = 11A		9.9	12.2	mΩ
g _{fs}	Transconductance	V _{DS} = 15V, I _{DS} = 11A		44		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		422	506	pF
C _{oss}	Output Capacitance			286	343	pF
C _{rss}	Reverse Transfer Capacitance			26	33	pF
R _G	Series Gate Resistance			4.7		Ω
Q _g	Gate Charge Total (4.5V)	V _{DS} = 15V, I _{DS} = 11A		2.8	3.4	nC
Q _{gd}	Gate Charge Gate to Drain			0.8		nC
Q _{gs}	Gate Charge Gate to Source			1.2		nC
Q _{g(th)}	Gate Charge at V _{th}			0.6		nC
Q _{oss}	Output Charge	V _{DS} = 13V, V _{GS} = 0V		6.8		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 15V, V _{GS} = 4.5V, I _{DS} = 11A,R _G = 2Ω		5.6		ns
t _r	Rise Time			8.2		ns
t _{d(off)}	Turn Off Delay Time			9.8		ns
t _f	Fall Time			3.2		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{SD} = 11A, V _{GS} = 0V		0.85	1	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 13V, I _F = 11A, di/dt = 300A/μs		10.5		nC
t _{rr}	Reverse Recovery Time			14.6		ns

THERMAL CHARACTERISTICS

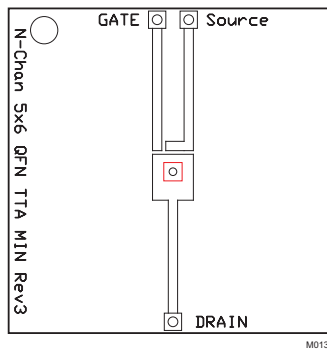
(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
R _{θJC}	Thermal Resistance Junction to Case ⁽¹⁾			1.9	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			51	°C/W

- (1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



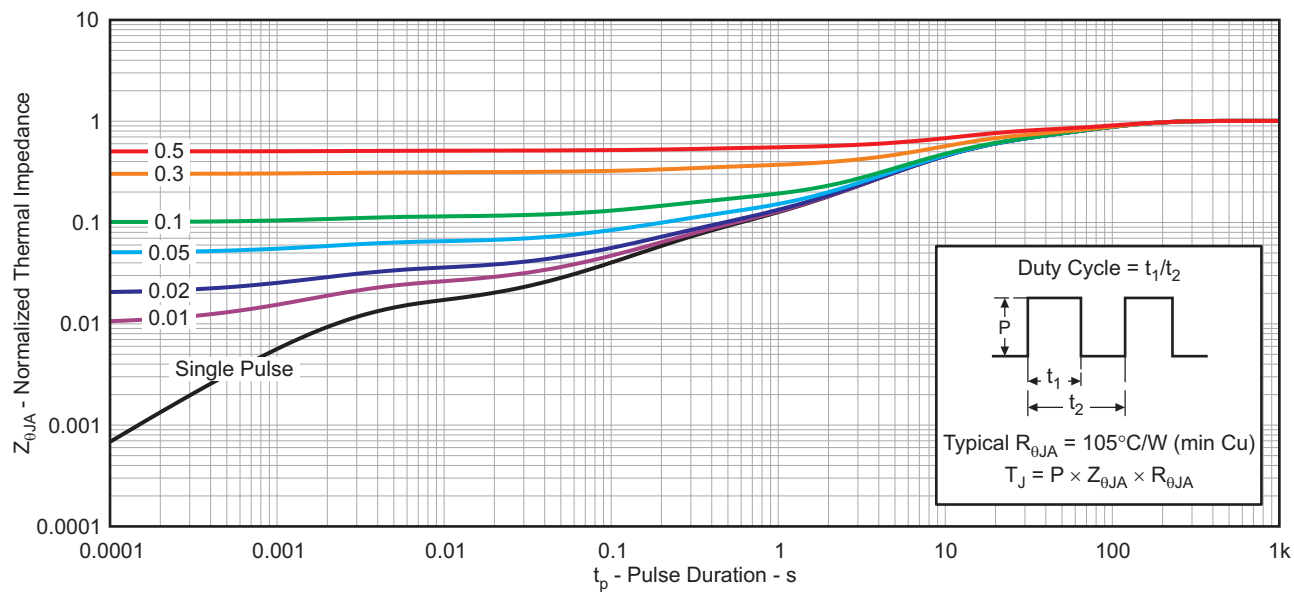
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M0137-02

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

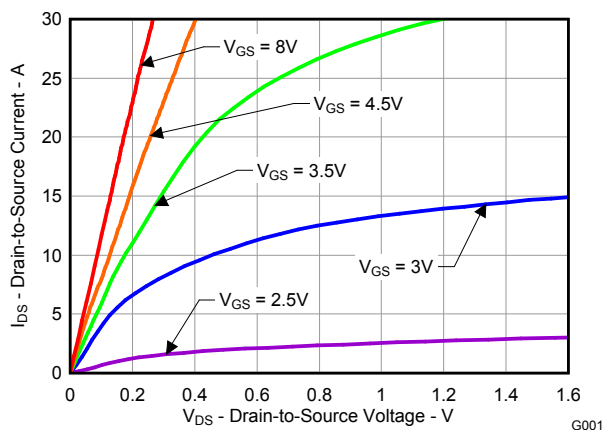


Figure 2. Saturation Characteristics

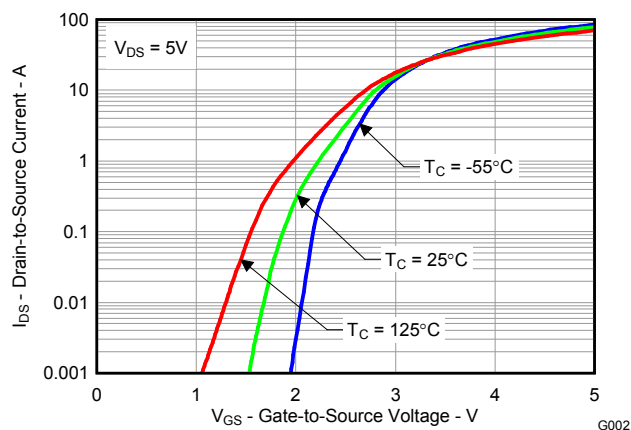


Figure 3. Transfer Characteristics

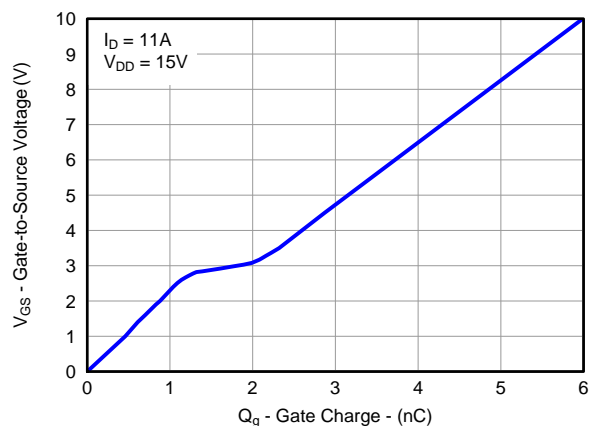


Figure 4. Gate Charge

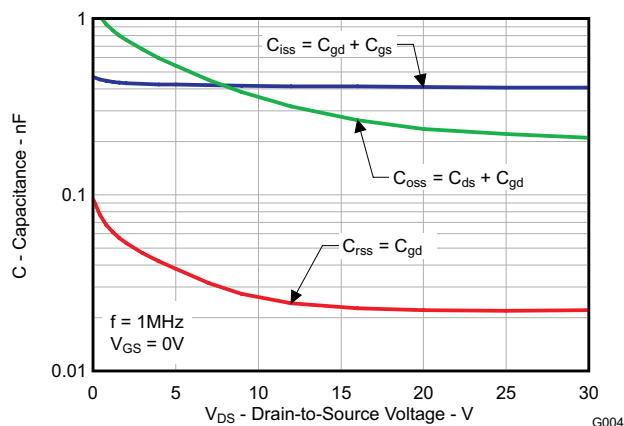


Figure 5. Capacitance

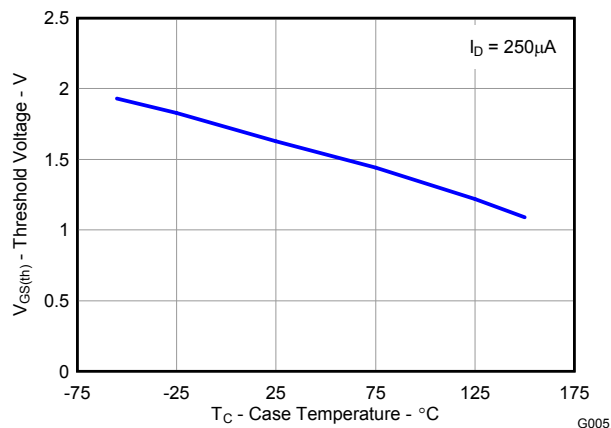


Figure 6. Threshold Voltage vs. Temperature

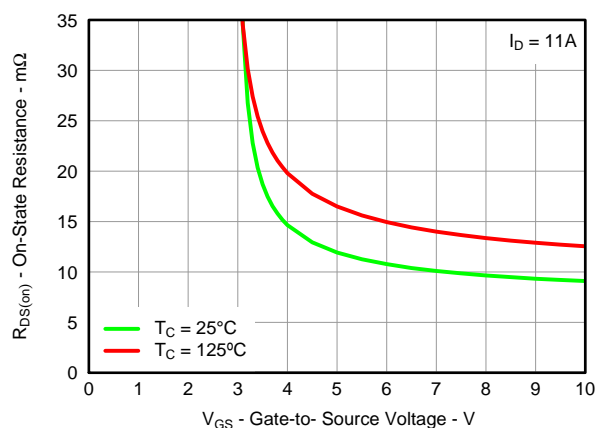


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

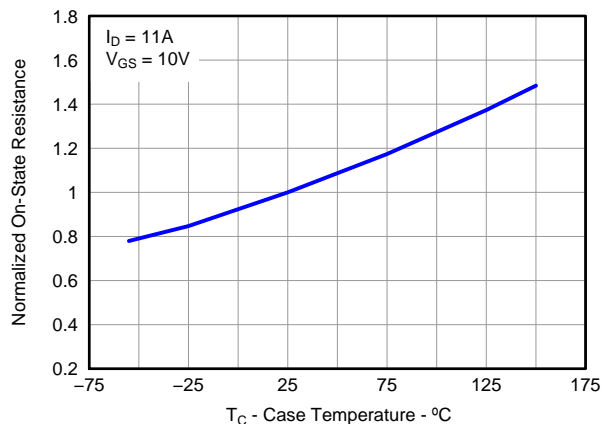


Figure 8. Normalized On-State Resistance vs. Temperature

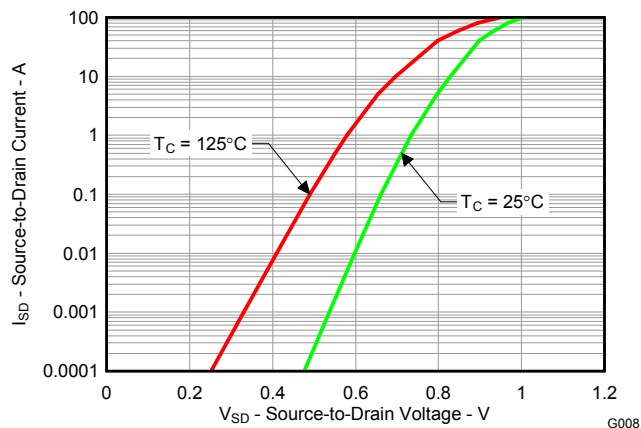


Figure 9. Typical Diode Forward Voltage

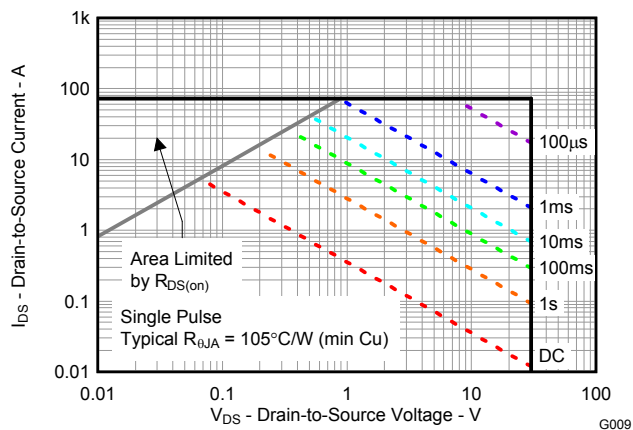


Figure 10. Maximum Safe Operating Area

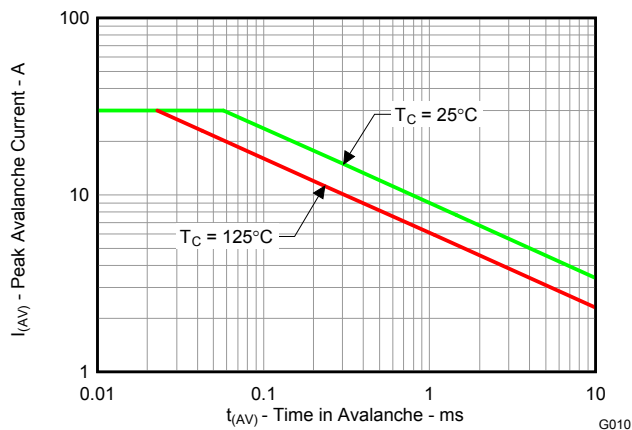


Figure 11. Single Pulse Unclamped Inductive Switching

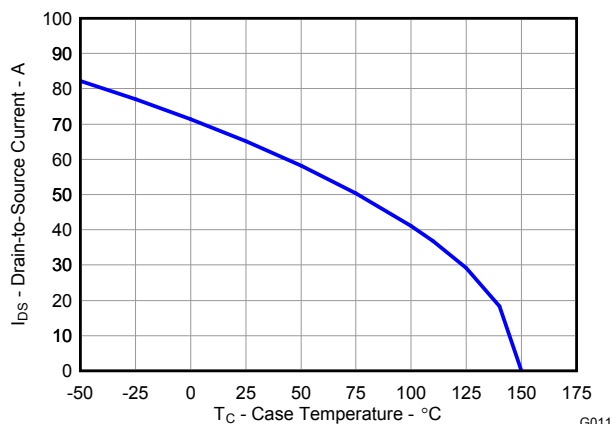
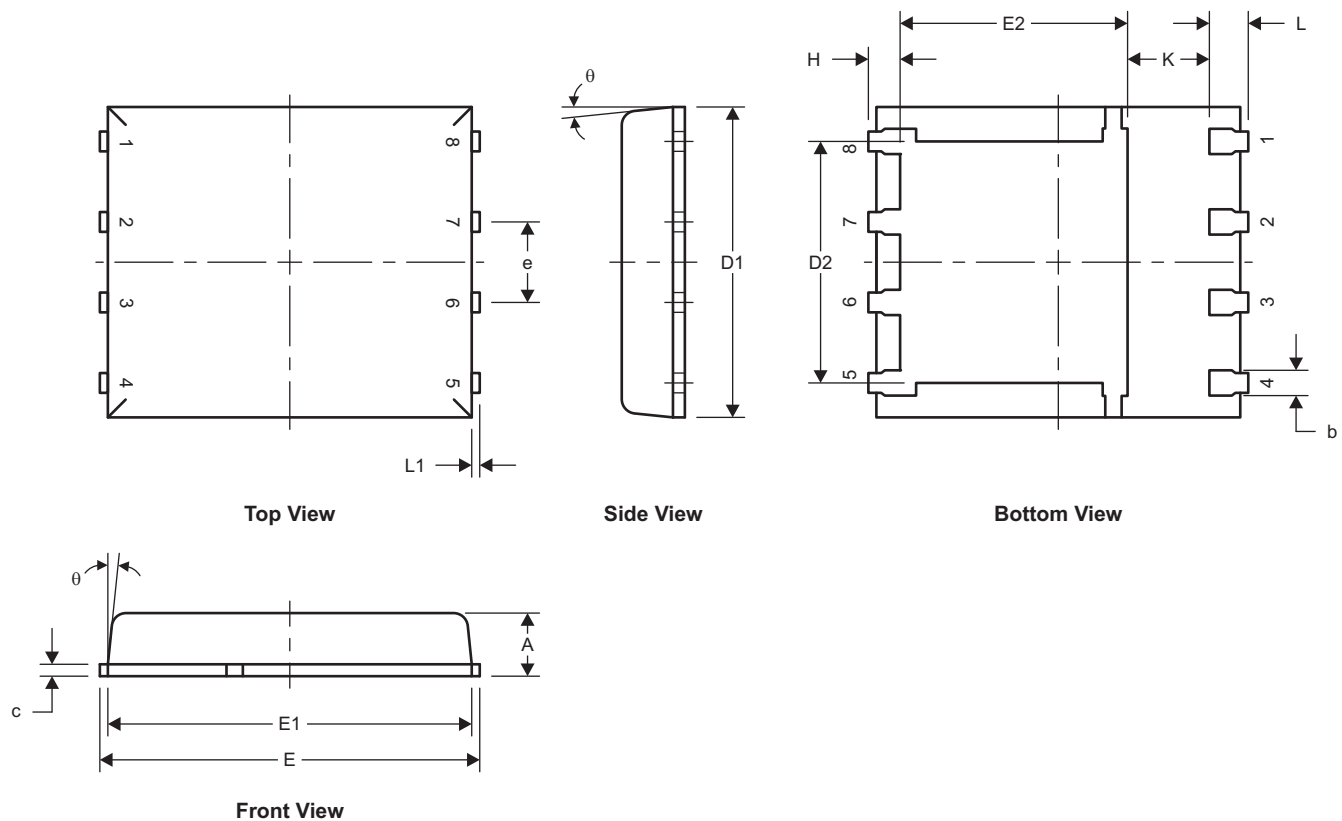


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

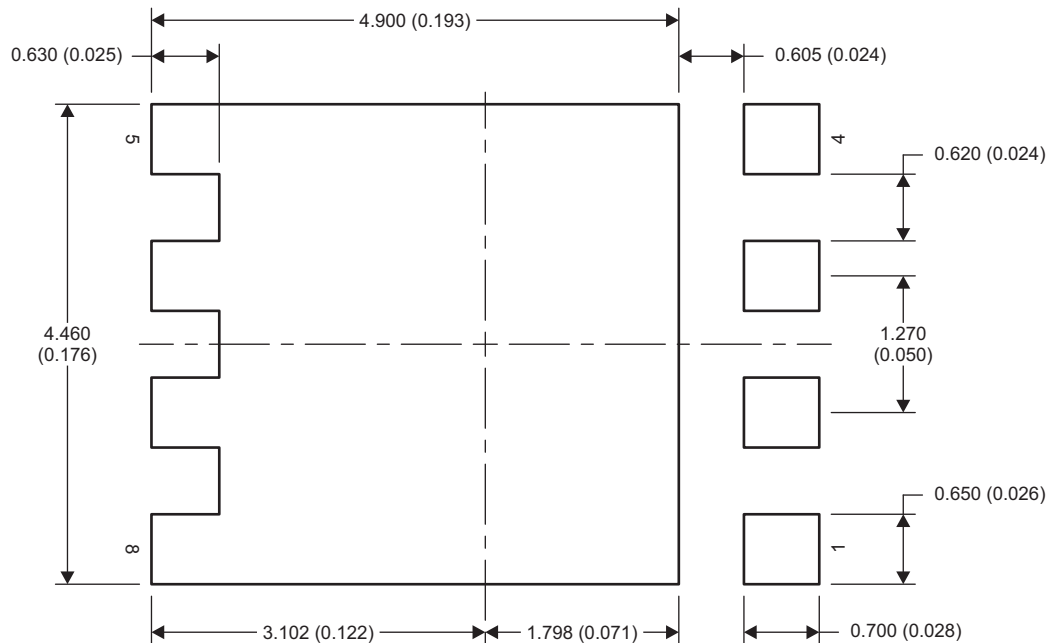
Q5A Package Dimensions



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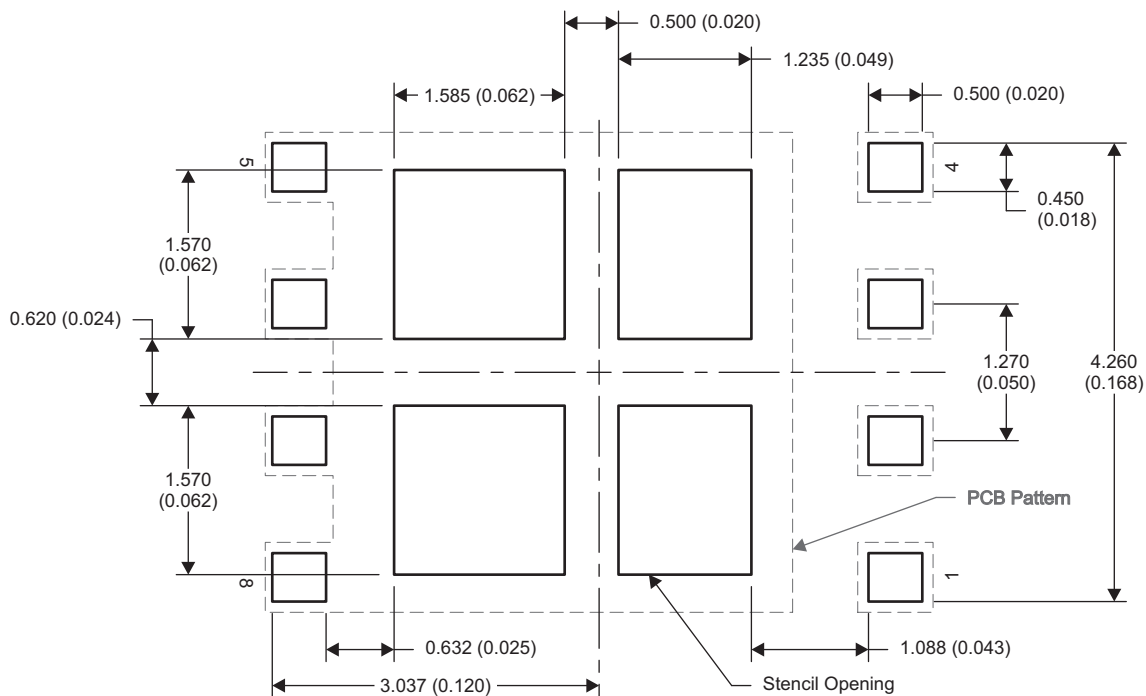
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.17	1.27	1.37
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°

Recommended PCB Pattern



NOTE: Dimensions are in mm (inches).

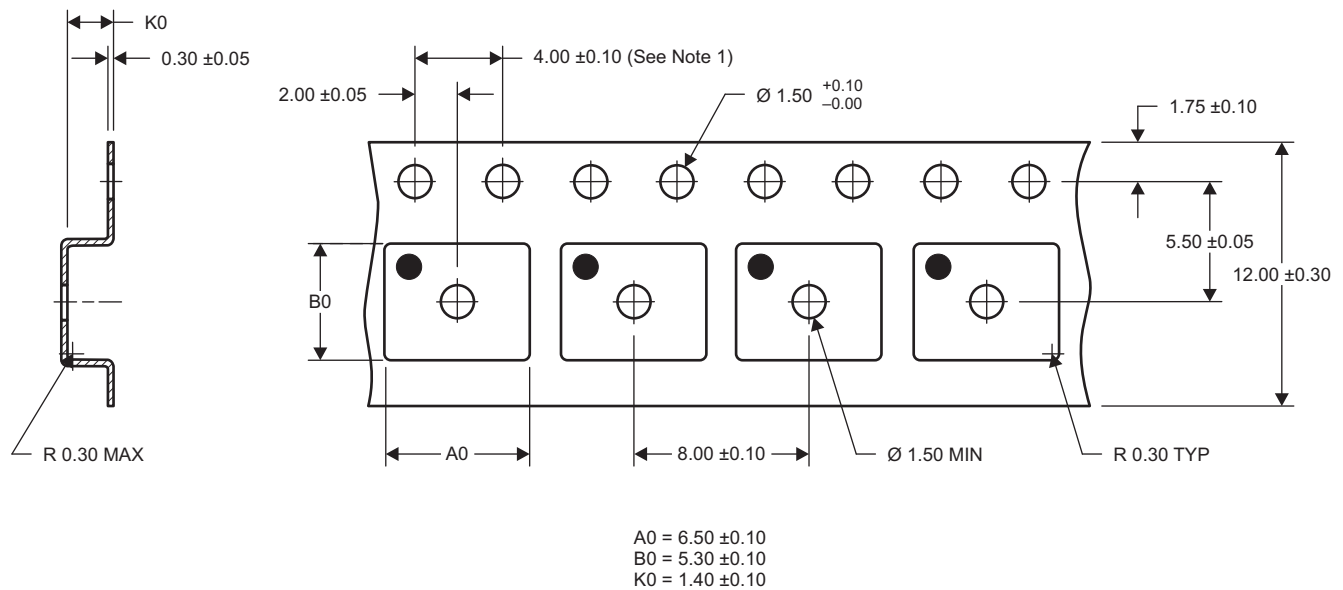
Stencil Recommendation



NOTE: Dimensions are in mm (inches).

For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

Q5A Tape and Reel Information



M0138-01

- NOTES:
1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
 2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
 3. Material: black static-dissipative polystyrene
 4. All dimensions are in mm (unless otherwise specified)
 5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CSD17327Q5A	ACTIVE	SON	DQJ	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

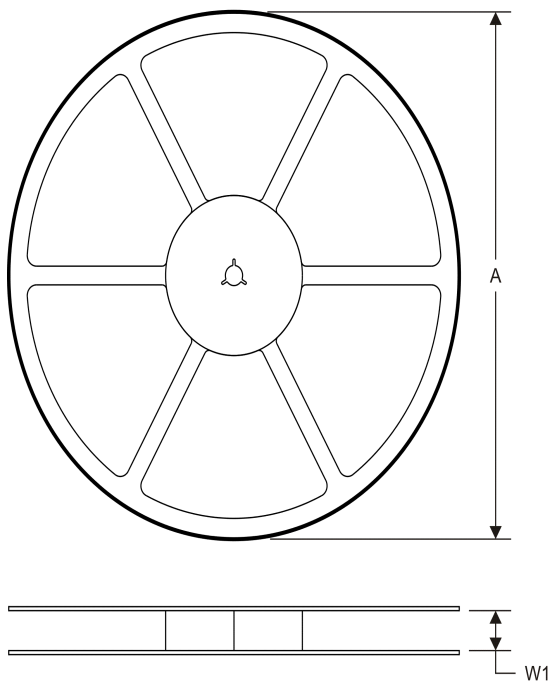
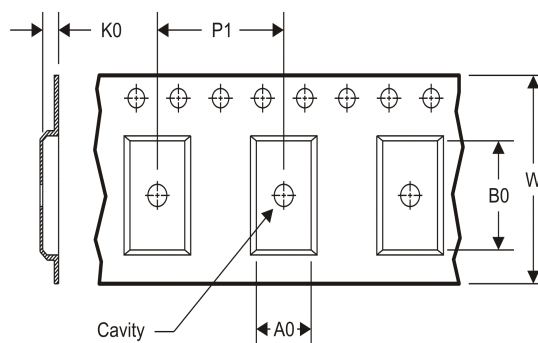
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17327Q5A	SON	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17327Q5A	SON	DQJ	8	2500	340.0	340.0	38.0

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