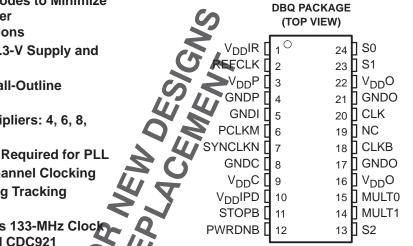
SCAS665B - APRIL 2001 REVISED OCTOBER 2005

- 533-MHz Differential Clock Source for Direct Rambus[™] Memory Systems for an 1066-MHz Data Transfer Rate
- Synchronizes the Clock Domains of the **Rambus Channel With an External System** or Processor Clock
- Three Power Operating Modes to Minimize **Power for Mobile and Other Power-Sensitive Applications**
- **Operates From a Single 3.3-V Supply and** 120 mW at 300 MHz (Typ)
- Packaged in a Shrink Small-Outline Package (DBQ)
- Supports Frequency Multipliers: 4, 6, 8, 16/3
- No External Components Required for PLL
- Supports Independent Channel Clocking
- Spread Spectrum Clocking Tracking **Capability to Reduce EMI**
- Designed for Use With TI's 133-MHz Clock Synthesizers CDC924 and CDC921

- Cycle-Cycle Jitter Is Less Than 40 ps at 533 MHz
- Certified by Gigatest Labs to Exceed the Rambus DRCG Validation Requirement
- Supports Industrial Temperature Range of –40°C to 85°C



description

NC - No internal connection

The Direct Rambus clock generator (DRCG) provides the necessary clock signals to support a Direct Rambus memory subsystem. It includes signals to synchronize the Direct Rambus channel clock to an external system or processor clock. It is designed to support Direct Rambus memory on a desktop, workstation, server, and mobile PC motherboards. DRCG also provides an off-the-shelf solution for a broad range of Direct Rambus memory applications.

The DRCG provides clock multiplication and phase alignment for a Direct Rambus memory subsystem to enable synchronous communication between the Rambus channel and ASIC clock domains. In a Direct Rambus memory subsystem, a system clock source provides the REFCLK and PCLK clock references to the DRCG and memory controller, respectively. The DRCG multiplies REFCLK and drives a high-speed BUSCLK to RDRAMs and the memory controller. Gear ratio logic in the memory controller divides the PCLK and BUSCLK frequencies by ratios M and N such that PCLKM = SYNCLKN, where SYNCLK = BUSCLK/4. The DRCG detects the phase difference between PCLKM and SYNCLKN and adjusts the phase of BUSCLK such that the skew between PCLKM and SYNCLK/PCLK minimized. This allows data to be transferred across the SYNCLK/PCLK boundary without incurring additional latency.

User control is provided by multiply and mode selection terminals. The multiply terminals provide selection of one of four clock frequency multiply ratios, generating BUSCLK frequencies ranging from 267 MHz to 533 MHz with clock references ranging from 33 MHz to 100 MHz. The mode select terminals can be used to select a bypass mode where the frequency multiplied reference clock is directly output to the Rambus channel for systems where synchronization between the Rambus clock and a system clock is not required. Test modes are provided to bypass the PLL and output REFCLK on the Rambus channel and to place the outputs in a high-impedance state for board testing.

The CDCFR83 is characterized for operation over free-air temperatures of -40° C to 85° C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

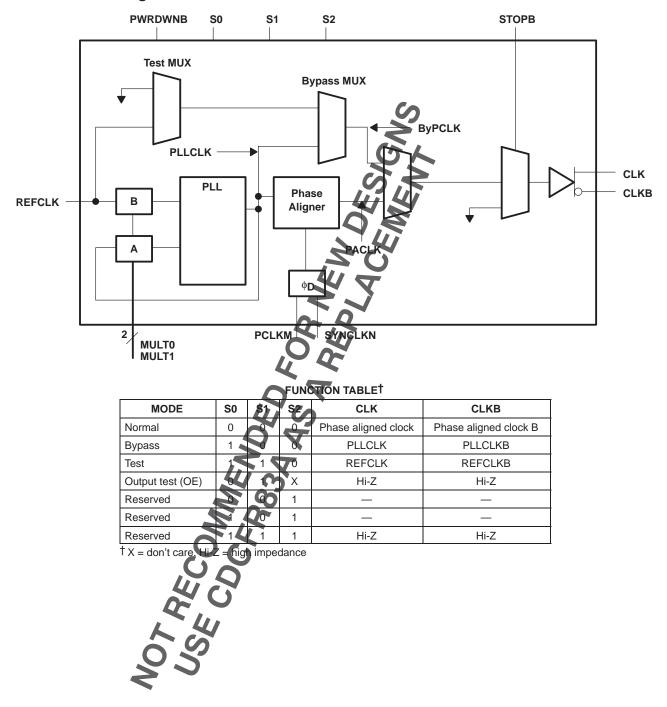
Direct Rambus and Rambus are trademarks of Rambus Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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functional block diagram





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Terminal Functions

TERMIN	IAL		DECODIDEION
NAME	NO.	I/O	DESCRIPTION
CLK	20	0	Output clock
CLKB	18	0	Output clock (complement)
GNDC	8		GND for phase aligner
GNDI	5		GND for control inputs
GNDO	17, 21		GND for clock outputs
GNDP	4		GND for PLL
MULT0	15	Ι	PLL multiplier select
MULT1	14	Ι	PLL multiplier select
NC	19		Not used
PCLKM	6	Т	Phase detector input
PWRDNB	12	Т	Active low power down
REFCLK	2	Ι	Reference clock
S0	24	Ι	Mode control
S1	23	Ι	Mode control
S2	13	Ι	Mode control
STOPB	11	Ι	Active low output disable
SYNCLKN	7	Т	Phase detector input
V _{DD} C	9		V _{DD} for phase aligner
V _{DD} IPD	10		Reference voltage for phase detector inputs and STOPB
V _{DD} IR	1		Reference voltage for REFCLK
V _{DD} O	16, 22		V _{DD} for clock outputs
V _{DD} P	3		V _{DD} for PLL

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PLL divider selection

Table 1 lists the supported REFCLK and BUSCLK frequencies. Other REFCLK frequencies are permitted, provided that (267 MHz < BUSCLK < 533 MHz) and (33 MHz < REFCLK < 100 MHz).

MULT0	MULT1	REFCLK (MHz)	MULTIPLY RATIO	BUSCLK (MHz)
0	0	67	4	267
0	1	50	8	300
0	1	67		400
1	1	33	NS N	267
1	1	50	8	400
1	1	67	8	533
1	0	67	16/3	356

Table 1. REFCLK and BUSCLK Frequencies

Table 2. Clock C	Output Driver States
------------------	----------------------

STATE	PWRDNB	STOPB	CLK	CLKB
Powerdown	0	x	GND	GND
CLK stop	1	0	VX, STOP	VX, STOP
Normal	1	1,0	ACLK/PLLCLK/ REFCLK [†]	PACLKB/PLLCLKB/ REFCLKB

[†] Depending on the state of S0, S1, and S2

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V _{DD} (see Note)	
Output voltage range, V _O , at any output terminal	–0.5 V to V _{DD} + 0.5 V
Input voltage range, V _I , at any input terminal	
Continuous total power dissipation	
Operating free-air temperature range	–40°C to 85°C
Storage temperature range, Tstor.	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. implied. Exposure to absolute-maximum-rated sonditions for exter IOTE 1: All voltage values are with respect to the GND terminals.

NOTE 1: All voltage values are with

	141	DISSIPATION RATING TAR	BLE	
PACKAGE	TA 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C [‡]	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
DBQ	1400 mW	11 mW/°C	905 mW	740 mW
L.				

[‡]This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.



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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{DD}	3.135	3.3	3.465	V
High-level input voltage, V _{IH} (CMOS)	$0.7 \times V_{DD}$			V
Low-level input voltage, VIL (CMOS)			$0.3 \times V_{DD}$	V
Initial phase error at phase detector inputs (required range for phase aligner)	$-0.5 \times t_{C(PD)}$		$0.5 \times t_{C(PD)}$	
REFCLK low-level input voltage, VIL	Ch		$0.3 \times V_{DD}IR$	V
REFCLK high-level input voltage, VIH	$0.7 \times V_{DD}IR$			V
Input signal low voltage, VIL (STOPB)			$0.3 \times V_{DD}$ IPD	V
Input signal high voltage, VIH (STOPB)	0.7 × V _{DD} IPD			V
Input reference voltage for (REFCLK) (V _{DD} IR)	1.235		3.465	V
Input reference voltage for (PCLKM and SYSCLKN) (VDDIPD)	1.235		3.465	V
High-level output current, IOH			-16	mA
Low-level output current, IOL			16	mA
Operating free-air temperature, TA	-40		85	°C

timing requirements

MIN	MAX	UNIT
10	40	ns
	250	ps
40%	60%	
30	33	kHz
	0.6%	
30	100	ns
1	4	V/ns
25%	75%	
	10 40% 30 30 1	10 40 250 40% 60% 30 33 0.6% 30 100 1 4

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETE	R	TEST CO	NDITIONS [†]	MIN	TYP‡	MAX	UNIT	
V _{O(STOP)}	Output voltag (STOPB = 0)	e during CLK Stop	See Figure 1		1.1		2		
V _{O(X)}	Output crossi	ng-point voltage	See Figure 1 and F	igure 6	1.3		1.8	V	
Vo	Output voltag	e swing	See Figure 1	60	0.4		0.6	V	
V _{IK}	Input clamp v	oltage	V _{DD} = 3.135 V,	lj = 18 mA			-1.2	V	
			See Figure 1	<u>.</u>			2		
∨он	High-level out	put voltage	V _{DD} = min to max,	IOH - MA	V _{DD} – 0.1 V			V	
			V _{DD} = 3.135 V,	/OH = -16-mA	2.4				
			See Figure 1		1				
Vol	Low-level out	put voltage	V _{DD} = min to max				0.1	V	
			V _{DD} = 3.135 V,	lot = 16 mA			0.5		
			V _{DD} = 3.135 V	V 0 ≓1V	-32	-52			
lон	High-level out	put current	V _{DD} = 3.3 V,	Vo = 1.65 V		-51		mA	
			V _{DD} = 3.465 V,	V _O = 3.135 V		-14.5	-21		
			V _{DD} = 3.135 V,	V _O = 1.95 V	43	61.5			
IOL	Low-level out	put current	V _{DD} 3 3, V, Q	V _O = 1.65 V		65		mA	
				$V_{O} = 0.4 V$		25.5	36		
loz	High-impedar current	nce-state output	SI = 0, G = 1				±10	μΑ	
IOZ(STOP)	High-impedance-state output current during CLK stop		Stop = $0, V_{O} = GN$	ID or V _{DD}			±100	μΑ	
IOZ(PD)		nce-state output ver-down state	PWRDNB = 0, V _O = GND or V _{DD}		-10		100	μΑ	
	High-level	REFCLK, PCLKM. SYNCLKN, STOPB	VDD = 3.465 V,	$V_I = V_{DD}$			10	A	
IIH	input current	PWRDNB, SO SI, S2, MULT0, MULT1	V _{DD} = 3.465 V,	$V_I = V_{DD}$			10	μA	
1	Low-level	REFCLK, PCLKM SYNCLKN, STOPB	V _{DD} = 3.465 V,	V I = 0			-10	μA	
liL	input current	PWRDNB, 50, 51 S2, MULT0, MULT1	V _{DD} = 3.465 V,	V _I = 0			-10	μΛ	
7	Output	High state	R _I at I _O –14.5 mA	to –16.5 mA	15	35	50	Ω	
ZO	impedance	Low state	R _I at IO 14.5 mA to		11	17	35	22	
	Reference		V _{DD} = 3.465 V	PWRDNB = 0			50	μΑ	
	current		vDD = 3.405 V	PWRDNB = 1			0.5	mA	
Cl	Input capacita	ance	$V_I = V_{DD}$ or GND			2		pF	
CO	Output capac	itance	$V_{O} = V_{DD}$ or GND			3		pF	
DD(PD)	Supply currer	t in power-down state	REFCLK = 0 MHz PWDNB = 0,	to 100 MHz, STOPB = 1			100	μA	
DD(CLKSTOP)	Supply currer	t in CLK stop state	BUSCLK configure	d for 533 MHz			45	mA	
DD(NORMAL)		t in normal state	BUSCLK = 533 MH				100	mA	

[†] V_{DD} refers to any of the following; V_{DD}, V_{DD}IPD, V_{DD}IR, V_{DD}O, V_{DD}C, and V_{DD}P [‡] All typical values are at V_{DD} = 3.3 V, T_A = 25° C.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER			TEST CO	ONDITIONS	MIN	TYP†	MAX	UNIT
^t c(out)	Clock output cycle time					1.87		3.75	ns
			267 MHz					80	
		Infinite and	300 MHz					70	
^t (jitter)	Total cycle jitter over 1, 2, 3, 4, 5, or 6 clock cycles	stopped phase	356 MHz	See Figure 3				60	ps
0,	3, 4, 3, 01 0 CIOCK Cycles	alignment	400 MHz					50	
			533 MHz§					40	
^t (phase)	Phase detector phase erro	r for distributed lo	ор	Static phase	error‡	-100		100	ps
^t (phase, SSC)	PLL output phase error whe	n tracking SSC		Dynamic pha	ise error [‡]	-100		100	ps
t(DC)	Output duty cycle over 10,0	000 cycles		See Figure 4		45%		55%	
()			267 MHz	22				80	
		Infinite and	300 MHz					70	
^t (DC, err)	Output cycle-to-cycle	stopped phase	356 MHz	See Figure 5				60	ps
	duty cycle error	alignment	400 MHz					50	•
			533 MHz	V				50	
t _r , t _f	Output rise and fall times (r output voltage)	measured at 20%	-80% of	See Figure 7		160		400	ps
	Difference between rise an	d fall times on a s	ingle device	See Figure 7	,			100	ne
Assured by des	(20%–80%) $ t_f - t_r $ es are at V _{DD} = 3.3 V, T _A = 2 sign ment according to Rambus v	25°C. alidation specifica	<u>2 2 2</u>	See Figure 7				100	ps
All typical value Assured by des Jitter measurer	$\begin{array}{l} (20\%-80\%) \ t_f-t_r \\ \hline es \ are \ at \ V_{DD} = 3.3 \ V, \ T_A = 2 \\ \hline sign \\ nent \ according \ to \ Rambus \ v \\ \hline tion \ latency \ specifi \end{array}$	25°C. alidation specifica	ation		TEST	MIN	тур†		
All typical value Assured by des Jitter measurer	(20%–80%) t _f – t _r es are at V _{DD} = 3.3 V, T _A = 2 sign ment according to Rambus v tion latency specifi PARAMETER	25°C. alidation specifica cations	FROM			MIN	түр†	MAX	UNI
All typical value Assured by des Jitter measurer	$(20\%-80\%) t_{f} - t_{r} $ as are at V _{DD} = 3.3 V, T _A = 2 sign ment according to Rambus v tion latency specifi PARAMETER Delay time, PWRDNB↑ to settled (excluding t(DISTL)	25°C. alidation specifica cations	Ation FROM	то	TEST	MIN	түр†		UNI
All typical value Assured by des Jitter measurer	$(20\%-80\%) t_{f} - t_{r} $ as are at V _{DD} = 3.3 V, T _A = 2 sign ment according to Rambus v tion latency specifi PARAMETER Delay time, PWRDNB [↑] to settled (excluding t _{(DISTL}) Delay time, PWRDNB [↑] to clock are on and settled	25°C. alidation specifica cations CLK/CLKB outpu CLK/CLKB outpu CLK/CLKB outpu CLK/CLKB outpu	FROM	то	TEST CONDITIONS	MIN	түр†	МАХ	
All typical value Assured by des Jitter measurer state transi	(20%-80%) t _f - t _r es are at V _{DD} = 3.3 V, T _A = 2 sign nent according to Rambus v tion latency specifi PARAMETER Delay time, PWRDNB↑ to settled (excluding t _(DISTL) Delay time, PWRDNB↑ to	25°C. alidation specifica cations CLK/CLKB outpu CLK/CLKB outpu CLK/CLKB outpu CLK/CLKB outpu	FROM t Powerdor	m Normal	TEST CONDITIONS	MIN	түр†	MAX 3	UNI ms
All typical value Assured by des Jitter measurer	(20%–80%) t _f – t _r es are at V _{DD} = 3.3 V, T _A = 2 sign nent according to Rambus v tion latency specifi PARAMETER Delay time, PWRDNB↑ to settled (excluding t _{(DISTL}) Delay time, PWRDNB↑ to clock are on and settled Delay time, power up to C settled Delay time, power up to C	25°C. alidation specifica cations CLK/CLKB output internal PLL and ternal PLL and	Ation FROM	то	TEST CONDITIONS See Figure 8	MIN	түр†	MAX 3 3	UNI
All typical value Assured by des Jitter measurer state transi	(20%-80%) t _f - t _r es are at V _{DD} = 3.3 V, T _A = 2 sign ment according to Rambus v tion latency specifi PARAMETER Delay time, PWRDNB↑ to settled (excluding t _{(DISTL}) Delay time, PWRDNB↑ to clock are on and settled Delay time, power up to C settled Delay time, power up to C	25°C. alidation specifica cations CLK/OLKB output CLK/CLKB output Internal PLL and e to CLK/CLKB	FROM t Powerdor	wn Normal	TEST CONDITIONS See Figure 8	MIN	түр†	MAX 3 3 3	UNI
All typical value Assured by des Jitter measurer state transi	(20%–80%) t _f – t _r es are at V _{DD} = 3.3 V, T _A = 2 sign ment according to Rambus v tion latency specifi PARAMETER Delay time, PWRDNB↑ to settled (excluding t _{(DISTL}) Delay time, PWRDNB↑ to clock are on and settled Delay time, power up to C settled Delay time, power up to C settled Delay time, power up to C settled Delay time, power up to C	25°C. alidation specifica cations CLK/CLKB output CLK/CLKB output Internal PLL and K/(CLKB output ternal PLL and e to CLK/CLKB ((DISTLOCK))	t Powerdor	wn Normal Normal	TEST CONDITIONS See Figure 8 See Figure 8	MIN	TYPT	MAX 3 3 3 3	UNI ms
All typical value Assured by des Jitter measurer state transi (powerup)	(20%–80%) t _f - t _r es are at V _{DD} = 3.3 V, T _A = 2 sign ment according to Rambus v tion latency specifi PARAMETER Delay time, PWRDNB↑ to settled (excluding t _{(DISTL}) Delay time, PWRDNB↑ to clock are on and settled Delay time, power up to C settled Delay time, power up to C settled MULT0 and MULT4 chang output resettled (excluding STOPB↑ to CLK/CLKP offer	25°C. alidation specifica cations CLKOLKB output CLKOLKB output ternal PLL and e to CLK/CLKB (DISTLOCK)) tch-free clock tput settled to	t Powerdor VDD Norma	TO TO Normal Normal Normal	TEST CONDITIONS See Figure 8 See Figure 8 See Figure 9	MIN	түрт	MAX 3 3 3 3 1	UNI ms ms

[†] All typical values are at V_{DD} = 3.3 V, T_A = 25°C.

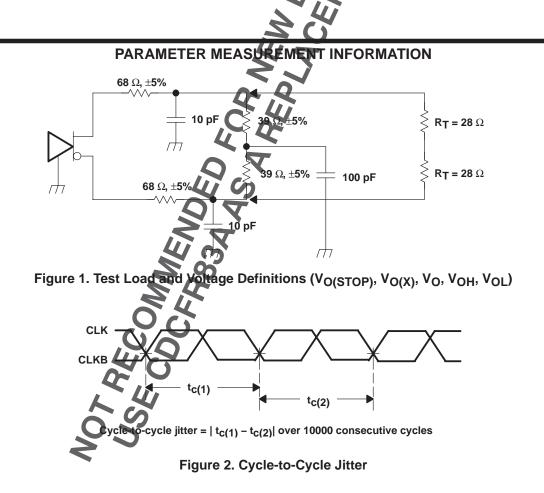


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state transition latency specifications (continued)

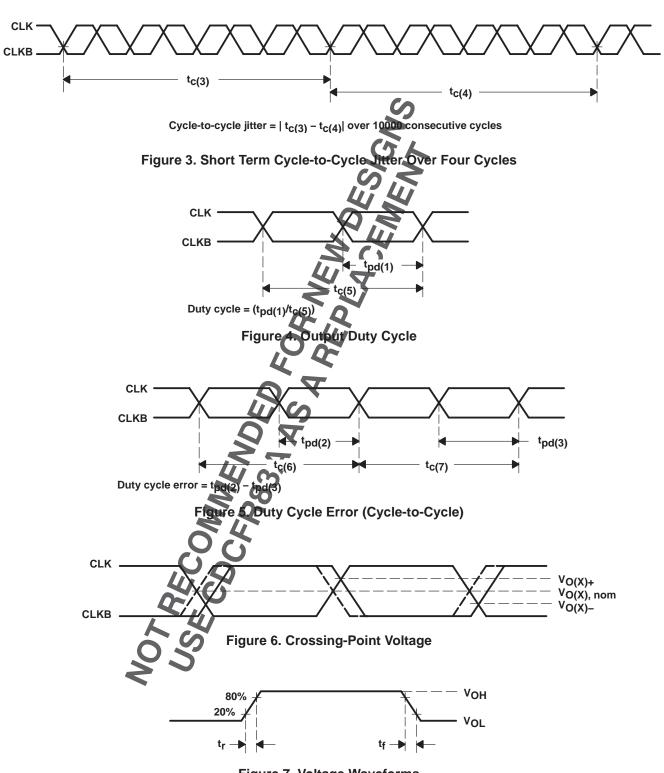
	PARAMETER	FROM	то	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
^t (powerdown)	Delay time, PWRDNB↓ to the device in the power-down mode	Normal	Powerdown	See Figure 8			1	ms
^t (STOP)	Maximum time in CLKSTOP (STOPB = 0) before reentering normal mode (STOPB = 1)	STOPB	Normal	See Figure 10			100	μs
^t (ON)	Minimum time in normal mode (STOPB = 1) before reentering CLKSTOP (STOPB = 0)	Normal	CLK Stop	See Figure 10	100			ms
^t (DISTLOCK)	Time from when CLK/CLKB output is settled to when the phase error between SYNCLKN and PCLKM falls within t _(phase)	Unlocked	Lecked				5	ms

[†] All typical values are at $V_{DD} = 3.3$ V, $T_A = 25^{\circ}$ C.





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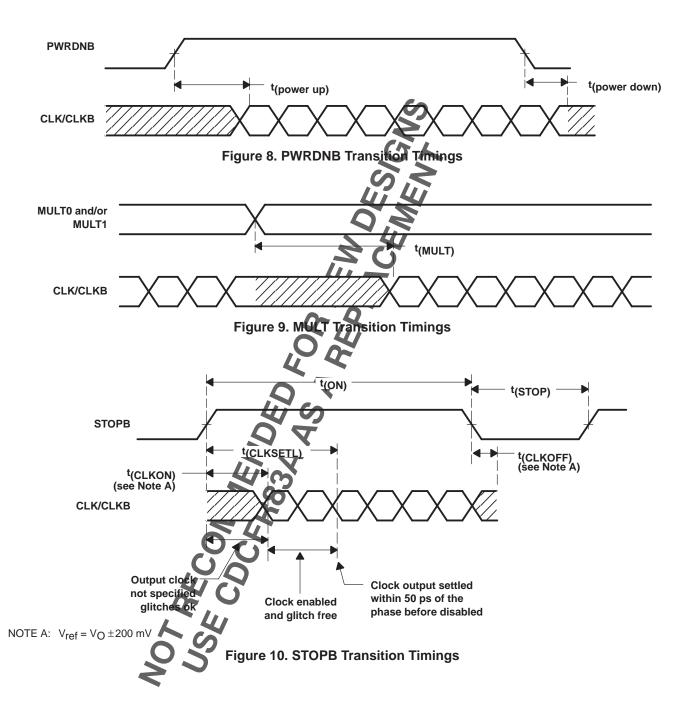
PARAMETER MEASUREMENT INFORMATION

Figure 7. Voltage Waveforms



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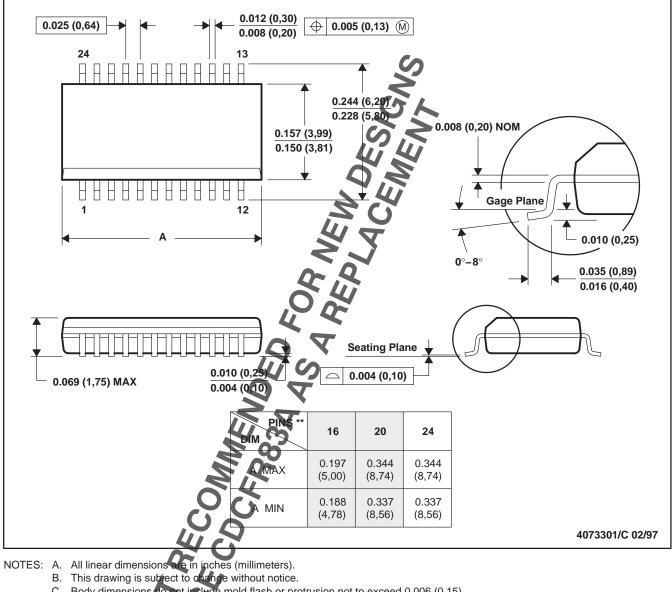
CDCFR83 DIRECT RAMBUSTM CLOCK GENERATOR

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MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

DBQ (R-PDSO-G**) 24-PIN SHOWN



- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDCFR83DBQ	NRND	SSOP/ QSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCFR83DBQG4	NRND	SSOP/ QSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCFR83DBQR	NRND	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCFR83DBQRG4	NRND	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

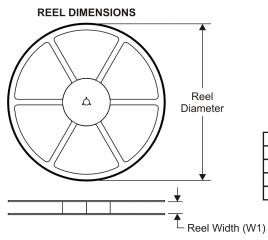
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

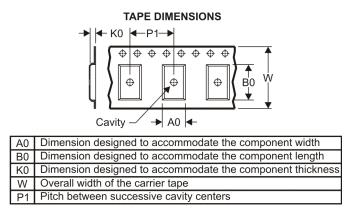
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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nomina	*All	dimensions	are	nomina	l
----------------------------	------	------------	-----	--------	---

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCFR83DBQR	SSOP/ QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1



PACKAGE MATERIALS INFORMATION

11-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCFR83DBQR	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0

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