

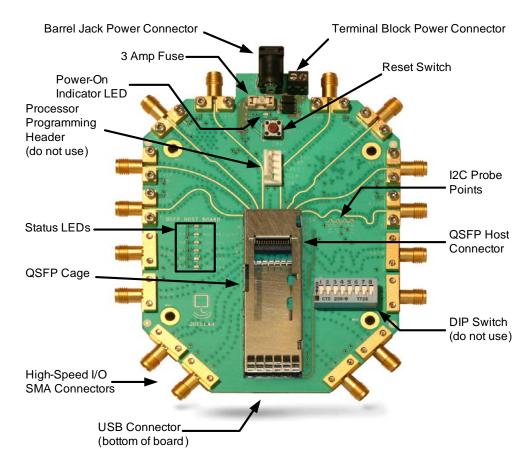
## **OSFP Powered Breakout Board User Guide**

### **Overview**

# **QSFP-BB Basic Operation**

The QSFP breakout board (QSFP-BB) connects a single active QSFP external receptacle connector to 16 surface mount SMA connectors to enable the test and evaluation of a single QSFP active or passive cable at speeds up to 10.3Gb/s per channel.

Figure 1 shows the layout of the QSFP-BB. The 16 SMA's are used to breakout four transmit (TX) and four receive (RX) channels. Each of the channels is a differential pair.



<sup>\*</sup>The QSFP-BB may operate with an active or passive cable.

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FIGURE 1. QSFP-BB BREAKOUT BOARD

### **QSFP-BB Features**

The features on the board include:

- 1. Green LED to indicate when power is being supplied to the active QSFP cable.
- 2. DC blocking capacitors on the RX side of the QSFP-BB.
- 3. Simple 2-pin power connector, to supply 5V
- 4. Matched PCB trace lengths between the QSFP receptacle and each of the 16 SMA connectors.

## **Connector Pin Assignment**

Figure 2 shows the arrangement of the output pins from the QSFP receptacle on the QSFP-BB. Table 1 lists each of the pins function.

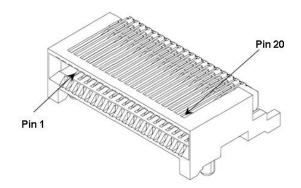


FIGURE 2. PINOUT OF THE QSFP RECEPTACLE CONNECTOR ON THE QSFP-BB

TABLE 1. QSFP ACTIVE BOARD PIN ASSIGNMENT TABLE

PIN	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTES
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted 3		
			Data Input		
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input 3		
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted	3	
			Data Input		
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc RX	+3.3V Power Supply	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground 1		1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	

# **Application Note 1512**

TABLE 1. QSFP ACTIVE BOARD PIN ASSIGNMENT TABLE (Continued)

PIN	LOGIC	SYMBOL	DESCRIPTION PLUG SEQUENCE		NOTES
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-I	IntL	Interrupt	3	
29		V <sub>CC</sub> T <sub>X</sub>	+3.3V Power supply transmitter	2	2
30		V <sub>CC1</sub>	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

#### NOTES:

- 1. GND is the symbol for signal and supply (power) common for the QSFP module.
- 2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

## **QSFP-BB Block Diagram**

The block diagram of the BCK-QSFP breakout board is shown in Figure 3.

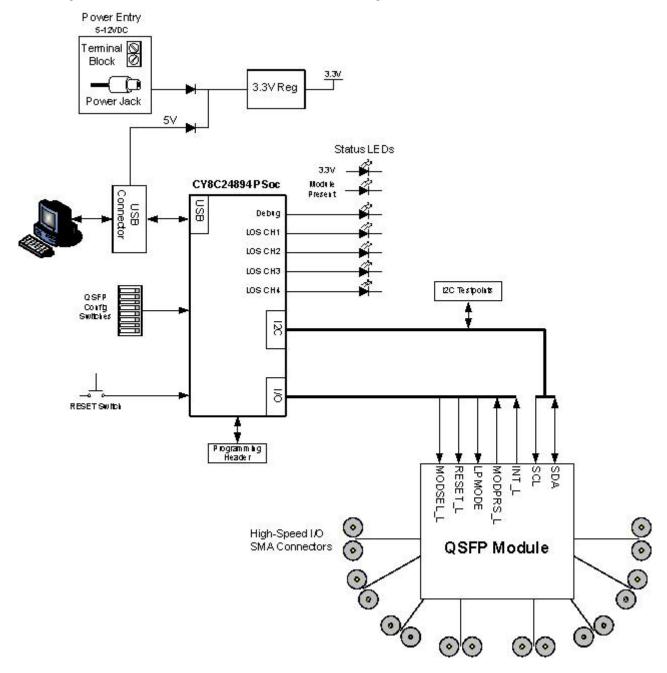
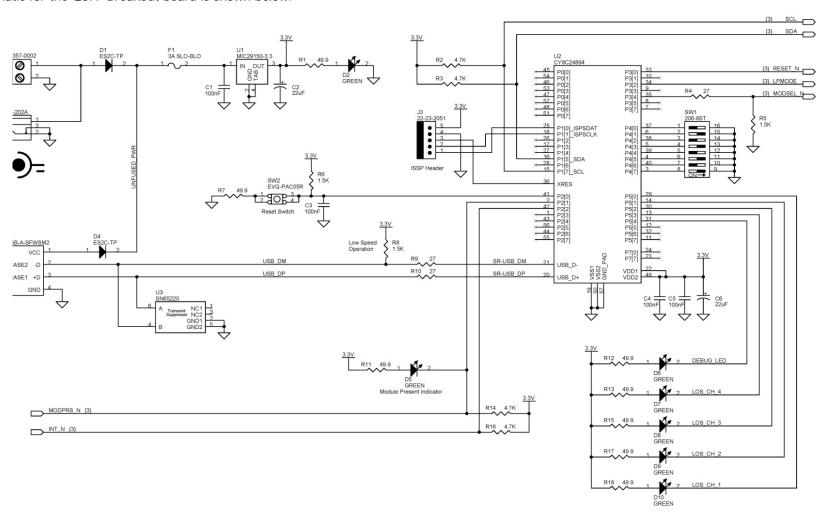


FIGURE 3. BCK-QSFP BLOCK DIAGRAM

## **Schematic**

The schematic for the QSFP Breakout board is shown below.



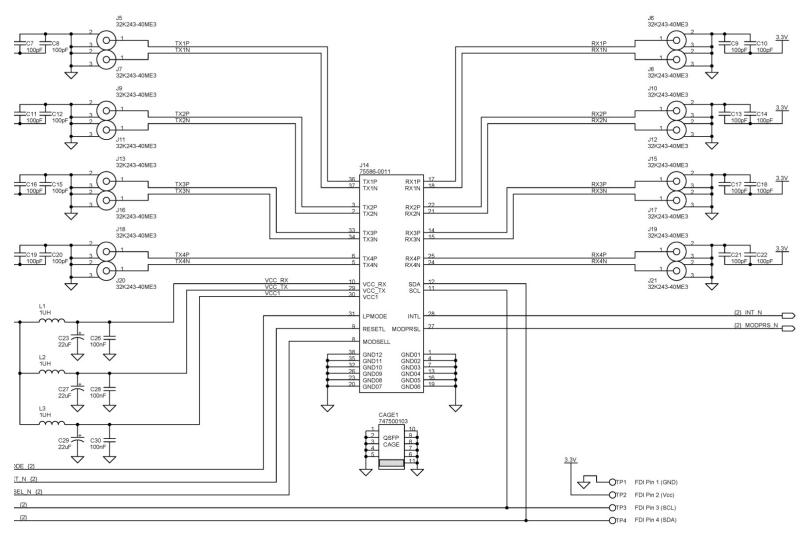


FIGURE 4. BCK-QSFP SCHEMATIC

## **Board Operation**

Board operation is straightforward. If an active cable is being used:

- 1. Apply 5V power supply to the 2-pin connector on the board. Ensure that proper polarity is observed! There is a stencil on the board discerning the GND pin from the 5V pin. Alternatively, connect a wall power adapter jack (having a 2mm tip and 6.5mm ring) to the power jack input J2, on the end of the board. The wall jack should supply a minimum of 5V (8V Max) @ 2.5A (Max).
- 2. Plug in the Intersil active cable module.
- 3. Check and ensure that the green LED is on, and that the current load on the power supply (PS) is no greater than 300mA @3.3V (275mA typ). Ensure also that the Mod Present LED is on.

If a passive cable is connected to the QSFP-BB, no power is supplied to the receptacle and the board operates in a passive mode. Signal throughput is identical on all four channels regardless of DC power.

## **Electrical and Mechanical Characteristics**

TABLE 2. ABSOLUTE MAXIMUM RATINGS

PARAMETER	RANGE (Note 3)
Supply Voltage	10.0V
ESD Rating at all pins	2kV (HBM)
Operating Ambient Temperature Range	0°C to +70°C
Storage Ambient Temperature Range	-55°C to +150°C

#### NOTE:

3. Exceeding the ranges and maximum values in Table 2 may permanently damage the device. These values are stress ratings only and are not meant to imply nominal operating conditions.

#### I<sup>2</sup>C Interface

The  $I^2C$  signals from the QSFP Host Connector are routed to the probe points shown in Figure 1. If the user wishes, an external third-party I<sup>2</sup>C programming device can be used to access the I<sup>2</sup>C memory space on the QSFP module.

### **Application Note 1512**

#### TABLE 3. OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage		4.0	5.0	8.0	V
Operating Ambient Temperature		0	25	70	°C
Bit Rate	NRZ data applied to any channel	1.5		10.3	Gb/s
Operating Voltage		3.14	3.3	3.47	V

#### **TABLE 4. MECHANICAL CHARACTERISTICS**

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
QSFP Connector insertions				250	
SMA connector insertions				500	

# About Q:ACTIVE®

Intersil has long realized that to enable the complex server clusters of next generation datacenters, it is critical to manage the signal integrity issues of electrical interconnects. To address this, Intersil has developed its groundbreaking Q: ACTIVE® product line. By integrating its analog ICs inside cabling interconnects, Intersil is able to achieve unsurpassed improvements in reach, power consumption, latency, and cable gauge size as well as increased airflow in tomorrow's datacenters. This new technology transforms passive cabling into intelligent "roadways" that yield lower operating expenses and capital expenditures for the expanding datacenter.

Intersil Lane Extenders allow greater reach over existing cabling while reducing the need for thicker cables. This significantly reduces cable weight and clutter, increases airflow, and improves power consumption.

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.