

SBAS518A - AUGUST 2011 - REVISED DECEMBER 2011

Analog Monitor and Control Circuit with 10-Bit, Multi-Channel ADC and Four DACs, Temperature Sensor, and 12 GPIOs

Check for Samples: AMC7891

FEATURES

- 10-Bit, 500-kSPS SAR ADC:
 - 8 External Analog Inputs
 - V_{RFF}, 2 × V_{RFF} Input Ranges
- Four 10-Bit Monotonic DACs:
 - 0 to 5-V Output Range
 - Up to 10-mA Sink and Source Capability
- Power-On Reset to 0 V
- Internal 2.5-V Reference
- **Internal Temperature Sensor:**
 - 40°C to +125°C Operation
 - Accuracy of ±2.5°C
- 12 General-Purpose I/O Ports:
 - 1.8-V to 5.5-V Operation
- Low-Power SPI[™]-Compatible Serial Interface:
 - 4-Wire Mode, 1.8-V to 5.5-V Operation
 - SCLK up to 30 MHz
- Temperature Range: -40°C to +105°C
- Low Power: 32.5 mW at 5 V, Full Operating Conditions
- Space-Saving Package: 36-pin, 6-mm x 6-mm QFN



APPLICATIONS

- **Cellular Base Stations**
- **RF** Communication Systems
- **Optical Networks**
- **General-Purpose Monitor and Control**

DESCRIPTION

The AMC7891 is a highly-integrated, low-power, complete analog monitoring and control system in a very small package.

For monitoring functions, the AMC7891 has 8 uncommitted inputs multiplexed into a 10-bit SAR analog-to-digital converter (ADC) and an accurate on-chip temperature sensor. Control signals are generated through four, independent, 10-bit digital-to-analog converters (DACs). Additional digital signal monitoring and control is accomplished through twelve configurable GPIOs. An internal reference can be used to drive the ADC and DACs.

Communication to the device is performed through a versatile, four-wire serial interface compatible with industry-standard microprocessors and microcontrollers. The serial interface can operate at clock rates up to 30 MHz, allowing quick access to critical system data.

The device is characterized for operation over the temperature range of -40°C to 105°C and is available in a very small, 36-pin, 6-mm x 6-mm QFN package.

The AMC7891's low power, small size and high-integration make it an ideal low-cost, bias control circuit for modern RF transistor modules such as the power amplifiers (PA) and low-noise amplifiers (LNA) found in RF communication systems. The AMC7891 feature set is similarly beneficial in general purpose monitor and control systems.

For applications that require a different channel count, additional features, or converter resolutions, Texas Instruments offers a complete family of Analog (AMC) Products. Monitor and Control See http://www.ti.com/amc.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



AMC7891 Pin Functions

	PIN	1/0	DESCRIPTION
NO.	NAME	1/0	DESCRIPTION
1	AV _{DD}	Ι	Analog supply voltage. (4.75 V to 5.5 V)
2	AGND1	Ι	Analog ground. Ground reference point for all analog circuitry on the device, AGND. Connect AGND1 and AGND2 to the same potential, AGND.
3	DGND	Ι	Digital ground. Ground reference point for all digital circuitry on the device. Ideally, AGND and DGND should be at the same potential and must not differ by more than 0.3 V.
4	GPIOV _{DD}	Ι	GPIO supply voltage. (1.8 V to 5.5 V) Sets the GPIO operating voltage and threshold levels.
5	SPIV _{DD}	Ι	Serial interface supply voltage. (1.8 V to 5.5 V) Sets the serial interface operating voltage and threshold levels.
6	CS	Ι	Active low serial data enable. Schmitt-trigger logic input.
			This input is the frame synchronization signal for the serial data. When this signal goes low, it enables the input shift register and data is sampled on subsequent falling clock edges. The DAC output and register settings update following the 24th clock. If \overline{CS} goes high before the 23th clock edge, the command is ignored.
7	SCLK	Ι	Serial interface clock. Schmitt-trigger logic input. Maximum SCLK rate is 30MHz.
8	SDI	Ι	Serial interface data input. Schmitt-trigger logic input. Data is clocked into the input shift register on each falling edge of SCLK.
9	SDO	0	Serial interface data output. The SDO pin is in high impedance when \overline{CS} is high. Data is clocked out of the input shift register on each rising edge of SCLK.
10	DACOUT3	0	DAC3 buffered output. (0 V to AV _{DD}). Can source/sink up to 10 mA.



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AMC7891 Pin Functions (continued)

	PIN	1/0	DESCRIPTION				
NO.	NAME	10	DESCRIPTION				
11	DACOUT2	0	DAC2 buffered output. (0 V to AV _{DD}). Can source/sink up to 10 mA.				
12	DACOUT1	0	DAC1 buffered output. (0 V to AV _{DD}). Can source/sink up to 10 mA.				
13	DACOUT0	0	DAC0 buffered output. (0 V to AV _{DD}). Can source/sink up to 10 mA.				
14	AGND2	Ι	Analog ground. Ground reference point for all analog circuitry on the device, AGND. Connect AGND1 and AGND2 to the same potential, AGND.				
15	GPIOC3	I/O	General purpose digital I/O C3. Maximum voltage is set by GPIOV _{DD}				
16	GPIOC2	I/O	General purpose digital I/O C2. Maximum voltage is set by GPIOV _{DD}				
17	GPIOC1	I/O	General purpose digital I/O C1. Maximum voltage is set by GPIOV _{DD}				
18	GPIOC0	I/O	General purpose digital I/O C0. Maximum voltage is set by GPIOV _{DD}				
19	DAV	0	ADC data available indicator. Open-drain, active low output.				
			In direct-mode, $\overline{\text{DAV}}$ goes low when an ADC conversion cycle finishes. In auto-mode a 1µs pulse appears on this pin when the conversion cycle finishes (see ADC Operation for details). $\overline{\text{DAV}}$ stays high when deactivated. If used, an external 10 k Ω pull-up resistor to GPIOV _{DD} is required. If unused, the pin can be connected to DGND.				
20	GPIOB3	I/O	General purpose digital I/O B3. Maximum voltage is set by GPIOV_{DD}				
21	GPIOB2	I/O	General purpose digital I/O B2. Maximum voltage is set by GPIOV _{DD}				
22	GPIOB1	I/O	General purpose digital I/O B1. Maximum voltage is set by GPIOV _{DD}				
23	GPIOB0	I/O	General purpose digital I/O B1. Maximum voltage is set by GPIOV _{DD}				
24	GPIOA3	I/O	General purpose digital I/O A3. Maximum voltage is set by GPIOV _{DD}				
25	GPIOA2	I/O	General purpose digital I/O A2. Maximum voltage is set by GPIOV _{DD}				
26	GPIOA1	I/O	General purpose digital I/O A1. Maximum voltage is set by GPIOV _{DD}				
27	GPIOA0	I/O	General purpose digital I/O A1. Maximum voltage is set by GPIOV _{DD}				
28	AIN0	Ι	Uncommitted analog input 0. (0 V to 5 V)				
29	AIN1	Ι	Uncommitted analog input 1. (0 V to 5 V)				
30	AIN2	Ι	Uncommitted analog input 2. (0 V to 5 V)				
31	AIN3	-	Uncommitted analog input 3. (0 V to 5 V)				
32	AIN4	Ι	Uncommitted analog input 4. (0 V to 5 V)				
33	AIN5	Ι	Uncommitted analog input 5. (0 V to 5 V)				
34	AIN6	Ι	Uncommitted analog input 6. (0 V to 5 V)				
35	AIN7	Ι	Uncommitted analog input 7. (0 V to 5 V)				
36	REF	I/O	Used as external ADC reference input when the internal reference buffer is disabled in register AMC_power, ref_on = '0' (default). A decoupling capacitor is recommended between the external reference output an AGND for noise filtering.				
			Used as internal reference output when the internal reference buffer is enabled in register AMC_power, ref_on = '1'. Requires a 4.7 μ F decoupling capacitor to AGND when used as reference output. An external buffer amplifier with high impedance input is required to drive an external load.				
-	THERMAL PAD	-	The thermal pad is located on the package underside. Connect to the board ground plane using multiple vias.				

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ORDERING INFORMATION⁽¹⁾

T _A	ORDER CODE	PACKAGE DRAWING/TYPE ⁽²⁾⁽³⁾	TRANSPORT MEDIA	QUANTITY
40°C to 105°C	AMC7891SRHHT	DUUL / 26 OFN Quad Elatrack No. Load	Topo and Dool	250
–40°C to 105°C	AMC7891SRHHR	אחח / סס-ערוא עומט Flatpack No-Lead	Tape and Reel	2000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

(2) Thermal Pad Size: 4.39 mm x 4.39 mm

(3) MSL Peak Temperature: Level-3-260C-168 HR

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range, unless otherwise noted.

			VALUE	UNIT
		MIN	MAX	
	AV _{DD} to AGND ⁽²⁾	-0.3	6	V
Supply voltage range	GPIOV _{DD} to DGND	-0.3	6	V
	SPIV _{DD} to DGND	-0.3	6	V
	AGND to DGND	-0.3	0.3	V
	AIN[0:7], DACOUT[0:3], REF to AGND	-0.3	AV _{DD} + 0.3	V
	CS, SCLK, SDI to DGND	-0.3	6	V
Pin voltage range	SDO to DGND	-0.3	SPIV _{DD} + 0.3	V
	GPIOA[0:3], GPIOB[0:3], GPIOC[0:3] to DGND	-0.3	GPIOV _{DD} + 0.3	V
	DAV to DGND	-0.3	6	V
Operating free-air temperation	ture range, T _A : AMC7891 ^{(3) (4)}	-40	105	°C
Storage temperature range)	-40	150	°C
	Human body model (HBM)		2.5	kV
ESD raungs:	Charged device model (CDM)		1.0	kV

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

(2) AGND1 and AGND2 must be tied together as AGND.

(3) Air flow or heat sinking reduces θ_{JA} and may be required for sustained operation at 105°C and maximum operating conditions.

(4) Soldering the device thermal pad to the board ground plane is strongly recommended.

THERMAL INFORMATION

		AMC7891	
	THERMAL METRIC ⁽¹⁾	RHH PACKAGE	UNITS
		36 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	30.6	
θ_{JCtop}	Junction-to-case (top) thermal resistance	16.0	
θ_{JB}	Junction-to-board thermal resistance	5.3	°C (M)
ΨJT	Junction-to-top characterization parameter	0.2	C/VV
Ψ _{JB}	Junction-to-board characterization parameter	5.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.8	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

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ELECTRICAL CHARACTERISTICS (DAC SPECIFICATIONS)

 AV_{DD} = 4.75 to 5.5 V, GPIOV_{DD} = 1.8 to 5.5 V, SPIV_{DD} = 1.8 to 5.5 V, AGND = DGND = 0 V, External ADC reference = AV_{DD} , $T_A = -40^{\circ}$ C to 105°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STAT	TIC ACCURACY					
	Resolution		10			Bits
INL	Relative accuracy			±0.05	±1	LSB
DNL	Differential nonlinearity	Specified monotonic		±0.1	±1	LSB
	Offset error	Code 0x008		±0.5	±5	mV
	Gain error			±0.025	±0.2	%FSR
	Offset temperature coefficient			±1		ppm/°C
	Gain temperature coefficient			±1		ppm/°C
DAC	OUTPUT ⁽¹⁾					
	Full scale output voltage range		0		AV_{DD}	V
	Output voltage settling time	Transition: Code 0x008 to 0x3F8 to within 1/2 LSB, $C_L = 2 nF$, $RL = \infty$		5		μs
	Slew rate			2		V/µs
	Short circuit current	Full-scale current shorted to ground or pulled to AVDD		±30		mA
	Load current	Source and/or sink within 300 mV of supply		±10		mA
	Capacitive load stability	R _L = ∞	10			nF
	DC output impedance			1		Ω
	Power-on overshoot	AV _{DD} 0 to 5 V, 2 ms ramp		10		mV
	Glitch energy	Transition: Code 0x1FF to 0x200; 0x200 to 0x1FF		0.15		nV-s
		T _A = 25°C, 1 kHz		260		nV/√Hz
		Integrated noise from 0.1 Hz to 10 Hz		20		μV _{PP}

(1) Specified by design and characterization. Not tested during production.



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ELECTRICAL CHARACTERISTICS – (ADC SPECIFICATIONS)

 AV_{DD} = 4.75 to 5.5 V, $GPIOV_{DD}$ = 1.8 to 5.5 V, $SPIV_{DD}$ = 1.8 to 5.5 V, AGND = DGND = 0 V, External ADC reference = AV_{DD} , $T_A = -40^{\circ}C$ to 105°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACC	CURACY					
	Resolution		10			Bits
INL	Integral nonlinearity			±0.1	±1	LSB
DNL	Differential nonlinearity	Specified monotonic		±0.1	±1	LSB
	Offset error			±0.5	±2	LSB
	Offset error match			±0.4		LSB
	Gain error			±0.5	±2	LSB
	Gain error match			±0.4		LSB
CONVE	RSION TIME					
	ADC conversion rate			500		kSPS
	Autocycle update rate	All 8 ADC input channels enabled		16		μs
	Throughput rate	SCLK \geq 12 MHz, single analog channel			500	kSPS
	Conversion delay	Delay from trigger to conversion start	2		4	μs
ANALO	G INPUT					
	Absolute input voltage range	Independent of gain setting	AGND – 0.2		$AV_{DD} + 0.2$	V
	Full coole input voltage renge	Gain = 1, <i>adcn_gain</i> = '0'	0		V_{REF}	V
	Fuil scale input voltage range	Gain = 2, <i>adcn_gain</i> = '1'	0		$2 \times V_{REF}$	V
	Input capacitance ⁽¹⁾			40		pF
	DC input leakage current	Measured with ADC in Hold mode			±1	μA
AC PER	FORMANCE					
SFDR	Spurious Free Dynamic Range	$f_{IN} = 1 \text{ kHz}, -1 \text{ dBFS}$ sine wave		76		dBc
SNR	Signal to Noise Ratio	$f_{IN} = 1 \text{ kHz}, -1 \text{ dBFS}$ sine wave		61		dBc
SINAD	Signal to Noise+Distortion Ratio	$f_{IN} = 1 \text{ kHz}, -1 \text{ dBFS}$ sine wave		60.5		dBc
THD	Total Harmonic Distortion	f_{IN} = 1 kHz, -1 dBFS sine wave, Measured up to the fifth harmonic		75		dBc
INTERN	IAL ADC REFERENCE ⁽²⁾		+			
V _{REF}	Reference output voltage	Internal ADC reference buffered output at REF pin		2.5		V
	Reference buffer power	AV _{DD} = 5 V		360		μA
	Reference temperature coefficient			10		ppm/°C
EXTER	NAL ADC REFERENCE					
V_{REF}	Reference input voltage	External ADC reference input to REF pin	0.3		AVDD	V
	Input resistance ⁽¹⁾	V _{REF} = 5 V, AIN = 5 V		20		kΩ
TEMPE	RATURE SENSOR					
	Operating range		-40		125	°C
	Accuracy	$T_A = -40^{\circ}C$ to 125°C, $AV_{DD} = 5$ V		±1	±2.5	°C
	Resolution	LSB size		0.125		°C
	Conversion time			15		ms

(1)

Specified by design. Not tested during production. Use an external buffer amplifier with high impedance input to drive any external load. (2)

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ELECTRICAL CHARACTERISTICS – GENERAL SPECIFICATIONS

 AV_{DD} = 4.75 to 5.5 V, $GPIOV_{DD}$ = 1.8 to 5.5 V, $SPIV_{DD}$ = 1.8 to 5.5 V, AGND = DGND = 0 V, External ADC reference = AV_{DD} , T_A = $-40^{\circ}C$ to 105°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENE	RAL PURPOSE I/O					
V		$GPIOV_{DD} = 1.8 V$	0.7×GPIOV _{DD}			V
VIН	High-level input voltage	$GPIOV_{DD} = 3.3$ to 5.5 V	2.1			V
V	Low lovel input veltage	$GPIOV_{DD} = 1.8 V$			0.3	V
۷IL	Low-level liput voltage	$GPIOV_{DD} = 3.3$ to 5.5 V			0.8	V
V		I_{load} = 1.6 mA, GPIOV _{DD} = 1.8V, All GPIOs loaded and set to '1'	GPIOV _{DD} - 0.25			V
∨он	High-level output voltage	I_{load} = 1.6 mA, GPIOV _{DD} = 3.3 to 5.5V, All GPIOs loaded and set to '1'	GPIOV _{DD} - 0.2			V
V _{OL}	Low-level output voltage	I _{load} = -1.6 mA, All GPIOs loaded			0.4	V
	Input capacitance ⁽¹⁾			1		pF
	High impedance output capacitance ⁽¹⁾			1		pF
LOGIC	INPUTS: CS, SDI, SCLK		•			
V		SPIV _{DD} = 1.8 V	0.7×SPIV _{DD}			V
VIH	Hign-level input voltage	SPIV _{DD} = 3.3 to 5.5 V	2.1			V
V		SPIV _{DD} = 1.8 V			0.3	V
۷IL	Low-level input voltage	SPIV _{DD} = 3.3 to 5.5 V			0.7	V
	Input current				±1	μA
	Input capacitance (1)			1		pF
	High impedance output capacitance ⁽¹⁾			1		pF
LOGIC	OUTPUT: SDO					
V _{OH}	High-level output voltage	I _{load} = 1.6 mA	SPIV _{DD} - 0.2			V
V _{OL}	Low-level output voltage	I _{load} = -1.6 mA			0.4	V
LOGIC	OUTPUT: DAV					
V _{OL}	Low-level output voltage	I _{load} = -2 mA			0.4	V
POWE	R REQUIREMENTS					
	AV _{DD}		4.75	5	5.5	V
	GPIOV _{DD}		1.8		5.5	V
	SPIV _{DD}		1.8		5.5	V
I _{DD}	Total supply current, AV _{DD} + GPIOV _{DD} + SPIV _{DD}	Operating mode ⁽²⁾		6.5	10	mA
		Power down mode		1.25	2	mA
	Power consumption	Operating mode ⁽²⁾		32.5	55	mW
		Power down mode		6.25	11	mW
OPER/	ATING RANGE					
	Specified temperature range		-40	25	105	°C

Specified by design. Not tested in production.
 AV_{DD} = GPIOV_{DD} = SPIV_{DD} = 5 V. No DAC load, all DACs at 0x200 code and ADC at the fastest auto conversion rate.

TIMING SPECIFICATIONS⁽¹⁾⁽²⁾

 AV_{DD} = 4.75 to 5.5 V, $GPIOV_{DD}$ = 1.8 to 5.5 V, $SPIV_{DD}$ = 1.8 to 5.5 V, AGND = DGND = 0 V, External ADC reference = AV_{DD} , $T_A = -40^{\circ}C$ to 105°C (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
		SPIV _{DD} = 5.5 V			30	MHz
f _{SCLK}	SCLK frequency	SPIV _{DD} = 2.7 V			15	MHz
		SPIV _{DD} = 1.8 V			10	MHz
t _R	Input rise time	10% to 90% of SPIV _{DD}			2	ns
t _F	Input fall time	10% to 90% of SPIV _{DD}			2	ns
		SPIV _{DD} = 5.5 V	33			ns
t ₁	SCLK cycle time	SPIV _{DD} = 2.7 V	66			ns
		SPIV _{DD} = 1.8 V	100			ns
		SPIV _{DD} = 5.5 V	13			ns
t ₂	SCLK high time	SPIV _{DD} = 2.7 V	30			ns
		SPIV _{DD} = 1.8 V	50			ns
		SPIV _{DD} = 5.5 V	13			ns
t ₃	SCLK low time	SPIV _{DD} = 2.7 V	26			ns
		SPIV _{DD} = 1.8 V	40			ns
t ₄	Frame start time	CS falling edge to SCLK rising edge	5			ns
t ₅	SDI setup time	SDI valid to falling edge of SCLK	4			ns
t ₆	SDI hold time	SDI valid after falling edge of SCLK	12			ns
t ₇	Frame stop time	SCLK falling edge to \overline{CS} rising edge	15			ns
t ₈	CS high time		50			ns
		$SPIV_{DD} = 5.5 V, C_{L} = 10 pF, 1 ns \le t_{R,F(SDO)} \le 4 ns$	5		16	ns
t ₉	SDO delay	$SPIV_{DD} = 2.7 V, C_{L} = 10 pF, 1 ns \le t_{R,F(SDO)} \le 5 ns$	6		22	ns
		$SPIV_{DD} = 1.8 V, C_{L} = 10 pF, 2 ns \le t_{R,F(SDO)} \le 8 ns$	8		39	ns
t ₁₀	Wait time	CS rising edge to next SCLK rising edge	5			ns

(1) Specified by design. Not tested during production.

(2) Digital inputs and outputs timed from a voltage level of SPIV_{DD}/2.

TIMING INFORMATION



Figure 1. Serial Interface Write Timing Diagram





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Figure 17. ADC GAIN ERROR vs. TEMPERATURE





Figure 22. TEMPERATURE SENSOR ERROR vs TEMPERATURE



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THEORY OF OPERATION

SERIAL INTERFACE

The AMC7891 is controlled through a flexible four-wire serial interface compatible with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers of the AMC7891 with clock rates up to 30 MHz.

The interface is compatible with most synchronous transfer formats and is configured as a 4 pin interface. SCLK is the serial interface input clock and \overline{CS} is serial interface enable. Data is input into SDI and latched into the 24-bit wide SPI shift register on SCLK falling edges, while \overline{CS} is low. Data is clocked out of SDO on SCLK rising edges, while \overline{CS} is low. The contents of the SPI shift register are loaded into the device internal register on a \overline{CS} rising edge after some delay. When \overline{CS} is high, both SCLK and SDI inputs are blocked out and the SDO output is in high-impedance state.

The serial interface works with both a continuous and a non-continuous serial clock. A continuous SCLK source can only be used if \overline{CS} is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and \overline{CS} must be taken high after the final clock to latch the data.

Each SPI command is input to SDI and framed by signal \overline{CS} (Serial Data Enable) asserted low. The frame's first byte into SDI is the instruction cycle which identifies the request as a read or write as well as the 7-bit address to be accessed. The following two bytes in the frame form the data cycle.



Figure 23. Serial Interface Command

- **Bit 23 R/W**. Identifies the communication as a read or write command to the addressed register. Bit = '0' sets the write operation. Bit = '1' sets the read operation.
- **Bits[22:16]** A[6:0]. Register address; specifies the register to be accessed during the read or write operation.

Bits[15:0] D[15:0]. Data cycle bits.

If a write command, the data cycle bits are the values to be written to the register with address A[6:0].

If a read command, the data cycle bits are don't care values.

A read command causes an output on the SDO pin during the next SPI command cycle. The SDO read value frame is formed by the previous communication instruction cycle and the data read from the specified register.

		INSTRUCT	DATA CYLE			
SPI FRAME	PIN	Di oo	DATA OTEL			
		Bit 23	Bits [22:16]	Bits [15:0]		
Write Command	SDI	0 (R/W)	A[6:0]	Data In[15:0]		
Frame	SDO	Undefined or Read Value Frame depending on previous command				
Dood Commond	SDI	1 (R/W) A[6:0]		Don't care		
Frame	SDO	Undefined or Read Value Frame depending on prev command				
Dood Value Frome	SDI	New Write or Read Command Frame				
Reau value Flame	SDO	1 (R/W)	A[6:0]	Data Out[15:0]		

Table 1. Serial Data Format



The serial clock can be continuous or gated as long as there are exactly 24 falling clock edges within the frame. A write command issued in frames whose width is not 24 bits is incorrect and ignored by the AMC7891. A read command frame not equal to 24 bits may result in abnormal data on SDO and must be ignored by the host processor. In order for another serial transfer to occur, \overline{CS} must be brought low again to start a new cycle. Figure 24 and Figure 25 show multiple write and read operations.



Wn = Write Command for Register N XX = Don't care, undefined

Figure 24. Serial Interface Write Operation





REGISTER MAP

The AMC7891 has 16-bit registers containing device configuration and conversion results. A 7-bit register address indicates the proper register.

			MSB															LSB
NAME	ADDR	DEFAULT	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TEMP_data	0x00	0x0000	0	0	0	0		1				tempda	ata(11:0)		1	1		1
TEMP_config	0x0A	0x0008	0	0	0	0	0	0	0	0	0	0	0	0	temp_ en	0	0	0
TEMP_rate	0x0B	0x0007	0	0	0	0	0	0	0	0	0	0	0	0	0	ter	mp_rate(2	2:0)
ADC0_data	0x23	0x0000	0	0	0	0	0	0					adc0_c	lata(9:0)				
ADC1_data	0x24	0x0000	0	0	0	0	0	0					adc1_c	lata(9:0)				
ADC2_data	0x25	0x0000	0	0	0	0	0	0					adc2_c	lata(9:0)				
ADC3_data	0x26	0x0000	0	0	0	0	0	0					adc3_c	lata(9:0)				
ADC4_data	0x27	0x0000	0	0	0	0	0	0					adc4_c	lata(9:0)				
ADC5_data	0x28	0x0000	0	0	0	0	0	0					adc5_c	lata(9:0)				
ADC6_data	0x29	0x0000	0	0	0	0	0	0					adc6_c	lata(9:0)				
ADC7_data	0x2A	0x0000	0	0	0	0	0	0					adc7_c	lata(9:0)				
DAC0_data	0x2B	0x0000	0	0	0	0	0	0					dac0_c	lata(9:0)				
DAC1_data	0x2C	0x0000	0	0	0	0	0	0					dac1_c	lata(9:0)				
DAC2_data	0x2D	0x0000	0	0	0	0	0	0	dac2_data(9:0)									
DAC3_data	0x2E	0x0000	0	0	0	0	0	0	dac3_data(9:0)									
DAC0_clear	0x2F	0x0000	0	0	0	0	0	0					dac0_c	lear(9:0)				
DAC1_clear	0x30	0x0000	0	0	0	0	0	0					dac1_c	lear(9:0)				
DAC2_clear	0x31	0x0000	0	0	0	0	0	0					dac2_c	lear(9:0)				
DAC3_clear	0x32	0x0000	0	0	0	0	0	0					dac3_c	lear(9:0)				
GPIO_config	0x33	0x0000	0	0	0	0	ioc3_ io	ioc2_ io	ioc1_ io	ioc0_ io	iob3_ io	iob2_ io	iob1_ io	iob0_ io	ioa3_ io	ioa2_ io	ioa1_ io	ioa0_ io
GPIO_out	0x34	0x0000	0	0	0	0	ioc3_ out	ioc2_ out	ioc1_ out	ioc0_ out	iob3_ out	iob2_ out	iob1_ out	iob0_ out	ioa3_ out	ioa2_ out	ioa1_ out	ioa0_ out
GPIO_in	0x35	NA	0	0	0	0	ioc3_ in	ioc2_ in	ioc1_ in	ioc0_ in	iob3_ in	iob2_ in	iob1_ in	iob0_ in	ioa3_ in	ioa2_ in	ioa1_ in	ioa0_ in
AMC_config	0x36	0x2000	0	0	<i>adc_</i> <i>mo</i> de	adc_tr ig	dac_lo ad	resvd	adc_ra	ate(1:0)	adc_r eady	0	0	0	0	0	0	0
ADC_enable	0x37	0x0000	0	adc0_ en	adc1_ en	resvd	adc2_ en	adc3_ en	resvd	adc4_ en	adc5_ en	adc6_ en	adc7_ en	0	0	0	0	0
ADC_gain	0x38	0xFF00	adc0_ gain	adc1_ gain	adc2_ gain	adc3_ gain	adc4_ gain	adc5_ gain	adc6_ gain	adc7_ gain	0	0	0	0	0	0	0	0
DAC_clear	0x39	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	<i>dac3_</i> clear	<i>dac2_</i> clear	<i>dac1_</i> clear	<i>dac0_</i> clear
DAC_sync	0x3A	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	dac3_ sync	dac2_ sync	dac1_ sync	dac0_ sync
AMC_power	0x3B	0x0000	0	adc_o n	ref_on	<i>dac0</i> on	dac1_ on	dac2_ on	dac3_ on	0	0	0	0	0	0	0	0	0
AMC_reset	0x3E	0x0000								reset	(15:0)							
AMC_ID	0x40	0x0044		device_id(15:0)														

Table 2. Register Map

NSTRUMENTS

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REGISTER DESCRIPTIONS

Register name: temp_data - Address: 0x00, Default: 0x0000 (READ ONLY)

Register Name	Address	Bit	Name	Function	Default Value
temp_data	0x00	15:12	Reserved	Reserved for factory use.	All zeros
		11:0	temp_data(11:0)	Stores the temperature sensor reading in twos complement format. 0.125°C/LSB.	0x000

Register name: temp_config – Address: 0x0A, Default: 0x0008 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
temp_config	0x0A	15:4	Reserved	Reserved for factory use.	All zeros
		3	temp_en	When set to '1', the on-chip temperature sensor is enabled.	1
		2:0	Reserved	Reserved for factory use.	All zeros

Register name: temp_rate - Address: 0x0B, Default: 0x0007 (READ/WRITE)

Register Name	Address	Bit	Name		F	Default Value	
temp_rate	0x0B	15:3	Reserved	Re	served for factory use.	All zeros	
		2:0	temp_rate(2:0)	Se	ts the temperature sensor A	DC conversion time	111
					temp_rate(2:0)	Conversion time	
					000	128x	
					001	64x	
					010	32x	
					011	16x	
					100	8x	
					101	4x	
					110	2x	
					111	15 ms	

Register name: ADCn_data - Address: 0x23 to 0x2A, Default: 0x0000 (READ ONLY)⁽¹⁾

		_				. ,		
Register Name	Address	Bit	Name			Default Value		
ADCn_	0x23 to	15:10	Reserved	Res	served for factory use			All zeros
data 0x2	0x2A	9:0	adcn_data(9:0)	Sto	res the 10-bit ADCn c	ht binary format.	All zeros	
					Input Channel	ADC Register Value	Register Address	
					AIN_0	adc0_data(9:0)	0x23	
					AIN_1	adc1_data(9:0)	0x24	
					AIN_2	adc2_data(9:0)	0x25	
					AIN_3	adc3_data(9:0)	0x26	
					AIN_4	adc4_data(9:0)	0x27	
					AIN_5	adc5_data(9:0)	0x28	
					AIN_6	adc6_data(9:0)	0x29	
					AIN 7	adc7 data(9:0)	0x2A	

(1) All ADCn_data registers are formatted in the manner shown here. n = 0, 1, ..., 7

EXAS

Register name: DACn_data - Address: 0x2B to 0x2E, Default: 0x0000 (READ/WRITE)⁽¹⁾

Register Name	Addres s	Bit	Name			De V	efault alue				
DACn_ data	0x2B to	15:10	Reserved	Re	Reserved for factory use.				zeros		
0x28	0x2E	9:0	dac <i>n_</i> data(9:0)	St bir	ores the 10-bit data to be hary format.	All	All zeros				
					Output Channel	DAC Register Value	Register Address				
							DACOUT_0	dac0_data(9:0)	0x2B		
									DACOUT_1	dac1_data(9:0)	0x2C
					DACOUT_2	dac2_data(9:0)	0x2D				
					DACOUT_3	dac3_data(9:0)	0x2E				

(1) All DACn_data registers are formatted in the manner shown here. n = 0, 1, ..., 3

Register name: DACn_clear – Address: 0x2F to 0x32, Default: 0x0000 (READ/WRITE)⁽¹⁾

Register Name	Address	Bit	Name			Default Value		
DACn_ clear	0x2F to	15:10	Reserved	R	eserved for factory us	All zeros		
	0x32	9:0	dac <i>n_</i> clear(9:0)	S S	tores the 10-bit data to traight binary format.	n when cleared.	All zeros	
					Output Channel	DAC Clear Value	Register Address	
					DACOUT_0	dac0_clear(9:0)	0x2F	
					DACOUT_1	dac1_clear(9:0)	0x30	
				DACOUT_2	dac2_clear(9:0)	0x31		
					DACOUT_3	dac3_clear(9:0)	0x32	

(1) All DAC*n*_data registers are formatted in the manner shown here. n = 0, 1, ..., 3

Register name: GPIO_config - Address: 0x33, Default: 0x0000 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
GPIO_config	0x33	15:12	Reserved	Reserved for factory use.	All zeros
		11	ioc3_io	When cleared to '0' the corresponding GPIO is configured as an input and set on high-impedance state (default).	0
		10	ioc2_io		0
		9	ioc1_io	When set to '1' the corresponding GPIO is configured as an output.	0
		8	ioc0_io		0
		7	iob3_io		0
		6	iob2_io		0
		5	iob1_io		0
		4	iob0_io		0
		3	ioa3_io		0
		2	ioa2_io		0
		1	ioa1_io		0
		0	ioa0_io		0



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Register name: GPIO_out – Address: 0x34, Default: 0x0000 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
GPIO_out	0x34	15:12	Reserved	Reserved for factory use.	All zeros
		11	ioc3_out	If the corresponding GPIO is configured as an output in register	0
		10	ioc2_out	<i>GPIO_config, 0x33</i> , the value on this bit sets the digital output.	0
		9	ioc1_out	If the corresponding GPIO is configured as an input in register	0
		8	ioc0_out	<i>GPIO_config, 0x</i> 33, this bit is a don't care.	0
		7	iob3_out		0
		6	iob2_out		0
		5	iob1_out		0
		4	iob0_out		0
		3	ioa3_out	1	0
		2	ioa2_out		0
		1	ioa1_out		0
		0	ioa0_out		0

Register name: GPIO_in – Address: 0x35, Default: NA (READ ONLY)

Register Name	Address	Bit	Name	Function	Default Value
GPIO_in	0x35	15:12	Reserved	Reserved for factory use.	All zeros
		11	ioc3_in	If the corresponding GPIO is configured as an output in register <i>GPIO_config, 0x33</i> , the value on this bit correspods to the digital output.	0
		10	ioc2_in		0
		9	ioc1_in	If the corresponding GPIO is configured as an output in register	0
	8	ioc0_in	<i>GPIO_config 0x33</i> , this bit matches the corresponding value in register <i>GPIO_out</i> , 0x34.	0	
		7 iob3_in		0	
		6	iob2_in		0
		5	iob1_in		0
		4	iob0_in		0
		3	ioa3_in		0
	2	ioa2_in		0	
		1	ioa1_in		0
		0	ioa0_in		0

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Register Name	Address	Bit	Name	Fu	inction	Default Value		
AMC_config	0x36	15:4	Reserved	erved for factory use.		All zeros		
		13	adc_mode	When set to '1', the ADC is in Auto-mode conversion. When cleared to '0', the ADC is in Direct-mode conversion.				
		12	adc_trig	n set to '1' triggers a new Al ed to '0' automatically after	DC conversion cycle. The bit is the ADC conversion cycle starts.	0		
		11	dac_load	n set to '1' data is loaded in hronous mode in register <i>da</i>	to the DAC output channels set to c_sync, 0x3A.	0		
		10		The AMC7891 updates the DAC output only if the corresponding <i>dacn_data</i> register has been accessed since the last <i>dac_load</i> trigger. Any DAC channels that have not been accessed are not reloaded again.				
		10	Reserved	erved for factory use.		0		
		9:8	adc_rate(1:0)	the primary ADC conversion	n rate	00		
				adc_rate(1:0)	Conversion time (kSPS)			
				00	500			
				01	250			
				10	125			
				11	62.5			
		7	adc_ready	data available indicator in E ed to '0' in Auto-mode conv	Direct-mode conversion. Always ersion.	0		
				A '1' read from this bit indicates the ADC conversion cycle is complete and new data is available.				
				A '0' read from this bit indicates the ADC conversion cycle is in progress or the ADC is in Auto-mode.				
			To	To clear this bit one of the following events has to occur:				
	6:0			 Reading the adcn_data re Starting a new ADC conve 	gisters. ersion cycle.			
		(6:0	Reserved	erved for factory use.		All zeros	

Register name: AMC_config - Address: 0x36, Default: 0x2000 (READ/WRITE)

Register name: ADC_enable - Address: 0x37, Default: 0x0000 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
ADC_enable	0x37	15	Reserved	Reserved for factory use.	All zeros
		14	adc0_en	When set to '1' the corresponding analog input channel AIN_n	0
		13	adc1_en	(n = 0, 1,, 7) is accessed during an ADC conversion cycle.	0
		11	adc2_en	When cleared to '0' the corresponding input channel AIN_n	0
-		10	adc3_en	(n = 0, 1,, 7) is ignored during an ADC conversion cycle.	0
	8	adc4_en		0	
		7	adc5_en		0
		6	adc6_en		0
		5	adc7_en		0
		12,9	Reserved	Reserved for factory use. Must be set to 0 for proper device operation.	All zeros
		4:0	Reserved	Reserved for factory use.	All zeros



	•••••_g				
Register Name	Address	Bit	Name	Function	Default Value
ADC_gain	0x38	15	adc0_gain	When set to '1' the corresponding analog input channel AIN_ n ($n = 0, 1,, 7$) input range is 2 × V _{REF} .	1
		14	adc1_gain		1
		13	adc2_gain	When cleared to '0' the corresponding input channel AIN_ n ($n = 0, 1,, 7$) input range is V _{REF} .	1
		12	adc3_gain		1
		11	adc4_gain		1
		10	adc5_gain		1
		9	adc6_gain		1
		8	adc7_gain		1
		7:0	Reserved	Reserved for factory use.	All zeros

Register name: ADC_gain – Address: 0x38, Default: 0xFF00 (READ/WRITE)

Register name: DAC_clear - Address: 0x39, Default: 0x0000 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
ADC_clear 0x39	15:4	Reserved	Reserved for factory use.	All zeros	
		3	dac3_clear	When set to '1' clears the corresponding DACout_ n ($n = 0, 1,, 3$) output to the value specified in register <i>dacn_clear</i> , 0x2F to 0x32. When cleared to '0' the corresponding DACout_ n ($n = 0, 1,, 3$) output returns to normal operation.	0
		2	dac2_clear		0
		1	dac1_clear		0
		0	dac0_clear		0

Register name: DAC_sync - Address: 0x3A, Default: 0x0000 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
DAC_sync	0x3A	15:4	Reserved	Reserved for factory use.	All zeros
		3	dac3_sync	When set to '1' clears the corresponding DACout_ n ($n = 0, 1,, 3$) is set to	0
		2	dac2_sync	synchronous-mode.	0
		1	dac1_sync	When cleared to '0' the corresponding DACout_ n ($n = 0, 1,, 3$) is set to asynchronous-mode.	0
		0	dac0_sync		0

Register name: AMC_power - Address: 0x3B, Default: 0x0000 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
AMC_power	wer 0x3B 15 Reserved Reserved for factory use.				0
		14	adc_on	When cleared to '0' the primary ADC is in power-down mode. When set to '1' the primary ADC is in active mode.	0
		13	ref_on	When cleared to '0' the internal reference buffer is in power-down mode; the device is in External ADC Reference mode and the REF pin is an input. When set to '1' the internal reference buffer is active; the device is in Internal ADC Reference mode and the REF pin is an output.	0
		12	dac0_on	When cleared to '0' DAC0 is in power-down mode. DACout_0 is in high-impedance state. When set to '1' DAC0 is in active mode.	0
		11	dac1_on	When cleared to '0' DAC1 is in power-down mode. DACout_1 is in high-impedance state. When set to '1' DAC1 is in active mode.	0
		10	dac2_on	When cleared to '0' DAC2 is in power-down mode. DACout_2 is in high-impedance state. When set to '1' DAC2 is in active mode.	0
		9	dac3_on	When cleared to '0' DAC3 is in power-down mode. DACout_3 is in high-impedance state. When set to '1' DAC3 is in active mode.	0
		8:0	Reserved	Reserved for factory use.	All zeros

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Register name: AMC_reset – Address: 0x3E, Default: 0x0000 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
AMC_reset	0x3E	15:0	reset(15:0)	Writing 0x6600 to this register forces a reset operation. During reset, all SPI communication is blocked. After issuing the reset, there is a wait of at least 30 μ s before communication can be resumed.	All zeros

Register name: AMC_ID - Address: 0x40, Default: 0x0044 (READ ONLY)

Register Name	Address	Bit	Name	Function	Default Value
AMC_ID	0x40	15:0	device_id(15:0)	A hardwired register that contains the AMC7891 ID.	0x0044



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ADC OPERATION

The AMC7891 has two analog-to-digital converters (ADCs): a primary ADC and a secondary ADC. The primary ADC consists of an 8-channel multiplexer, an on-chip track-and-hold, and a successive approximation register (SAR) ADC based on a capacitive digital-to-analog converter (DAC). This ADC runs at rates up to 500 kSPS and converts the uncommitted analog channel inputs, AIN0 to AIN7.

The analog input range for the device can be selected as 0 V to V_{REF} or 0 V to (2 × V_{REF}). The AMC7891 has an on-chip buffered 2.5V reference that can be disabled when an external reference is preferred. The secondary ADC is a part of the on-chip temperature sensing function.

PRIMARY ADC OPERATION

The following sections describe the operation of the primary ADC. The temperature sensor ADC always operates in the background.

ANALOG INPUT FULL SCALE RANGE

The values in register *ADC_gain* determine the full-scale range of the analog inputs. The full-scale range for input channel AIN*n* is V_{REF} when bit *adcn_gain* = 0, or 2 × V_{REF} when *adcn_gain* = 1. Each input must not exceed the supply value of AV_{DD} + 0.2 V or AGND - 0.2 V.

When internal ADC reference is enabled, the buffered internal reference is used as the ADC reference. When external ADC reference is selected, an external reference voltage applied to the REF pin is the ADC reference.

ANALOG INPUTS

The AMC7891 has 8 uncommitted single-ended analog inputs. Figure 26 shows the equivalent input circuit of the AMC7891. The (peak) input current through the analog inputs depends on the sample rate, input voltage, and source impedance. The current into the AMC7891 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance to a 10-bit settling level within the acquisition time. When the converter goes into hold mode, the input impedance is greater than 1 G Ω .

In applications where the signal source has high impedance, it is recommended to buffer the analog input before applying it to the ADC. The analog input range can be programmed to be either 0 V to V_{REF} or 0 V to (2 × V_{REF}). With a gain of 2, the input is effectively divided by two before the conversion takes place. Note that the voltage with respect to AGND on the ADC analog input cannot exceed AV_{DD} .



Figure 26. ADC Equivalent Input Circuit

ADC TRIGGER SIGNALS

The ADC can be triggered internally by writing to the *adc_trig* bit in register *AMC_config*. When a new trigger activates, the ADC stops any existing conversion immediately and starts a new cycle. For example, the ADC is programmed to sample input channels 0 to channel 3 repeatedly (auto-mode). During the conversion of channel 1, a trigger is activated. The ADC stops the conversion of channel 1 immediately and starts the conversion of channel 0 again, instead of proceeding to convert channel 2.

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CONVERSION MODES

Two types of ADC conversions are available: direct-mode and auto-mode. *adc_mode bit* (*AMC_config* register, bit 13) sets the conversion mode. The default conversion mode is auto-mode (*adc_mode* = '1').

In direct-mode conversion, each analog channel within the specified group in register *ADC_enable* is converted a single time. After the last channel is converted, the ADC goes into an idle state and waits for a new trigger.

Auto-mode conversion, on the other hand, is a continuous operation. In auto-mode, each analog channel within the specified group is converted sequentially and repeatedly.

The flow chart of the ADC conversion sequence in Figure 27 shows the conversion process.



Figure 27. ADC Conversion Sequence



When any of the following events occur, the current conversion cycle stops immediately:

- A new trigger is issued.
- The conversion mode changes.
- Either ADC channe register is rewritten.

When a new trigger activates, the ADC starts a new conversion cycle. The trigger should not be issued at the same time the conversion mode is changed. If a '1' is simultaneously written to the *adc_trig* bit when changing the adc_mode bit from '0' to '1', the current conversion stops and immediately returns to the *wait for ADC trigger* state.

To avoid noise caused by the bus clock, it is recommended that no bus clock activity occurs for at least the conversion process time immediately after the ADC conversion starts.

DOUBLE-BUFFERED ADC DATA REGISTER

The host can access all eight, double-buffered $ADCn_data$ registers, as shown in Figure 28. The conversion result from the analog input with channel address n, (where n = 0 to 7) is stored in $adcn_data[9:0]$ in straight binary format. When the conversion of an individual channel is completed, the data is immediately transferred into the corresponding $adcn_tmpry$ temporary register, the first stage of the data buffer. When the conversion of the last channel completes, all data in the $adcn_tmpry$ registers is simultaneously transferred to the corresponding $adcn_data[9:0]$ value, the second stage of the data buffer.

In the case when a data transfer is in progress between any *ADCn_data* register and the AMC7891 shift register, all *ADCn_data* registers are not updated until the data transfer is complete.



Figure 28. ADC Structure

PROGRAMMABLE CONVERSION RATE

The maximum ADC conversion rate is 500 kSPS for a single channel in auto mode, as shown in Table 3. The conversion rate is programmable through *adc_rate[1:0]* (*AMC_config* register, [9:8] bits). When more than one channel is selected, the conversion rate is divided by the number of channels selected in register *ADC_enable*.

In auto mode, the $adc_rate[1:0]$ value determines the actual conversion rate. In direct mode, $adc_rate[1:0]$ limits the maximum possible conversion rate. The actual conversion rate in direct mode is determined by the rate of the conversion trigger. Note that when a trigger is issued, there may be a delay of up to 4 µs to internally synchronize and initiate the start of the sequential channel conversion process. In both direct- and auto- modes, when $adc_rate[1:0]$ is set to a value other than the maximum rate ('00'), nap mode is activated between conversions. By activating nap mode, the AV_{DD} supply current is reduced.

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adc_rate[1:0]	t _{ACQ} (μs)	t _{conv} (μs)	NAP ENABLED	THROUGHPUT (Single-Channel Auto Mode)							
00	0.375	1.625	No	500 kSPS (default)							
01	2.375	1.625	Yes	250 kSPS							
10	6.375	1.625	Yes	125 kSPS							
11	14.375	1.625	Yes	62.5 kSPS							

Table 3. ADC Conversion Rate

HANDSHAKING WITH THE HOST

a) Direct Mode

The DAV pin and *adc_ready* bit (*AMC_config* register, bit 7) provide handshaking with the host. The DAV pin is an open-drain, active low output. If used, an external 10 k Ω pull-up resistor to GPIOV_{DD} is required. If unused, the pin can be connected to DGND. Pin and bit status depend on the conversion mode (direct or auto), as shown in Figure 29.

In direct mode, after the *ADCn_data* registers of all the selected channels in register *adc_enable* are updated, *adc_ready* is set immediately to '1' and the DAV pin is active (low) to signify that new data is available.

The *adc_ready* bit is reset to '0' and the DAV pin goes back to inactive (high) either by reading any of the *ADCn_data* registers or when a new ADC conversion is started by issuing a trigger by *adc_trig*. The update takes place immediately after the read command frame indicating the read operation or trigger event.

In auto-mode, after the *adcn_data[9:0]* values are updated, a pulse of 1µs (low) appears on the DAV pin to signify that new data is available. However, the *adc_trig* bit is inactive and always set to '0'.







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TEMPERATURE SENSOR OPERATION (SECONDARY ADC)

The AMC7891 contains an on-chip temperature sensor used to measure the device temperature. The temperature sensor is continuously monitoring, and new readings are automatically available every cycle. The analog temperature reading is converted by a secondary ADC that runs in the background at a lower speed than the primary ADC.

The temperature measurement relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward voltage of the diode (V_{BE}) depends on the current passing through it and the ambient temperature. The change in V_{BE} when the diode operates at two different currents (a low current of I_{LOW} and a high current of I_{HIGH} , is shown in Equation 1:

$$V_{BE_{HIGH}} - V_{BE_{LOW}} = \eta kT/q \times \ln(I_{HIGH}/I_{LOW})$$

(1)

Where:

- k is Boltzmann's constant.
- q is the charge of the carrier.
- T is the absolute temperature in Kelvins (K).
- η is the ideality of the transistor as sensor.



Figure 30. Integrated Temperature Sensor

The temperature sensor can be disabled by clearing to '0' the *temp_en* bit (*TEMP_config* register, bit 3). When disabled, the sensor is not converted. The AMC7891 continuously monitors the temperature sensor in the background, leaving the user free to perform conversions on the primary ADC. When one monitor cycle finishes, a signal passes to the control logic to automatically initiate a new conversion.

The analog sensing signal is preprocessed by a low-pass filter and signal conditioning circuitry, and then digitized by the secondary ADC. The resulting digital signal is further processed by the digital filter and processing unit. The final result is stored as a 12-bit value in the *TEMP_data* register as *tempdata[11:0]*. The format of the final result is in twos complement, as shown in Table 4. Note that the device measures the temperature from -40° C to 150° C.

If a data transfer is in progress between the *TEMP_data* register and the AMC Shift Register, the *TEMP_data* register is frozen until the data transfer is complete.

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TEMPERATURE (°C)	DIGITAL CODE							
+255.875	01111111111							
+150	010010110000							
+100	001100100000							
+50	000110010000							
+25	000011001000							
+1	00000001000							
0	0000000000							
-1	11111111000							
-25	111100111000							
-50	111001110000							
-100	110011100000							
-150	1011010000							
-256	10000000000							

Table 4. Temperature Data Format

The temperature conversion time is by default 15 ms but it can be increased by setting *temp_rate[2:0]* (*TEMP_rate* register, bits [2:0]) as shown in Table 5.

adc_rate[2:0]	CONVERSION TIME
000	128x
001	64x
010	32x
011	16x
100	8x
101	4x
110	2x
111	15 ms

Table 5. Temperature Conversion Time



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REFERENCE OPERATION

The AMC7891 includes a buffered internal reference for the ADC, DACs and temperature sensor. The internal reference is a 2.5 V, bipolar transistor-based, precision bandgap reference.

The internal reference always drives the DACs and the internal temperature sensor directly (unbuffered); however the ADC can be driven either by the internal reference (buffered) or by an external one as determined by the *ref_on* bit (*AMC_power* register, bit 13). If used, the external reference is applied to the dual purpose REF pin. A decoupling capacitor is recommended between the external reference output an AGND for noise filtering.

In internal ADC reference mode, the buffered internal reference is available at the REF pin. A compensating 4.7µF capacitor is recommended between the internal buffered reference output and AGND.

On power-up, the AMC7891 is configured for ADC external reference (*ref_on* bit cleared to '0'). In this case it is important that the external reference source is not input into the REF pin until AV_{DD} is stable. If using the internal reference to drive the ADC, the *ref_on* must be set to '1' to enable the internal reference buffer.



Figure 31. External ADC Reference







DAC OPERATION

The AMC7891 contains 4 independent DACs that provide analog control with 10 bits of resolution using an internal reference. Each DAC core consists of a 10-bit string DAC and an output voltage buffer.

The DAC latch stores the code that determines the output voltage from the DAC string. The code is transferred from the *DACn_data* registers to the DACn data latches when the internal DAC load signal is generated.



Figure 33. DAC Block Diagram

The resistor string structure is shown in Figure 34. It consists of a string of resistors, each of value R. The code loaded to the DAC Latch determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. This architecture has inherent monotonicity, voltage output, and low glitch. It is also linear because all the resistors are of equal value.



Figure 34. Resistor String



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DAC OUTPUT

The full-scale output range of each DAC is set by the product of the internal reference voltage times a fixed gain of 2 in the DAC output buffer ($2 \times V_{REF}$). The full-scale output range of each DAC is limited by the analog power supply. The maximum and minimum outputs from the DAC cannot exceed AV_{DD} or be lower than AGND, respectively.

After power-on or a reset event, the DAC output buffers are in power-down mode. In this mode all *dacn_data* registers and DAC*n* data latches are set to their default values, the output buffers are in a high-impedance state and each DACout*n* output pin connects to AGND through an internal 10 k Ω resistor.

DOUBLE-BUFFERED DAC DATA REGISTERS

There are 4 double-buffered DAC data registers. Each DAC has an internal latch preceded by a DAC data register. Data is initially written to the individual $DACn_data$ register as the value $dacn_data[9:0]$ and then transferred to its corresponding DAC*n* latch. When the DAC*n* latch is updated, the output from pin DACout*n* changes to the newly set value. When the host reads from $DACn_data$, the value held in the DAC*n* latch is returned (not the value held in the data register).

The DACs update mode is determined by the *dacn_sync* setting in the *DAC_sync* register. When *dacn_sync* is cleared to '0', the DAC*n* is in asynchronous mode. In asynchronous mode, a write to the *DACn_data* register results in an immediate update of the DACn latch and corresponding DACout*n* output.

Synchronous mode is selected by setting *dacn_sync* to '1'. In synchronous mode writing to the *DACn_data* register does not update the DAC*n* latch DACout_*n* output. Instead, the update occurs only until the *dac_load* bit (*AMC_config* register, bit 11) is set to '1'. By setting the *DAC_sync* register properly, several DACs can be updated at the same time.

MODE	dacn_sync	WRITING TO dac_load	OPERATION
Asynchronous	0	Don't care	Update DACn individually. The DAC <i>n</i> latch and DACout <i>n</i> output are immediately updated after writing to DACn_data.
Synchronous	1	1	Simultaneously update all DACs by internal trigger. Writing '1' to <i>dac_load</i> generates an internal load DAC trigger signal that updates the DAC <i>n</i> latches and DACout <i>n</i> outputs with the contents of the corresponding <i>dacn_data[9:0]</i> register values.

Table 6. DAC Output Modes

The AMC7891 updates the DAC latches only if it has been accessed since the last time *dac_load* was issued, thereby eliminating any unnecessary glitch. Any DAC channels that have not been accessed are not reloaded again. When the DAC latch is updated, the corresponding output changes to the new level immediately.

CLEAR DACS

Each DAC can be cleared using the DAC_clear register. When setting the corresponding dacn_clear bit to '1', DACn goes to a clear state in which the DACoutn is immediately updated with the predefined value in the DACn_clear register, regardless of the dacn_sync status. The data register value dacn_data[9:0] does not change.

When the DAC goes back to normal operation, the DACout*n* output is set back to the DAC*n* latch value regardless of the *dac_sync* status.



Figure 35. Clear DAC Operation

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GENERAL PURPOSE INPUT/OUTPUT PINS

The AMC7891 has twelve GPIO pins. Each GPIO provides a bidirectional, digital I/O signal. These pins can receive an input or produce an output as configured by the *GPIO_config* register.

To configure the GPIOxx pin as an output, the corresponding *ioxx_io* bit needs to be set to '1'. The GPIOxx is an output driver with a pull to the value of the corresponding *ioxx_out* bit in register GPIO_out.

To set the *GPIOxx* pin as an input, the corresponding *ioxx_io* bit has to be cleared to '0'. In this mode the GPIOxx pin is in high-impedance state and the read value is stored in the corresponding *ioutxx_in* bit in register *GPIO_in*. When set as an input, writes to the *GPIO_out* register do not affect the GPIO values.

After a power-on or reset event, all the GPIO pins are set as inputs and, hence in high-impedance state.

POWER-UP SEQUENCE

After all supplies are established, serial communication with the AMC7891 is valid only after a 200 μ s power-up reset delay. Following this, a software reset should be issued to ensure proper operation of the AMC7891. A software reset is issued by writing the value '0x6600' to *reset[15:0]* in register *AMC_reset*. Communication to the AMC7891 is re-established after a 200 μ S delay from the reset operation (measured from the rising edge of CS establishing the end of the reset command frame).

At power-up or after a software-reset command all registers are set to the default values (see Table 6). The default state of all analog blocks is off as determined by the default value of the *AMC_power* register.

For the device to work properly, AV_{DD} must power up before applying any inputs to the GPIO pins. In addition, if using an external ADC reference AV_{DD} must power up before the external reference voltage is applied to the REF pin.

The following power-up sequence is recommended for the AMC7891.

- 1. No input should be applied to the GPIO pins. Also, if using an external ADC reference, it should not be applied to the REF pin.
- Supply all voltages (AV_{DD}, GPIOV_{DD} and SPIV_{DD}). If possible, it is recommended to apply IOV_{DD} before AV_{DD}. However, the supplies can be powered up simultaneously or in any order with no detrimental effect to the device.
- 3. After AV_{DD} has been applied there is a 200 μ s power-up reset delay. No serial communication should be attempted during this time.
- 4. Issue a software-reset command by writing the value '0x6600' to reset[15:0] in register AMC_reset.
- 5. Wait at least 200 μ s from the rising edge of \overline{CS} to complete the software-reset.
- 6. Program the registers according to the desired mode of operation.



APPLICATION INFORMATION

BASE STATION AMPLIFIER MONITOR AND CONTROL

The AMC7891 is a highly integrated, low-power, complete analog monitoring and control system in a small package; all of these features make the AMC7891's an ideal low-cost, bias control circuit for modern RF transistor modules such as the power amplifiers (PA) and low-noise amplifiers (LNA) found in RF communication systems.

The AMC7891 is used in RF amplifier signal chains to set the transistor's optimal bias condition as well as to monitor for any possible malfunction. The AMC7891 four independent DAC outputs allow control of the transistor's gate bias voltages as well as of any variable-gain amplifiers (VGAs) in the signal chain. The AMC7891 twelve configurable GPIOs enable digital signal control and monitoring. Additionally, the device has 8 uncommitted analog inputs driving a highly precise ADC and an accurate on-chip temperature sensor that allow continuous monitoring of the main factors determining optimal amplifier operation such as temperature, supply voltages as well as drain bias currents through external current shunt monitors. The use of external current shunt monitors gives the system designer the flexibility to choose the optimal number of current measurements for the amplifier topology as well as the accuracy, voltage range and gain setting according to the drain current level to be measured. The Texas Instruments' INA282 family, which includes the INA282, INA283, INA284, INA285 and INA286 devices, are highly-accurate, wide common-mode range current shunt monitors with gains going from 50V/V to 1000V/V.

The circuit in Figure 36 shows a typical multi-stage Doherty PA monitoring and control system using the AMC7891. The AMC7891 DAC outputs are used to set the bias gate voltage of each LDMOS transistor in the PA as well as to set the gain of the VGA driving the PA. The AMC7891 ADC inputs are used to monitor the most important parameters in the PA operation: supply voltages, drain bias currents as well as the TX and RX signal power. The GPIOs give additional system flexibility. In the system example below three GPIOs are used to address an external 8:1 multiplexer used for giving additional inputs to the AMC7891 ADC.



Figure 36. PA Monitor and Control System

REVISION HISTORY

Cł	anges from Original (August 2011) to Revision A Page								
•	Changed from a 3 page Product Preview To a Prodcution Data Sheet	1							
•	Added the TYPICAL CHARACTERISTICS: DAC section	10							
•	Added the TYPICAL CHARACTERISTICS: ADC section	12							

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30-May-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)		(3)		(4/5)	
AMC7891SRHHR	ACTIVE	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC7891	Samples
AMC7891SRHHT	ACTIVE	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC7891	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC7891SRHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
AMC7891SRHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

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PACKAGE MATERIALS INFORMATION

31-Jul-2013



*All dimensions are nominal

Device Package Type		Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
AMC7891SRHHR	VQFN	RHH	36	2500	367.0	367.0	38.0	
AMC7891SRHHT	VQFN	RHH	36	250	210.0	185.0	35.0	

MECHANICAL DATA



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

F. Falls within JEDEC MO-220.





THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



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