SBAS262C – APRIL 2003 – REVISED JUNE 2007

12-Bit, 65MSPS Sampling, +3.3V ANALOG-TO-DIGITAL CONVERTER

FEATURES

- HIGH SNR: 70dB
- HIGH SFDR: 88dBFS
- LOW POWER: 285mW
- INTERNAL/EXTERNAL REFERENCE OPTION
- SINGLE-ENDED OR FULLY DIFFERENTIAL ANALOG INPUT
- FLEXIBLE DUTY CYCLE ADJUST CIRCUITRY
- LOW DNL: 0.5LSB
- SINGLE +3.3V SUPPLY OPERATION
- TQFP-48

APPLICATIONS

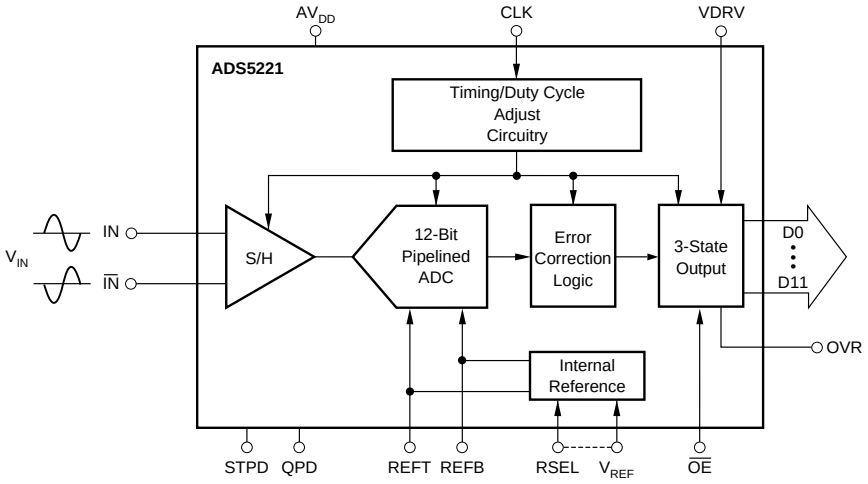
- WIRELESS LOCAL LOOP
- COMMUNICATIONS
- MEDICAL IMAGING
- PORTABLE INSTRUMENTATION

DESCRIPTION

The ADS5221 is a pipeline, CMOS Analog-to-Digital Converter (ADC) that operates from a single +3.3V power supply. This converter provides excellent performance with a single-ended input and can be operated with a differential input for added spurious performance. This high-performance converter includes a 12-bit quantizer, high bandwidth track-and-hold, and a high accuracy internal reference; it also allows for the user to disable the internal reference and utilize external references, providing excellent gain and offset matching in multi-channel applications or in applications where full-scale range adjustment is required.

The ADS5221 employs digital error correction techniques to enable excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for medical imaging, communications, video, and test instrumentation. The ADS5221 offers power dissipation of 285mW and also provides two power-down modes.

The ADS5221 is specified at a maximum sampling frequency of 65MHz and a differential input range of 1V to 2V. The ADS5221 is available in a TQFP-48.



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ABSOLUTE MAXIMUM RATINGS[1]

AV_{DD}, DV_{DD}, VDRV	+3.8V
Analog Input	–0.3V to (AV_{DD} + 0.3V)
Logic Input	–0.3V to (AV_{DD} + 0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5221	TQFP-48	PFB	–40°C to +85°C	ADS5221PFB	ADS5221PFBT	Tape and Reel, 250
"	"	"	"	"	ADS5221PFBR	Tape and Reel, 2000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ELECTRICAL CHARACTERISTICS: AV_{DD} = 3.3V

T_{MIN} = –40°C, T_{MAX} = +85°C, typical values are at T_A = +25°C, sampling rate = 65MSPS, 50% clock duty cycle, AV_{DD} = 3.3V, VDRV = 2.5V, –1dBFS, internal reference voltage, and $2V_{PP}$ differential input, unless otherwise noted.

PARAMETER	CONDITIONS	ADS5221 MIN	ADS5221 TYP	ADS5221 MAX	UNITS
RESOLUTION			12 Tested		Bits
SPECIFIED TEMPERATURE RANGE	Ambient Air		–40 to +85		°C
ANALOG INPUT					
Single-Ended Input Range	$2V_{PP}$	0.5		2.5	V
Optional Single-Ended Input Range	$1V_{PP}$	1		2	V
Differential Input Range	$2V_{PP}$	1		2	V
Analog Input Bias Current			1		µA
Input Impedance	Static, No Clock		1.25 || 5		MΩ || pF
Analog Input Bandwidth	–3dBFS Input		300		MHz
CONVERSION CHARACTERISTICS					
Sample Rate		1M		65M	Samples/s
Data Latency			4.5		Clock Cycle
DYNAMIC CHARACTERISTICS					
Differential Linearity Error (largest code error)					
f = 2.4MHz			±0.3	±0.75	LSB
f = 9.7MHz			±0.5		LSB
No Missing Codes			Tested		
Integral Nonlinearity Error, f = 2.4MHz			±0.5	±1.75	LSBs
Spurious-Free Dynamic Range[1]	Referred to Full-Scale				
f = 2.4MHz			90		dBFS[2]
f = 9.7MHz	at 25°C	78	88		dBFS
f = 32.5MHz			85		dBFS
2-Tone Intermodulation Distortion[3]					
f = 9.5MHz and 10.5MHz (–7dB each tone)			92		dBFS
Signal-to-Noise Ratio (SNR)	Referred to Full-Scale				
f = 2.4MHz			70		dB
f = 9.7MHz	at 25°C	68	70		dB
f = 32.5MHz			69		dB
Signal-to-(Noise + Distortion) (SINAD)	Referred to Full-Scale				
f = 2.4MHz			70		dB
f = 9.7MHz	at 25°C	67	70		dB
f = 32.5MHz			68		dB
Effective Number of Bits[4], f = 2.4MHz			11.2		Bits
Output Noise	Input Tied to Common-Mode		0.2		LSBs rms
Aperture Delay Time			3.0		ns
Aperture Jitter			1.2		ps rms
Over-Voltage Recovery Time			1.0		Clock Cycle
Full-Scale Step Acquisition Time			5		ns

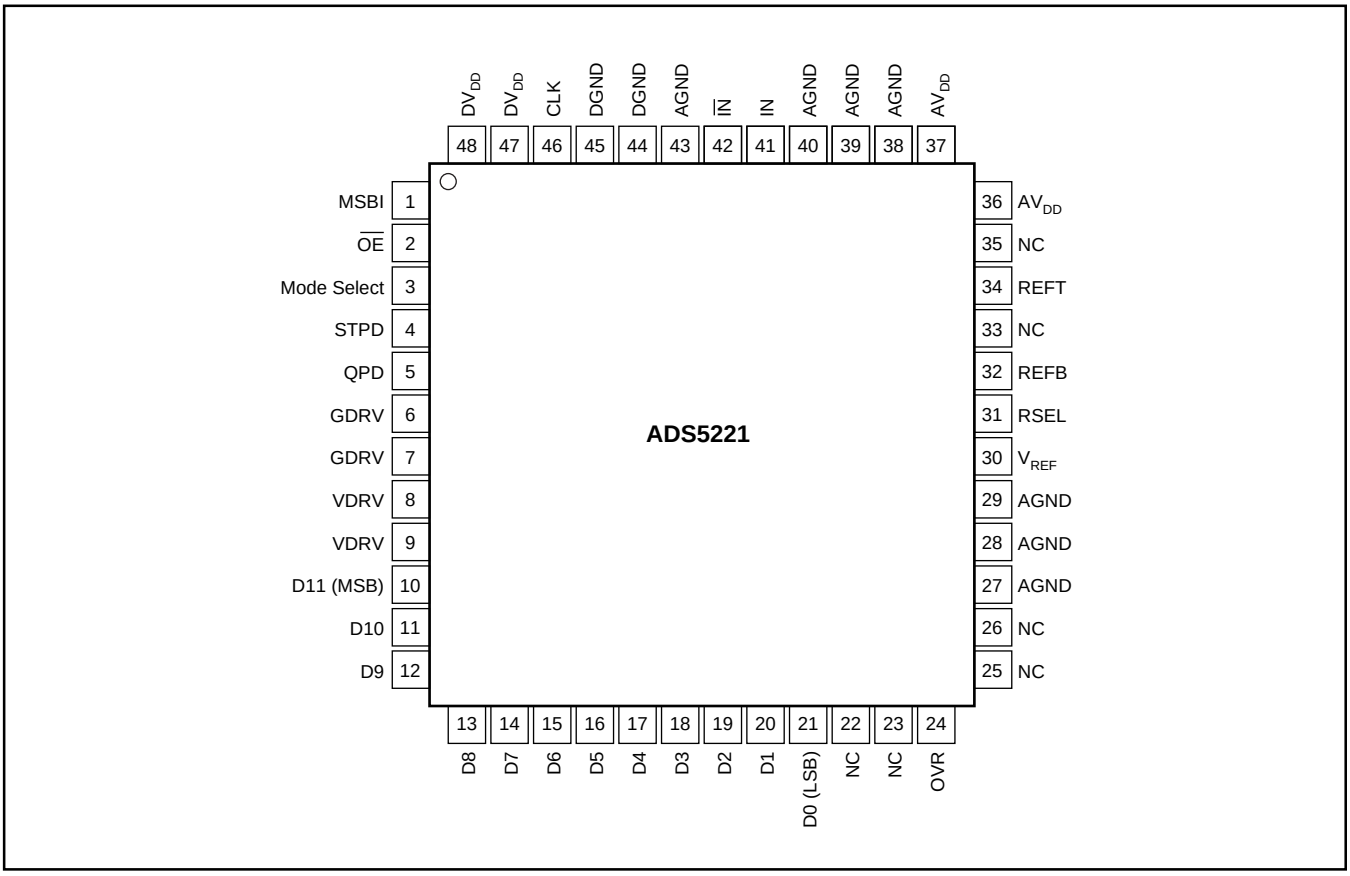
ELECTRICAL CHARACTERISTICS: AV_{DD} = 3.3V (Cont.)

T_{MIN} = –40°C, T_{MAX} = +85°C, typical values are at T_A = +25°C, sampling rate = 65MSPS, 50% clock duty cycle, AV_{DD} = 3.3V, VDRV = 2.5V, –1dBFS, internal reference voltage, and $2V_{PP}$ differential input, unless otherwise noted.

PARAMETER	CONDITIONS	ADS5221 MIN	ADS5221 TYP	ADS5221 MAX	UNITS
DIGITAL INPUTS					
Logic Family			CMOS-Compatible		
Convert Command	Start Conversion		Rising Edge of Convert Clock		
High Level Input Current[5] (V_{IN} = $3V_{DD}$)				100	µA
Low Level Input Current (V_{IN} = 0V)				10	µA
High Level Input Voltage		+1.7			V
Low Level Input Voltage				+0.7	V
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Logic Family			CMOS-Compatible		
Logic Coding			Straight Offset Binary or BTC		
Low Output Voltage (I_{OL} = 50µA to 1.5mA)	VDRV = 2.5V			+0.1	V
High Output Voltage (I_{OH} = 50µA to 0.5mA)		+2.4			V
3-State Enable Time	$\overline{OE}$ = H		20	40	ns
3-State Disable Time	$\overline{OE}$ = L		2	10	ns
Output Capacitance			5		pF
ACCURACY (Internal Reference, $2V_{PP}$, Unless Otherwise Noted)					
Zero Error (referred to midscale)	f_{IN} = 2.4MHz, at 25°C		±0.5	±1.5	%FS
Zero Error Drift (referred to midscale)			5		ppm/°C
Gain Error[6]	f_{IN} = 9.7MHz, at 25°C		±0.4		%FS
Gain Error Drift[6]			38		ppm/°C
Power-Supply Rejection of Gain	ΔAV_{DD} = ±5%		56		dB
INTERNAL VOLTAGE REFERENCE					
Output Voltage Error (1V)			±5	±35	mV
Load Regulation at 1.0mA			0.8		mV
Output Voltage Error (0.5V)			±2.5		mV
Load Regulation at 0.5mA			0.1		mV
POWER-SUPPLY REQUIREMENTS					
Supply Voltage: AV_{DD}, DV_{DD}	Operating	+3.0	+3.3	+3.6	V
Driver Supply Voltage: VDRV		+2.3	+2.5	+3.6	V
Supply Current: $+I_S$	Operating (External Reference)		86		mA
Power Dissipation: VDRV = 2.5V			285	295	mW
VDRV = 3.3V			290		mW
Standard Power-Down			15		mW
Quasi Power-Down			70		mW
Thermal Resistance, θ_{JA}					
TQFP-48			63.7		°C/W
QFN-48			26.1		°C/W

NOTES: (1) Spurious-Free Dynamic Range refers to the magnitude of the largest harmonic.
(2) dBFS means dB relative to Full-Scale.
(3) 2-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the 2-tone fundamental envelope.
(4) Effective Number of Bits (ENOB) is defined by (SINAD – 1.76)/6.02.
(5) A 50kΩ pull-down resistor is inserted internally on the $\overline{OE}$ pin.
(6) Includes internal reference.

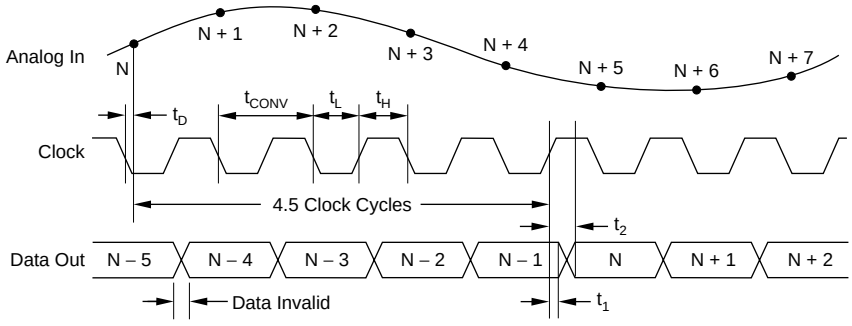
PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	I/O	NAME	DESCRIPTION	PIN	I/O	NAME	DESCRIPTION
1		MSBI	Most Significant Bit Invert (HI = Binary Two's Complement, LO = Straight Offset Binary)	25		NC	No Internal Connection
2		$\overline{OE}$	Tri-State (LO = Enabled, HI = Tri-State)	26		NC	No Internal Connection
3		Mode Select	Duty Cycle Adjust (HI = Enabled, LO = Normal Operation)	27		AGND	Analog Ground
4		STPD	Standard Power-Down (LO = Normal Operation, HI = Enabled)	28		AGND	Analog Ground
5		QPD	Quasi Power-Down (LO = Normal Operation, HI = Enabled)	29		AGND	Analog Ground
6		GDRV	Output Driver Ground	30		V_{REF}	Internal Reference Voltage (1/2V Reference)
7		GDRV	Output Driver Ground	31		RSEL	Reference Mode Select (see Table I for settings)
8		VDRV	Output Driver Supply	32		REFB	Bottom Reference Bypass
9		VDRV	Output Driver Supply	33		NC	No Internal Connection
10	O	D11 (MSB)	Data Bit 12	34		REFT	Top Reference Bypass
11	O	D10	Data Bit 11	35		NC	No Internal Connection
12	O	D9	Data Bit 10	36		AV_{DD}	Analog Supply
13	O	D8	Data Bit 9	37		AV_{DD}	Analog Supply
14	O	D7	Data Bit 8	38		AGND	Analog Ground
15	O	D6	Data Bit 7	39		AGND	Analog Ground
16	O	D5	Data Bit 6	40		AGND	Analog Ground
17	O	D4	Data Bit 5	41	I	IN	Analog Input
18	O	D3	Data Bit 4	42	I	$\overline{IN}$	Complementary Analog Input
19	O	D2	Data Bit 3	43		AGND	Analog Ground
20	O	D1	Data Bit 2	44		DGND	Digital Ground
21	O	D0 (LSB)	Data Bit 1	45		DGND	Digital Ground
22		NC	No Internal Connection	46	I	CLK	Convert Clock Input
23		NC	No Internal Connection	47	I	DV_{DD}	Digital Supply
24		OVR	Over-Range Indicator	48	I	DV_{DD}	Digital Supply

TIMING DIAGRAM



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	15.4		1000	ns
t_L	Clock Pulse LOW	6.7	7.7		ns
t_H	Clock Pulse HIGH	6.7	7.7		ns
t_D	Aperture Delay		3		ns
t_1	New Data Delay Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 5pF max			6.5	ns

TYPICAL CHARACTERISTICS: AV_{DD} = 3.3V

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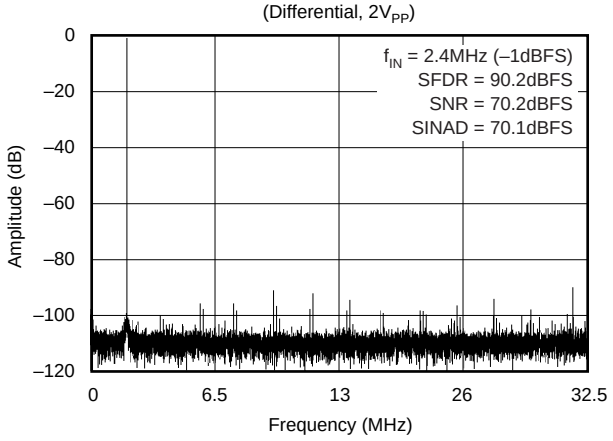
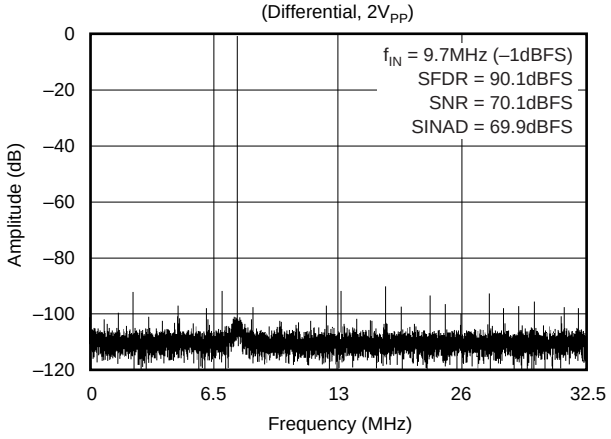
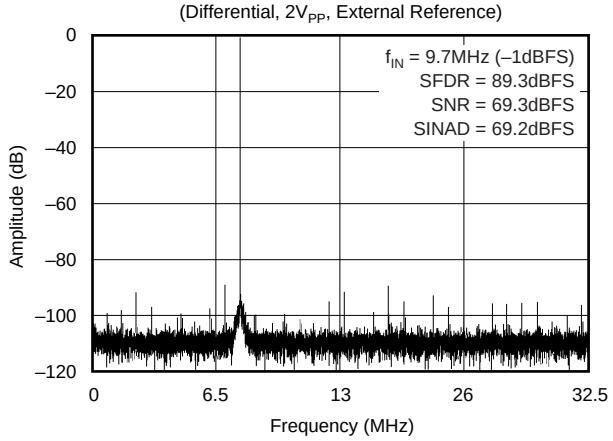
SPECTRAL PERFORMANCE
(Differential, $2V_{PP}$)



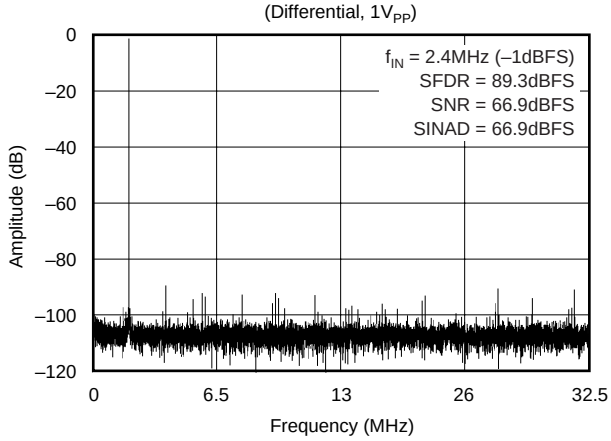
SPECTRAL PERFORMANCE
(Differential, $2V_{PP}$)



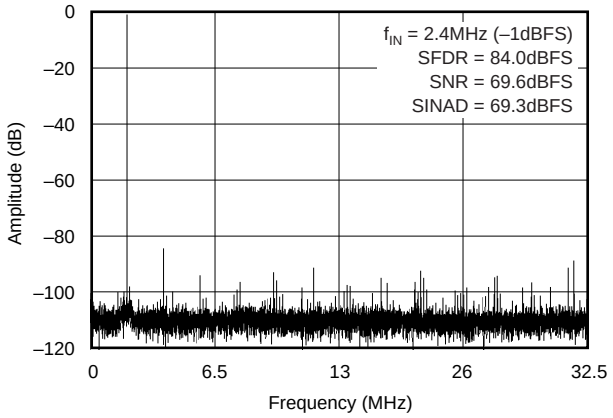
SPECTRAL PERFORMANCE
(Differential, $2V_{PP}$, External Reference)



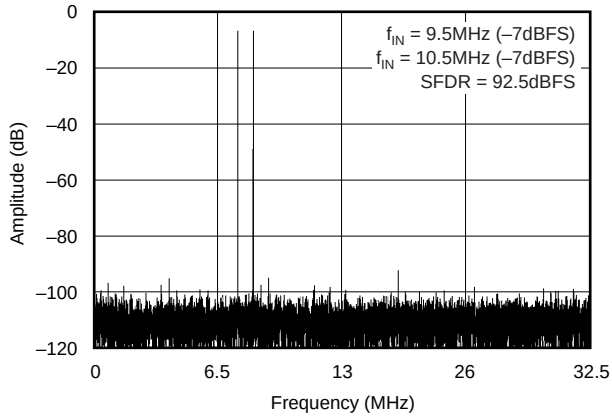
SPECTRAL PERFORMANCE
(Differential, $1V_{PP}$)



SPECTRAL PERFORMANCE
(Single-Ended, $2V_{PP}$)



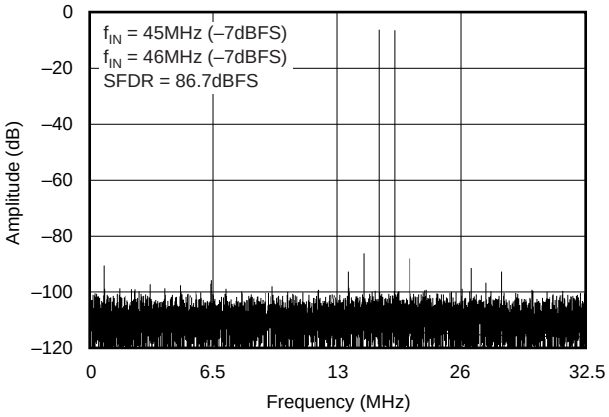
TWO TONE INTERMODULATION DISTORTION



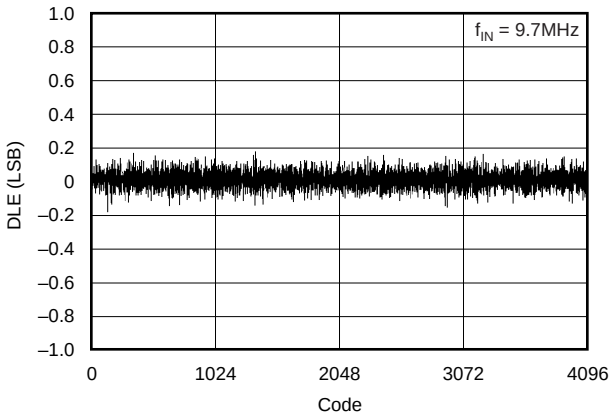
TYPICAL CHARACTERISTICS: AV_{DD} = 3.3V (Cont.)

T_{MIN} = –40°C, T_{MAX} = +85°C, typical values are at T_A = +25°C, sampling rate = 65MSPS, 50% clock duty cycle, AV_{DD} = 3.3V, VDRV = 2.5V, –1dBFS, internal reference voltage, and $2V_{PP}$ differential input, unless otherwise noted.

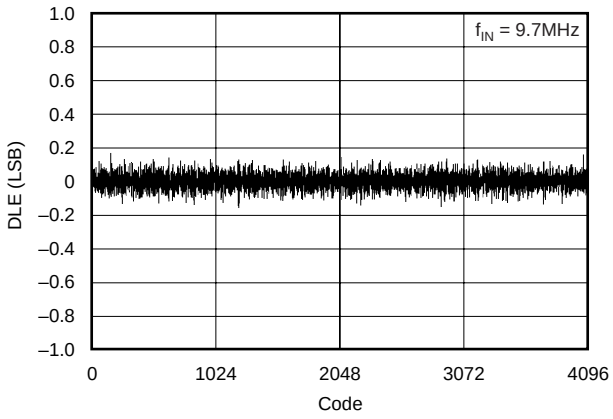
TWO-TONE INTERMODULATION DISTORTION



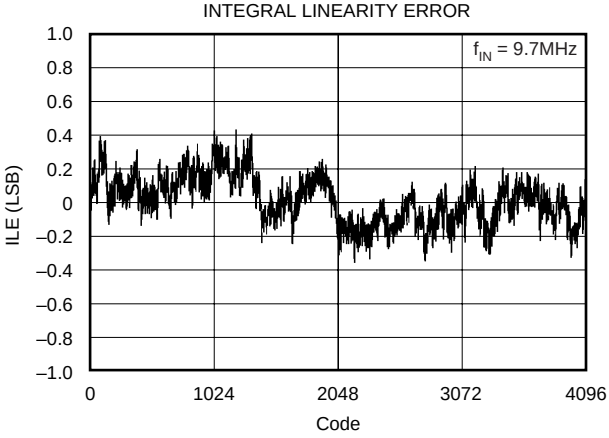
DIFFERENTIAL LINEARITY ERROR
EXTERNAL REFERENCE



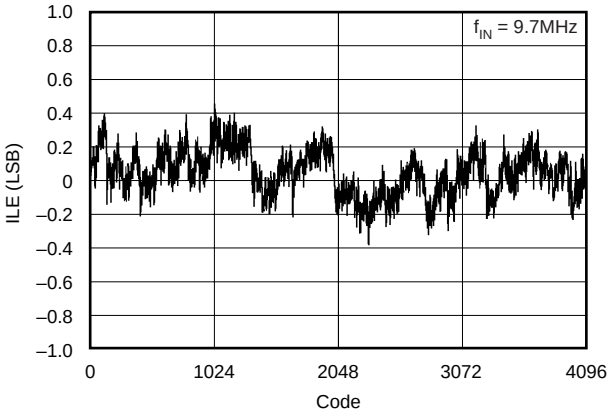
DIFFERENTIAL LINEARITY ERROR



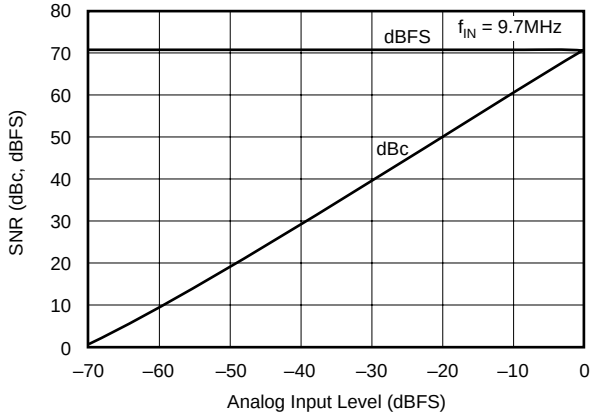
INTEGRAL LINEARITY ERROR



INTEGRAL LINEARITY ERROR
EXTERNAL REFERENCE



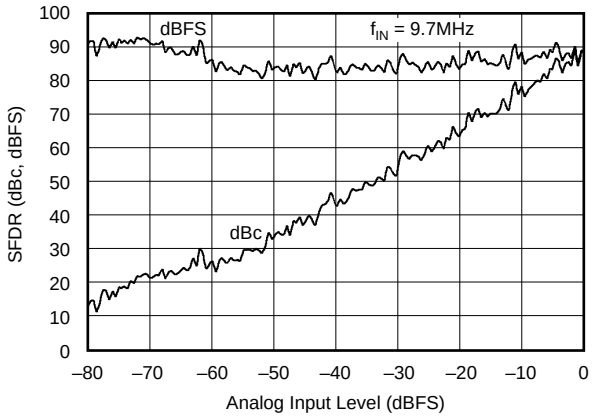
SWEPT POWER (SNR)



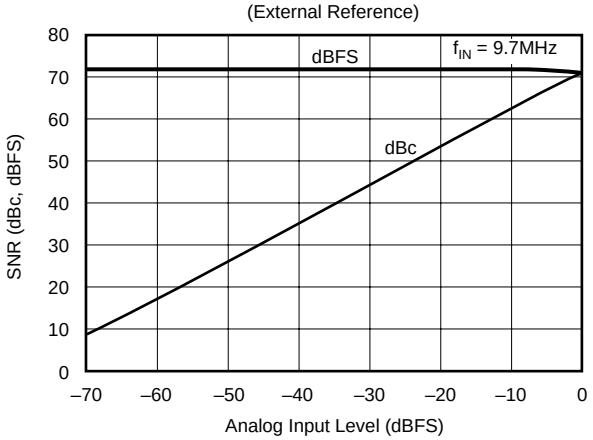
TYPICAL CHARACTERISTICS: AV_{DD} = 3.3V (Cont.)

T_{MIN} = –40°C, T_{MAX} = +85°C, typical values are at T_A = +25°C, sampling rate = 65MSPS, 50% clock duty cycle, AV_{DD} = 3.3V, VDRV = 2.5V, –1dBFS, internal reference voltage, and $2V_{PP}$ differential input, unless otherwise noted.

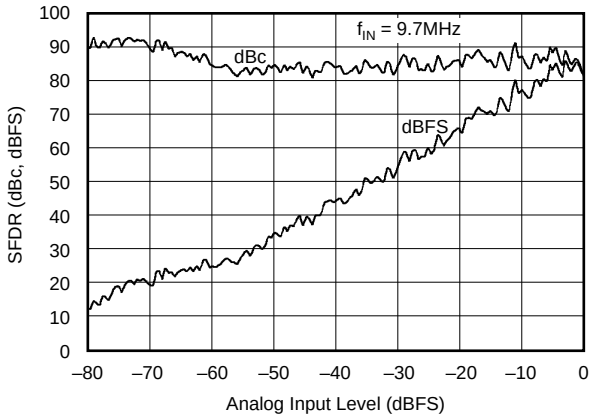
SWEPT POWER (SFDR)



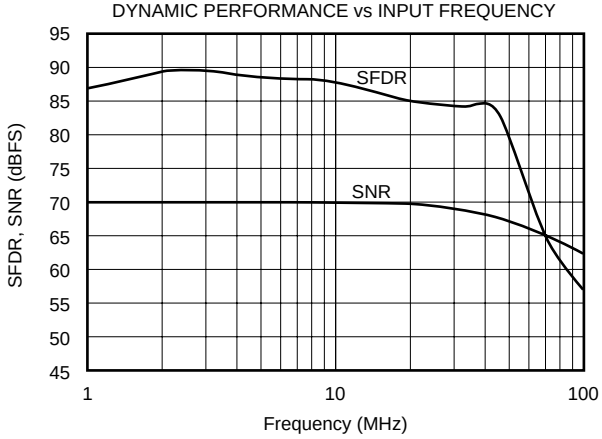
SWEPT POWER (SNR)
(External Reference)



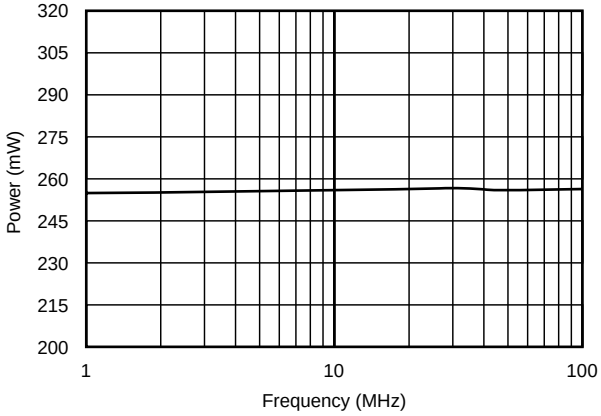
SWEPT POWER (SFDR)
(External Reference)



DYNAMIC PERFORMANCE vs INPUT FREQUENCY



POWER DISSIPATION vs INPUT FREQUENCY



APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5221 is a 12-bit, 65MSPS, CMOS ADC designed with a fully differential pipeline architecture. The pipeline consists of three sections: a 3-bit quantizer, seven stages with a 1.5-bit quantizer for each stage, and a 4-bit flash. The output of each pipeline stage is processed and formed into 12-bit data in the digital error correction logic section to ensure good differential linearity of the ADC. The converter includes a high bandwidth track-and-hold amplifier in the input stage as shown in Figure 1. It provides excellent performance for a single-ended input or differential input of IF (Intermediate Frequency) or an under-sampling signal. The falling edge of the input clock initiates the conversion process. Once the signal is captured by the input track-and-hold, the bits are sequentially encoded starting with the Most Significant Bit (MSB). This process results in a data latency of 4.5 clock cycles. The ADS5221 includes a high accuracy internal reference and also allows the use of an external reference. The input full-scale range is up to +2V and is selectable based on the reference voltage setting. For normal operation, both analog inputs (IN, $\overline{IN}$) require external common-mode voltage as signal swing center. The output data of ADS5221 are available as a 12-bit parallel word either coded in a Straight Offset Binary or Binary Two's Complement format. The ADS5221 includes an option of a duty cycle stabilizer (DCS) that allows ADS5221 to operate with a non-square wave input clock, such as from a 30% to 70% duty cycle. When the DCS is selected the ADS5221 maintains an internal clock duty cycle at 50% with ±5% tolerance. The ADS5221 has low power dissipation in normal mode and has two power down modes for energy saving. The device operates from a single +3.3V power supply and has a separate digital output driver supply pin.

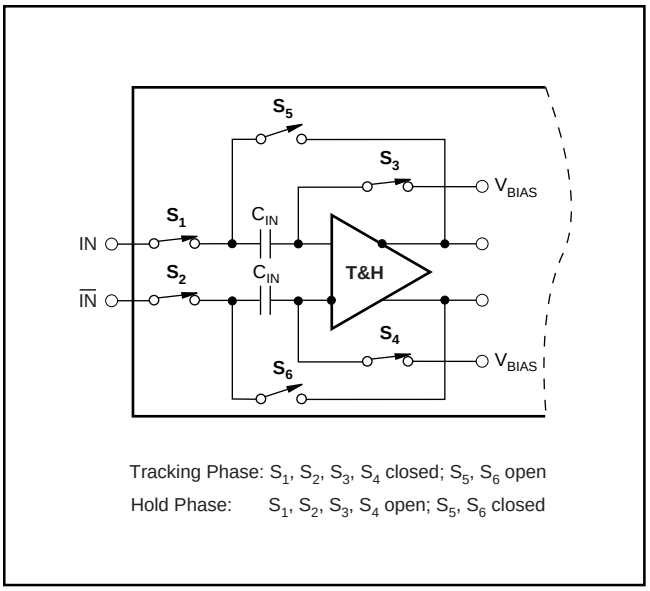


FIGURE 1. Simplified Circuit of Input Track-and-Hold Amplifier of ADS5221.

ANALOG INPUT

Depending on the application and the desired level of performance , the analog input of the ADS5221 can be configured in various ways and driven with different circuits. The ADS5221 is particularly well-suited for communication systems that digitize large scale and wideband signals. In any case, the analog interface requirements should be carefully examined before selecting the appropriate circuit configuration. The circuit definition should include considerations on the input frequency band and amplitude, as well as the available power supplies.

INPUT IMPEDANCE

The input impedance of the ADS5221 is capacitive due to the input stray and sampling capacitors. These capacitors effectively result in a dynamic input impedance that is a function of the sampling and input frequency. Figure 2 depicts the differential input impedance of the ADS5221 as a function of the signal input frequency. At certain sampling rates, increasing the signal frequency will decrease the input impedance. This factor needs to be considered when the signal source is designed. For applications that use op amps to drive the ADC, it is recommended that a series resistor be added between the amplifier output and the converter inputs. This will isolate the capacitive input of the converter from the driving source and avoid gain peaking, or instability; furthermore, it will create a 1st-order, low-pass filter (LPF) in conjunction with the specified input capacitance of the ADS5221. The cutoff frequency of this LPF can be further adjusted by adding an external shunt capacitor from each signal input to ground. In any case, the use of the RC network is optional, but optimizing the values to adapt to the specific application is encouraged.

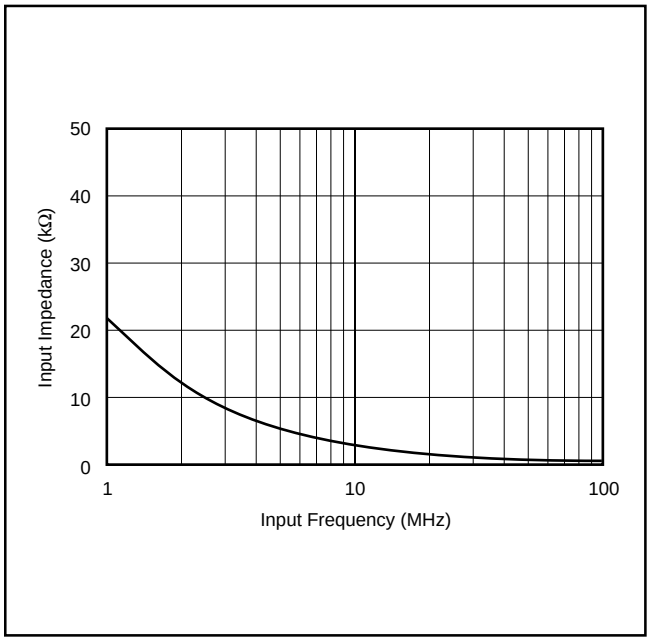


FIGURE 2. Differential Input Impedance vs Input Frequency.

INPUT COMMON-MODE VOLTAGE

The ADS5221 operates from a single +3.3V supply, and requires a external common-mode voltage. This allows a symmetrical signal swing while maintaining sufficient headroom to the supply rail. The common-mode voltage can be from an external DC voltage source, for example, an analog +3.3V supply with a simple resister divider, or from the input signal source with DC-coupling. When it is a single-ended input configuration, the common-mode voltage is typically +1.25V. When the input configuration is differential, the common-mode voltage is +1.5V.

INPUT FULL-SCALE RANGE

The input full-scale range (FSR) of the ADS5221 is selectable from +1V to +2V and any value within this range, by setting the reference select pin RSEL and reference voltage pin V_{REF} (see Table I). The input FSR (differential) is always twice V_{REF} (the voltage at the V_{REF} pin) for all reference modes.

By choosing different signal input ranges, trade-offs can be made between noise and distortion performance. For maximizing SNR, the maximum signal input $2V_{PP}$ range may be selected. This range may also be selected for low-level (–6dBFS to –40dBFS) but high-frequency multi-tone input. The signal distortion at the output of the device could be sensitive to the input signal with large full-scale. Reducing signal amplitude will improve the distortion performance. The large input signal amplitude of the converter will impose additional design constraints to the op amp due to its headroom requirements when the op amp is from single-supply and DC-coupling.

DIFFERENTIAL INPUTS

The ADS5221 input structure is designed to accept both a single-end or differential analog signal. Distortion performance, however, can be improved by utilizing the differential input configuration. Differential operation of the ADS5221 requires that an input signal at the inputs (IN, $\overline{IN}$) has the same amplitude and is 180 degrees out-of-phase. Differential signals offer a number of advantages:

- The signal amplitude is half that required for the single-ended operation, and is therefore less demanding to achieve, while maintaining good linearity performance from the signal source.
- The reduced signal swing allows for more headroom of the interface circuitry, and therefore also allows a wider selection of the best suitable driver amplifier.
- Minimization of even-order harmonics.
- Improved noise immunity based on the common-mode input rejection of the converter.

ANALOG INPUT DRIVEN BY TRANSFORMER

The ADS5221 can be driven by a transformer, which provides signal AC-coupling and allows a signal conversion from single-ended input to differential output, or from single-ended input to single-ended output. Using a transformer offers a number of advantages. As a passive component, it does not add to the total noise and has better harmonics in wide frequency bands, compared to an op amp driver. By using a step-up transformer, further signal amplification can be realized; as a result, the signal swing from the source can be reduced. For transformer selection, it is important to carefully examine the application requirements and determine the correct model, the desired impedance ratio, and frequency characteristics. Furthermore, the appropriate model must support the targeted distortion level and should not exhibit any core saturation at full-scale voltage levels. A variety of miniature RF transformers from different manufacturers (such as Mini-Circuits, Coilcraft, or Trak) can be selected.

Figure 3 shows a transformer-coupled input configuration of the ADS5221. The ADS5221 receives a differential AC signal from the output of the transformer and common-mode voltage of +1.5V from the center tap. A source termination resistor, R_T, is required, which can be placed at the input or output of the transformer to satisfy the termination requirements of the source impedance, R_S. The circuit also shows the use of an additional RC low-pass filter placed in series with each converter input to attenuate some of the wideband noise. The resistor values are typically in the range of 10Ω to 50Ω, and capacitors are in the range of 10pF to 100pF for individual application requirements.

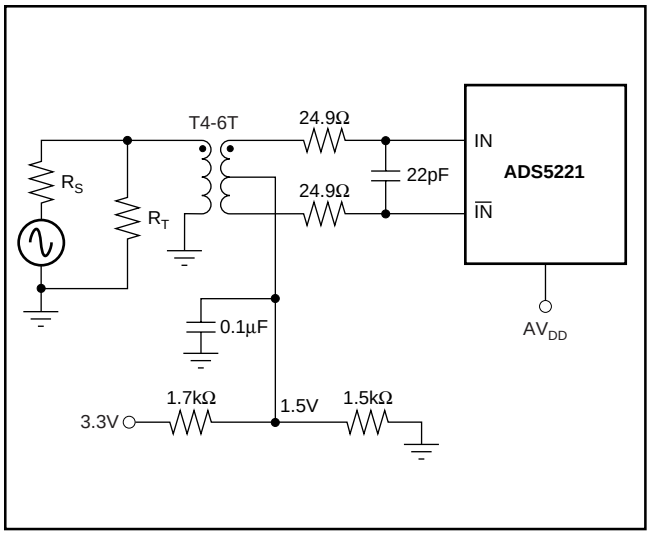


FIGURE 3. Transformer-Coupled Differential Input Configuration of ADS5221.

ANALOG INPUT DRIVEN BY OP AMPLIFIER

The ADS5221 can be driven by an operational amplifier with DC or AC signal coupling, as shown in Figure 4 and Figure 5. In Figure 4, the THS4503, a differential amplifier, is used to convert a single-ended input to differential output with a gain of 2. The THS4503 provides an output common-mode voltage set by the V_{OCM} pin, and is DC-coupled to the input of ADS5221. A low-pass filter can be created by adding small capacitors (for example, 10pF) in parallel with the feedback resistors of the THS4503 as needed for some applications. Due to the THS4503 driving a capacitive load, small series resistors in the output ensure stable operation. Further details of this and other functions of the THS4503 may be found in its product datasheet, located on the Texas Instruments web site (www.ti.com). In general, differential amplifiers provide a higher performance driver solution as compared to a single-ended amplifier.

As shown in Figure 5, an AC-coupled, single-ended input configuration is realized with TI's OPA695 for wideband applications. For narrowband applications, the OPA2822 can be used. In Figure 5, the OPA695 is configured at single supply +5V and noninverting operation. The AC gain of the amplifier is 2 and the DC offset of the amplifier is +2.5V, set by the voltage divider from the op amp power supply. The output of the amplifier can provide maximum full-scale voltage range for the ADS5221. The OPA695 is a very high bandwidth, current-feedback op amp that combines 4200V/µs slew rate and low input voltage noise. It is optimized for high gain operation. Further details of the OPA695 can be found in the OPA695 data sheet. The common-mode voltage at the ADS5221 input is +1.25V, set by a voltage divider from +3.3V power supply. The +3.3V power supply must be decoupled, as shown in Figure 11.

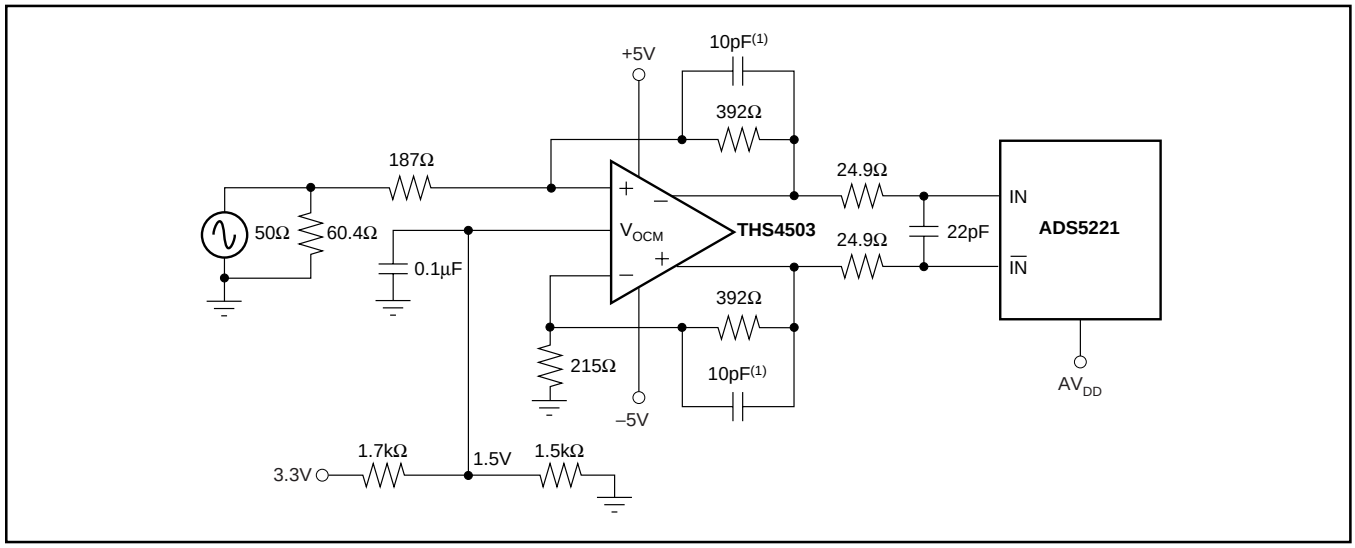


FIGURE 4. Using the THS4503 Differential Amplifier (Gain = 2) to Drive the ADS5221 in a DC-Coupled Configuration.

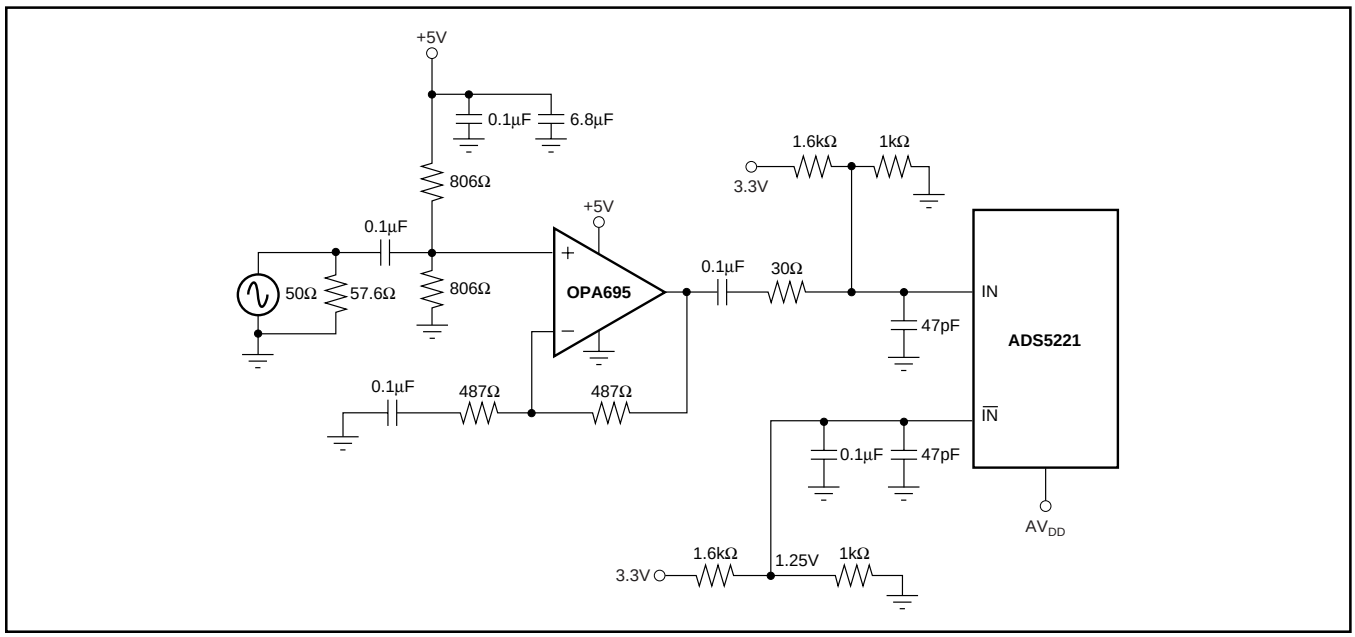


FIGURE 5. Single-Ended Input of ADS5221 Driven by OPA695 with Gain = 2.

CLOCK INPUT

The clock input of the ADS5221 is designed to receive a single-ended pulse clock with CMOS/TTL level and DC-coupling. There is no external common-mode voltage requirement at the clock input pin (see Figure 6). The typical tolerance of the internal clock duty cycle is ±5% at its nominal value of 50% in order to maintain the high performance of the device.

The ADS5221 contains an optional clock duty cycle adjust (DCA). When the DCA is enabled (Mode Select = high), a wide range of input clock duty cycle can be adjusted internally to 50% (±5% tolerance) by correcting the non-sampling edge of the clock. In this case, the noise and distortion performance will not be affected by the input clock duty cycle within this range. When the DCA is disabled (Mode Select = low), a clock duty cycle variation greater than ±5% will degrade the dynamic performance of the device. In this case, an input clock duty cycle less than 45% will automatically request a reduction in the sampling rate in order to maintain the track/hold period within the specified values for stable performance. The DCA disabled mode is suitable for non-uniform sampling ADC applications.

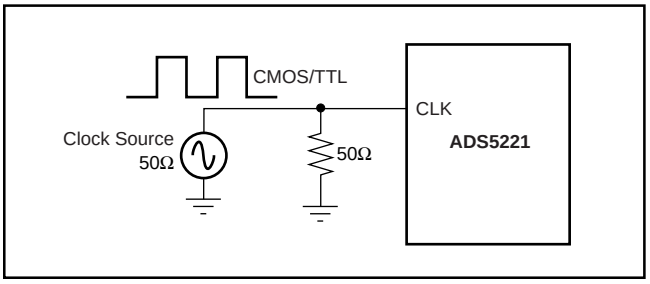


FIGURE 6. General Input Clock Interface of ADS5221.

In any case, a very low jitter clock is fundamental to preserving the excellent AC performance of the ADS5221. The device itself is specified for a low jitter, characterizing the outstanding capability of the internal clock and track-and-hold circuitry. Generally, as input frequency increases, clock jitter becomes more critical to maintain a good signal-to-noise ratio. The following equation can be used to calculate the achievable SNR for a given input frequency and clock jitter (t_{JA} in ps rms):

$$SNR = 20 \log [1/(2 \bullet \pi \bullet f_{IN} \bullet t_{JA})]$$

Here, the t_{JA} is the rms aperture jitter from all jitter sources, such as clock edge, input signal and the device. The f_{IN} is input frequency. The crystal oscillator has very low jitter, but if using a clock conditioning circuit (gate, divider, logic lever converter, and so forth), an extra jitter and timing variation must be limited. In addition, the input clock is treated as an analog signal and its power supply should be separated from the power supply of the digital output driver to limit the digital noise.

MINIMUM SAMPLING RATE

The pipeline architecture of the ADS5221 uses a switched-capacitor technique in its internal track-and-hold stages. The high sampling speed necessitates the use of very small capacitor values. In order to hold the droop errors low, the capacitors require a minimum refresh rate. To maintain accuracy of the acquired sample charge, the sampling clock on the ADS5221 must not drop below the specified minimum of 1MHz.

REFERENCE

ADS5221 provides both internal reference and external reference modes by setting pins RSEL and V_{REF} (see Table 1). The input full-scale range (FSR) of ADS5221 is always twice the voltage V_{REF} at the V_{REF} pin. The REFT and REFB are internally buffered, and drive the ADC core for both the external reference and internal reference modes. The REFT and REFB are designed for external bypass only. The output resistance between the REFT and REFB pins is approximately 1Ω. When the internal reference mode is selected the voltage at V_{REF} is generated by an internal 0.5V bandgap voltage through a V_{REF} amplifier, and the V_{REF} output can supply 2.5mA source current. When the external reference is selected, the internal V_{REF} amplifier is powered down, the external reference voltage is added at the V_{REF} pin, and the voltage is input to the internal REFT/REFB amplifier. The voltage at pins REFT, REFB and V_{REF}, the full scale range (FSR) voltage at analog input for both external and internal reference modes, and the differential/single-ended input configurations are as follows:

$$V_{REFT} = V_{REF}/2 + 1.5V$$
$$V_{REFB} = 1.5V - V_{REF}/2$$
$$V_{REF} = V_{REFT} - V_{REFB}$$
$$FSR\ (Differential) = 2 \bullet V_{REF}$$

SELECTED MODE	RSEL PIN CONNECT TO	V_{REF} PIN (V)	INPUT FSR (V) (Differential)	REFT (V)	REFB (V)
Internal Fixed	GND to 0.2V	1.0	2	2	1
Internal Fixed	V_{REF} Pin	0.5	1	1.75	1.25
Internal Program	0.2V to V_{REF}	0.5 • (1+R_2/R_1)	2 • V_{REF}	V_{REF}/2 + 1.5	1.5 – V_{REF}/2
External	AV_{DD} (3.3V)	Ext. 0.5V to 1V	2 • V_{REF}	V_{REF}/2 + 1.5	1.5 – V_{REF}/2

TABLE I. Reference Configuration.

The ADS5221 requires solid bypassing for all reference pins to keep the effects of clock feedthrough to a minimum and to achieve the specified levels of performance. Figure 7 to Figure 10 show the recommended decoupling scheme. All 0.1µF capacitors must be located as close to the pins as possible. In addition, pins REFT, V_{REF}, and REFB must be decoupled with tantalum surface-mount capacitors (2.2µF, 4.7µF, 10µF or higher).

INTERNAL REFERENCE

There are two internal fixed reference modes and one internal programmable reference mode as shown in Table I and Figure 7 through Figure 9. Setting RSEL to ground (or < 0.2V) provides an internal reference voltage of +1.0V at V_{REF} pin, +2V at REFT, and +1V at REFB pin. In this case, the input FSR is +2V peak-to-peak. Connecting RSEL to the V_{REF} pin provides an internal reference voltage of +0.5V at V_{REF}, +1.75V at REFT, and +1.25V at REFB. In this case, the input FSR is +1V peak-to-peak. Setting the resister divider as in Figure 9 provides an internal voltage between +0.5V and +1V at V_{REF}, which is as follows:

$$V_{REF} = 0.5 \bullet (1+R_2/R_1)$$

In this case, the voltage at REFT and REFB and input FSR is calculated based on Table I.

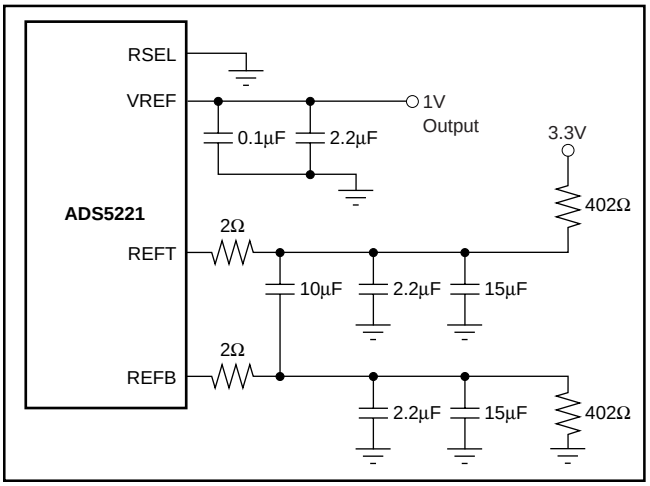


FIGURE 7. Internal Reference Mode for V_{REF} = 1V.

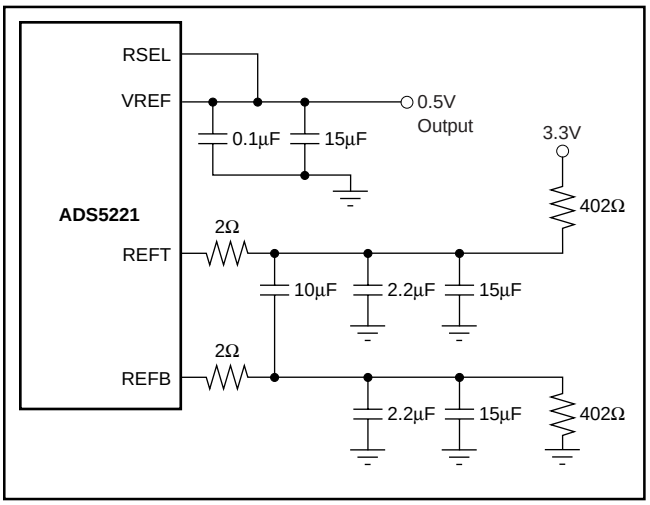


FIGURE 8. Internal Reference Mode for V_{REF} = 0.5V.

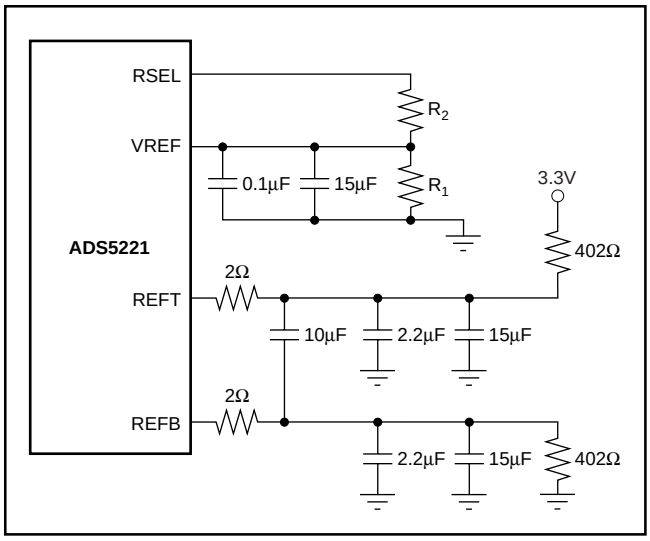


FIGURE 9. Internal Reference Mode for $V_{REF} = 0.5 \bullet (1 + R_2/R_1)$.

EXTERNAL REFERENCE

For even more design flexibility, the ADS5221 can be operated with external references. Utilization of an external reference voltage may be considered for applications requiring higher accuracy, improved temperature stability, or flexible full-scale range. Particularly in multi-channel applications, the use of a common external reference offers the benefit of improving gain matching between converters. Setting RSEL to AV_{DD} (+3.3V) provides an external reference mode for the ADS5221. In this case, the internal V_{REF} amplifier is powered down, and the V_{REF} pin requires an external reference voltage between +0.5V to +1V to provide an input FSR voltage of +1V to +2V. The REFT and REFB will appear with the voltage as shown in Table I and input FSR is always twice the voltage at the V_{REF} pin. A voltage reference (REF1004 or TPS79225) and a single-supply amplifier (OPA2234 or OPA4227) can be used to generate a precision external reference.

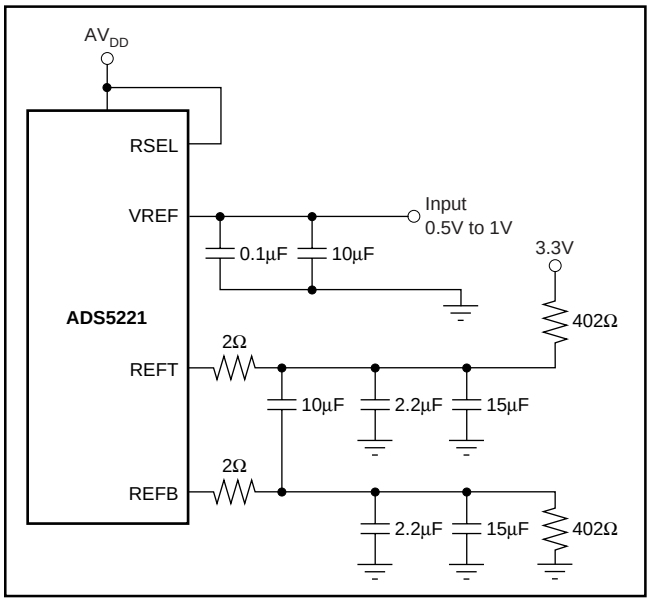


FIGURE 10. External Reference Configuration.

DIGITAL OUTPUTS

DATA OUTPUT FORMAT

The ADS5221 makes two data output formats available, either the Straight Offset Binary (SOB) code or the Binary Two's Complement (BTC) code. The selection of the output coding is controlled through the MSBI pin. Applying a logic high will enable the BTC coding, whereas a logic low will enable the SOB code. The two code structures are identical with one exception: the MSB is inverted for the BTC format, as shown in Table II. If the input signal exceeds the FSR, the output code will remain at all 1s or all 0s.

DIFFERENTIAL INPUT	STRAIGHT OFFSET BINARY (SOB)	BINARY TWO'S COMPLEMENT (BTC)
+FS – 1LSB (+FS: VIP = 2V, VIN = 1V)	1111 1111 1111	0111 1111 1111
+1/2 FS (VIP = 1.75V, VIN = 1.25V)	1100 0000 0000	0100 0000 0000
Bipolar Zero (VIP = VIN = 1.5V)	1000 0000 0000	0000 0000 0000
–1/2 FS (VIN = 1.75V, VIP = 1.25V)	0100 0000 0000	1100 0000 0000
–FS (VIN = 2V, VIP = 1V)	0000 0000 0000	1000 0000 0000

TABLE II. Coding Table for Differential Input Configuration with FSR of 2V.

OUTPUT ENABLE ($\overline{OE}$)

The digital outputs of the ADS5221 can be set to output enable or output high impedance (tri-state) by the $\overline{OE}$ pin. For normal operation, this pin must be at a logic low, whereas a logic high disables the outputs or sets the output tri-state.

OUTPUT LOADING

It is recommended to keep the capacitive loading on the data output lines as low as possible, preferably below 5pF. Higher capacitive loading will cause larger dynamic currents as the digital outputs are changing. These high current surges can feed back to the analog portion of the ADC and adversely affect device performance. If necessary, external buffers or latches (for example, the SN74LVTH16374) close to the converter output pins can be used to minimize capacitive loading. Buffers or latches also provide the added benefit of isolating the ADS5221 from any digital activities on the bus to limit the high-frequency noise.

OVER-RANGE INDICATOR

The ADS5221 has control functions for the input voltage over full-scale that includes output data code control and over-range indication. The output data code control of over full-scale is shown in Table II. In SOB format, for example, when the input voltage is (+FS – 1 LSB) or above this value, the ADS5221 outputs all 1s at 12 data bits; when the input voltage is –FS or below this value, the ADS5221 outputs all 0s at 12 data bits. When the input voltage is 0 (middle scale) or only the common-mode voltage at the input, the ADS5221 outputs 1 at MSB and 0s at the remaining 11 data bits. Another over-range control function of the ADS5221 is over-range indication, which is output by the OVR pin. The OVR pin is the function of the reference voltage and the output data bits, and has the same pipeline delay as the output data bits. OVR is at logic low if the input voltage is within the FSR, and is at logic high if the input voltage is over full-scale or under full-scale. OVR changes from logic low to high or logic high to low immediately following the change of the output data, when the input voltage changes from normal value to over FS or from over FS to normal value. When the input signal continues under full-scale or over full-scale, OVR stays high.

TIMING

The ADS5221 samples the analog signal at the rising edge of its input clock, and outputs the digital data at the falling edge of the input clock after a pipeline delay of 4.5 clocks. There is an aperture delay (typically 3ns) between the sampling edge and the actual sampling time. There is also a propagation delay between the rising edge of the clock and the time that data is valid on the data bus (see the timing diagram on page 5). The output data of the ADS5221 are latched data.

POWER SUPPLIES AND POWER DISSIPATION

ANALOG AND DIGITAL POWER SUPPLY

The ADS5221 includes power-supply pins of AV_{DD}, DV_{DD} and VDRV. The analog supply AV_{DD} is +3.3V and digital supply DV_{DD} is +3.3V. A digital output driver supply, VDRV, can be +2.5V up to +3.3V. AV_{DD}, DV_{DD} and VDRV are not tied together internally. Each of these supply pins must be bypassed separately with at least one 0.1µF ceramic chip capacitor. The analog supply (AV_{DD}) and the digital supply (DV_{DD} or VDRV) may be tied together externally with a ferrite bead or inductor between the supply pins. The digital output driver supply, VDRV, of +2.5V is used commonly. It is highly recommended to consider linear supplies instead of switching types. Even with good filtering, switching supplies can radiate noise that could interfere with any high-frequency input signal and cause unwanted modulation products. The supply voltage should stay within the tolerance given in the specification table. A basic application configuration with the power supply decoupling is shown in Figure 11.

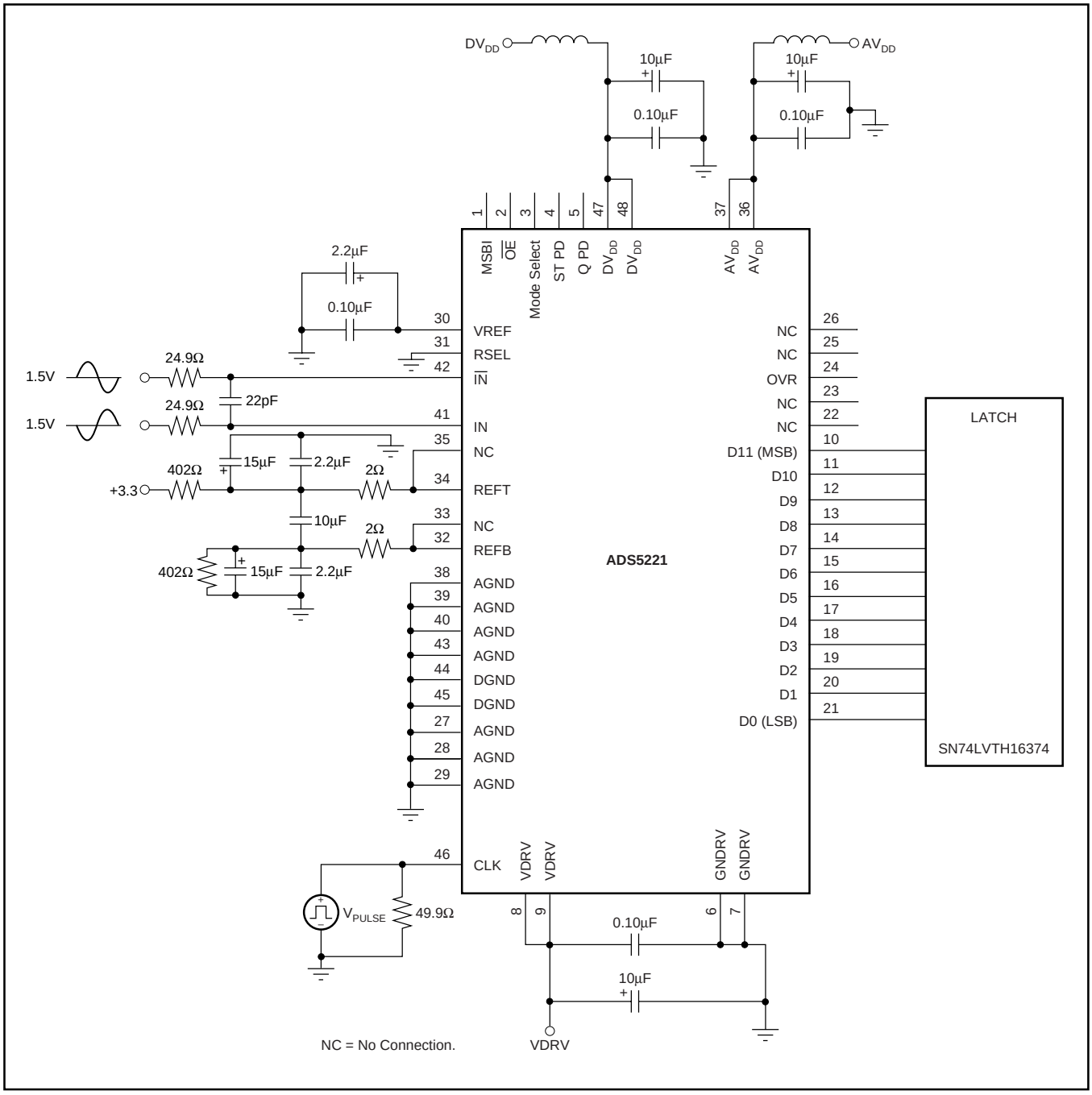


FIGURE 11. General Layout for the ADS5221.

POWER DISSIPATION

In normal operating mode (STPD = low and QPD = low), the typical total power dissipation of the ADS5221 is 285mW. The majority of the power consumption is due to biasing; therefore, this part of the total power dissipation is independent of the applied clock frequency. The digital power dissipation from the output driver is less than 10% of the total power dissipation. This portion of the power consumption is proportional to the sampling rate, digital output load and number of the bits. The current on the VDRV supply is directly related to the capacitive loading of the data output pins; care must be taken to minimize such loading.

POWER DOWN (PD)

The ADS5221 provides two power-down modes for different application requirements. One is standard power down (STPD); the second is quasi power down (QPD). Setting STPD to logic high (and QPD to logic low or high) will shut down the internal ADC core and power down the reference circuit. In this case the power dissipation is typically 15mW. With 10µF external decoupling capacitor at REFT and REFB, it takes about 800µs to fully restore normal operation after the normal mode is enabled. Setting QPD to logic high (and STPD to logic low) will shut down the internal ADC core and while the internal reference circuit power remains on. In this

case, power dissipation is typically 70mW. It takes about 2µs to fully restore normal operation after the normal mode is enabled. During power-down, data in the converter pipeline will be lost and new valid data will be subject to the specified pipeline delay.

LAYOUT AND DECOUPLING

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high-frequency designs. Achieving optimum performance with a fast sampling converter like the ADS5221 requires careful attention to the printed circuit board (PCB) layout in order to minimize the effect of board parasitics and optimize component placement. A multi-layer board usually ensures best results and allows convenient component placement. The ADS5221 must be treated as an analog component, and the AV_{DD} pins connected to a clean analog supply. This ensures the most consistent results, because digital supplies often carry a high level of switching noise that could couple into the converter and degrade the performance. The driver supply pins (VDRV) must also be connected to a low-noise supply. Supplies of adjacent digital circuits can carry substantial current transients. The supply voltage must be thoroughly filtered before connecting to the VDRV supply of the converter. All ground connections on the ADS5221 are internally bonded to the metal flag (bottom of package) that forms a large ground plane. All ground pins must directly connect to an analog ground plane that covers the PCB area under the converter. Due to its high sampling frequency, the ADS5221 generates high frequency current transients and noise (clock feedthrough) that are fed back into the supply and reference lines. If not sufficiently bypassed, this adds noise to the conversion process. See Figure 11 for the recommended supply decoupling scheme for the ADS5221. All AV_{DD} pins should be bypassed with a combination of 0.1µF ceramic chip capacitors (0805, low ESR) and a 10µF tantalum tank capacitor. A similar approach may be used on the digital supply pins DV_{DD} and driver supply pins, VDRV. In order to minimize the lead and trace inductance, the capacitors must be located as close to the supply pins as possible. They are best placed directly under the package where double-sided component mounting is allowed. In addition, larger bipolar decoupling capacitors (2.2µF to 10µF), effective at lower frequencies, must also be used on the main supply pins. They can be placed on the PCB in close proximity (< 0.5 inches) to the ADC. If the analog inputs to the ADS5221 are driven differentially, it is especially important to optimize towards a highly symmetrical layout. Small trace length differences can create phase shifts compromising a good distortion performance. For this reason, the use of two single op amps rather than one dual amplifier enables a more symmetrical layout and a better match of parasitic capacitances. The pin orientation of the ADS5221 package follows a flow-through design with the analog inputs located on one side of the package, whereas the digital outputs are located on the opposite side of the quad-flat package. This provides a good physical isolation between the analog and digital connections. While designing the layout, it is important to keep the analog signal traces separated from any digital lines to prevent noise coupling onto the analog portion. Try to match trace length for the differential clock signal (if used) to avoid mismatches in propagation delays. Single-ended clock lines must be short and should not cross any other signal traces. Short circuit traces on the digital outputs will minimize capacitive loading. Trace length must be kept short to the receiving gate (< 2 inches) with only one CMOS gate connected to one digital output. If possible, the digital data outputs must be buffered (with the TI SN74LTH16374, for example). Dynamic performance can also be improved with the insertion of series resistors at each data output line. This sets a defined time constant and reduces the slew rate that would otherwise flow as the fast edge rate. The resistor value may be chosen to give a time constant of 15% to 25% of the used data.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
5/07	C	2	Electrical Characteristics	Changed *Data Latency* from 5 to 4.5
		5	Timing Diagram	Changed Clock from 5 to 4.5 clock cycles, and adjusted related symbols.
				Changed timing table.
		9	Theory of Operation	Changed "eight middle stages" to "seven stages."
				Changed "rising edge" to "falling edge."
				Changed "5 clock cycles" to "4.5 clock cycles."
		14	Timing	Changed Figure 2. Corrected grid lines and X,Y axes.
				Changed "rising edge" to "falling edge."
				Changed "5 clocks" to "4.5 clocks."

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADS5221PFBT	NRND	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS5221PFBTG4	NRND	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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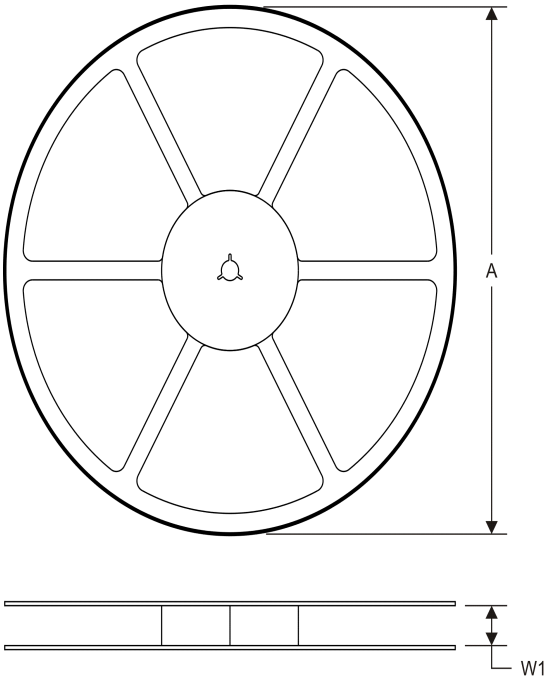
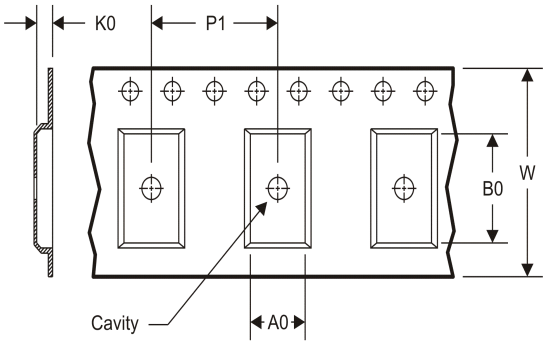
REEL DIMENSIONS



TAPE DIMENSIONS



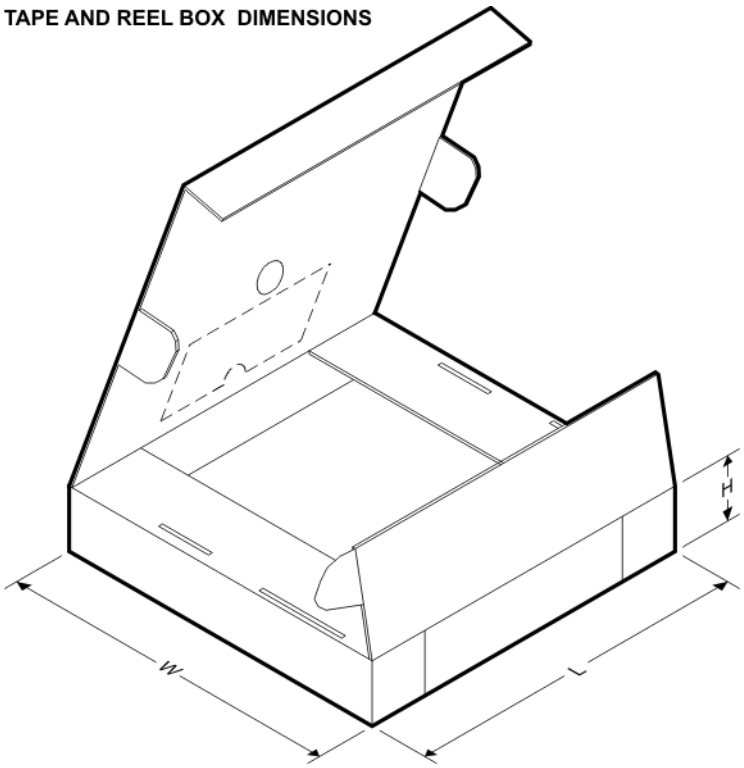
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5221PFBT	TQFP	PFB	48	250	177.8	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

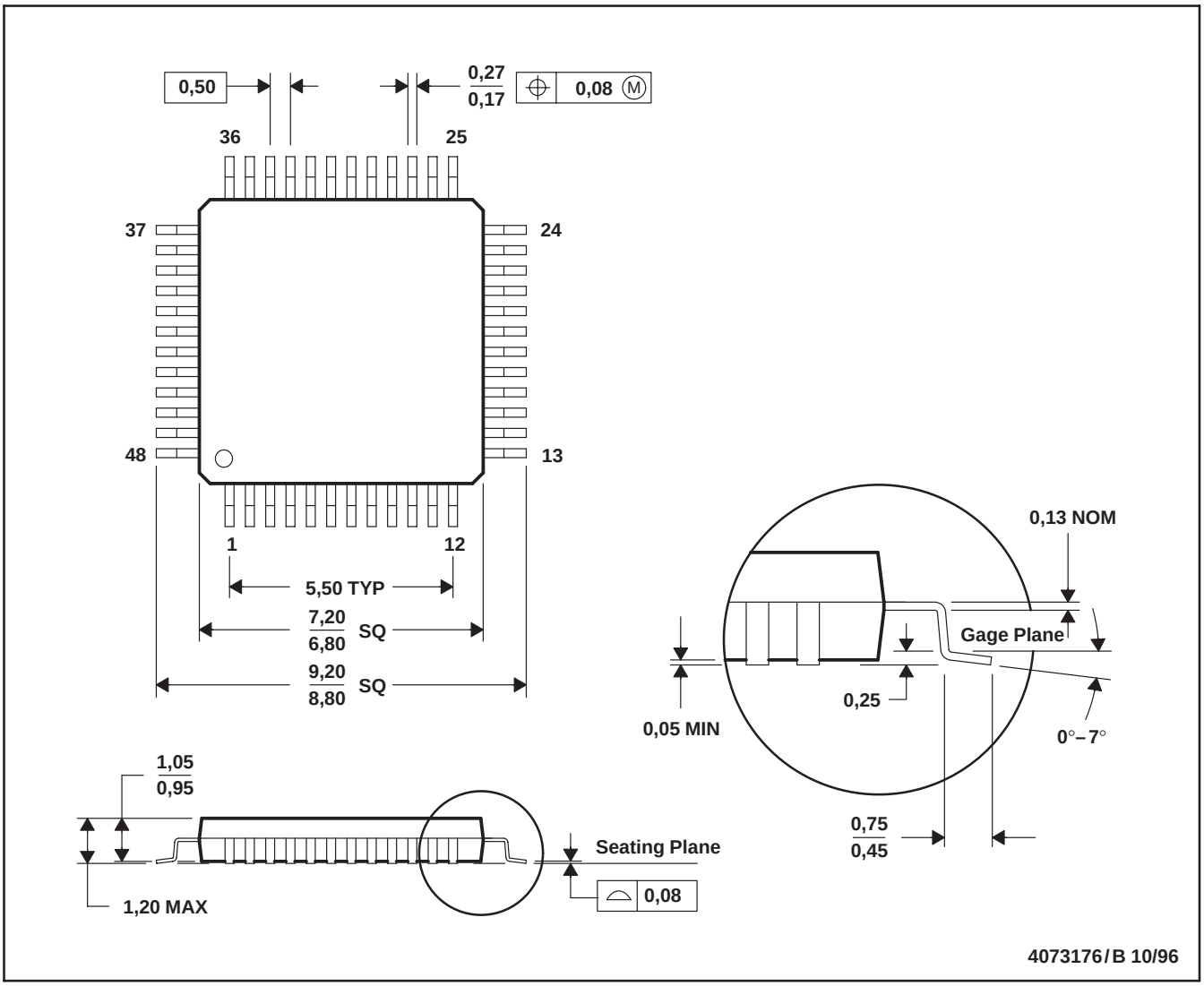


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5221PFBT	TQFP	PFB	48	250	210.0	185.0	35.0

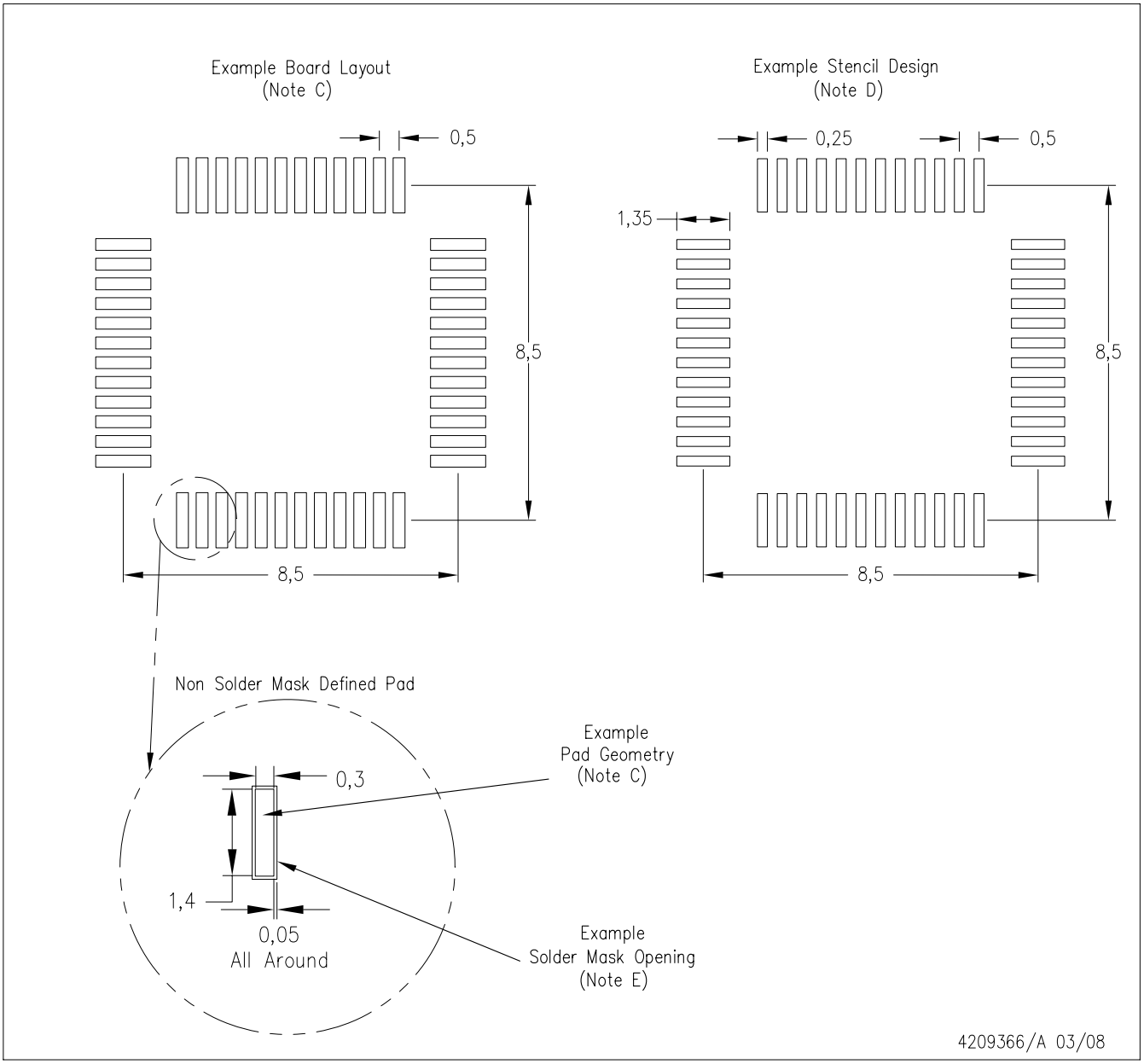
MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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