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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Customer Notification

μPD78F9222 Subseries™

8-Bit Single-Chip Microcontrollers

Operating Precautions

μPD78F9221

μPD78F9222

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μPD78F9222 Subseries

Global Document No. U18105EE3V0IF00 (3rd edition)

(A) Table of Operating Precautions

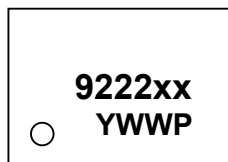
No.	Outline	μPD78F9222							
		Rev. <small>Note</small>	1.0	1.1	1.2	2.1	2.2	2.3	
		Rank <small>Note</small>					K	E	P
1	Restriction for Flash Memory self-programming (Technical Limitation)		X	X	✓	✓	✓	✓	✓
2	Restriction for WDT reset (Technical Limitation)		X	X	✓	✓	✓	✓	✓
3	Restriction for WDT count (Technical Limitation)		X	X	✓	✓	✓	✓	✓
4	Restriction for Clock Generator (Technical Limitation)		X	X	✓	✓	✓	✓	✓
5	Restriction for LVI (Technical Limitation)		X	X	X	✓	✓	✓	✓
6	Restriction for INTP0 when LIN bus mode is used (Technical Limitation)		X	X	✓	✓	✓	✓	✓
7	ESD resistibility (Technical Limitation)		X	X	X	X	✓	✓	✓
8	Restriction for STOP mode		X	X	X	X	X	X	✓

✓ : Not applicable

X : applicable

Note: The version is indicated by the in the lot number, marked on each product.
Pls refer to the below marking on each package

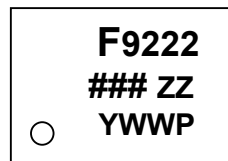
Marking for versions below V2.3



xx: DS or ES

Y: Year Code
WW: Week Code
P: Rank

Marking for versions V2.3 or later



###: Code Number (only preprogrammed flash)
ZZ: Flash Grade

Y: Year Code
WW: Week Code
P: Rank

μPD78F9221/2

Revision	Marking
V 1.0 (DS)	9222DS 411A 9222DS 416A
V 1.1 (ES)	9222ES 422I
V 1.2 (DS)	9222DS MMME
V 2.1 (ES)	9222ES 441I F9222ES 440K
V 2.1	F9221 xxxK F9222 xxxK
V 2.2 (ES)	F9222 V22ES 448K
V 2.3	F9221 xxxE F9222 xxxE

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(B) Description of Operating Precautions

No. 1	Restriction for Flash Memory self-programming (Technical Limitation)
	<p><u>Details</u></p> <p>If “Crystal/Ceramic oscillation” or “External clock input” is selected as clock generator by “Option byte”, Self-programming for Flash memory cannot be executed. Self-programming for Flash memory can be executed only when “Internal High-speed Ring-osc” is selected by “Option byte”.</p>
No. 2	Restriction for WDT reset (Technical Limitation)
	<p><u>Details</u></p> <p>If “Crystal/Ceramic oscillation” or “External clock input” is selected as clock generator by “Option byte”, Internal reset signal by WDT will not be generated. WDT can be used only when “Internal High-speed Ring-osc” is selected by “Option byte”.</p>
No. 3	Restriction for WDT count (Technical Limitation)
	<p><u>Details</u></p> <p>WDT counter will be incremented when write access for all SFR is executed.</p> <p><u>Workaround</u></p> <p>Shorten WDT counter clear interval, or Set WDT overflow time longer.</p>

No. 4	<p>Restriction for Clock Generator (Technical Limitation)</p> <p><u>Restriction</u> “Crystal/ Ceramic oscillation” cannot be used. The system clock which can be used for Ver 1.1(ES) is only “Internal High-speed Ring-osc”.</p> <p><u>Details</u> During reset period, “Pull-down resistor” is connected with X1, X2 terminal for initialization (Figure 1-A). These pull-down resistors need to be cut when “Crystal/Ceramic oscillation” or “External clock input” is selected by “Option byte” (Figure 1-B). But, for Ver 1.0(DS) and Ver 1.1(ES), these pull-down resistors are connected until Program execution timing (Figure 1-D). So, “Crystal/Ceramic oscillation” cannot operate correctly.</p> <p>For Ver 1.0(DS), Internal High-speed Ring-osc is operating during oscillation stability period (Figure 1-C). Oscillation stability is counted by using this clock, and Clock change to “Crystal/Ceramic oscillation” or “External clock” which start oscillation at Program execution timing (Figure 1-D) can be executed correctly. So after that, CPU can operate by “Crystal/Ceramic oscillation” or “External clock” correctly. But, for Ver 1.1(ES), Internal High-speed Ring-osc will stop if “Crystal/Ceramic oscillation” or “External clock” is selected by “Option byte”. So CPU cannot operate because oscillation stability (Figure 1-C) cannot be counted.</p> <p style="text-align: center;">Figure 1. Clock state after RESET</p> <div><p>The diagram shows three horizontal timelines. The top timeline is labeled 'RESET' and has a high pulse during period A. The middle timeline is labeled 'OSC Clock' and shows a series of vertical bars of increasing height starting at the beginning of period B, continuing through periods C and D. The bottom timeline is labeled 'Operation State' and is divided into four segments: A, B, C, and D. A vertical dashed line marks the start of period B.</p></div> <table><tr><th>Period</th><th>Normal Operation</th><th>DS1.0</th><th>DS1.1</th></tr><tr><td>A</td><td>Reset period</td><td>←</td><td>←</td></tr><tr><td>B</td><td>Reset is released, and Internal Ring-osc start, and “Option byte” setting is executed.</td><td>←</td><td>←</td></tr><tr><td>C</td><td>Oscillation stability period “External oscillation” will start, and CPU doesn’t start operation.</td><td>X1/X2 is pull-downed, So “External oscillation” doesn’t start. But oscillation stability is counted by Internal High-speed Ring-osc</td><td>X1/X2 is pull-downed, so “External oscillation” doesn’t start. Oscillation stability cannot be counted.</td></tr><tr><td>D</td><td>Internal CPU reset is released CPU operates by oscillation clock.</td><td>Internal CPU reset is released. CPU operates by internal High-speed Ring-osc. And “External oscillation” will start, so 、 after several instruction executed, clock source will be changed to “External oscillation”</td><td>Not operate.</td></tr></table> <p>“External oscillation” : “Crystal/Ceramic oscillation” or “External clock input”</p>	Period	Normal Operation	DS1.0	DS1.1	A	Reset period	←	←	B	Reset is released, and Internal Ring-osc start, and “Option byte” setting is executed.	←	←	C	Oscillation stability period “External oscillation” will start, and CPU doesn’t start operation.	X1/X2 is pull-downed, So “External oscillation” doesn’t start. But oscillation stability is counted by Internal High-speed Ring-osc	X1/X2 is pull-downed, so “External oscillation” doesn’t start. Oscillation stability cannot be counted.	D	Internal CPU reset is released CPU operates by oscillation clock.	Internal CPU reset is released. CPU operates by internal High-speed Ring-osc. And “External oscillation” will start, so 、 after several instruction executed, clock source will be changed to “External oscillation”	Not operate.
Period	Normal Operation	DS1.0	DS1.1																		
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No. 5	Restriction for LVI (Technical Limitation)
	<p><u>Details</u></p> <p>If a short pulse, but lower than the detection voltage (i.e. caused by noise) is applied, the internal RESET generated by the LVI function might be not sufficient to initialize the CPU. Consequently, there is same risk for an incorrect operation of the CPU.</p> <p><u>Workaround</u></p> <p>There is no complete countermeasure. The influence of the noise can be reduced by adding a bypass capacitor between VDD and VSS.</p>

No. 6	Restriction for INTP0 when LIN bus mode is used (Technical Limitation)																	
	<p><u>Details</u></p> <p>When UART6 is used as LIN(Local Interconnect Network), and “RxD6” terminal is selected for input source of “INTP0” (ISC0=1), the interrupt operation of INTP0 will be as follows.</p> <table><tr><th>INTP0 input source (ISC0)</th><th>INTP0 valid edge (ES01,ES00)</th><th>Interrupt detect operation</th></tr><tr><td rowspan="3">P30/INTP0</td><td>Falling edge (ES01,ES00=0,0)</td><td>Correct operation</td></tr><tr><td>Rising edge (ES01,ES00=0,1)</td><td>Correct operation</td></tr><tr><td>Both edge (ES01,ES00=1,1)</td><td>Correct operation</td></tr><tr><td rowspan="3">P44/RxD6</td><td>Falling edge (ES01,ES00=0,0)</td><td>Correct operation</td></tr><tr><td>Rising edge (ES01,ES00=0,1)</td><td>Rising edge for P44/RxD6 : interrupt cannot be detected Rising edge for P30/INTP0 : interrupt will be detected</td></tr><tr><td>Both edge (ES01,ES00=1,1)</td><td>【P44/RxD6】 Falling edge input : interrupt can be detected Rising edge input : interrupt cannot be detected 【P30/INTP0】 Falling edge input : interrupt will not be detected. Rising edge input : interrupt will be detected.</td></tr></table>	INTP0 input source (ISC0)	INTP0 valid edge (ES01,ES00)	Interrupt detect operation	P30/INTP0	Falling edge (ES01,ES00=0,0)	Correct operation	Rising edge (ES01,ES00=0,1)	Correct operation	Both edge (ES01,ES00=1,1)	Correct operation	P44/RxD6	Falling edge (ES01,ES00=0,0)	Correct operation	Rising edge (ES01,ES00=0,1)	Rising edge for P44/RxD6 : interrupt cannot be detected Rising edge for P30/INTP0 : interrupt will be detected	Both edge (ES01,ES00=1,1)	【P44/RxD6】 Falling edge input : interrupt can be detected Rising edge input : interrupt cannot be detected 【P30/INTP0】 Falling edge input : interrupt will not be detected. Rising edge input : interrupt will be detected.
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	<p><u>Workaround</u></p> <p>When “RxD6” is selected as “INTP0” input source, it is recommended to set the valid edge to falling edge, or to set input source to “INTP0”.</p>																	

No. 7	ESD resistibility (Technical Limitation)
Global Document No. U18105EE3V0IF00 (3rd edition)	<p><u>Details</u></p> <p>This product will not reach the NEC internal ESD guidelines.</p>

No. 8	Restriction for STOP mode (Technical Limitation)
	<p><u>Details</u></p> <p>When CPU execute STOP instruction with IE flag = 0(DI instruction executed) and IF flag = 1 that is not masked, STOP mode will not be released. Then any other interrupts are occurred, STOP mode is not released, either.</p> <p>Case 1 : When CPU execute STOP instruction with IE flag = 0 and IF flag = 1, MK flag = 0. DI ; Interrupt is disabled SET1 PIF0 ; Set interrupt request flag(INTP0) CLR1 PMK0 ; Clear interrupt mask flag(INTP0) SET1 P2.0 ; Set Port20 to "1" STOP ; Changing STOP mode CLR1 P2.0 ; Clear Port20(Will not be executed)</p> <p>When interrupt enabled and standby release signal is occurred, and CPU execute interrupt request pending instruction right before STOP instruction executing, then STOP mode will not be released.</p> <p>Case2 : When CPU execute STOP instruction with IE flag = 1 and IF flag = 1, MK flag = 0. EI ; Interrupt is enabled SET1 P2.0 ; Set Port20 to "1" SET1 PIF0 ; Set interrupt request flag(INTP0) CLR1 PMK0 ; Executing interrupt request pending instruction STOP ; Changing STOP mode CLR1 P2.0 ; Clear Port20(Never executed)</p> <p>Note : interrupt request pending instruction Write access instruction for interrupt request flag register 0 (IF0) Write access instruction for interrupt mask flag register 0 (MK0)</p> <p><u>Workaround</u></p> <p>Execute EI instruction before STOP instruction execution. Then do not execute Interrupt request pending instruction right before STOP execution.</p> <p>Case3 : Executing EI instruction right before STOP instruction. DI ; Interrupt disabled SET1 PIF0 ; Set interrupt request flag(INTP0) CLR1 PMK0 ; Clear interrupt mask flag(INTP0) SET1 P2.0 ; Set Port20 to "1". EI ; Interrupt enabled STOP ; Changing STOP mode CLR1 P2.0 ; Clear Port20(will execute)</p> <p>Note: If interrupt is occurred before executing STOP instruction, it's necessary to generate interrupt for releasing from STOP mode because interrupt request flag is cleared before executing STOP instruction.</p>

(C) Valid Specification

Item	Date published	Document No.	Document Title
1	November 2004	U16898EJ...	User's Manual

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(D) Revision History

Item	Date published	Document No.	Comment
1	January 21, 2005	TPS-LE-OP-F9222-1	1 st Release
2	March 07, 2005	TPS-LE-OP-F9222-2	2 nd Release addition of version V 2.1 and later
3	March 22, 2006	TPS-LE-OP-F9222-3	3 rd Release addition of Rank "P"

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