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## **Customer Notification**

# IE-78K0-NS-A<sup>TM</sup>

**In-Circuit Emulator** 

**Operating Precautions** 

Target Devices 78K/0 Series

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IE-78K0-NS-A

#### (A) Table of Operating Precautions

			IE-7	8K0-I	NS-A			
No.	Outline	Control Code Note	Е	F	G	Н		
1	P50P52 output (Technical Limitation)			3	3	3		
2	Improvement of operation clock characteristics (Technical Limitation)			3	3	3		
3	Support of specification change for several devices (Technical Limitation)			7	3	3		
4	Execution time measurement (Technical Limitation)			7	7	3		
5	Section Trace – Displayed trace data (Technical Limitation)			7	7	7		
6	Break – Software breakpoints (Technical Limitation)			7	7	7		
7	Break – Peripheral break at subclock operation (Technical Limitation)			7	7	7		
8	Flash self-programming mode emulation (Technical Limitation)			7	7	7		
9	Timer Event – Execution time measurement (Technical Limitation)		7	7	7	3		
10	Memory banking (Technical Limitation)			7	7	3		
11	ROMIess microcontroller support (Technical Limitation)		7	7	7	3		

- 3: Not applicable
- 7: Applicable

#### Notes:

- The "control code" is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code. The rank is indicated by the letter appearing at the 5<sup>th</sup> position from the left in the lot number, marked on each product.
- 2. The Operating Precautions for products with control codes A-D have been deleted from this document, because it is expected, that all products used in the field have at least a control code E or later.

#### (B) Description of Operating Precautions

No. 1	P50P52 output
	(Technical Limitation)
	<u>Details</u>
	A high-level signal is output from ports 50 to 52 while the power of the emulator is on and the
	debugger has not been started.

# No. 2 Improvement of operation clock characteristics (Technical Limitation)

#### Details

The characteristics of the operation clock used in the in-circuit emulator have been improved (addition of specification). This is supported on products control code F or later.

# No. 3 Support of specification change for several devices (Technical Limitation)

#### Details

A specification change in the following devices (high-speed specification: 12 MHz operation) has been supported.

Target devices:

μPD780024A, 780024AY, 780034A, 780034AY Subseries μPD780078, 780078Y Subseries μPD780988 Subseries

Target emulation board:

IE-780034-NS-EM1 (control code J or later)

IE-780078-NS-EM1 (control code D or later)

IE-780988-NS-EM4 (control code B or later) + IE-78K0-NS-P01 (control code D or later)

The high-speed specification is not supported in IE-78K0-NS-A products with a control code F or lower. It is not possible to upgrade those products to control code G or later, because products with control code F or lower are using separated main and option boards, which are limiting the high-speed operation.

# No. 4 Execution time measurement (Technical Limitation)

#### Details

If a setting which causes DMM or snap shot to occur is made during execution time measurement with a zone specified, the measured execution time is greater than the actual value.

#### Workaround

Do not specify DMM or snap shot during execution time measurement.

# No. 5 Section Trace – Displayed trace data (Technical Limitation) Details If a DMM or snap shot event is specified with section trace specified, the trace data may not be displayed correctly. Workaround

When executing section trace, do not specify DMM or a snap shot event. When specifying DMM or a snap shot event, do not specify section trace.

# No. 6 Break – Software breakpoints (Technical Limitation) Details If 00H is written by the program or by DMM at an address where a software break has been set,

the data when the break occurs returns to the value before the program was executed.

#### **Workaround**

Do not set a software break at a memory address that is written to during program execution.

# No. 7 Break – Peripheral break at subclock operation (Technical Limitation) Details If Break is selected for the peripheral break of the Debugger and the subclock is used as the cpuclock, the operation of the peripheral emulation chip will not stop, even if a break is applied.

# No. 8 Flash self-programming mode emulation (Technical Limitation)

#### Details

- Of the four access events in flash self-mode, only one may be consumed. Consequently, users should release the above events on the debugger side and then set a maximum of three events each when switching to flash self-mode.
- The system may enter restart processing once a break occurs in flash self-mode that is not the result of break settings. This will cause some of the time measurement results and some trace data and path count to become invalid.

No. 9	Timer Event – Execution time measurement (Technical Limitation)		
	<u>Details</u> The error message "EX_SE_NONTIMER" may be displayed, when the execution time is measured by using a timer event, the initialize button is clicked to erase the result, the program is resumed and a break occurs.		
No. 10	Memory banking (Technical Limitation)		
	<u>Details</u> The memory banking is not supported.		
No. 11	ROMIess microcontroller support (Technical Limitation)		
	<u>Details</u> When a CPU reset is executed on a ROMless microcontroller, the program jumps to the reset vector set to the emulation ROM.		
	Workaround Pls. refer to chapter 1.4 "Cautions on μPD78070A and 78070AY Development" in the IE-78078-NS-EM1 User's Manual (DOCNo. U14741E)		

### (C) Valid Specification

Item	Date published	Document No.	Document Title
1	October 2003	U14889E	IE-78K0-NS-A In-Circuit Emulator User's Manual

### (D) Revision History

Item	Date published	Document No.	Comment
1	August 28, 2002	TPS-LE-OP-0T016	1 <sup>st</sup> Release This document is a replacement of the document TPS-LE-B-0T016-3
2	December 11, 2003	TPS-LE-OP-0T016-1	1 <sup>st</sup> Update Level G inserted
3	January 12, 2005	TPS-LE-OP-0T016-2	2 <sup>nd</sup> Update Level A-D removed Level H inserted Items for level A-D removed Remaining items renumbered Items 9, 10, and 11 added