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April 1st, 2010
Renesas Electronics Corporation

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User's Manual

Phase-out/Discontinued

IE-703217-G1-EM1

Emulation Board

Target Devices

V850ES/KF1™

V850ES/KG1™

V850ES/KJ1™

[MEMO]

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- Availability of related technical literature
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INTRODUCTION

Target Readers This manual is intended for users who design and develop application systems using the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 microcontrollers.

Purpose The purpose of this manual is to describe the basic specifications of the IE-703217-G1-EM1 and its proper operation.

Organization This manual is broadly divided into the following parts.

- Outline
- Part names and functions
- Switch settings
- Setup procedure
- Cautions
- Restrictions

How to Read This Manual It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers. Use the IE-703217-G1-EM1 connected to the in-circuit emulator (IE-V850ES-G1). This manual describes the basic setup procedures and switch settings of the IE-703217-G1-EM1 and IE-V850ES-G1. For the part names, functions, and configuration parts of the IE-V850ES-G1, refer to the **IE-V850ES-G1 User's Manual (U16313E)** provided separately.

To learn about the basic specifications and operation
→Read this manual in the order listed in **CONTENTS**.

To learn software settings such as the operation methods, command functions, etc., of the IE-V850ES-G1 or IE-703217-G1-EM1
→Read the user's manual of the debugger (sold separately) that is used.

Conventions

Note: Footnote for item marked with **Note** in the text

Caution: Information requiring particular attention

Remark: Supplementary information

Numeral representation: Binary ... xxxx or xxxxB
Decimal ... xxxx
Hexadecimal ... xxxxH

Prefix representing a power of 2 (address space, memory capacity):
K (kilo): $2^{10} = 1024$
M (mega): $2^{20} = 1024^2$

Terminology The meanings of terms used in this manual are listed below.

Target device	This is the device to be emulated.
Target system	The system (user-built system) to be debugged. This includes the target program and hardware configured by the user.
Emulation CPU	The CPU that executes the program created by the user in the emulator.

Related Documents

When using this manual, refer to the following manuals.

The related documents (user's manuals) indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Development Tools (User's Manuals)

Document Name		Document Number
IE-V850ES-G1 (In-Circuit Emulator for V850ES)		U16313E
IE-703217-G1-EM1 (In-Circuit Emulator Emulation Board for V850ES/KF1, V850ES/KG1, V850ES/KJ1)		This manual
V850ES/KF1, V850ES/KG1, V850ES/KJ1 Hardware		U15862E
CA850 Ver.2.50 C Compiler Package	Operation	U16053E
	C Language	U16054E
	PM Plus	U16055E
	Assembly Language	U16042E
ID850 Ver.2.50 Integrated Debugger	Operation Windows™ based	U16217E
SM850 Ver.2.50 System Simulator	Operation Windows based	U16218E
SM850 Ver.2.00 or Later System Simulator	External Part User Open Interface Specifications	U14873E
RX850 Ver.3.13 or Later (Real-Time OS)	Basics	U13430E
	Installation	U13410E
	Technical	U13431E
RX850 Pro Ver.3.13 (Real-Time OS)	Basics	U13773E
	Installation	U13774E
	Technical	U13772E
RD850 Ver.3.01 Task Debugger		U13737E
RD850 Pro Ver.3.01 Task Debugger		U13916E
AZ850 Ver.3.10 System Performance Analyzer		U14410E
PG-FP4 Flash Memory Programmer		U15260E

Caution The related documents listed above are subject to change without notice.

Be sure to use the latest version of each document when designing.

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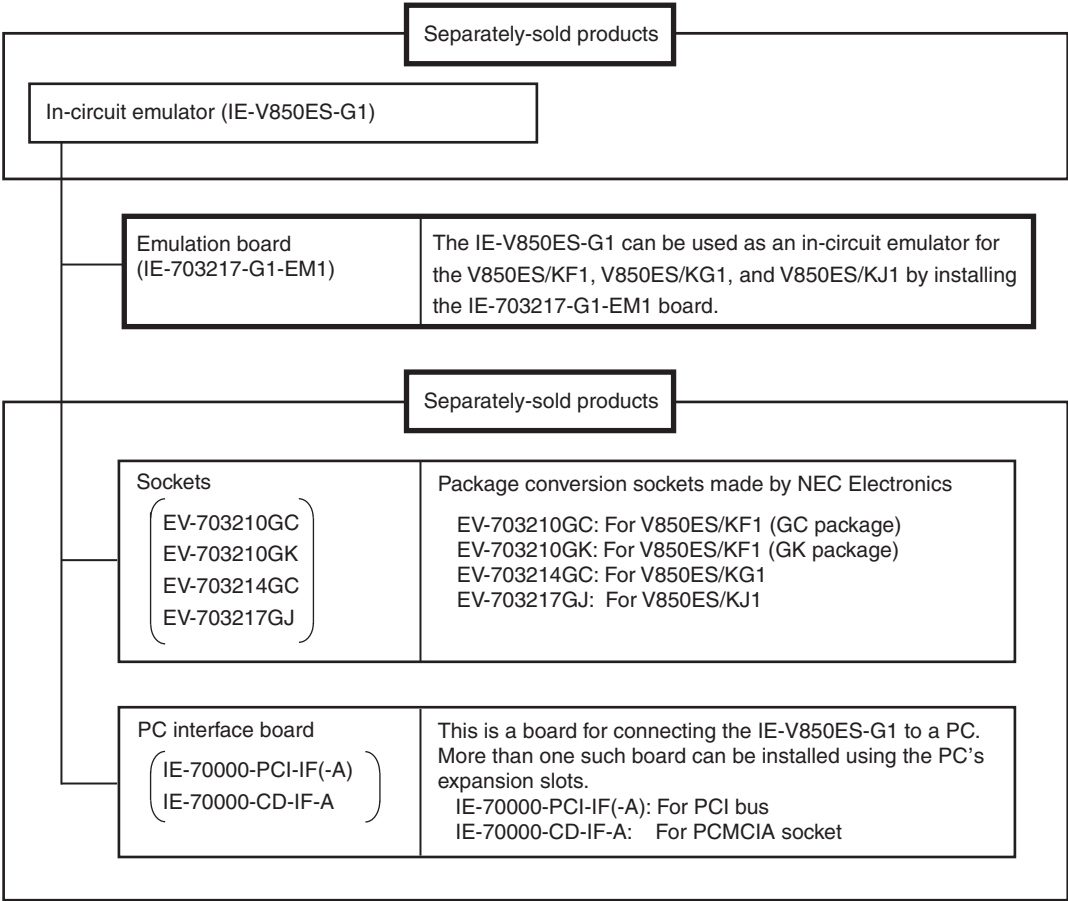
CHAPTER 1 OUTLINE

The IE-703217-G1-EM1 is an emulation board for the IE-V850ES-G1 in-circuit emulator.

Connected to the IE-V850ES-G1, the IE-703217-G1-EM1 can be used for efficient hardware and software debugging during system development using the V850ES/KF1, V850ES/KG1, and V850ES/KJ1.

This manual describes the basic setup procedure and the switch settings of the IE-V850ES-G1 when connected to the IE-703217-G1-EM1. For the part names and functions of the IE-V850ES-G1, refer to the separate **IE-V850ES-G1 User's Manual (U16313E)**.

1.1 Product Configuration



1.2 Features

- Maximum operating frequency: 20 MHz (2.7 V to 5.5 V)
- The following pins can be masked.
NMI, WAIT, RESET, HLD $\overline{\text{RQ}}$
- The external dimensions of the IE-703217-G1-EM1 are listed below

Item		Value
External dimensions	Height	35 mm
	Width	205 mm
	Depth	140 mm

1.3 Function Specifications (When Connected to IE-V850ES-G1)

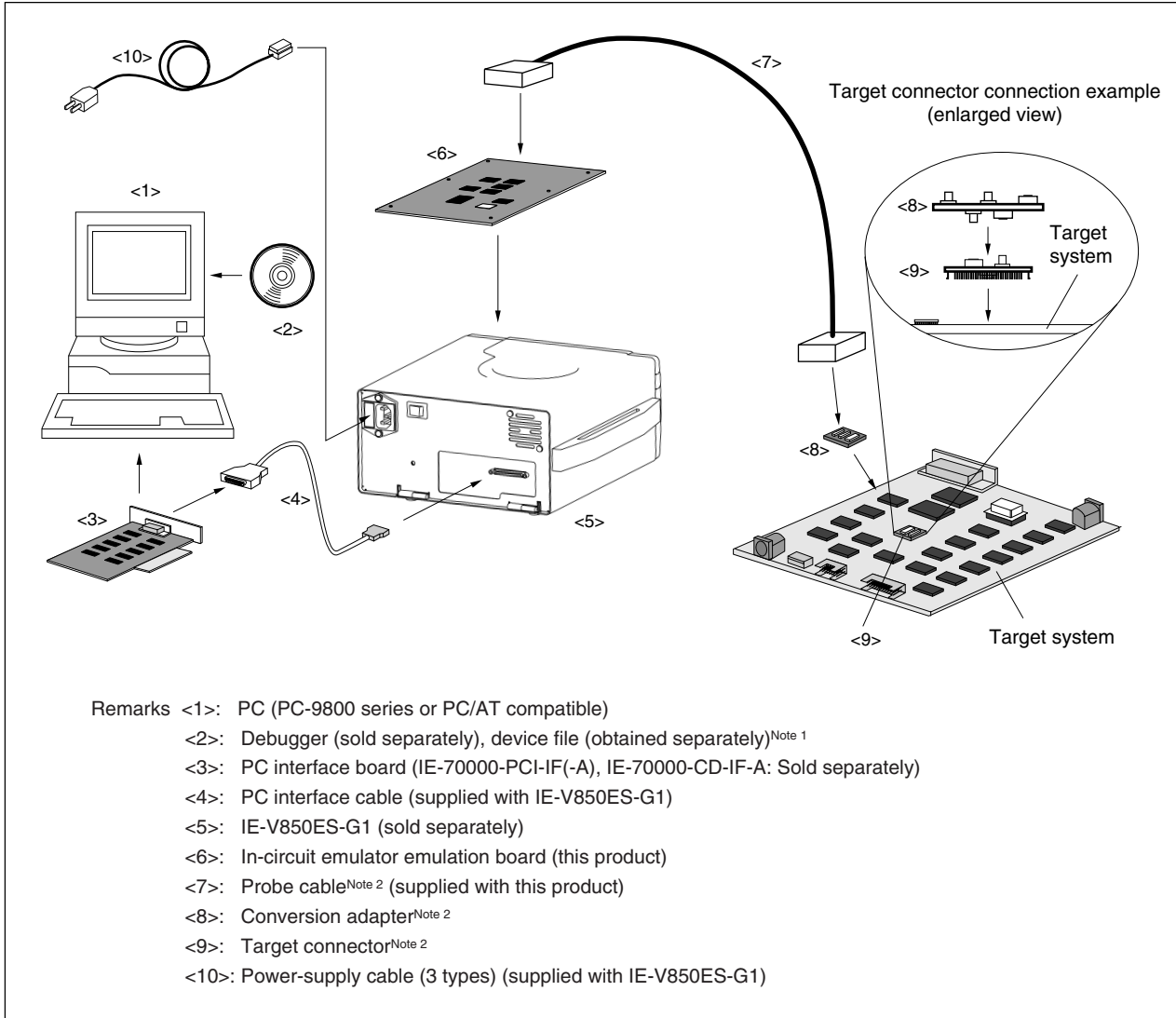
Item		Specification
Emulation memory capacity	Internal ROM	1 MB
	For user memory	4 MB
Execution/pass detection coverage memory capacity	Internal ROM	256 KB
	External memory	1 MB
Memory access detection coverage memory capacity	External memory	1 MB
Branch destination entry count calculation coverage memory capacity	Internal ROM	256 KB
	External memory	1 MB
Trace memory capacity		168 bits × 32 K frames
Time measurement function		Internal timers × 3
External logic probe		8-bit external trace possible
		Trace/break event setting possible
Break function		Event break
		Step execution break
		Forced break
		Fail-safe break <ul style="list-style-type: none"> • Illegal access to peripheral I/O • Access to guard area • Write to ROM area

Caution Some functions may not be supported depending on the debugger that is used.

1.4 System Configuration

The system configuration when using the IE-703217-G1-EM1 connected to the IE-V850ES-G1, which itself is connected to a PC (PC-9800 series or PC/AT™ compatible) is shown below.

Figure 1-1. System Configuration

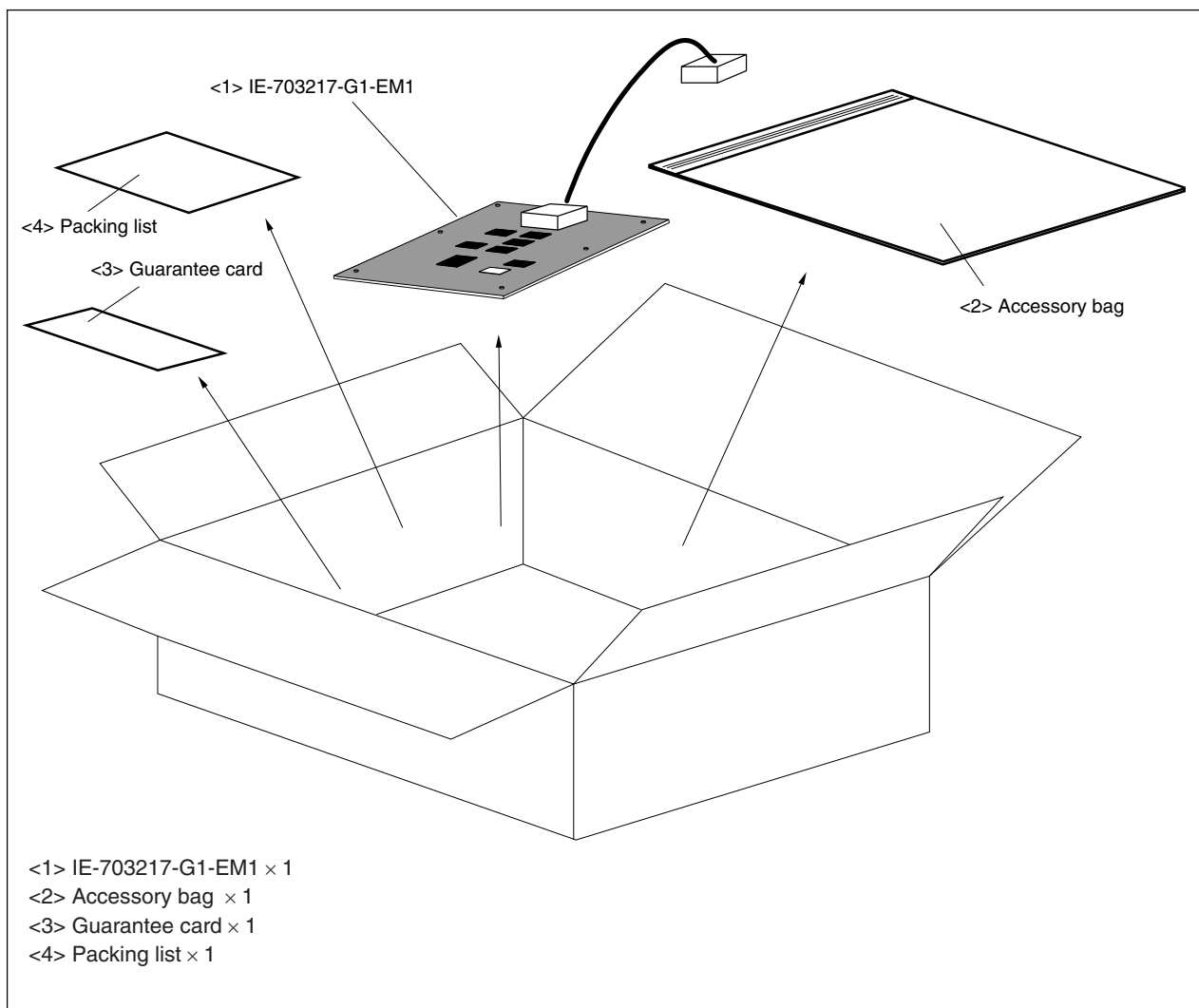


- Notes**
1. The device file can be downloaded from the NEC Electronics website. (URL: <http://www.necel.com/micro>)
 2. For the probe cable, conversion adapter, and target connector, refer to the user's manual of the emulation board.

1.5 Contents in Carton

The IE-703217-G1-EM1 package contains the IE-703217-G1-EM1 emulation board, a guarantee card, a packing list, this manual, and an accessory bag. Check whether the accessory bag contains the items listed below. If you find any missing or damaged items, contact an NEC Electronics sales representative or distributor.

Figure 1-2. Contents in Carton



Check whether the accessory bag contains the following items in addition to this manual and the packing list (× 1).

- | | |
|---|-------------------------------|
| (a) 8-pin header (for resonator replacement): | × 1 |
| (b) 4-pin header (for reference voltage replacement): | × 1 |
| (c) Socket (for REGC capacitor replacement): | × 1 |
| (d) Screws/washers: | 6 sets (6 screws + 6 washers) |

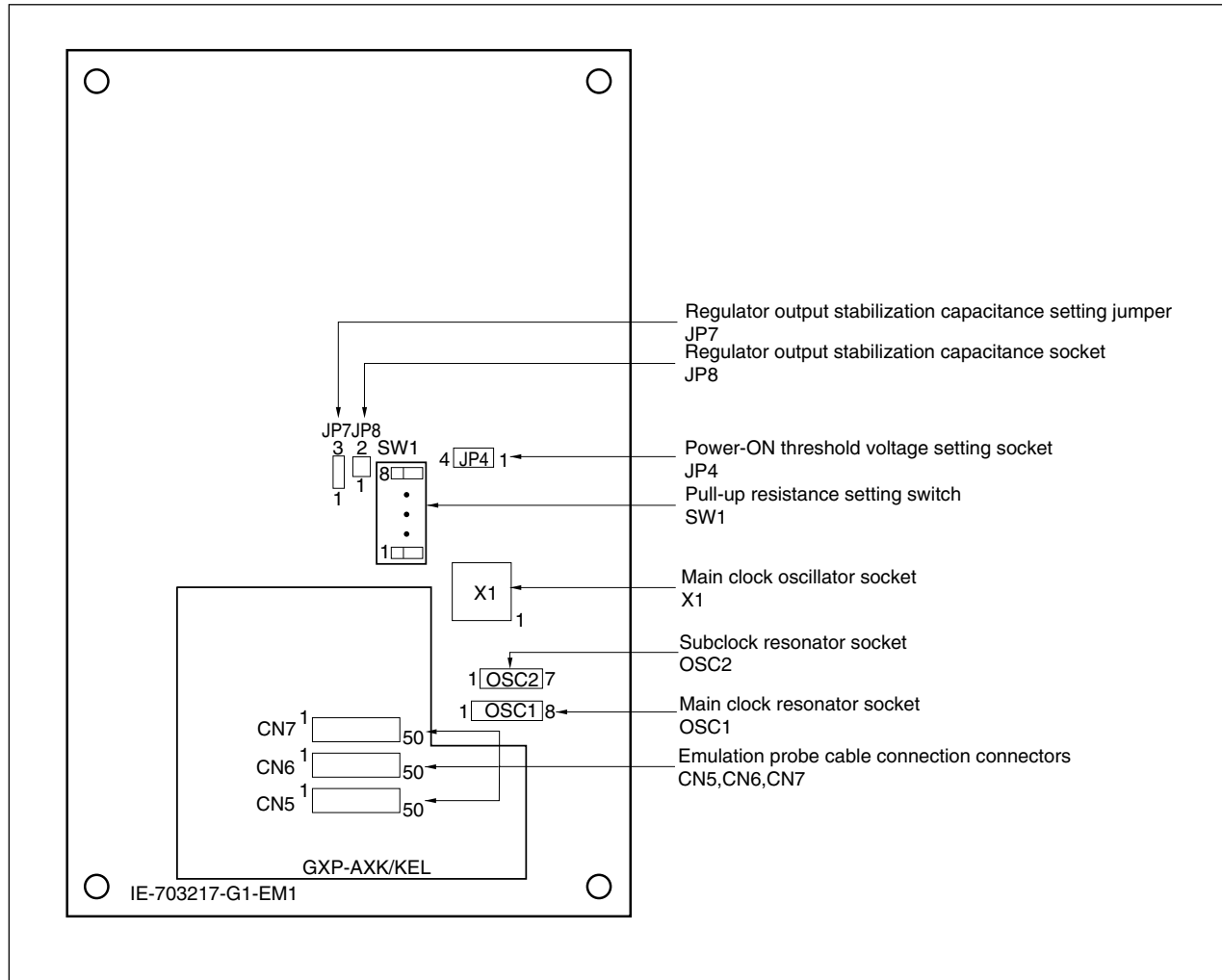
CHAPTER 2 PART NAMES AND FUNCTIONS

This chapter describes the part names and functions of the IE-703217-G1-EM1.

For the part names and functions of the IE-V850ES-G1, refer to the **IE-V850ES-G1 User's Manual (U16313E)**.

2.1 Part Names and Functions of IE-703217-G1-EM1

Figure 2-1. Part Names of IE-703217-G1-EM1



(1) Emulation probe cable connection connectors (CN5, CN6, CN7)

Connect the supplied probe cable.

(2) Main clock resonator socket (OSC1)

This socket is used to connect the main clock resonator. (For details, refer to **3.1 Clock Settings**.)

(3) Subclock resonator socket (OSC2)

This socket is used to connect the subclock resonator. (For details, refer to **3.1 Clock Settings**.)

(4) Main clock oscillator socket (X1)

This socket is used to connect the main clock oscillator. (For details, refer to **3.1 Clock Settings**.)

(5) Pull-up resistance setting switch (SW1)

This switch is used to set emulation of the pull-up resistance, which is a mask option of the V850ES/KF1, V850ES/KG1, and V850ES/KJ1. (For details, refer to **3.2 Pull-Up Resistor Settings**.)

(6) Power-ON threshold voltage setting socket (JP4)

This socket is used to set the threshold voltage for judging whether the target system is connected. (For details, refer to **3.3 Power-ON Threshold Voltage Settings**.)

(7) Regulator output stabilization capacitance socket (JP8)

This socket is used to stabilize the output when using the regulator of the V850ES/KF1, V850ES/KG1, or V850ES/KJ1. (For details, refer to **3.4 Regulator Output Stabilization Capacitance Setting Jumpers**.)

(8) Regulator output stabilization capacitance setting jumper (JP7)

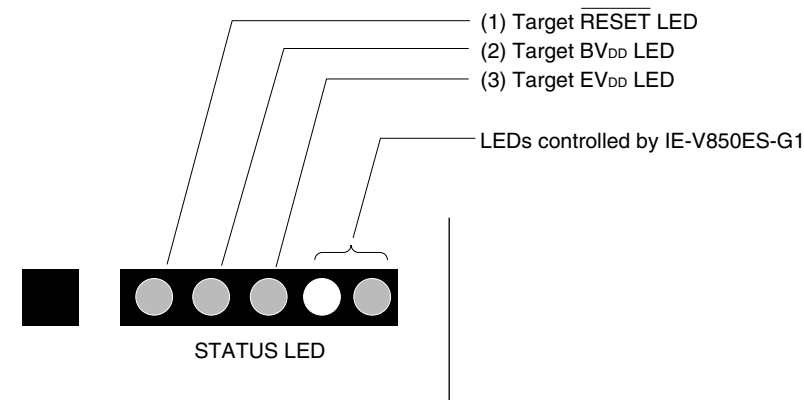
This jumper is used to set whether to use the regulator of the V850ES/KF1, V850ES/KG1, or V850ES/KJ1. (For details, refer to **3.4 Regulator Output Stabilization Capacitance Setting Jumpers**.)

2.2 LEDs Controlled by IE-703217-G1-EM1

Some of the LEDs mounted in the IE-V850ES-G1 are controlled by the IE-703217-G1-EM1.

For the LEDs that are controlled by the IE-V850ES-G1, refer to the **IE-V850ES-G1 User's Manual (U16313E)**.

Figure 2-2. LEDs Controlled by IE-703217-G1-EM1



(1) Target $\overline{\text{RESET}}$ LED

The status of the $\overline{\text{RESET}}$ signal connected to the target system is indicated as follows.

Lit (ON): The target system is connected and the $\overline{\text{RESET}}$ signal is active (GND level).

Unlit (OFF): Either the target system is not connected, or the $\overline{\text{RESET}}$ signal is inactive (V_{DD} level).

(2) Target BV_{DD} LED

The status of the BV_{DD} signal connected to the target system is indicated as follows.

Lit (ON): The target system is connected, and voltage is being applied to the BV_{DD} pin.

Unlit (OFF): Either the target system is not connected, or voltage is not being applied to the BV_{DD} pin.

(3) Target EV_{DD} LED

The status of the EV_{DD} signal connected to the target system is indicated as follows.

Lit (ON): The target system is connected and voltage is being applied to the EV_{DD} pin.

Unlit (OFF): Either the target system is not connected, or voltage is not being applied to the EV_{DD} pin.

3.2 Pull-Up Resistor Settings

Table 3-2 lists the settings for pull-up resistor emulation, which is a mask option of the V850ES/KF1, V850ES/KG1, and V850ES/KJ1. For the location of SW1, refer to Figure 2-1.

Table 3-2. Pull-Up Resistor Settings

SW1	Port
1	P36
2	P37
3	P38
4	P39
5	P614
6	P615
7	Not used
8	Not used

ON: Connect pull-up resistor.

OFF: Don't connect pull-up resistor.

Remark All the settings are OFF at shipment.

3.3 Power-ON Threshold Voltage Settings

The threshold voltage used to judge whether the target system is connected (hereafter called "power-ON threshold voltage") is set to 1.7 V at shipment. (Refer to **Figure 3-1 JP4 Settings at Shipment**.) To change this threshold voltage, insert a 4-pin jumper (standard accessory) on which resistors have been mounted to JP4 as shown in Figure 3-2. For the location of JP4, refer to Figure 2-1.

Figure 3-1. JP4 Settings at Shipment

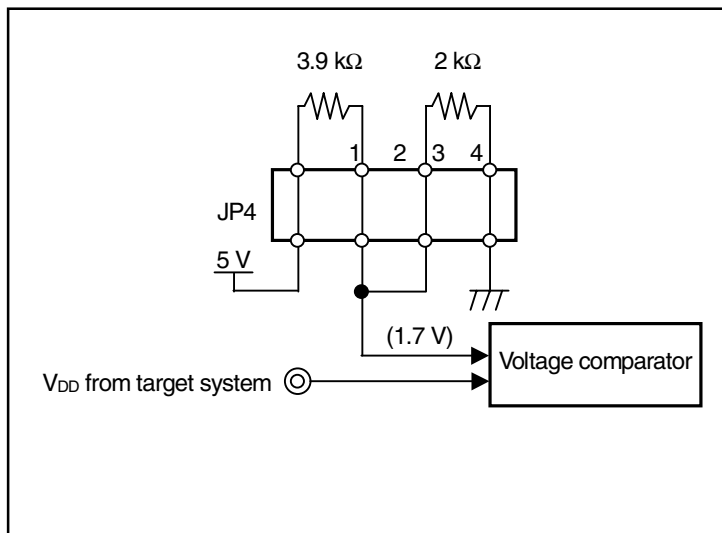
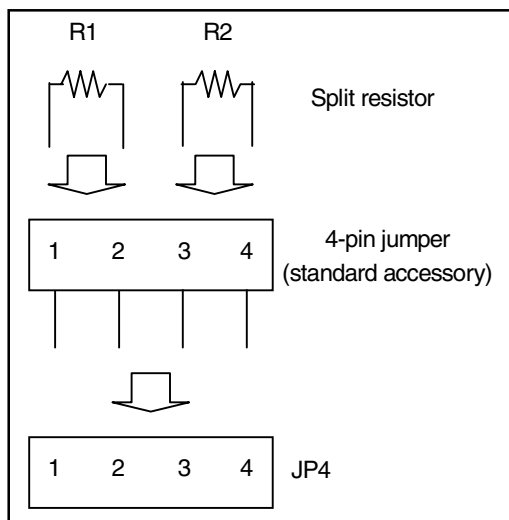


Figure 3-2. Changing Power-ON Threshold Voltage




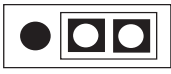

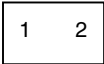
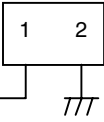

The threshold voltage can be obtained with the following equation.

$$\text{Threshold voltage} = 5 \text{ V} \times R2 / (R1 + R2)$$

3.4 Regulator Output Stabilization Capacitance Setting Jumpers

These are the jumpers for connecting the capacitance for stabilizing the output when using the regulator of the V850ES/KF1, V850ES/KG1, or V850ES/KJ1. For the location of JP7 and JP8, refer to Figure 2-1. A 10 μ F electrolytic capacitor is mounted on JP8 at shipment.

Table 3-3. Regulator Output Stabilization Capacitance Settings

Regulator	JP7	JP8
Don't use (setting at shipment)	1  3	– (don't care)
Use	1  3	<p>Output stabilization capacitance </p> <p>2-pin jumper (standard accessory) </p> <p></p> <p>JP8</p> <p>To REGC pin of emulation CPU</p> <p></p>

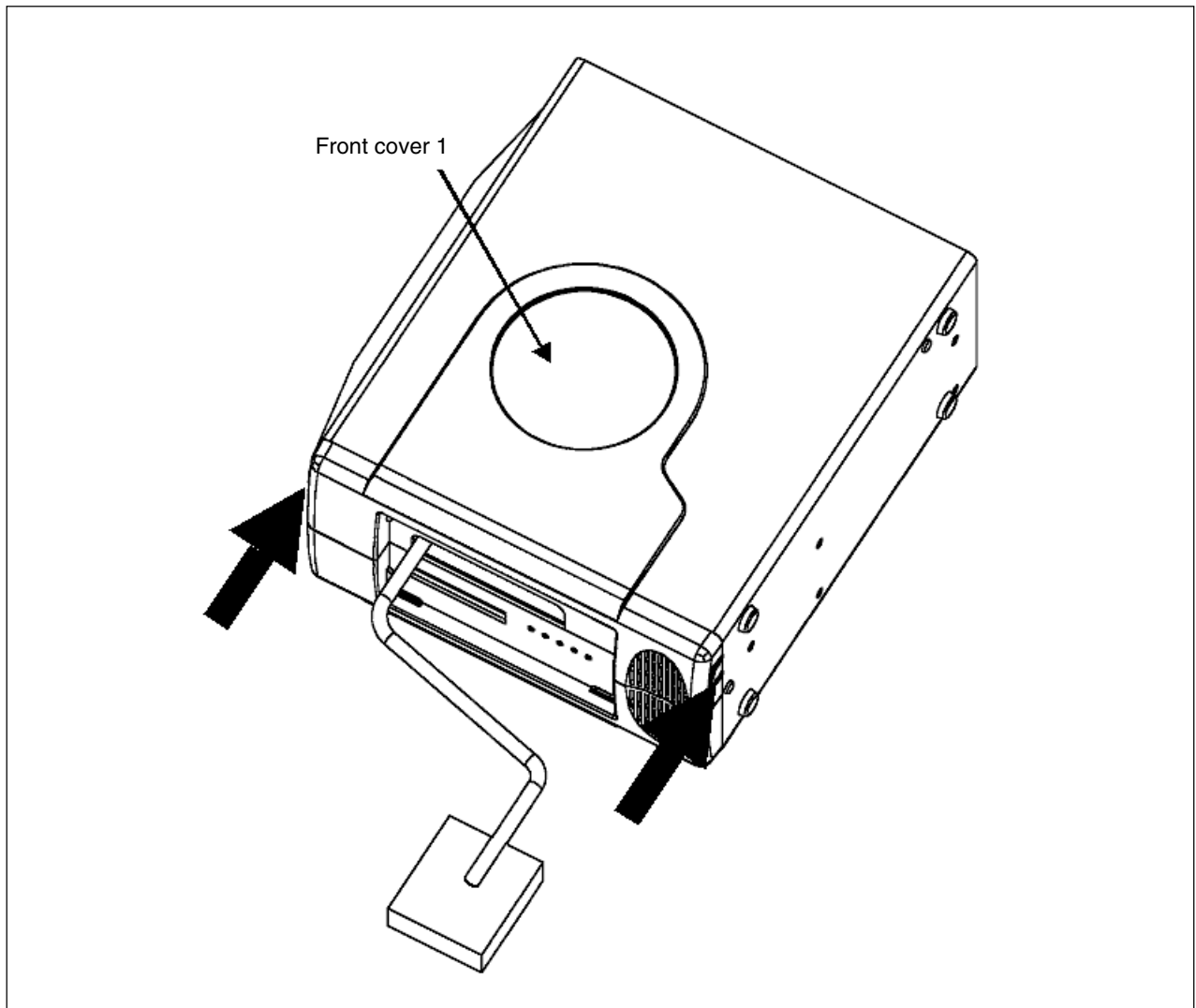
CHAPTER 4 SETUP PROCEDURE

This chapter describes how to connect the IE-703217-G1-EM1 and related products.

4.1 Removing Probe and Replacing Clock Module

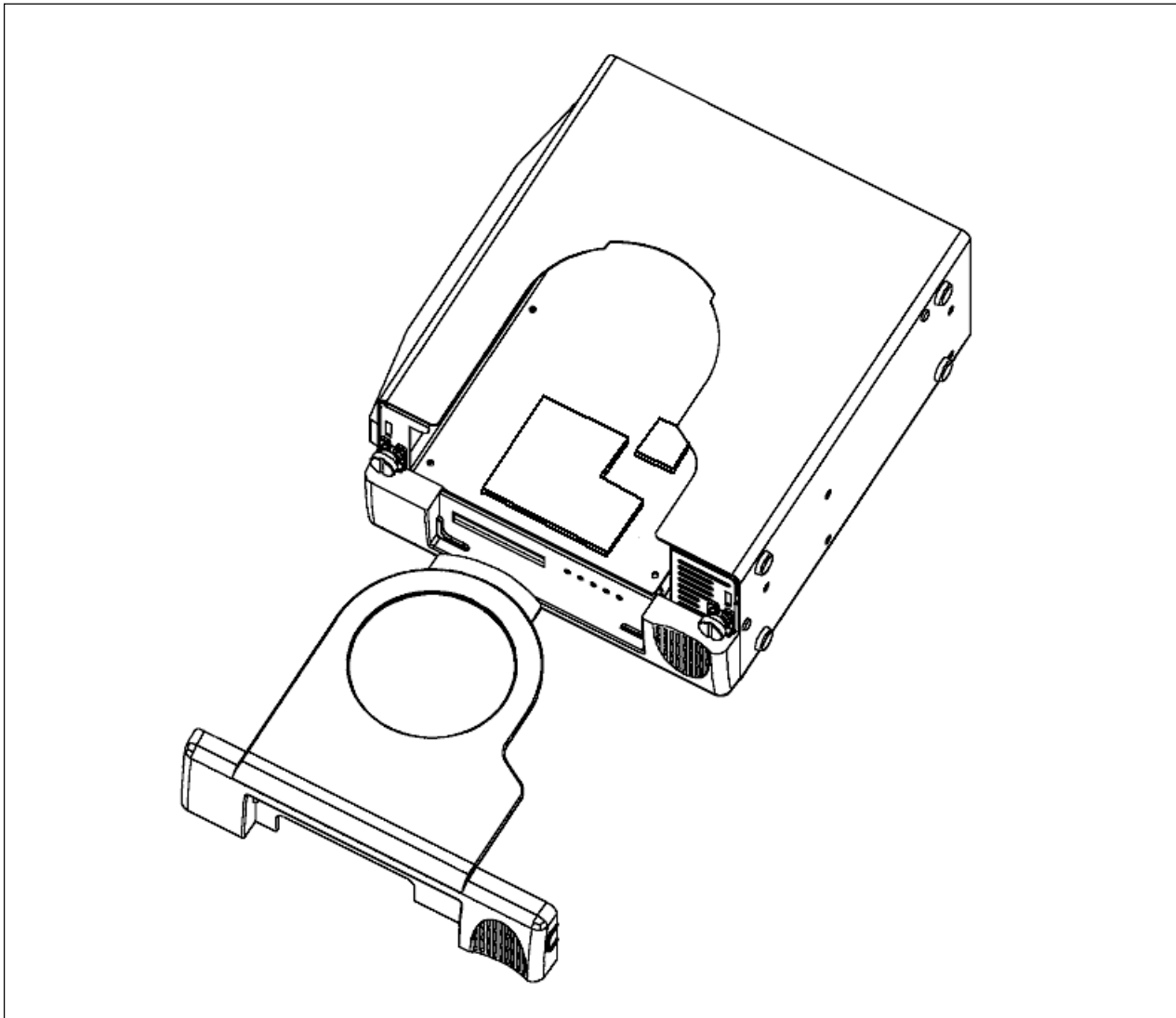
- <1> Hold the IE-703217-G1-EM1 by placing the fingers at the two locations indicated by the arrows and pull out front cover 1.

Figure 4-1. Opening/Closing Cover Step 1 (Removing Front Cover 1)



<2> Then remove the probe and change the clock.

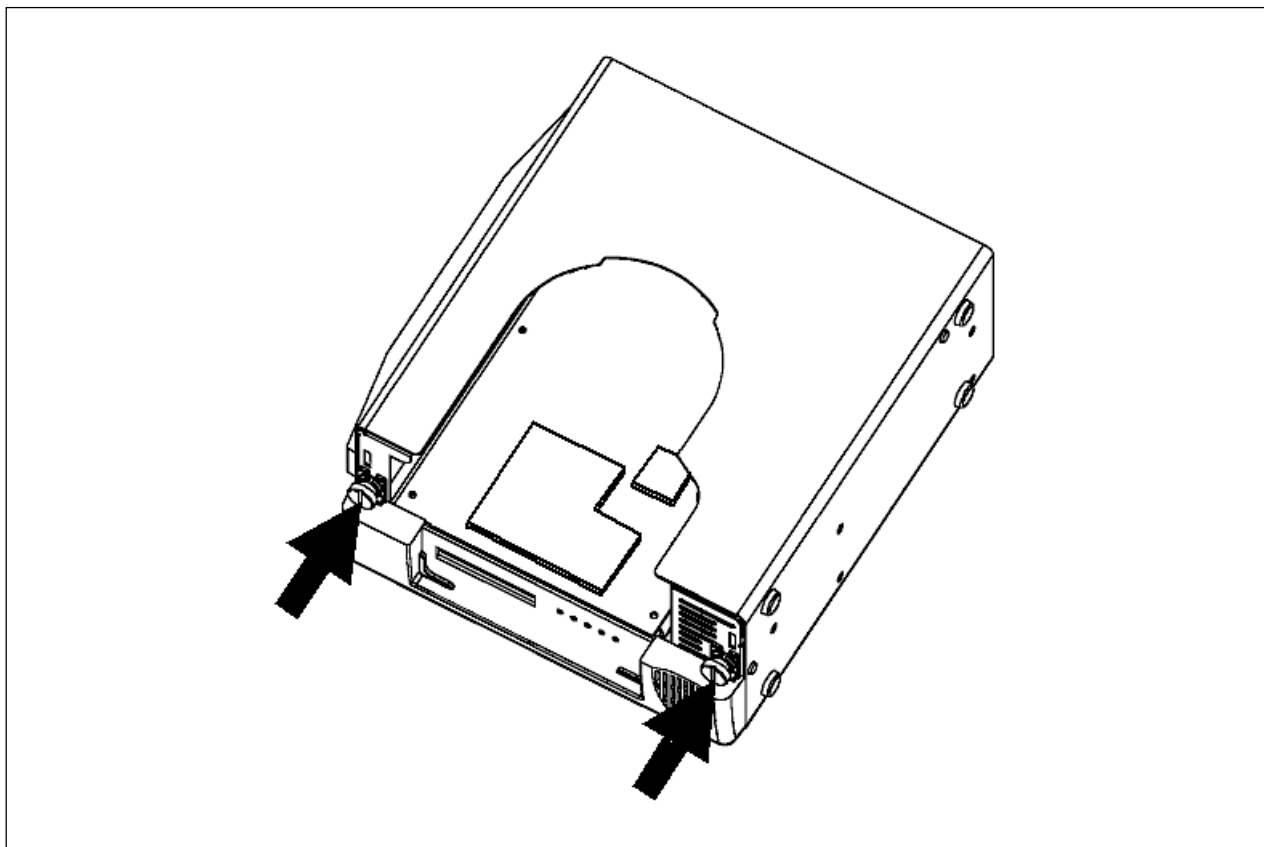
Figure 4-2. Opening/Closing Cover Step 1 (After Removing Front Cover 1)



4.2 Removing Emulation Board

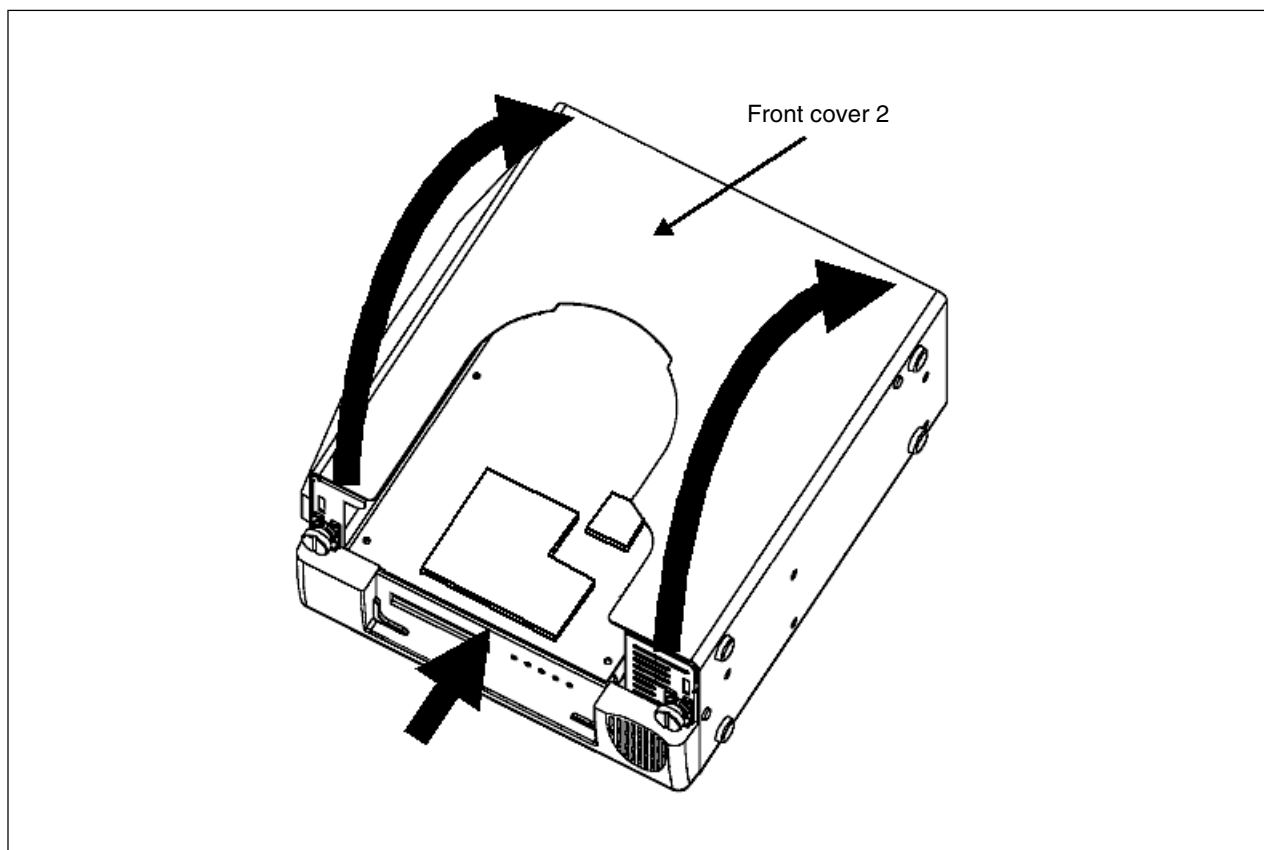
- <1> Place the case down horizontally.
- <2> Disconnect the power supply cable and the host interface cable.
- <3> Refer to **4.1 Removing Probe and Replacing Clock Module** for the procedure up to the removal of front cover 1.
- <4> Loosen the 2 screws indicated by the arrows.

Figure 4-3. Opening/Closing Cover Step 2 (Loosening Screws)



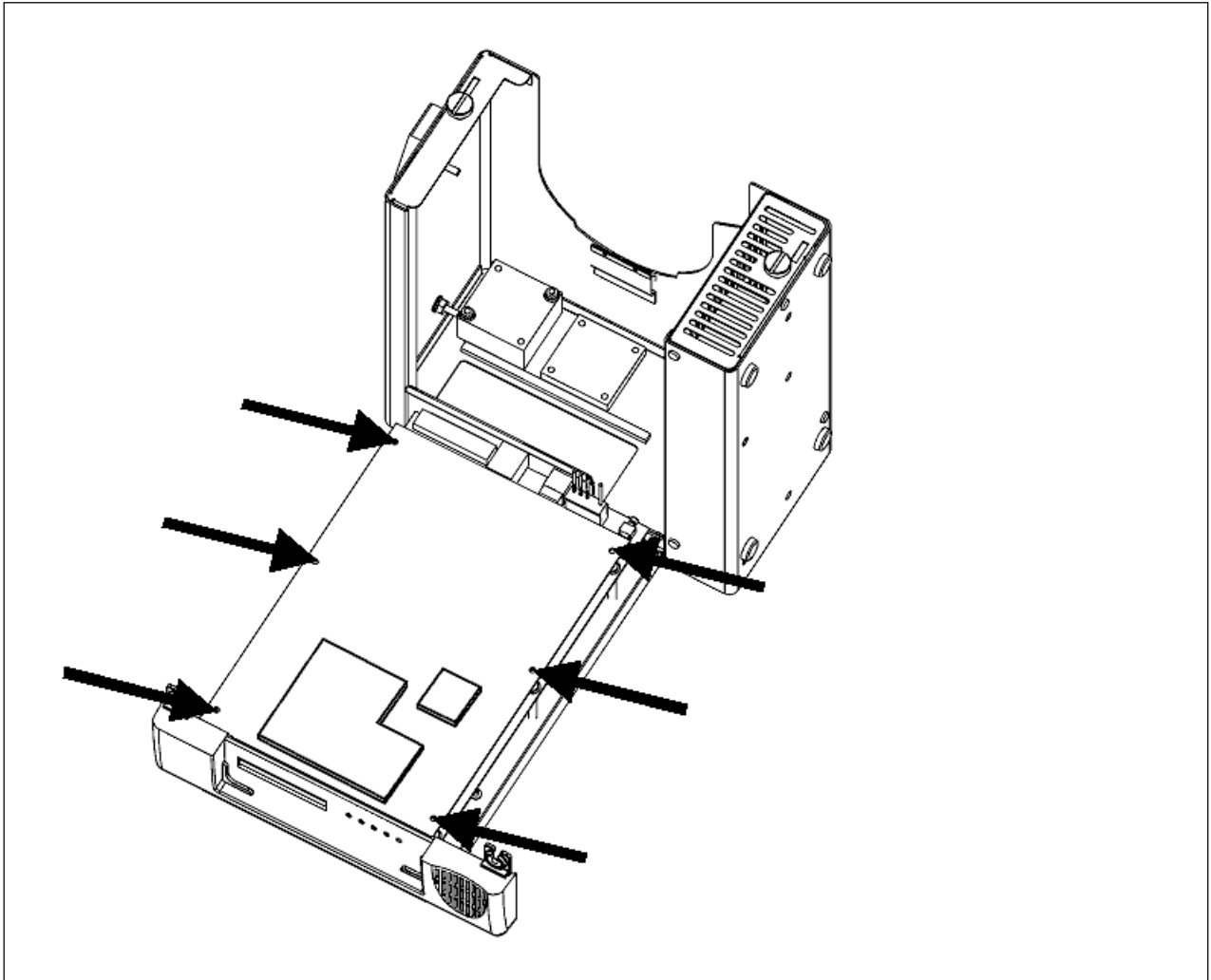
- <5> Holding front cover 2 down, lift the case using the hinges that connect front cover 2 to the rear panel of the case until the case stands vertically.

Figure 4-4. Opening/Closing Cover Step 2 (Lifting Front Cover 2)



<6> Remove the 6 screws on the board indicated by the arrows, and replace the board.

Figure 4-5. Opening/Closing Cover Step 2 (After Lifting Front Cover 2)



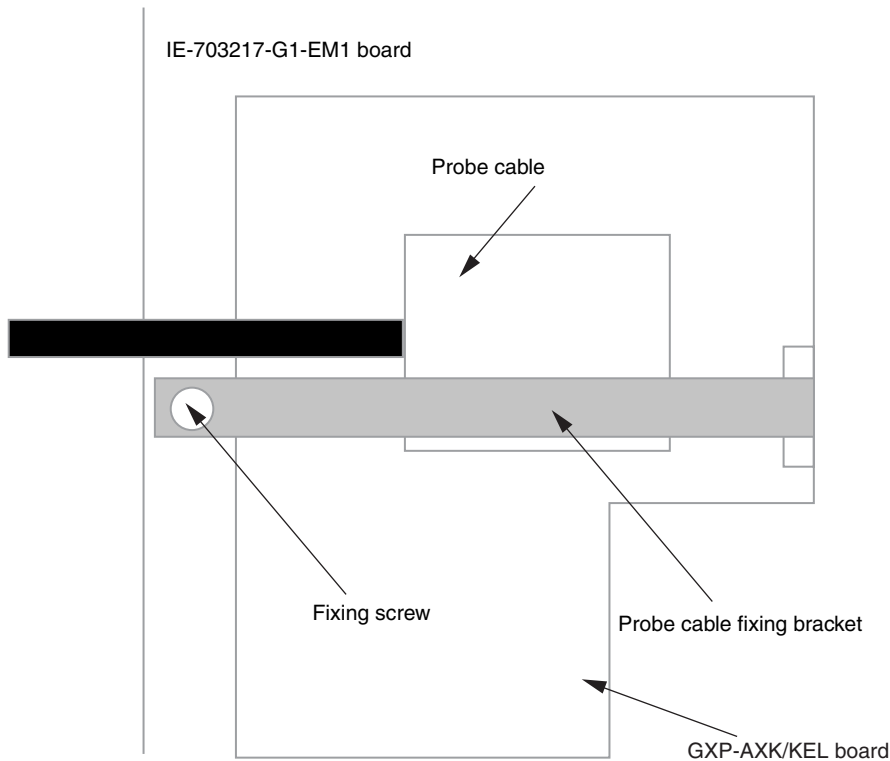
4.3 Probe Cable Connection

The probe cable is connected to the IE-703217-G1-EM1 at shipment. To remove the probe cable, use the following procedure.

(1) To remove the probe cable

- <1> Remove front cover 1 of the case.
- <2> Remove the fixing screws from the EM1 board.
- <3> Remove the probe cable fixing bracket. Proceed with caution when doing so as one end of the probe cable fixing bracket covers the probe cable positioning mark.
- <4> Remove the probe cable.
- <5> Close front cover 1 of the case.

Figure 4-6. Probe Cable Attachment Position



(2) To connect the probe cable

- <1> Remove front cover 1 from the case.
- <2> Insert the probe cable in the socket on the EM1 board.
- <3> Connect the probe cable fixing bracket so that one end covers the probe cable positioning mark.
- <4> Tighten the fixing screw.
- <5> Close front cover 1 of the case.

CHAPTER 5 CAUTIONS

The following cautions apply to the IE-703217-G1-EM1.

- Target system connection

Before connecting the IE-703217-G1-EM1 and the target system, be sure to set the power supply switch of the IE-V850ES-G1 to OFF.

- V850ES/KF1 emulation

To perform V850ES/KF1 emulation with the target board unconnected, do so after connecting the conversion adapter (GEA) supplied with the EV-703210GK or EV-703210GC to the probe cable.

If emulation is performed without connecting a conversion adapter, the fixed bit values of the following ports become undefined.

Bits 6 and 7 of port 3

Bits 2, 3, 4, 5, 10, 11, and 12 of port 9

CHAPTER 6 RESTRICTIONS

The following restrictions apply to the IE-703217-G1-EM1.

Permanent restrictions

(1) Clock generator

- Emulation of oscillation stabilization time after reset release
An oscillation stabilization time is inserted after reset release for the emulation target device, but no oscillation stabilization time is inserted in the in-circuit emulator.
- Operating clock after reset
The operating clock after reset is $f_{xx}/8$ in the emulation target device, but in the in-circuit emulator, there may be a period during which the operating clock is not initialized to $f_{xx}/8$. (This depends on the timing after reset release.)

(2) Standby mode set/release timing

The standby mode set/release timing differs in the target device and the in-circuit emulator.

When the standby mode is set, the timing difference is 1 clock or less, and when it is released, the difference is 2 to 3 clocks.

(3) Timing of reset via watchdog timer

The reset timing using WDT1, WDT2 overflow differs for the target device and the in-circuit emulator.

- Operation during break

Since various peripheral functions operate even during breaks in the in-circuit emulator, differences in the operations of the in-circuit emulator and the target device may occur.

(However, the watchdog timer counter stops during an in-circuit emulator break.)

APPENDIX A TARGET INTERFACE CHARACTERISTICS

From a functional aspect, the target interface (signals that connect the in-circuit emulator and target system) appears to operate as if an actual device were connected, but there may be differences with the actual device from a performance aspect. The target interface of this product can be any one of the interfaces described in Figures A-1 to A-10. The processing of the target interface for each target device is described in Tables A-1 to A-3.

Figure A-1. Equivalent Circuit A

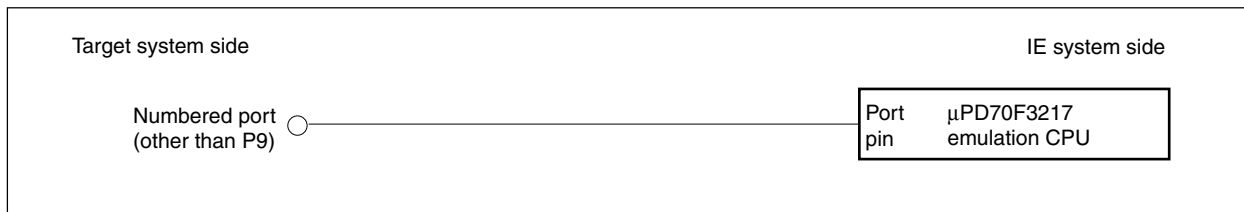


Figure A-2. Equivalent Circuit B

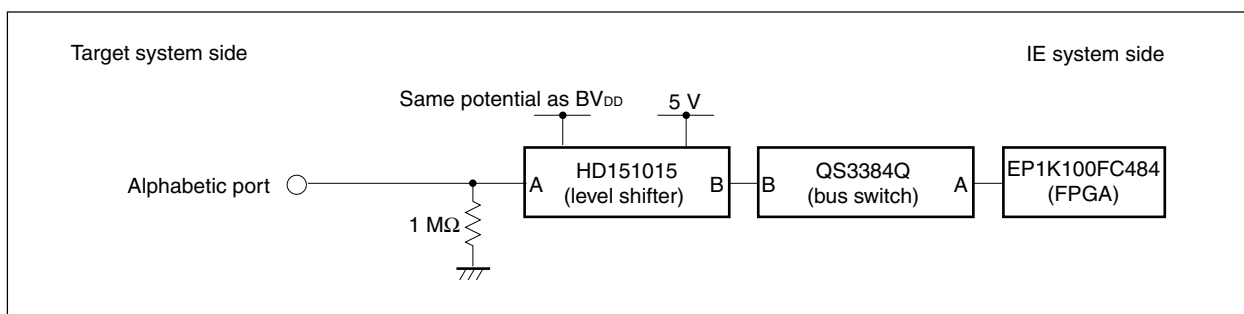


Figure A-3. Equivalent Circuit C

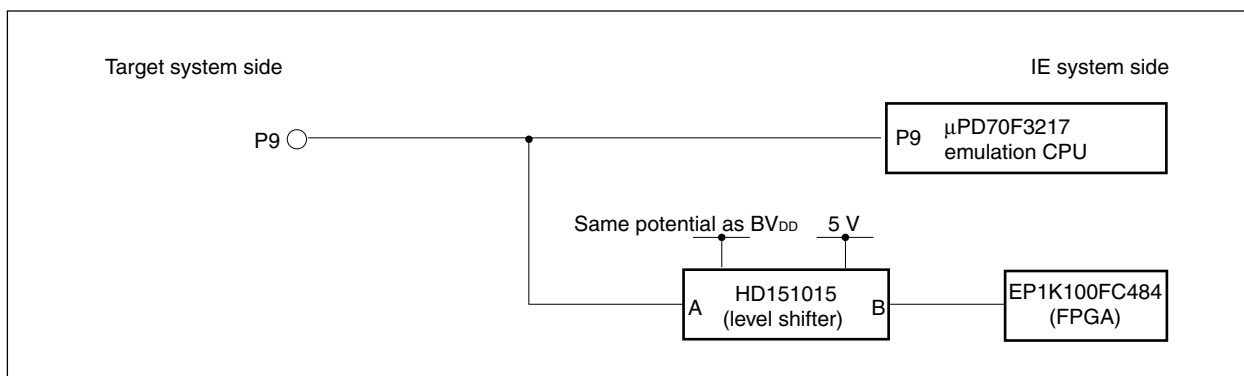
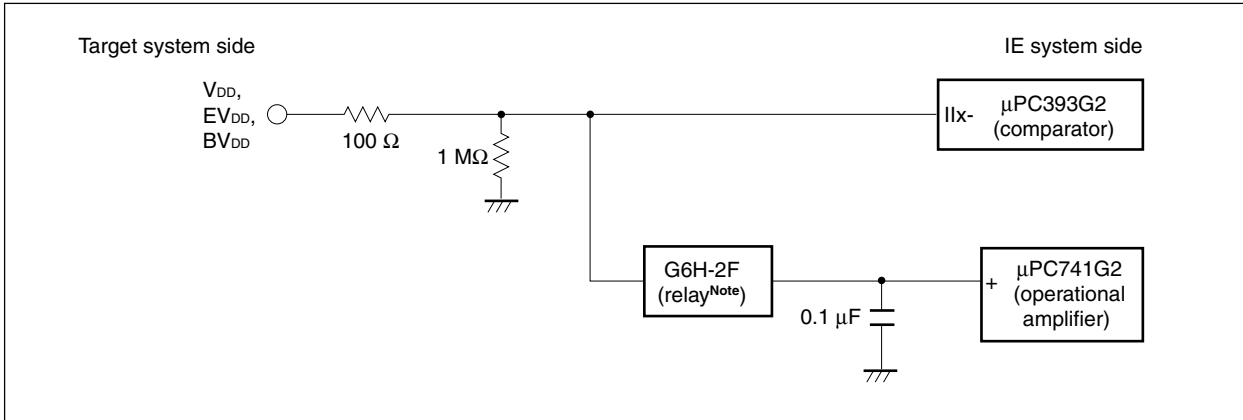
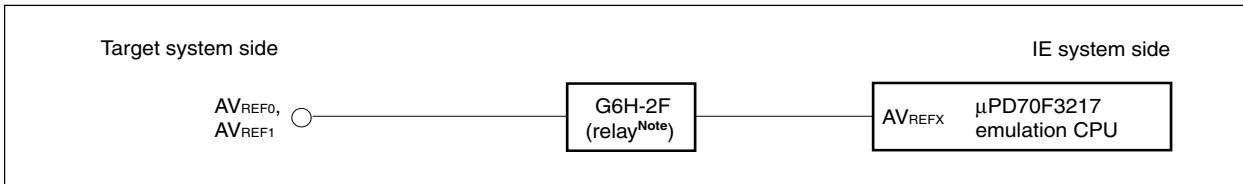


Figure A-4. Equivalent Circuit D



Note Conducts only when a target system is connected.

Figure A-5. Equivalent Circuit E



Note Conducts only when a target system is connected.

Figure A-6. Equivalent Circuit F

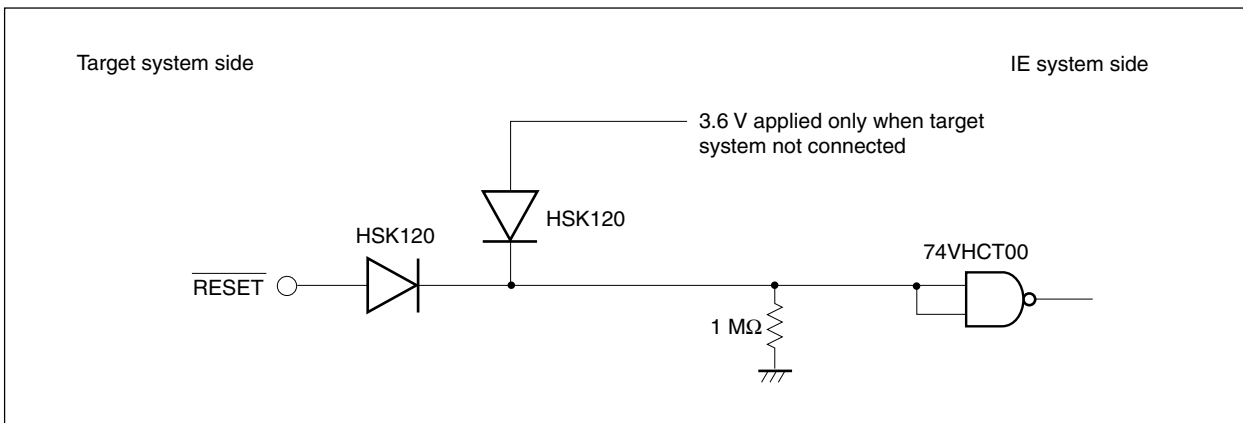


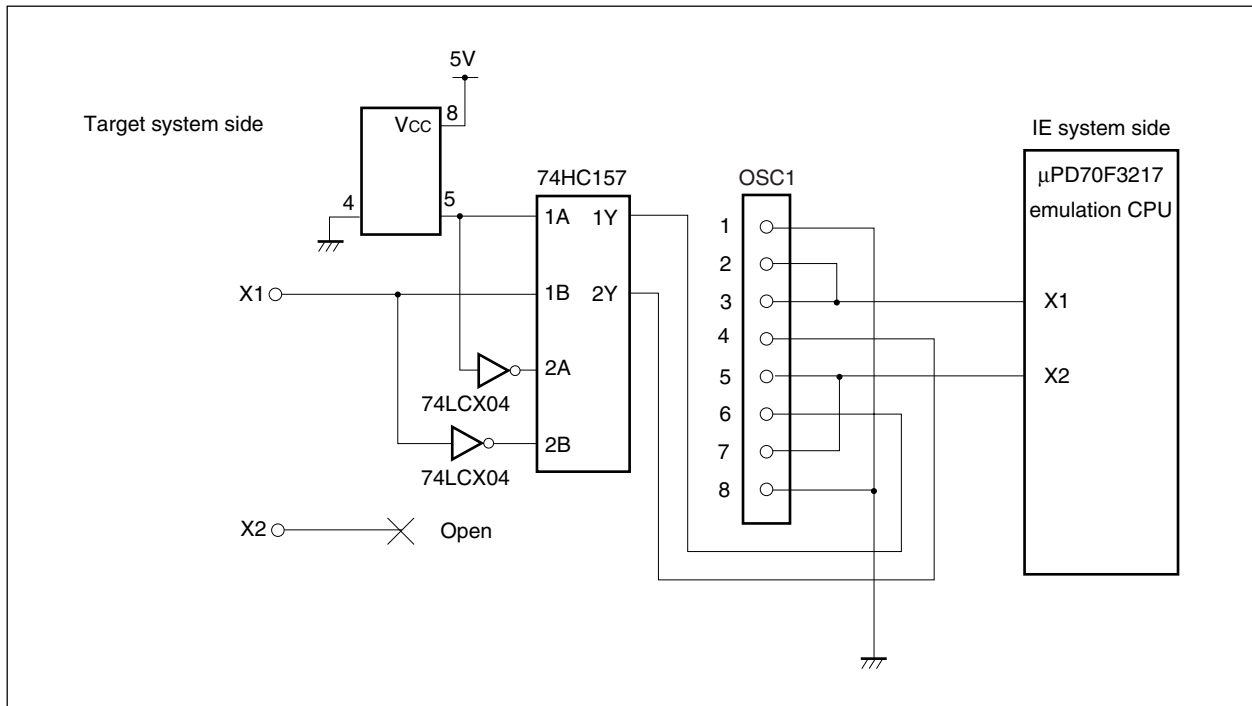
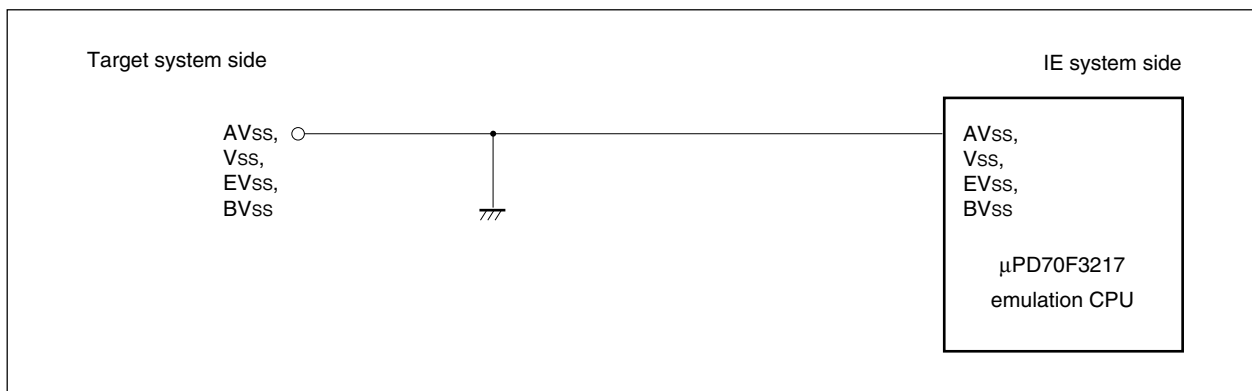
Figure A-7. Equivalent Circuit G**Figure A-8. Equivalent Circuit H**

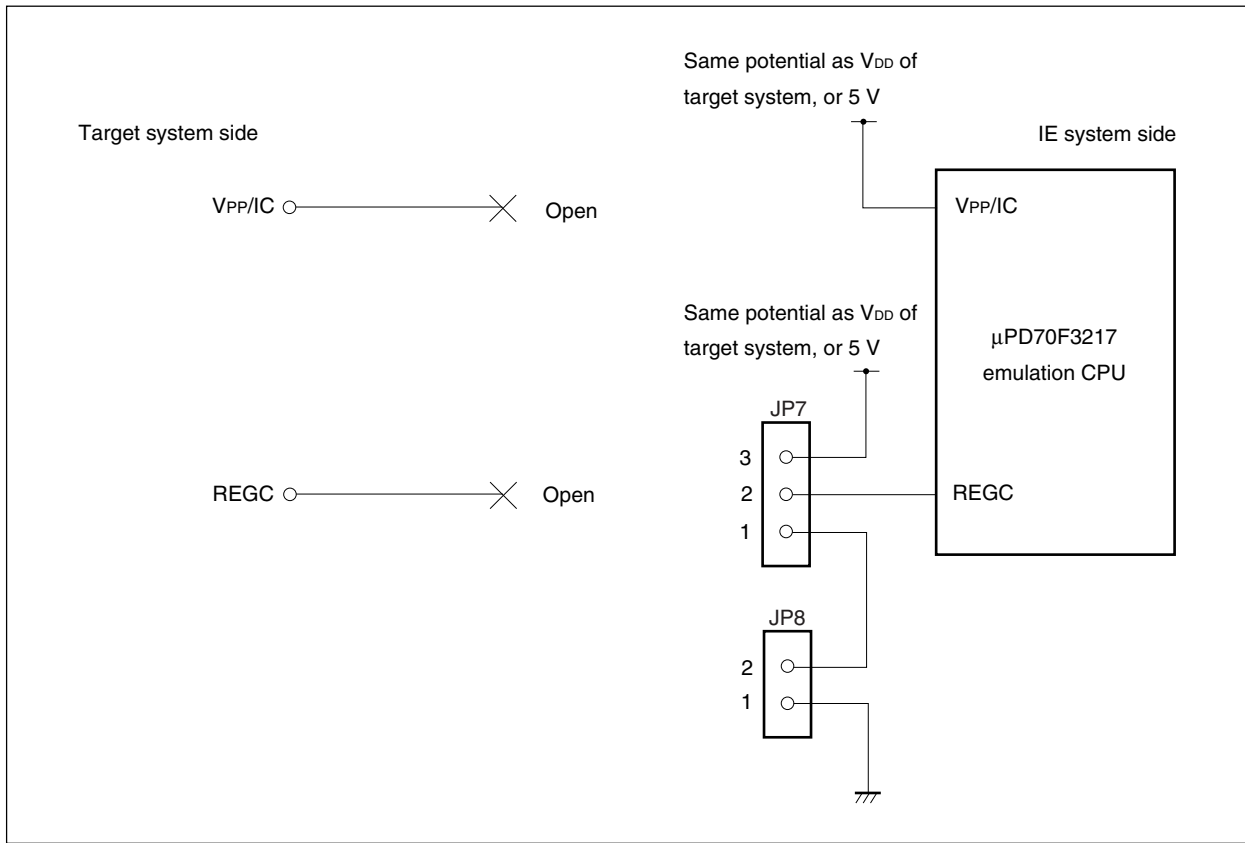
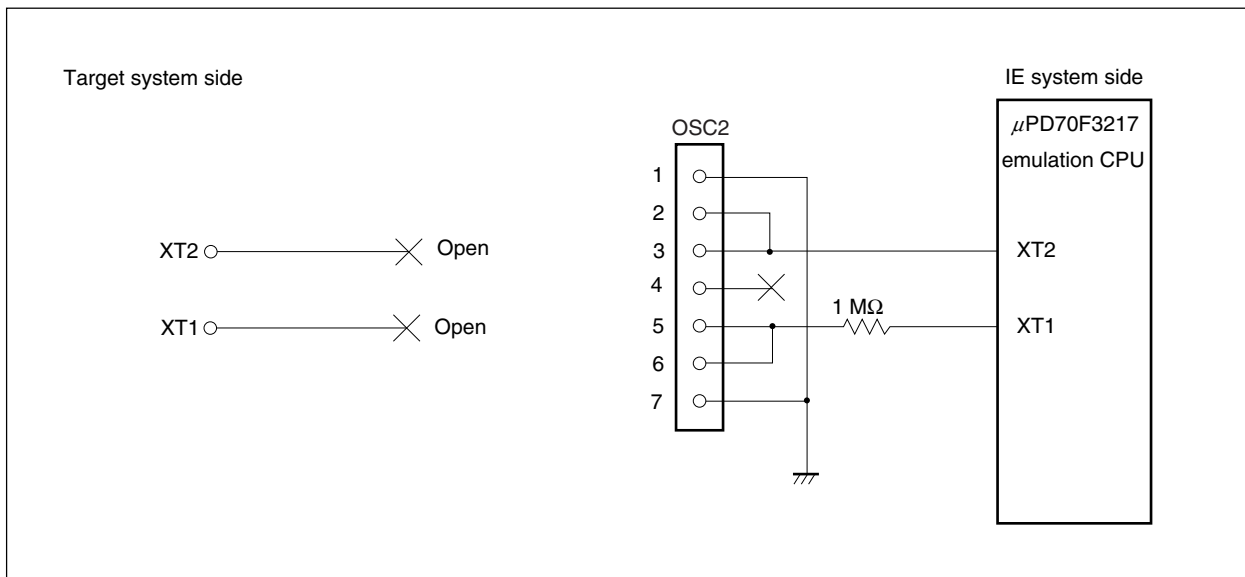
Figure A-9. Equivalent Circuit I**Figure A-10. Equivalent Circuit J**

Table A-1. Pin Correspondence List (V850ES/KJ1 Pin Names) (1/4)

V850ES/KJ1 Pin No.	Target Interface Name (V850ES/KJ1 Pin Name)	In-Circuit Emulator Processing
1	AV _{REF0}	Equivalent circuit E
2	AV _{SS}	Equivalent circuit H
3	P10/ANO0	Equivalent circuit A
4	P11/ANO1	Equivalent circuit A
5	AV _{REF1}	Equivalent circuit E
6	P00/TOH0	Equivalent circuit A
7	P01/TOH1	Equivalent circuit A
8	V _{PP} /IC	Equivalent circuit I
9	V _{DD}	Equivalent circuit D
10	REGC	Equivalent circuit I
11	V _{SS}	Equivalent circuit H
12	X1	Equivalent circuit G
13	X2	Equivalent circuit G
14	$\overline{\text{RESET}}$	Equivalent circuit F
15	XT1	Equivalent circuit J
16	XT2	Equivalent circuit J
17	P02/NMI	Equivalent circuit A
18	P03/INTP0	Equivalent circuit A
19	P04/INTP1	Equivalent circuit A
20	P05/INTP2	Equivalent circuit A
21	P06/INTP3	Equivalent circuit A
22	P40/SI00	Equivalent circuit A
23	P41/SO00	Equivalent circuit A
24	P42/SCK00	Equivalent circuit A
25	P30/TXD0	Equivalent circuit A
26	P31/RXD0	Equivalent circuit A
27	P32/ASCK0	Equivalent circuit A
28	P33/TI000/TO00	Equivalent circuit A
29	P34/TI001	Equivalent circuit A
30	P35/TI010/TO01	Equivalent circuit A
31	P36	Equivalent circuit A
32	P37	Equivalent circuit A
33	EV _{SS}	Equivalent circuit H
34	EV _{DD}	Equivalent circuit D
35	P38/SDA0	Equivalent circuit A
36	P39/SCL0	Equivalent circuit A
37	P50/TI011/RTP00/KR0	Equivalent circuit A
38	P51/TI50/RTP01/KR1	Equivalent circuit A
39	P52/TO50/RTP02/KR2	Equivalent circuit A
40	P53/SIA0/RTP03/KR3	Equivalent circuit A

Table A-1. Pin Correspondence List (V850ES/KJ1 Pin Names) (2/4)

V850ES/KJ1 Pin No.	Target Interface Name (V850ES/KJ1 Pin Name)	In-Circuit Emulator Processing
41	P54/SOA0/RTP04/KR4	Equivalent circuit A
42	P55/SCKA0/RTP05/KR5	Equivalent circuit A
43	P60/RTP10	Equivalent circuit A
44	P61/RTP11	Equivalent circuit A
45	P62/RTP12	Equivalent circuit A
46	P63/RTP13	Equivalent circuit A
47	P64/RTP14	Equivalent circuit A
48	P65/RTP15	Equivalent circuit A
49	P66/SI02	Equivalent circuit A
50	P67/SO02	Equivalent circuit A
51	P68/SCK02	Equivalent circuit A
52	P69/TI040	Equivalent circuit A
53	P610/TI041	Equivalent circuit A
54	P611/TO04	Equivalent circuit A
55	P612/TI050	Equivalent circuit A
56	P613/TI051/TO05	Equivalent circuit A
57	P614	Equivalent circuit A
58	P615	Equivalent circuit A
59	P80/RXD2/SDA1	Equivalent circuit A
60	P81/TXD2/SCL1	Equivalent circuit A
61	P90/A0/TXD1/KR6	Equivalent circuit C
62	P91/A1/RXD1/KR7	Equivalent circuit C
63	P92/A2/TI020/TO02	Equivalent circuit C
64	P93/A3/TI021	Equivalent circuit C
65	P94/A4/TI030/TO03	Equivalent circuit C
66	P95/A5/TI031	Equivalent circuit C
67	P96/A6/TI51/TO51	Equivalent circuit C
68	P97/A7/SI01	Equivalent circuit C
69	P98/A8/SO01	Equivalent circuit C
70	P99/A9/SCK01	Equivalent circuit C
71	P910/A10/SIA1	Equivalent circuit C
72	P911/A11/SOA1	Equivalent circuit C
73	P912/A12/SCKA1	Equivalent circuit C
74	P913/A13/INTP4	Equivalent circuit C
75	P914/A14/INTP5	Equivalent circuit C
76	P915/A15/INTP6	Equivalent circuit C
77	PCD0	Equivalent circuit B
78	PCD1	Equivalent circuit B
79	PCD2	Equivalent circuit B
80	PCD3	Equivalent circuit B

Table A-1. Pin Correspondence List (V850ES/KJ1 Pin Names) (3/4)

V850ES/KJ1 Pin No.	Target Interface Name (V850ES/KJ1 Pin Name)	In-Circuit Emulator Processing
81	PCS0/ $\overline{\text{CS0}}$	Equivalent circuit B
82	PCS1/ $\overline{\text{CS1}}$	Equivalent circuit B
83	PCS2/ $\overline{\text{CS2}}$	Equivalent circuit B
84	PCS3/ $\overline{\text{CS3}}$	Equivalent circuit B
85	PCM0/ $\overline{\text{WAIT}}$	Equivalent circuit B
86	PCM1/ $\overline{\text{CLKOUT}}$	Equivalent circuit B
87	PCM2/ $\overline{\text{HLDK}}$	Equivalent circuit B
88	PCM3/ $\overline{\text{HLDRQ}}$	Equivalent circuit B
89	PCM4	Equivalent circuit B
90	PCM5	Equivalent circuit B
91	PCS4	Equivalent circuit B
92	PCS5	Equivalent circuit B
93	PCS6	Equivalent circuit B
94	PCS7	Equivalent circuit B
95	PCT0/ $\overline{\text{WR0}}$	Equivalent circuit B
96	PCT1/ $\overline{\text{WR1}}$	Equivalent circuit B
97	PCT2	Equivalent circuit B
98	PCT3	Equivalent circuit B
99	PCT4/ $\overline{\text{RD}}$	Equivalent circuit B
100	PCT5	Equivalent circuit B
101	PCT6/ $\overline{\text{ASTB}}$	Equivalent circuit B
102	PCT7	Equivalent circuit B
103	BV _{SS}	Equivalent circuit H
104	BV _{DD}	Equivalent circuit D
105	PDL0/AD0	Equivalent circuit B
106	PDL1/AD1	Equivalent circuit B
107	PDL2/AD2	Equivalent circuit B
108	PDL3/AD3	Equivalent circuit B
109	PDL4/AD4	Equivalent circuit B
110	PDL5/AD5	Equivalent circuit B
111	PDL6/AD6	Equivalent circuit B
112	PDL7/AD7	Equivalent circuit B
113	PDL8/AD8	Equivalent circuit B
114	PDL9/AD9	Equivalent circuit B
115	PDL10/AD10	Equivalent circuit B
116	PDL11/AD11	Equivalent circuit B
117	PDL12/AD12	Equivalent circuit B
118	PDL13/AD13	Equivalent circuit B
119	PDL14/AD14	Equivalent circuit B
120	PDL15/AD15	Equivalent circuit B

Table A-1. Pin Correspondence List (V850ES/KJ1 Pin Names) (4/4)

V850ES/KJ1 Pin No.	Target Interface Name (V850ES/KJ1 Pin Name)	In-Circuit Emulator Processing
121	PDH0/A16	Equivalent circuit B
122	PDH1/A17	Equivalent circuit B
123	PDH2/A18	Equivalent circuit B
124	PDH3/A19	Equivalent circuit B
125	PDH4/A20	Equivalent circuit B
126	PDH5/A21	Equivalent circuit B
127	PDH6/A22	Equivalent circuit B
128	PDH7/A23	Equivalent circuit B
129	P715/ANI15	Equivalent circuit A
130	P714/ANI14	Equivalent circuit A
131	P713/ANI13	Equivalent circuit A
132	P712/ANI12	Equivalent circuit A
133	P711/ANI11	Equivalent circuit A
134	P710/ANI10	Equivalent circuit A
135	P79/ANI9	Equivalent circuit A
136	P78/ANI8	Equivalent circuit A
137	P77/ANI7	Equivalent circuit A
138	P76/ANI6	Equivalent circuit A
139	P75/ANI5	Equivalent circuit A
140	P74/ANI4	Equivalent circuit A
141	P73/ANI3	Equivalent circuit A
142	P72/ANI2	Equivalent circuit A
143	P71/ANI1	Equivalent circuit A
144	P70/ANI0	Equivalent circuit A

Table A-2. Pin Correspondence List (V850ES/KG1 Pin Names) (1/3)

V850ES/KG1 Pin No.	Target Interface Name (V850ES/KG1 Pin Name)	In-Circuit Emulator Processing
1	AV _{REF0}	Equivalent circuit E
2	AV _{SS}	Equivalent circuit H
3	P10/ANO0	Equivalent circuit A
4	P11/ANO1	Equivalent circuit A
5	AV _{REF1}	Equivalent circuit E
6	P00/TOH0	Equivalent circuit A
7	P01/TOH1	Equivalent circuit A
8	V _{PP} /IC	Equivalent circuit I
9	V _{DD}	Equivalent circuit D
10	REGC	Equivalent circuit I
11	V _{SS}	Equivalent circuit H
12	X1	Equivalent circuit G
13	X2	Equivalent circuit G
14	RESET	Equivalent circuit F
15	XT1	Equivalent circuit J
16	XT2	Equivalent circuit J
17	P02/NMI	Equivalent circuit A
18	P03/INTP0	Equivalent circuit A
19	P04/INTP1	Equivalent circuit A
20	P05/INTP2	Equivalent circuit A
21	P06/INTP3	Equivalent circuit A
22	P40/SI00	Equivalent circuit A
23	P41/SO00	Equivalent circuit A
24	P42/SCK00	Equivalent circuit A
25	P30/TXD0	Equivalent circuit A
26	P31/RXD0	Equivalent circuit A
27	P32/ASCK0	Equivalent circuit A
28	P33/TI000/TO00	Equivalent circuit A
29	P34/TI001	Equivalent circuit A
30	P35/TI010/TO01	Equivalent circuit A
31	P36	Equivalent circuit A
32	P37	Equivalent circuit A
33	EV _{SS}	Equivalent circuit H
34	EV _{DD}	Equivalent circuit D
35	P38/SDA0	Equivalent circuit A
36	P39/SCL0	Equivalent circuit A
37	P50/TI011/RTP00/KR0	Equivalent circuit A
38	P51/TI50/RTP01/KR1	Equivalent circuit A
39	P52/TO50/RTP02/KR2	Equivalent circuit A
40	P53/SIA0/RTP03/KR3	Equivalent circuit A

Table A-2. Pin Correspondence List (V850ES/KG1 Pin Names) (2/3)

V850ES/KG1 Pin No.	Target Interface Name (V850ES/KG1 Pin Name)	In-Circuit Emulator Processing
41	P54/SOA0/RTP04/KR4	Equivalent circuit A
42	P55/SCKA0/RTP05/KR5	Equivalent circuit A
43	P90/A0/TXD1/KR6	Equivalent circuit C
44	P91/A1/RXD1/KR7	Equivalent circuit C
45	P92/A2/TI020/TO02	Equivalent circuit C
46	P93/A3/TI021	Equivalent circuit C
47	P94/A4/TI030/TO03	Equivalent circuit C
48	P95/A5/TI031	Equivalent circuit C
49	P96/A6/TI51/TO51	Equivalent circuit C
50	P97/A7/SI01	Equivalent circuit C
51	P98/A8/SO01	Equivalent circuit C
52	P99/A9/SCK01	Equivalent circuit C
53	P910/A10/SIA1	Equivalent circuit C
54	P911/A11/SOA1	Equivalent circuit C
55	P912/A12/SCKA1	Equivalent circuit C
56	P913/A13/INTP4	Equivalent circuit C
57	P914/A14/INTP5	Equivalent circuit C
58	P915/A15/INTP6	Equivalent circuit C
59	PCS0/CS0	Equivalent circuit B
60	PCS1/CS1	Equivalent circuit B
61	PCM0/WAIT	Equivalent circuit B
62	PCM1/CLKOUT	Equivalent circuit B
63	PCM2/HLDAK	Equivalent circuit B
64	PCM3/HLDRQ	Equivalent circuit B
65	PCT0/WR0	Equivalent circuit B
66	PCT1/WR1	Equivalent circuit B
67	PCT4/RD	Equivalent circuit B
68	PCT6/ASTB	Equivalent circuit B
69	BV _{SS}	Equivalent circuit H
70	BV _{DD}	Equivalent circuit D
71	PDL0/AD0	Equivalent circuit B
72	PDL1/AD1	Equivalent circuit B
73	PDL2/AD2	Equivalent circuit B
74	PDL3/AD3	Equivalent circuit B
75	PDL4/AD4	Equivalent circuit B
76	PDL5/AD5	Equivalent circuit B
77	PDL6/AD6	Equivalent circuit B
78	PDL7/AD7	Equivalent circuit B
79	PDL8/AD8	Equivalent circuit B
80	PDL9/AD9	Equivalent circuit B

Table A-2. Pin Correspondence List (V850ES/KG1 Pin Names) (3/3)

V850ES/KG1 Pin No.	Target Interface Name (V850ES/KG1 Pin Name)	In-Circuit Emulator Processing
81	PDL10/AD10	Equivalent circuit B
82	PDL11/AD11	Equivalent circuit B
83	PDL12/AD12	Equivalent circuit B
84	PDL13/AD13	Equivalent circuit B
85	PDL14/AD14	Equivalent circuit B
86	PDL15/AD15	Equivalent circuit B
87	PDH0/A16	Equivalent circuit B
88	PDH1/A17	Equivalent circuit B
89	PDH2/A18	Equivalent circuit B
90	PDH3/A19	Equivalent circuit B
91	PDH4/A20	Equivalent circuit B
92	PDH5/A21	Equivalent circuit B
93	P77/ANI7	Equivalent circuit A
94	P76/ANI6	Equivalent circuit A
95	P75/ANI5	Equivalent circuit A
96	P74/ANI4	Equivalent circuit A
97	P73/ANI3	Equivalent circuit A
98	P72/ANI2	Equivalent circuit A
99	P71/ANI1	Equivalent circuit A
100	P70/ANI0	Equivalent circuit A

Table A-3. Pin Correspondence List (V850ES/KF1 Pin Names) (1/2)

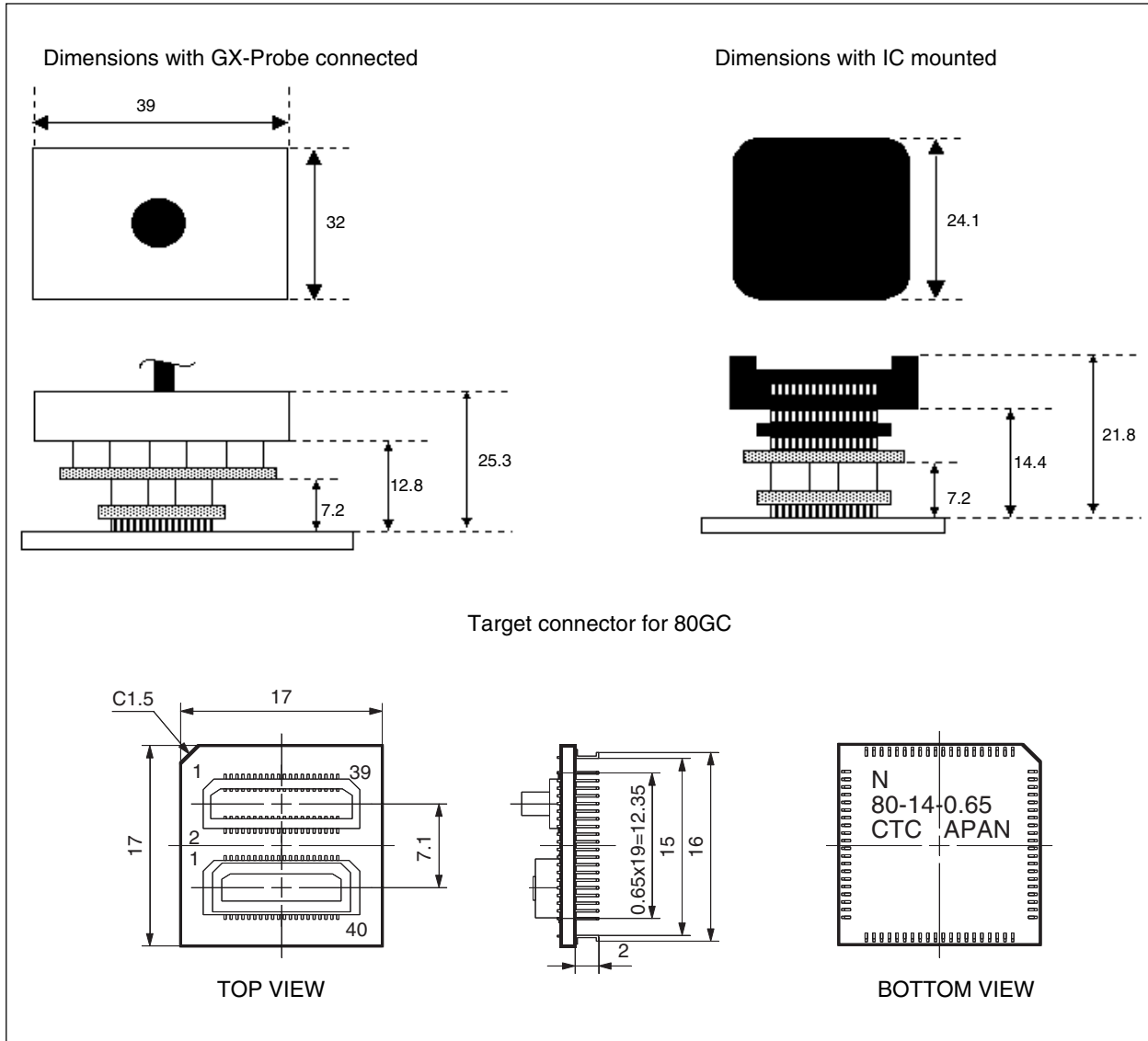
V850ES/KF1 Pin No.	Target Interface Name (V850ES/KF1 Pin Name)	In-Circuit Emulator Processing
1	AV _{REF0}	Equivalent circuit E
2	AV _{SS}	Equivalent circuit H
3	P00/TOH0	Equivalent circuit A
4	P01/TOH1	Equivalent circuit A
5	P02/NMI	Equivalent circuit A
6	P03/INTP0	Equivalent circuit A
7	P04/INTP1	Equivalent circuit A
8	V _{PP} /IC	Equivalent circuit I
9	V _{DD}	Equivalent circuit D
10	REGC	Equivalent circuit I
11	V _{SS}	Equivalent circuit H
12	X1	Equivalent circuit G
13	X2	Equivalent circuit G
14	RESET	Equivalent circuit F
15	XT1	Equivalent circuit J
16	XT2	Equivalent circuit J
17	P05/INTP2	Equivalent circuit A
18	P06/INTP3	Equivalent circuit A
19	P40/SI00	Equivalent circuit A
20	P41/SO00	Equivalent circuit A
21	P42/SCK00	Equivalent circuit A
22	P30/TXD0	Equivalent circuit A
23	P31/RXD0	Equivalent circuit A
24	P32/ASCK0	Equivalent circuit A
25	P33/TI000/TO00	Equivalent circuit A
26	P34/TI001	Equivalent circuit A
27	P35/TI010/TO01	Equivalent circuit A
28	P38/SDA0	Equivalent circuit A
29	P39/SCL0	Equivalent circuit A
30	EV _{SS}	Equivalent circuit H
31	EV _{DD}	Equivalent circuit D
32	P50/TI011/RTP00/KR0	Equivalent circuit A
33	P51/TI50/RTP01/KR1	Equivalent circuit A
34	P52/TO50/RTP02/KR2	Equivalent circuit A
35	P53/SIA0/RTP03/KR3	Equivalent circuit A
36	P54/SOA0/RTP04/KR4	Equivalent circuit A
37	P55/SCKA0/RTP05/KR5	Equivalent circuit A
38	P90/A0/TXD1/KR6	Equivalent circuit C
39	P91/A1/RXD1/KR7	Equivalent circuit C
40	P96/A6/TI51/TO51	Equivalent circuit C

Table A-3. Pin Correspondence List (V850ES/KF1 Pin Names) (2/2)

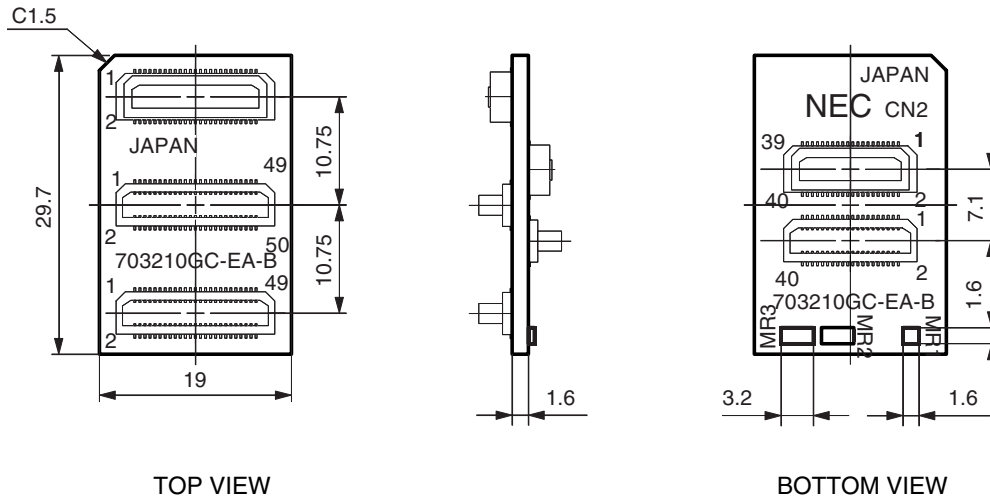
V850ES/KF1 Pin No.	Target Interface Name (V850ES/KF1 Pin Name)	In-Circuit Emulator Processing
41	P97/A7/SI01	Equivalent circuit C
42	P98/A8/SO01	Equivalent circuit C
43	P99/A9/SCK01	Equivalent circuit C
44	P913/A13/INTP4	Equivalent circuit C
45	P914/A14/INTP5	Equivalent circuit C
46	P915/A15/INTP6	Equivalent circuit C
47	PCS0/CS0	Equivalent circuit B
48	PCS1/CS1	Equivalent circuit B
49	PCM0/WAIT	Equivalent circuit B
50	PCM1/CLKOUT	Equivalent circuit B
51	PCM2/HLDAK	Equivalent circuit B
52	PCM3/HLDRQ	Equivalent circuit B
53	PCT0/WR0	Equivalent circuit B
54	PCT1/WR1	Equivalent circuit B
55	PCT4/RD	Equivalent circuit B
56	PCT6/ASTB	Equivalent circuit B
57	PDL0/AD0	Equivalent circuit B
58	PDL1/AD1	Equivalent circuit B
59	PDL2/AD2	Equivalent circuit B
60	PDL3/AD3	Equivalent circuit B
61	PDL4/AD4	Equivalent circuit B
62	PDL5/AD5	Equivalent circuit B
63	PDL6/AD6	Equivalent circuit B
64	PDL7/AD7	Equivalent circuit B
65	PDL8/AD8	Equivalent circuit B
66	PDL9/AD9	Equivalent circuit B
67	PDL10/AD10	Equivalent circuit B
68	PDL11/AD11	Equivalent circuit B
69	PDL12/AD12	Equivalent circuit B
70	PDL13/AD13	Equivalent circuit B
71	PDL14/AD14	Equivalent circuit B
72	PDL15/AD15	Equivalent circuit B
73	P77/ANI7	Equivalent circuit A
74	P76/ANI6	Equivalent circuit A
75	P75/ANI5	Equivalent circuit A
76	P74/ANI4	Equivalent circuit A
77	P73/ANI3	Equivalent circuit A
78	P72/ANI2	Equivalent circuit A
79	P71/ANI1	Equivalent circuit A
80	P70/ANI0	Equivalent circuit A

APPENDIX B EXTERNAL VIEWS

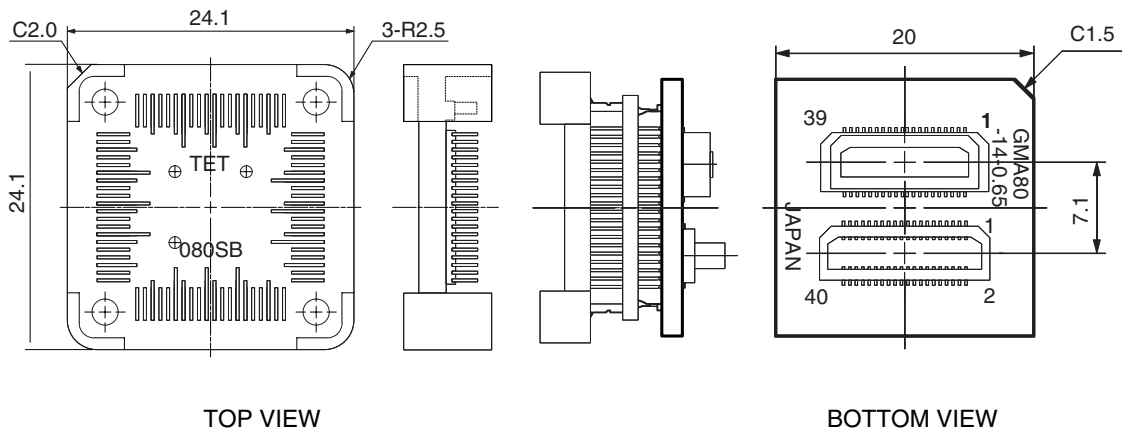
(1) EV-703210GC (for 80GC) Unit: mm



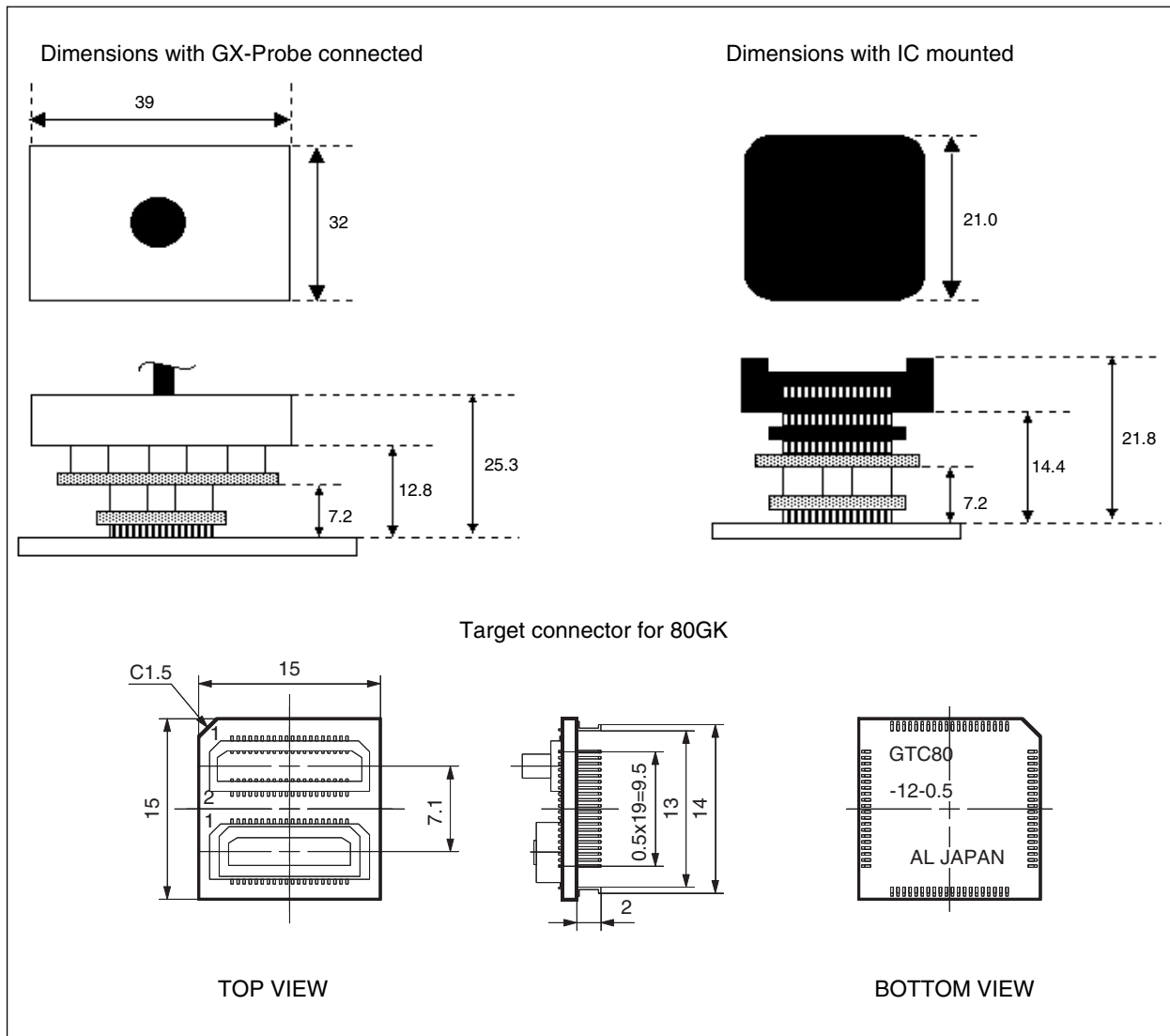
Conversion adapter for 80GC



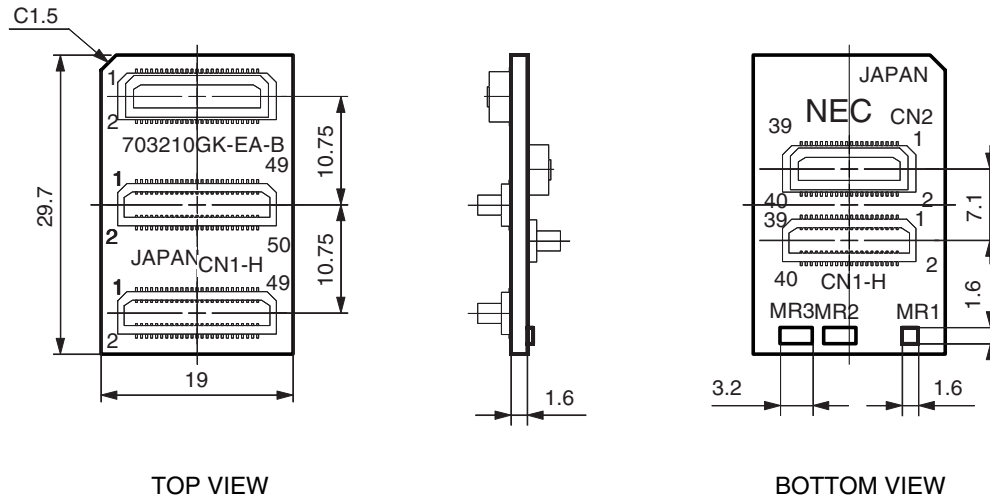
IC mounting adapter for 80GC



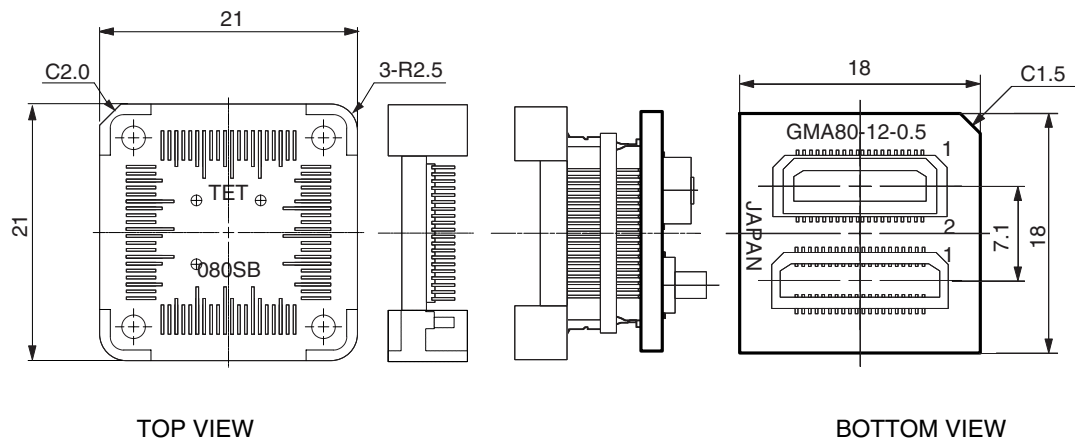
(2) EV-703210GK (for 80GK) Unit: mm



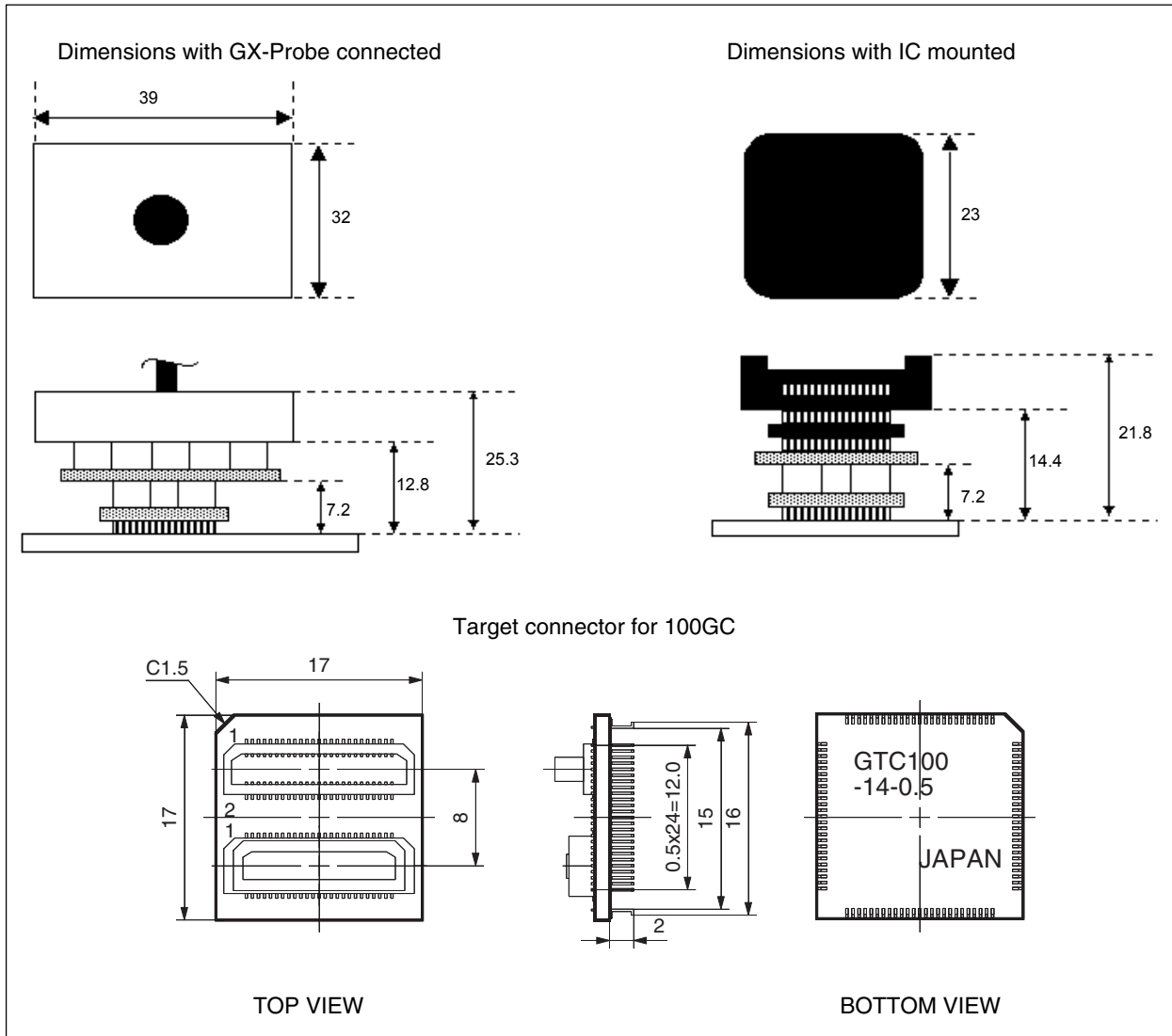
Conversion adapter for 80GK



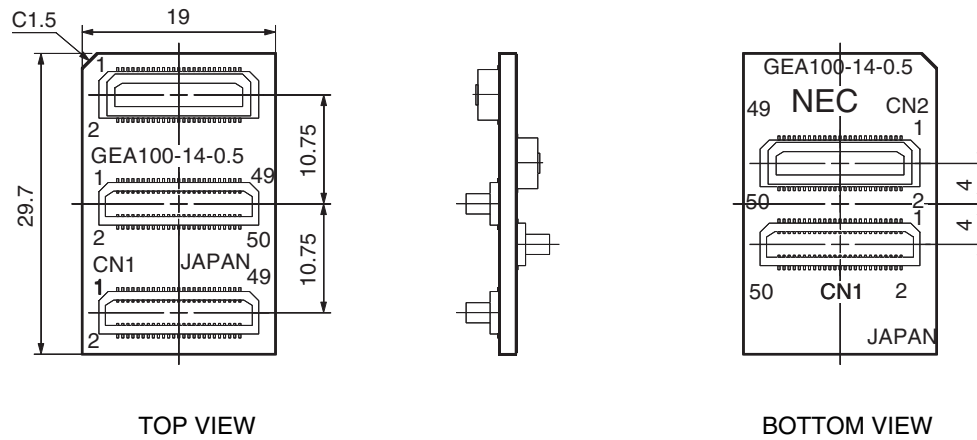
IC mounting adapter for 80GK



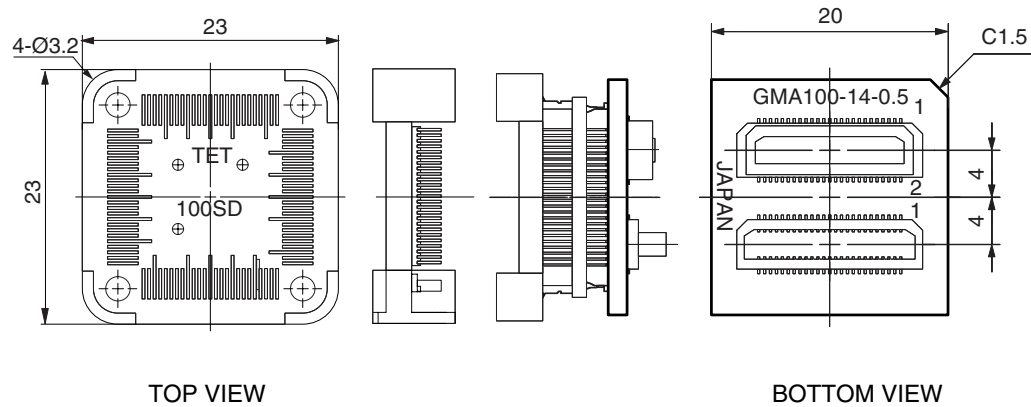
(3) EV-703214GC (for 100GC) Unit: mm



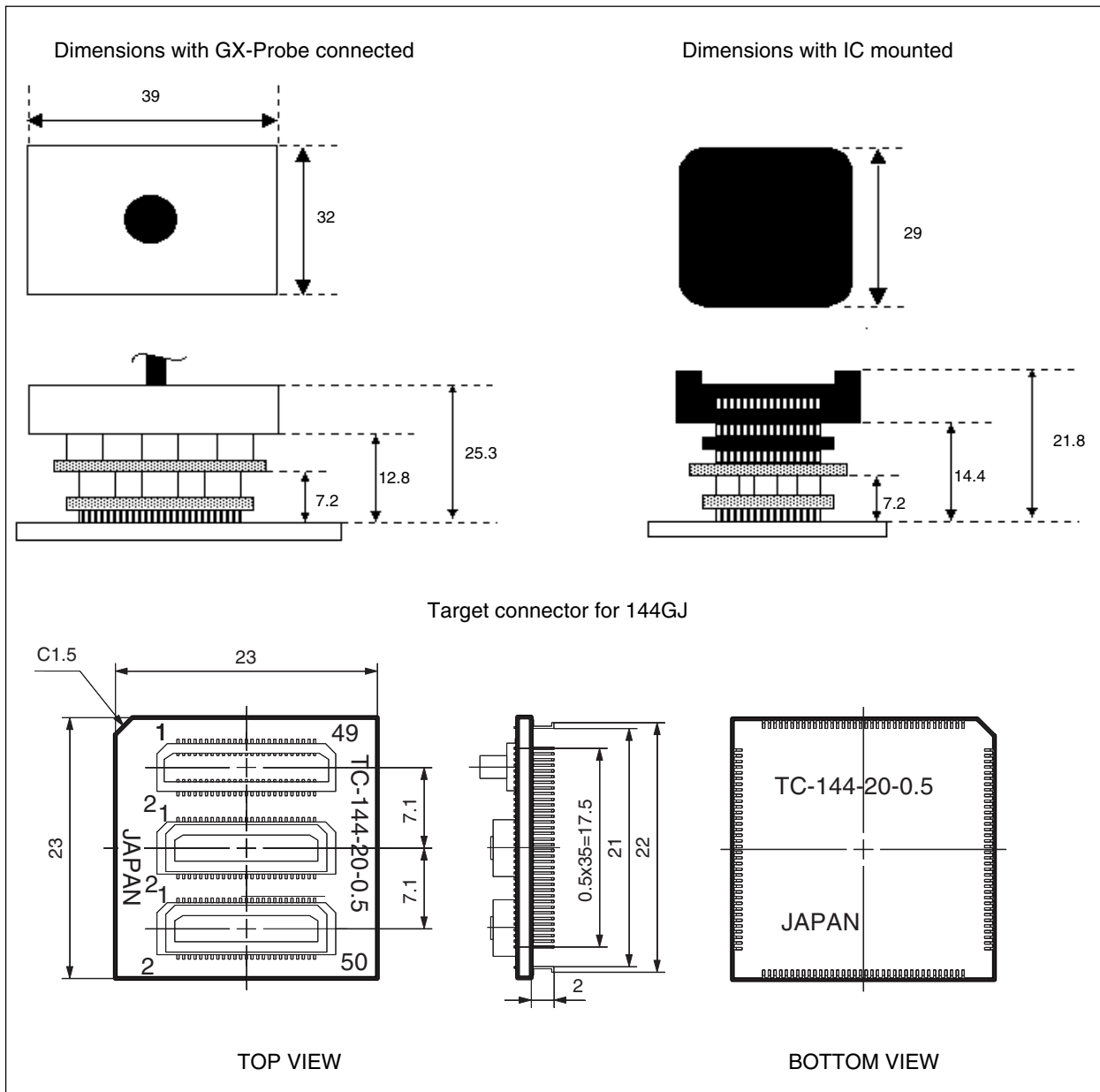
Conversion adapter for 100GC



IC mounting adapter for 100GC



(4) EV-703217GJ (for 144GJ) Unit: mm



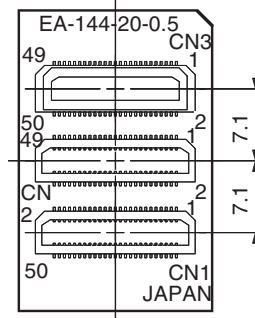
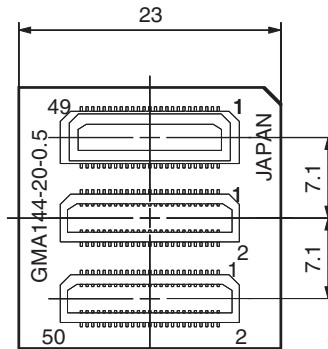


Figure 1 is a mechanical drawing of the TET 144 SD module. The drawing shows a square module with dimensions 29 mm by 29 mm. It features a central area labeled 'TET' and '144 SD'. The module has four corners with mounting holes and four sides with pins. A detail view on the right shows a cross-section of the module with a dimension of 3-R2.5 and a pin dimension of C2.0.

The diagram illustrates the experimental setup for studying the effect of pressure on the permeability of a porous medium. It consists of two main parts: a vertical column and a cross-sectional view. The vertical column on the left is composed of 100 horizontal bars, with a 'Pressure' sensor at the bottom. The cross-sectional view on the right shows the internal structure of the column, including a 'Pressure' sensor and a 'Flow' meter. The flow is indicated by arrows pointing downwards through the column.



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(5) Emulation probe cable Unit: mm