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**Preliminary User's Ma**

# **IE-703003-MC-EM1**

**IN-CIRCUIT EMULATOR OPTION BOARD**

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**Target device**  
**V853™**

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### Main Revisions in This Edition

Pages	Description
P2	CLKOUT of maskable pin is deleted in <b>1.2 Features (When connected to IE-703002-MC)</b> .
P2	Emulation Memory Capacity is modified in <b>1.3 Function Specifications (When connected to IE-703002-MC)</b> .
P3	Target Connection Socket is modified from YQSOCKET100SDF to YQSCKETSDN in <b>1.4 System Configuration</b> .
P7	Insertion guides is modified to 4 in <b>Figure 1-4. (c) Connecting part (IE-703003-MC-EM1)</b> .
P12	<b>3.3 NMI Signal</b> Addition of Description

The mark ★ shows major revised points.

[MEMO]

# INTRODUCTION

## READERS

This manual is intended for users who design and develop application systems using the V853.

## PURPOSE

The purpose of this manual is to describe the proper operation of the IE-703003-MC-EM1 and its basic specifications.

## ORGANIZATION

This manual is broadly divided into the following parts:

- Overview
- Settings of IE-703003-MC
- Cautions

## HOW TO READ THIS MANUAL

This manual assumes readers who have general knowledge of electric engineering, logic circuits, and microcomputers.

The IE-703003-MC-EM1 is used connected to the in-circuit emulator IE-703002-MC for the V851™ and V852™. This manual explains the basic setup procedure and switch settings of the IE-703002-MC when it is connected to the IE-703003-MC-EM1. For the names and functions, and the connection of parts, refer to the "IE-703002-MC User's Manual Hardware".

To learn the basic specifications and operation methods broadly

→ Read this manual in the order listed in **CONTENTS**.

To learn the operation methods and command functions, etc., of the IE-703002-MC and IE-703003-MC-EM1

→ Read the user's manual of the debugger (optional) that is used.

## LEGEND

Note	: Describe items noted in text.
Caution	: Describe points that require special attention.
Remark	: Provide supplementary remarks to description in text.
Numeral representations	: Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... 0xxxxx or xxxxH
Prefix representing the power of 2 (Address space, Memory capacity):	
K (kilo)	: $2^{10} = 1024$
M (mega)	: $2^{20} = 1024^2$



## TERMINOLOGY

The meaning of terms used in this manual is listed below.

Target device	Device that is emulated.
Target system	The system (user-built system) to be debugged. This includes the target program and user-configured hardware.

## RELATED DOCUMENTS

Some of the related documents listed below may be preliminary editions, but are not noted as such.

### ○ Documents related V853

Document	Document Number
V853 User's Manual Hardware	U10913E
μPD703003 Data Sheet	Planned
μPD70F3003 Data Sheet	Planned
V850 family™ User's Manual Architecture	U10243E
V850 family Instruction List	U10229E

### ○ Documents related to development tools

Product		Document Number
IE-703002-MC Hardware		U11595E
IE-70000-MC-SV2 (Communication module)		U11781E
IE-70000-MC-IF (Communication module adopter)		U11601E
CA850 (C Compiler package)	Operation UNIX™ based	U11013E
	Operation Windows™ based	U11068E
	C language	U11010E
	Assembly Language	U10543E
RX850 (Real-time OS)	Basics	U11037E
	Technical	U11117E
	Nucleus installation	U11038E
	Debugger Windows-based	U11158E
AZ850 (System performance analyzer) Operation		U11181E
ID850 (C source debugger)	Operation Windows-based	Planned
	Operation UNIX-based	Planned
	Installation Windows-based	Planned
	Installation UNIX-based	Planned

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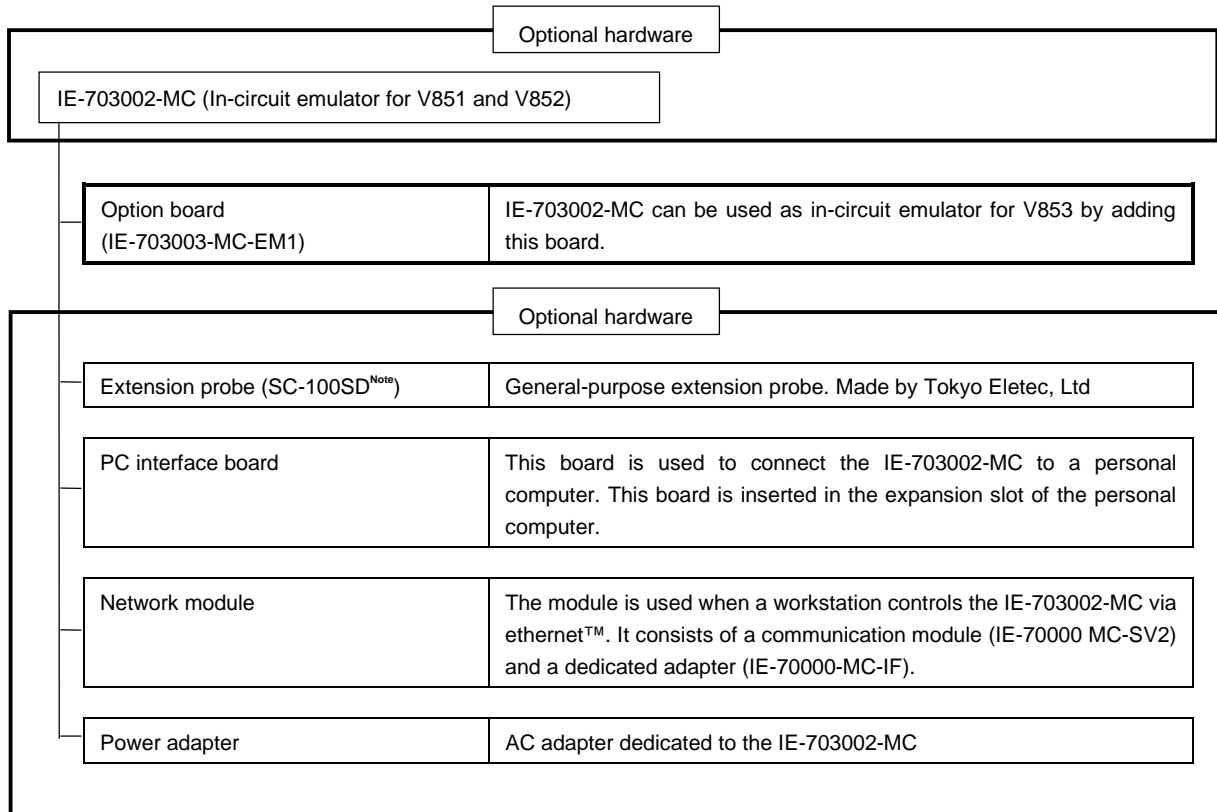
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## CHAPTER 1 OVERVIEW

The IE-703003-MC-EM1 is an optional board for the in-circuit emulator IE-703002-MC for the V851 and V852. By connecting the IE-703003-MC-EM1 and IE-703002-MC, hardware and software can be debugged efficiently in system development using the V853. In this manual, the basic setup sequences and switch settings of the IE-703003-MC are described. For the names and functions of the parts of the IE-703002-MC, and for the connection of elements, refer to the "IE-703002-MC User's Manual".

### 1.1 Hardware Configuration



**Note** Contact: Daimaru Kogyo Co., Ltd. Tokyo Electronic Components Department TEL 03-3820-7112  
Osaka Electronic Components Department TEL 06-244-6672

## 1.2 Features (When connected to IE-703002-MC)

- Maximum operation frequency: 33 MHz (at 5-V operation)
- Extremely light in weight and compact
- Higher equivalence with target device can be achieved by omitting buffer between signal cables.
- Following pins can be masked.  
★ RESET, NMI, WAIT, HLDRQ
- Two methods of connection to target system:
  - Pod tip direct connection (For information on the pod, refer to the **IE-703002-MC User's Manual**)
  - Attach an extension probe (optional) to the pod tip for connection.
- Dimensions of the option board (IE-703003-MC-EM1) are as follows.

Parameter		Value
Power dissipation (Max. value at 5-V supply voltage)		0.35 W (at 33-MHz operation frequency) <sup>Note</sup>
	Height	13 mm
	Length	160 mm
	Width	96 mm
Weight		125 g

**Note** 10.35 W when IE-703002-MC with IE-703003-MC-EM1

## 1.3 Function Specifications (When connected to IE-703002-MC)

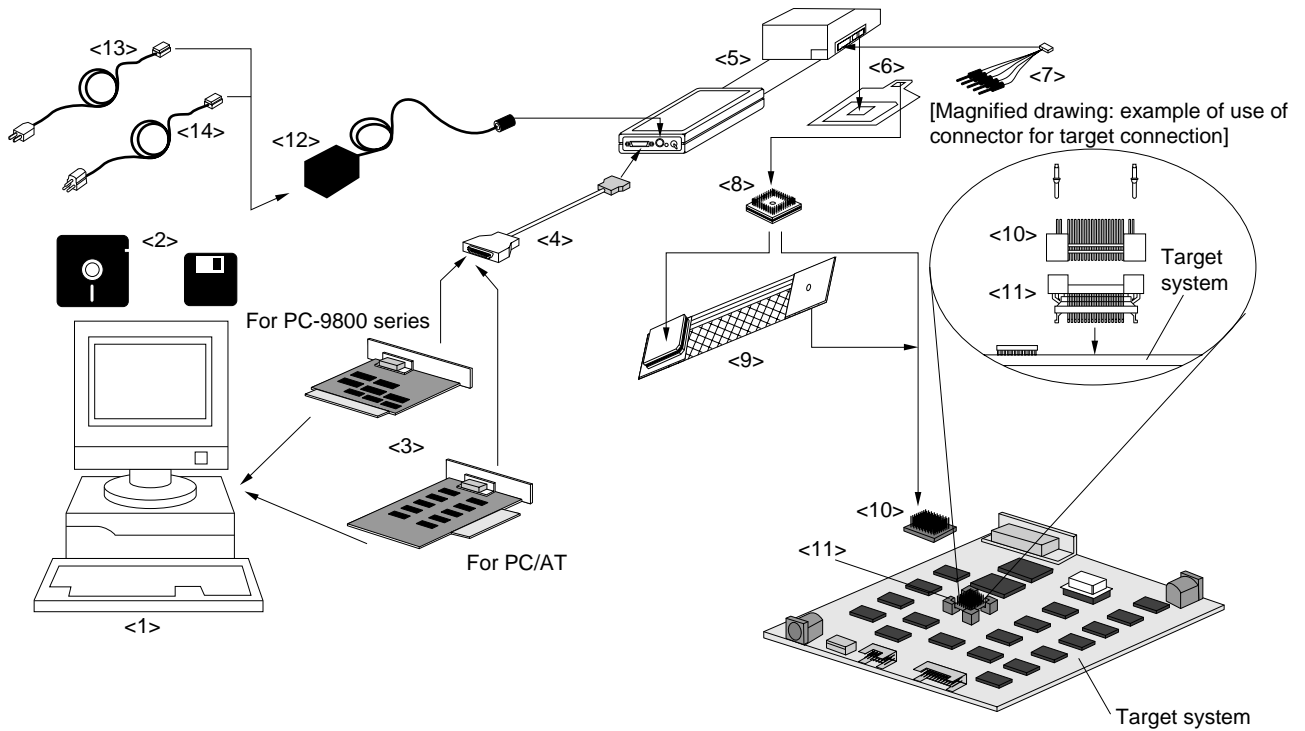
Parameter			Capacity
Emulation memory capacity	Internal ROM		128 Kbytes
	External memory	In ROM-less mode	2 Mbytes
		When using iROM	1 Mbyte
Execution/pass detection	Internal ROM		128 Kbytes
	External memory	In ROM-less mode	2 Mbytes
		When using iROM	1 Mbyte
Memory access detection coverage memory capacity (external memory)			1 Mbyte
Coverage memory capacity for branching entry number counting	Internal ROM		128 Kbytes
	External memory	In ROM-less mode	2 Mbytes
		When using iROM	1 Mbyte

**Caution** Some of the functions may not be supported depending on the debugger used.

## 1.4 System Configuration

The system configuration when connecting the IE-703003-MC to a personal computer (PC-9800 series or PC/AT™ (or compatible machine)) is shown below.

Figure 1-1. System Configuration



### Remark

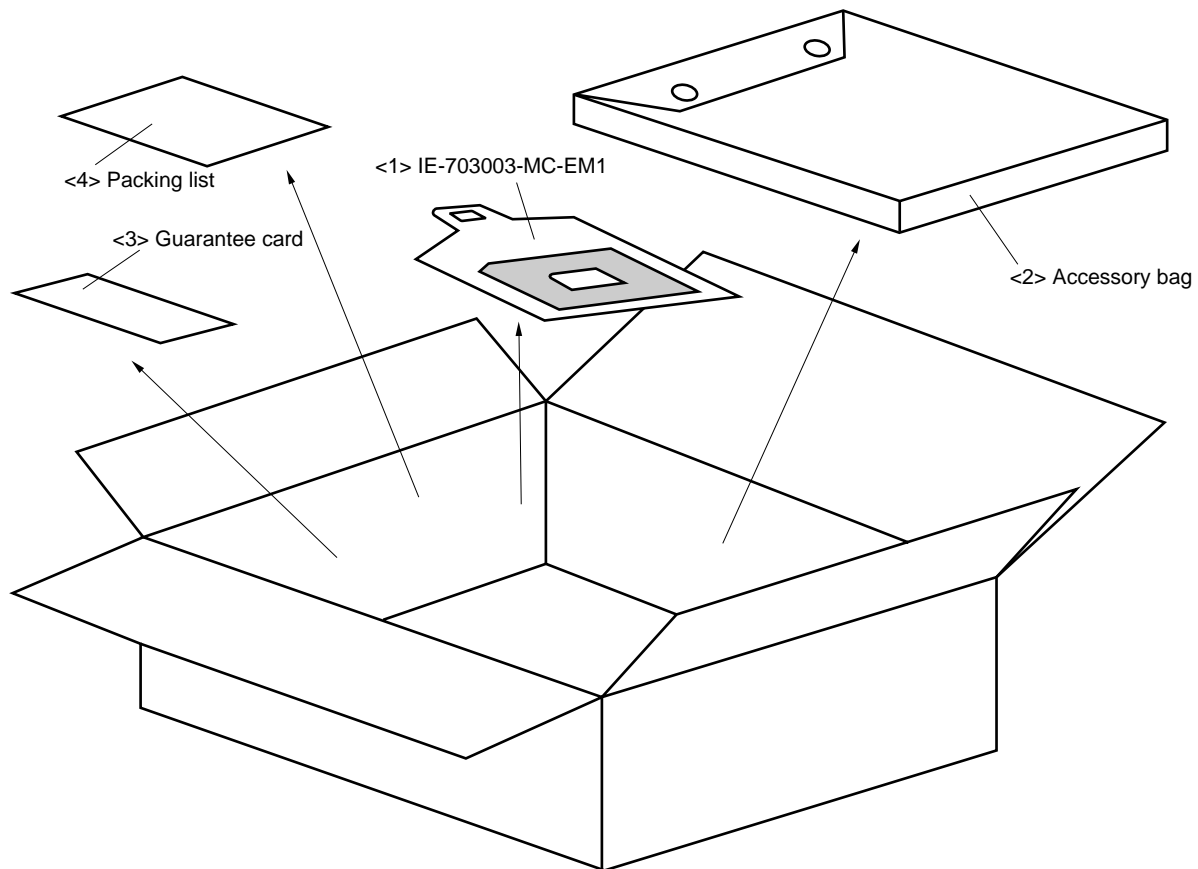
- <1> Personal computer (PC-9800 series or PC/AT)
- <2> Debugger (optional)
- <3> PC interface board (IE-70000-98-IF-B, IE-70000-PC-IF-B: optional)
- <4> PC interface cable (included with IE-703002-MC)
- <5> IE-703002-MC (In-circuit emulator)
- <6> IE-703003-MC-EM1 (Option board)
- <7> External logic probe (included with IE-703002-MC)
- ★ <8> Socket for target connection (YQSOCKET100SDF: included with IE-703002-MC)
- <9> Extension probe (SC-100SD: Optional)
- <10> Connector for emulator connection (YQPACK100SD: included in IE-703002-MC)
- <11> Connector for target connection (NQPACK100SD: included)
- <12> Power adapter (IE-70000-MC-PS-B optional)
- <13> 100-VAC power cable (attachment of optional IE-70000-MC-PS-B)
- <14> 220-VAC power cable (attachment of optional IE-70000-MC-PS-B)



## 1.5 Contents in Carton

The carton of the IE-703003-MC-EM1 contains a main unit, guarantee card, packing list, and accessory bag. Make sure that the accessory bag contains this manual and connector accessories. In case of missing or damaged contents, please contact an NEC sales representative or NEC dealer.

**Figure 1-2. Contents in Carton**

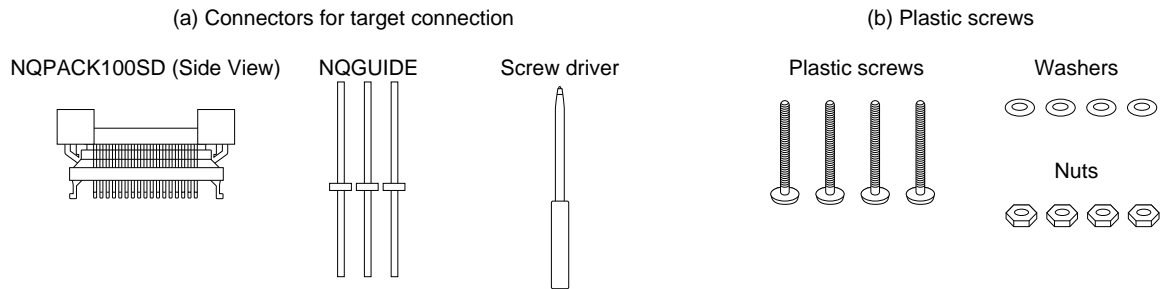


- <1> IE-703003-MC-EM1 × 1 pc.
- <2> Accessory bag × 1 pc.
- <3> Guarantee card × 1 pc.
- <4> Packing list × 1 sheet

Check that the accessory bag contains this manual, an accessory list, and the following accessories.

- (a) Connector for target connection (NQPACK100SD) × 1 set  
(including NQGUIDE 3 pcs., screw driver × 1 pc.)
- (b) Plastic screws × 4 pcs.  
(including nuts and washer × 4 sets)

**Figure 1-3. Accessories**



## 1.6 Connection between IE-703002-MC and IE-703003-MC-EM1

The procedure for connecting the IE-703002-MC and IE-703003-MC-EM1 is described below.

**Caution** Connect carefully so as not to break or bend connector pins.

- <1> Remove the pod cover of the IE-703002-MC.
- <2> Set the PGA socket lever of the IE-703003-MC-EM1 to the OPEN position as shown in Figure 1-4 (b).
- <3> Connect the IE-703003-MC-EM1 to the PGA socket at the back of the pod (refer to Figure 1-4 (c)). When connecting, position the IE-703002-MC and IE-703003-MC-EM1 so that they are horizontal.
- <4> Set the PGA socket lever of the IE-703003-MC-EM1 to the CLOSE position as shown in Figure 1-4 (b).
- <5> Set the jumpers (JP1 to JP4) and switches (SW1 and SW2). Open JP1 (Remove the jumper contact. Attach the removed jumper contact to one of the jumper pins to avoid losing them.) Set JP2 to JP4 and SW1 and SW2 depending on the use. Short the first and second pin of JP4.
- <6> Fix the IE-703003-MC-EM1 between the pod covers (upper and lower) with the plastic screws.
- <7> Secure the pod cover (upper) end with nylon rivets.

**Figure 1-4. Connection between IE-703002-MC and IE-703003-MC-EM1 (1/2)**

**(a) Overview**

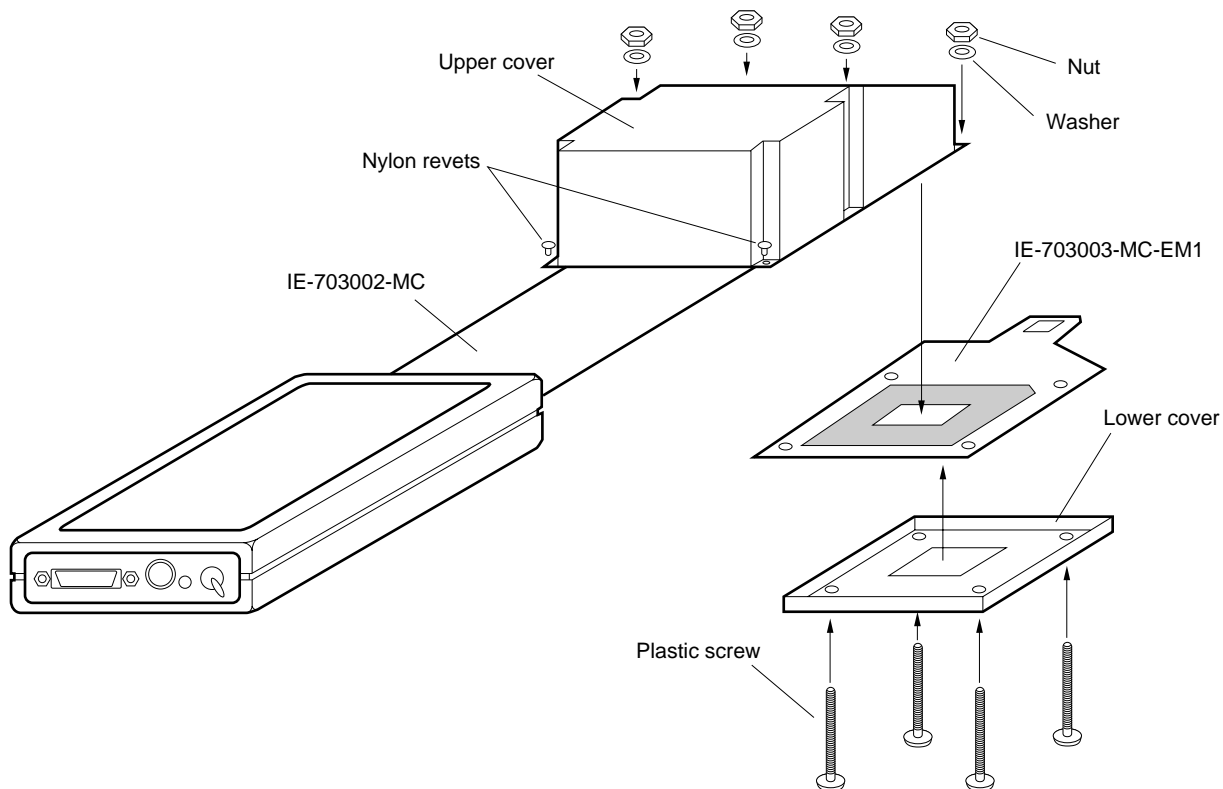
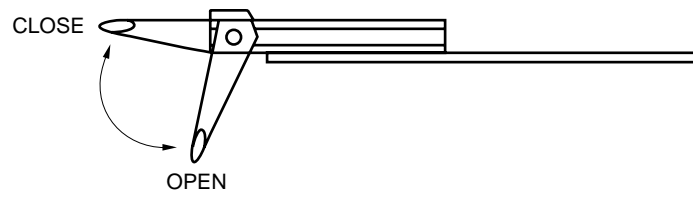
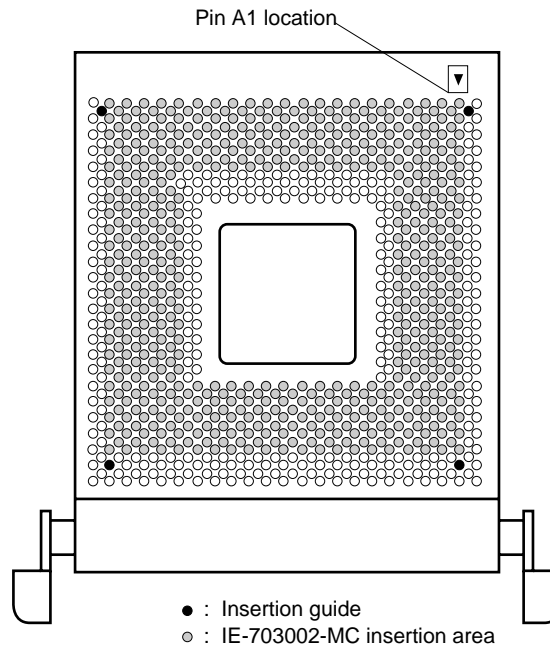


Figure 1-4. Connection between IE-703002-MC and IE-703003-MC-EM1 (2/2)

(b) PGA Socket Lever of IE-703003-MC-EM1



(c) Connecting part (IE-703003-MC-EM1)



[MEMO]

## CHAPTER 2 IE-703002-MC SETTING

This chapter describes settings of the IE-703002-MC when the IE-703003-MC-EM1 is connected.

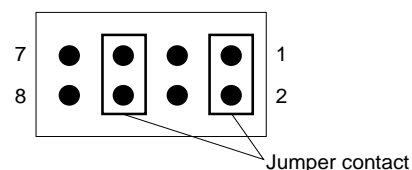
All settings are performed using the jumper and switches in the pod of the IE-703002-MC.

For the location of the pod, jumper, and switches, refer to the **IE-703003-MC User's Manual Hardware**.

### 2.1 Settings of JP2, SW1, and SW2

These jumper and switches set the clock. Set the jumper (JP2) and switches (SW1, SW2) depending on the use.

**Remark** The factory-set JP2 setting in the pod is as shown in the diagram at right. (The numbers 1, 2, 7, 8 are the jumper pin numbers printed on the board.)



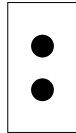
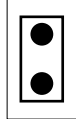
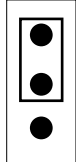
**Table 2-1. Settings of JP2, SW1, and SW2**

Setting of clock supply source			Setting of clock mode	
Supply method of clock			SW1 setting in pod (PLLSEL setting)	SW2 setting in pod (CKSEL setting)
Internal clock	PLL mode	5 × multiplication (input × 5)	ON	OFF
		1 × multiplication (input × 1)	OFF	
	Direct mode (input × 1/2)		Don't care	ON
Target clock	PLL mode	5 × multiplication (input × 5)	ON	OFF
		1 × multiplication (input × 1)	OFF	
	Direct mode (input × 1/2)		Don't care	ON

## 2.2 Settings of JP1, JP3, and JP4

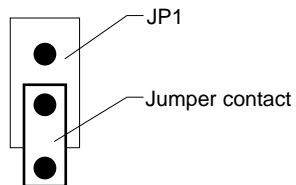
Set the JP1, JP3, and JP4 in the pod as follows.

**Table 2-2. Settings of JP1, JP3, and JP4**

Jumper	Status	
JP1 <sup>Note 1, 2</sup>	Open	
JP3	Short	
JP4 <sup>Note 1</sup>	1-2 short	

**Notes 1.** Differs from factory-set status.

**2.** Keep the removed connector attached to one pin as shown in the drawing below.



**Remark** IE-703002-MC operates under 5 V with the above described settings of JP3 and JP4, regardless of the target system voltage.

## CHAPTER 3 CAUTIONS

### 3.1 Internal RAM and ROM

Because the internal RAM (iRAM) and internal ROM (iROM) capacity of the IE-703002-MC are set in steps, the memory capacity is different from that of the target device. If access is performed to addresses that exceed the target device capacity, the memory of the IE-703002-MC is accessed. Memory capacities are as follows.

**Table 3-1. Memory Capacity Limitation List**

(a) iRAM capacity (Unit: byte)		(b) iROM capacity (Unit: byte)	
Target device	IE-703002-MC	Target device	IE-703002-MC (Emulation memory)
1 K	1 K	1 K to 32 K	32 K
2 K	2 K	33 K to 64 K	64 K
3 K	3 K	65 K to 128 K (V853)	128 K
4 K (V853)	4 K	129 K to 256 K	256 K
5 K to 6 K	6 K	257 K to 512 K	512 K
7 K to 8 K	8 K	513 K to 1024 K	512 K
9 K to 10 K	10 K		
11 K to 12 K	12 K		
13 K to 16 K	16 K		
17 K to 20 K	20 K		
21 K to 24 K	24 K		
25 K to 28 K	28 K		

**Remark** The IE-703002-MC incorporates 512 Kbytes of iROM emulation memory.

### 3.2 Target System V<sub>DD</sub>

The target system V<sub>DD</sub> does not connect to the IE-703002-MC V<sub>DD</sub>. The IE-703002-MC uses the V<sub>DD</sub> (pin No. 13) of the system for the following purposes:

- Power ON/OFF detection of target system
- Power supply voltage emulation of target voltage

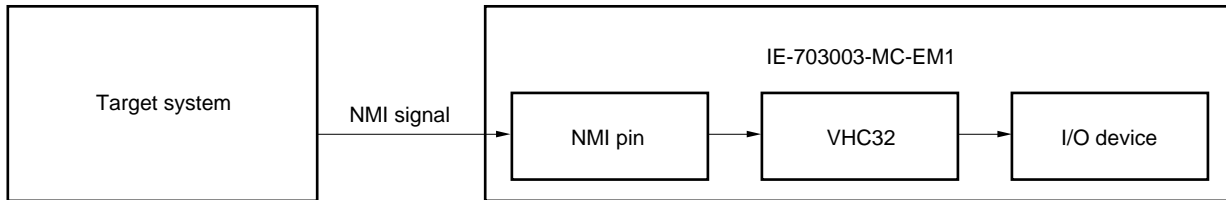


### 3.3 NMI Signal

The NMI signal from the target system is delayed because it passes through VHC32 before being input into the IE-703003-MC-EM1. ( $t_{pLH} = t_{pHL} = 8 \text{ ns}$  (TYP.))

- ★ Moreover, DC characteristics are changed to input voltage  $V_{IH} = 0.7 V_{DD}$  (MIN.),  $V_{IL} = 0.3 V_{DD}$  (MAX.), input current  $I_{IN} = \pm 1.0 \mu\text{A}$  (MAX.).

Figure 3-1. NMI Signal-Flow Path

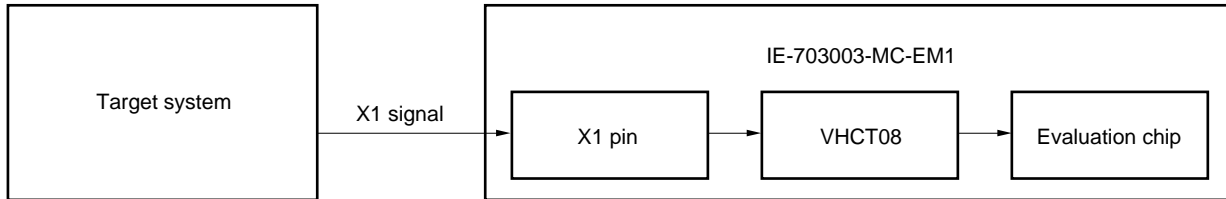


### 3.4 X1 Signal

The X1 signal from the target system is delayed because it passes through VHCT08 before being input into the evaluation chip of the IE-703003-MC-EM1. ( $t_{pLH} = 8 \text{ ns}$  (MAX.),  $t_{pHL} = 9 \text{ ns}$  (MAX.))

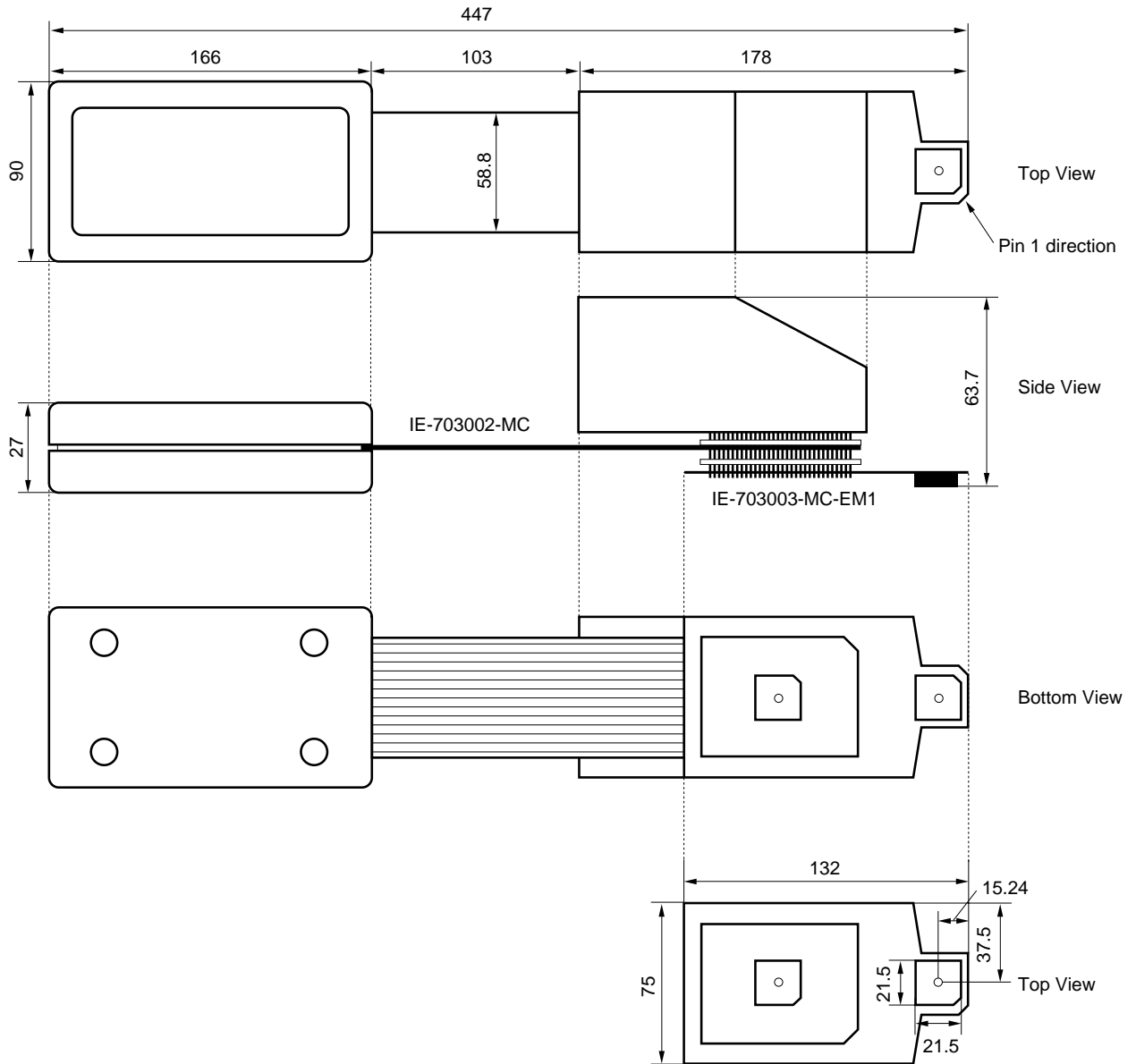
Moreover, DC characteristics are changed to input voltage  $V_{IH} = 2.0 \text{ V}$  (MIN.),  $V_{IL} = 0.8 \text{ V}$  (MAX.), input current  $I_{IN} = \pm 1.0 \mu\text{A}$  (MAX.).

Figure 3-2. X1 Signal-Flow Path



## APPENDIX DIMENSIONS

IE-703002-MC + IE-703003-MC-EM1 (Unit: mm)



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