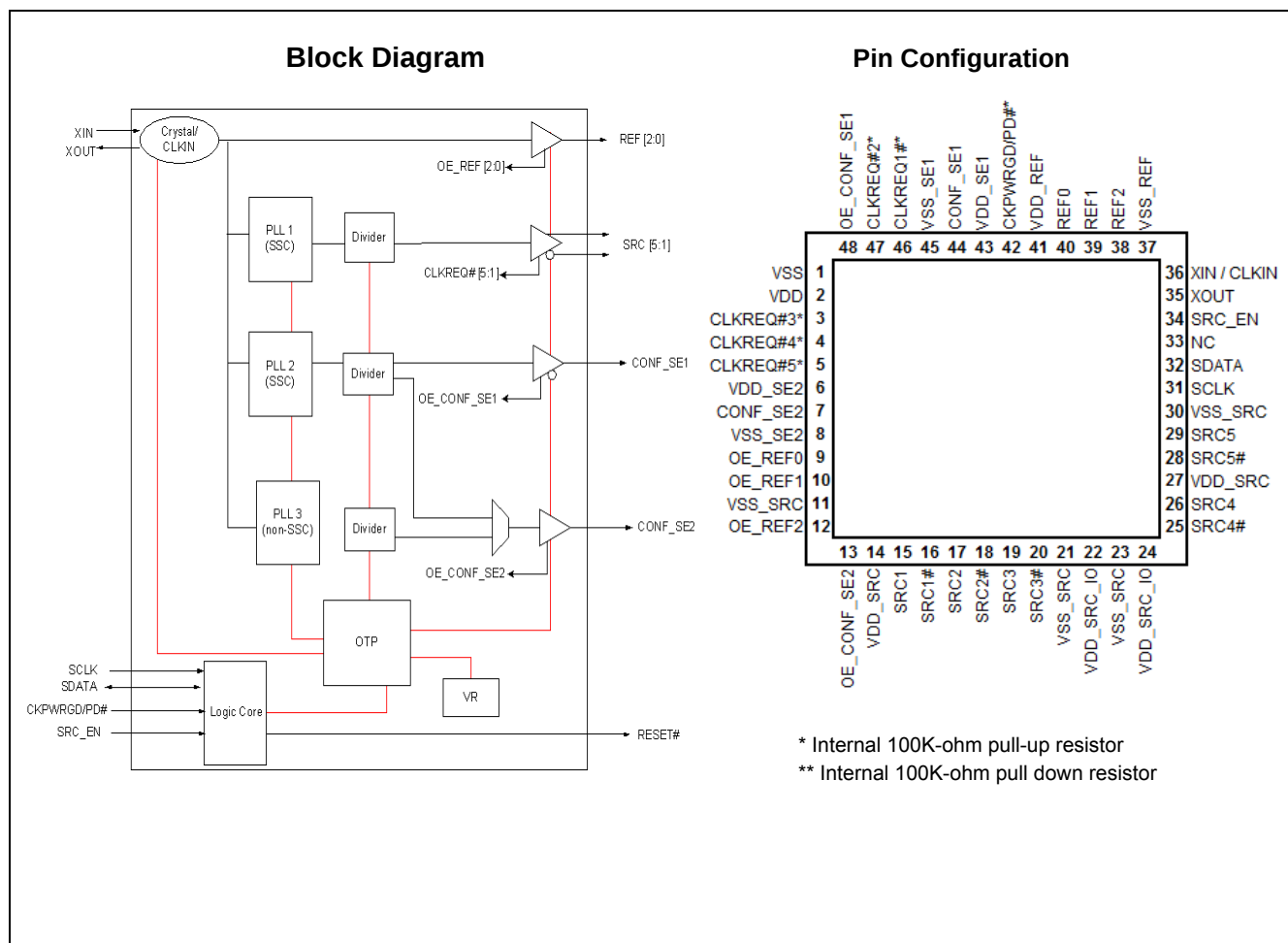


## EProClock® Generator

### Features

- PCI-Express Gen 2 Compliant
- Low power push-pull type differential output buffers
- Integrated resistors on all differential outputs
- Dedicated Output Enable pin for all outputs
- Dedicated SRC Bank Enable HW pin
- Scalable VDD\_IO support 1.05V to 3.3V
- Five 100MHz Differential PCIe Gen 2 clocks
- Two Configurable Single-Ended Clocks
- Three Buffered Reference Clock 25MHz
- 25MHz Crystal Input or Clock input
- EProClock® Programmable Technology
- I<sup>2</sup>C support with readback capabilities
- Triangular Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- 3.3V Power supply
- 48-pin QFN package

| SRC | 25M | CONF_SE1 | CONF_SE2 |
|-----|-----|----------|----------|
| x5  | x3  | x1       | x1       |



**32-QFN Pin Definitions**

| Pin No. | Name        | Type   | Description                                                                                                                                |
|---------|-------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | VSS_PCI     | GND    | Ground for PCI clock                                                                                                                       |
| 2       | VDD_PCI     | PWR    | 3.3V, Power Supply for PCI clock                                                                                                           |
| 3       | CLKREQ#3*   | I, PU  | 3.3V, active low input clock request to enable SRC3<br>(internal 100k-ohm internal pull-up)                                                |
| 4       | CLKREQ#4*   | I, PU  | 3.3V, active low input clock request to enable SRC4<br>(internal 100k-ohm internal pull-up)                                                |
| 5       | CLKREQ#5*   | I, PU  | 3.3V, active low input clock request to enable SRC5<br>(internal 100k-ohm internal pull-up)                                                |
| 6       | VDD_SE2     | PWR    | 3.3V, Power Supply for CONF_SE2 clock                                                                                                      |
| 7       | CONF_SE2    | O, SE  | 3.3V, configurable single-ended clock                                                                                                      |
| 8       | VSS_SE2     | GND    | Ground for SE2 clock                                                                                                                       |
| 9       | OE_REF0     | I      | 3.3V, active high input pin to enabled REF0                                                                                                |
| 10      | OE_REF1     | I      | 3.3V, active high input pin to enabled REF1                                                                                                |
| 11      | VSS_SRC     | GND    | Ground for SRC clocks                                                                                                                      |
| 12      | OE_REF2     | I      | 3.3V, active high input pin to enabled REF2                                                                                                |
| 13      | OE_CONF_SE2 | I      | 3.3V, active high input pin to enabled CONF_SE2                                                                                            |
| 14      | VDD_SRC     | PWR    | 3.3V Power Supply for SRC clocks                                                                                                           |
| 15      | SRC1        | O, DIF | 100MHz True differential serial reference clock                                                                                            |
| 16      | SRC1#       | O, DIF | 100MHz Complement differential serial reference clock                                                                                      |
| 17      | SRC2        | O, DIF | 100MHz True differential serial reference clock                                                                                            |
| 18      | SRC2#       | O, DIF | 100MHz Complement differential serial reference clock                                                                                      |
| 19      | SRC3        | O, DIF | 100MHz True differential serial reference clock                                                                                            |
| 20      | SRC3#       | O, DIF | 100MHz Complement differential serial reference clock                                                                                      |
| 21      | VSS_SRC     | GND    | Ground for SRC clocks                                                                                                                      |
| 22      | VDD_SRC_IO  | PWR    | Scalable 3.3V to 1.05V Power supply for SRC clocks                                                                                         |
| 23      | VSS_SRC     | GND    | Ground for SRC clocks                                                                                                                      |
| 24      | VDD_SRC_IO  | PWR    | Scalable 3.3V to 1.05V Power supply for SRC clocks                                                                                         |
| 25      | SRC4#       | O, DIF | 100MHz Complement differential serial reference clock                                                                                      |
| 26      | SRC4        | O, DIF | 100MHz True differential serial reference clock                                                                                            |
| 27      | VDD_SRC     | PWR    | 3.3V, Power Supply for SRC clocks                                                                                                          |
| 28      | SRC5#       | O, DIF | 100MHz Complement differential serial reference clock                                                                                      |
| 29      | SRC5        | O, DIF | 100MHz True differential serial reference clock                                                                                            |
| 30      | VSS_SRC     | GND    | Ground for SRC clocks                                                                                                                      |
| 31      | SCLK        | I      | SMBus compatible SCLOCK                                                                                                                    |
| 32      | SDATA       | I/O    | SMBus compatible SDATA                                                                                                                     |
| 33      | NC          | NC     | No Connect                                                                                                                                 |
| 34      | SRC_EN      | I      | 3.3V, active high input for master enable for all SRC clocks. When set to low, all SRC clocks will be disabled regardless of CLKREQ state. |
| 35      | XOUT        | O, SE  | 25.00MHz Crystal output, <i>Float XOUT if using only CLKIN (Clock input)</i>                                                               |
| 36      | XIN / CLKIN | I      | 25.00MHz Crystal input or 3.3V, 25MHz Clock Input                                                                                          |
| 37      | VSS_REF     | GND    | Ground for REF clocks                                                                                                                      |
| 38      | REF2        | O, SE  | 3.3V, 25MHz reference output clock                                                                                                         |
| 39      | REF1        | O, SE  | 25MHz reference output clock                                                                                                               |
| 40      | REF0        | O, SE  | 25MHz reference output clock                                                                                                               |
| 41      | VDD_REF     | PWR    | 3.3V, Power Supply for REF clock and power to support WOL                                                                                  |

| Pin No. | Name        | Type  | Description                                                                                                                                                                                                     |
|---------|-------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 42      | CKPWRGD/PD# | I     | 3.3V LVTTTL input. This pin is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled /this pin becomes a real-time active low input for asserting power down (PD#) |
| 43      | VDD_SE1     | PWR   | 3.3V Power Supply for CONF_SE1 clock                                                                                                                                                                            |
| 44      | CONF_SE1    | O, SE | 3.3V, configurable single-ended clock                                                                                                                                                                           |
| 45      | VSS_SE1     | GND   | Ground for CONF_SE1 clock                                                                                                                                                                                       |
| 46      | CLKREQ#1*   | I, PU | 3.3V, active low input clock request to enable SRC1<br>(internal 100k-ohm internal pull-up)                                                                                                                     |
| 47      | CLKREQ#2*   | I, PU | 3.3V, active low input clock request to enable SRC2<br>(internal 100k-ohm internal pull-up)                                                                                                                     |
| 48      | OE_CONF_SE1 | I     | 3.3V, active high input clock request to enable CONF_SE1                                                                                                                                                        |

### EProClock® Programmable Technology

EProClock® is the world's first non-volatile programmable clock. The EProClock® technology allows board designer to promptly achieve optimum compliance and clock signal integrity; historically, attainable typically through device and/or board redesigns.

EProClock® technology can be configured through SMBus or hard coded.

#### Features:

- > 4000 bits of configurations
- Can be configured through SMBus or hard coded
- Custom frequency sets

- Differential skew control on true or compliment or both
- Differential duty cycle control on true or compliment or both
- Differential amplitude control
- Differential and single-ended slew rate control
- Program Internal or External series resistor on single-ended clocks
- Programmable different spread profiles
- Programmable modulation rates

### Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

### Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 1. Command Code Definition**

| Bit   | Description                                                                                                                 |
|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 7     | 0 = Block read or block write operation, 1 = Byte read or byte write operation                                              |
| (6:0) | Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000' |

**Table 2. Block Read and Block Write Protocol**

| Block Write Protocol |                       | Block Read Protocol |                       |
|----------------------|-----------------------|---------------------|-----------------------|
| Bit                  | Description           | Bit                 | Description           |
| 1                    | Start                 | 1                   | Start                 |
| 8:2                  | Slave address--7 bits | 8:2                 | Slave address--7 bits |

**Table 2. Block Read and Block Write Protocol (continued)**

| Block Write Protocol |                               | Block Read Protocol |                                     |
|----------------------|-------------------------------|---------------------|-------------------------------------|
| Bit                  | Description                   | Bit                 | Description                         |
| 9                    | Write                         | 9                   | Write                               |
| 10                   | Acknowledge from slave        | 10                  | Acknowledge from slave              |
| 18:11                | Command Code–8 bits           | 18:11               | Command Code–8 bits                 |
| 19                   | Acknowledge from slave        | 19                  | Acknowledge from slave              |
| 27:20                | Byte Count–8 bits             | 20                  | Repeat start                        |
| 28                   | Acknowledge from slave        | 27:21               | Slave address–7 bits                |
| 36:29                | Data byte 1–8 bits            | 28                  | Read = 1                            |
| 37                   | Acknowledge from slave        | 29                  | Acknowledge from slave              |
| 45:38                | Data byte 2–8 bits            | 37:30               | Byte Count from slave–8 bits        |
| 46                   | Acknowledge from slave        | 38                  | Acknowledge                         |
| ....                 | Data Byte /Slave Acknowledges | 46:39               | Data byte 1 from slave–8 bits       |
| ....                 | Data Byte N–8 bits            | 47                  | Acknowledge                         |
| ....                 | Acknowledge from slave        | 55:48               | Data byte 2 from slave–8 bits       |
| ....                 | Stop                          | 56                  | Acknowledge                         |
|                      |                               | ....                | Data bytes from slave / Acknowledge |
|                      |                               | ....                | Data Byte N from slave–8 bits       |
|                      |                               | ....                | NOT Acknowledge                     |
|                      |                               | ....                | Stop                                |

**Table 3. Byte Read and Byte Write Protocol**

| Byte Write Protocol |                        | Byte Read Protocol |                        |
|---------------------|------------------------|--------------------|------------------------|
| Bit                 | Description            | Bit                | Description            |
| 1                   | Start                  | 1                  | Start                  |
| 8:2                 | Slave address–7 bits   | 8:2                | Slave address–7 bits   |
| 9                   | Write                  | 9                  | Write                  |
| 10                  | Acknowledge from slave | 10                 | Acknowledge from slave |
| 18:11               | Command Code–8 bits    | 18:11              | Command Code–8 bits    |
| 19                  | Acknowledge from slave | 19                 | Acknowledge from slave |
| 27:20               | Data byte–8 bits       | 20                 | Repeated start         |
| 28                  | Acknowledge from slave | 27:21              | Slave address–7 bits   |
| 29                  | Stop                   | 28                 | Read                   |
|                     |                        | 29                 | Acknowledge from slave |
|                     |                        | 37:30              | Data from slave–8 bits |
|                     |                        | 38                 | NOT Acknowledge        |
|                     |                        | 39                 | Stop                   |

**Control Registers**
**Byte 0: Control Register 0**

| Bit | @Pup | Type | Name         | Description                                                |
|-----|------|------|--------------|------------------------------------------------------------|
| 7   | 0    | R/W  | CONF_SE1_OE  | Output Enable for CONF_SE1<br>0=Disabled, 1=Enabled        |
| 6   | 0    | R/W  | CONF_SE2_OE  | Output Enable for CONF_SE2<br>0=Disabled, 1=Enabled        |
| 5   | 1    | R/W  | SRC5_CLKREQ# | Output Enable for SRC5<br>0=Enabled, 1=Disabled            |
| 4   | 1    | R/W  | SRC4_CLKREQ# | Output Enable for SRC4<br>0=Enabled, 1=Disabled            |
| 3   | 1    | R/W  | SRC3_CLKREQ# | Output Enable for SRC3<br>0=Enabled, 1=Disabled            |
| 2   | 1    | R/W  | SRC2_CLKREQ# | Output Enable for SRC2<br>0=Enabled, 1=Disabled            |
| 1   | 1    | R/W  | SRC1_CLKREQ# | Output Enable for SRC1<br>0=Enabled, 1=Disabled            |
| 0   | 1    | R/W  | SRC_EN       | Global Output Enable for SRC[5;1]<br>0=Disabled, 1=Enabled |

**Byte 1: Control Register 1**

| Bit | @Pup | Type | Name         | Description                                                                 |
|-----|------|------|--------------|-----------------------------------------------------------------------------|
| 7   | 0    | R/W  | REF0_OE      | Output Enable for REF0<br>0=Disabled, 1=Enabled                             |
| 6   | 0    | R/W  | REF1_OE      | Output Enable for REF1<br>0=Disabled, 1=Enabled                             |
| 5   | 0    | R/W  | REF2_OE      | Output Enable for REF2<br>0=Disabled, 1=Enabled                             |
| 4   | 1    | R/W  | SRC5_FREERUN | SRC_EN Control for SRC5<br>0=Free Running, 1=Stoppable by SRC_EN Pin or Bit |
| 3   | 1    | R/W  | SRC4_FREERUN | SRC_EN Control for SRC4<br>0=Free Running, 1=Stoppable by SRC_EN Pin or Bit |
| 2   | 1    | R/W  | SRC3_FREERUN | SRC_EN Control for SRC3<br>0=Free Running, 1=Stoppable by SRC_EN Pin or Bit |
| 1   | 1    | R/W  | SRC2_FREERUN | SRC_EN Control for SRC2<br>0=Free Running, 1=Stoppable by SRC_EN Pin or Bit |
| 0   | 1    | R/W  | SRC1_FREERUN | SRC_EN Control for SRC1<br>0=Free Running, 1=Stoppable by SRC_EN Pin or Bit |

**Byte 2: Control Register 2**

| Bit | @Pup | Type | Name            | Description         |
|-----|------|------|-----------------|---------------------|
| 7   | 0    | R    | Rev Code Bit 3  | Revision Code Bit 3 |
| 6   | 0    | R    | Rev Code Bit 2  | Revision Code Bit 2 |
| 5   | 0    | R    | Rev Code Bit 1  | Revision Code Bit 1 |
| 4   | 1    | R    | Rev Code Bit 0  | Revision Code Bit 0 |
| 3   | 1    | R    | Vendor ID bit 3 | Vendor ID Bit 3     |
| 2   | 0    | R    | Vendor ID bit 2 | Vendor ID Bit 2     |
| 1   | 0    | R    | Vendor ID bit 1 | Vendor ID Bit 1     |
| 0   | 0    | R    | Vendor ID bit 0 | Vendor ID Bit 0     |

**Byte 3: Control Register 3**

| Bit | @Pup | Type | Name | Description                                                                                                                                                                                          |
|-----|------|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | 0    | R/W  | BC7  | Byte count register for block read operation. The default value for Byte count is 8. In order to read more than 8 bytes, the system needs to change this register to the number of bytes to be read. |
| 6   | 0    | R/W  | BC6  |                                                                                                                                                                                                      |
| 5   | 0    | R/W  | BC5  |                                                                                                                                                                                                      |
| 4   | 0    | R/W  | BC4  |                                                                                                                                                                                                      |
| 3   | 1    | R/W  | BC3  |                                                                                                                                                                                                      |
| 2   | 0    | R/W  | BC2  |                                                                                                                                                                                                      |
| 1   | 0    | R/W  | BC1  |                                                                                                                                                                                                      |
| 0   | 0    | R/W  | BC0  |                                                                                                                                                                                                      |

**Byte 4: Control Register 4**

| Bit               | @Pup         | Type      | Name          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|-------------------|--------------|-----------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|--------------|-----------|------|-----------------|---|-------|---|---|-----------------------------------|-------|---------|---|---|---------|---|---|---|--------|---|---|---|--|---|---|---|-------------------|---|---|---|--|---|---|---|--|---|---|---|
| 7                 | 0            | R/W       | SRC_AMP1      | Amplitude Control for SRC clocks <table><tr><th>Byte 4, bit7</th><th>Byte 4, bit6</th><th>Amplitude</th><th>Note</th></tr><tr><td>0</td><td>0</td><td>700mV</td><td></td></tr><tr><td>0</td><td>1</td><td>800mV</td><td>Default</td></tr><tr><td>1</td><td>0</td><td>900mV</td><td></td></tr><tr><td>1</td><td>1</td><td>1000mV</td><td></td></tr></table>                                                                                                                                                                                                                                                                           | Byte 4, bit7                      | Byte 4, bit6 | Amplitude | Note | 0               | 0 | 700mV |   | 0 | 1                                 | 800mV | Default | 1 | 0 | 900mV   |   | 1 | 1 | 1000mV |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| Byte 4, bit7      | Byte 4, bit6 | Amplitude | Note          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 0                 | 0            | 700mV     |               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 0                 | 1            | 800mV     | Default       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 1                 | 0            | 900mV     |               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 1                 | 1            | 1000mV    |               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 6                 | 1            | R/W       | SRC_AMP0      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 5                 | 0            | R/W       | CONF_SE1_BIT2 | Slew Rate Control for CONF_SE1 and CONF_SE2 clocks <table><tr><th>Mode</th><th>BIT2</th><th>BIT1</th><th>BIT0</th><th>Buffer Strength</th></tr><tr><td></td><td>0</td><td>0</td><td>0</td><td rowspan="8"><div>Strong</div><div>Weak</div></td></tr><tr><td></td><td>0</td><td>0</td><td>1</td></tr><tr><td>Default</td><td>0</td><td>1</td><td>0</td></tr><tr><td></td><td>0</td><td>1</td><td>1</td></tr><tr><td></td><td>1</td><td>0</td><td>0</td></tr><tr><td>Wireless Friendly</td><td>1</td><td>0</td><td>1</td></tr><tr><td></td><td>1</td><td>1</td><td>0</td></tr><tr><td></td><td>1</td><td>1</td><td>1</td></tr></table> | Mode                              | BIT2         | BIT1      | BIT0 | Buffer Strength |   | 0     | 0 | 0 | <div>Strong</div> <div>Weak</div> |       | 0       | 0 | 1 | Default | 0 | 1 | 0 |        | 0 | 1 | 1 |  | 1 | 0 | 0 | Wireless Friendly | 1 | 0 | 1 |  | 1 | 1 | 0 |  | 1 | 1 | 1 |
| Mode              | BIT2         | BIT1      | BIT0          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Buffer Strength                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 0            | 0         | 0             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | <div>Strong</div> <div>Weak</div> |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 0            | 0         | 1             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| Default           | 0            | 1         | 0             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 0            | 1         | 1             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 1            | 0         | 0             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| Wireless Friendly | 1            | 0         | 1             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 1            | 1         | 0             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 1            | 1         | 1             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 4                 | 1            | R/W       | CONF_SE1_BIT1 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 3                 | 0            | R/W       | CONF_SE1_BIT0 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 2                 | 0            | R/W       | CONF_SE2_BIT2 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 1                 | 1            | R/W       | CONF_SE2_BIT1 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 0                 | 0            | R/W       | CONF_SE2_BIT0 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                   |              |           |      |                 |   |       |   |   |                                   |       |         |   |   |         |   |   |   |        |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |

| Byte 4, bit7 | Byte 4, bit6 | Amplitude | Note    |
|--------------|--------------|-----------|---------|
| 0            | 0            | 700mV     |         |
| 0            | 1            | 800mV     | Default |
| 1            | 0            | 900mV     |         |
| 1            | 1            | 1000mV    |         |

| Mode              | BIT2 | BIT1 | BIT0 | Buffer Strength                                                                |
|-------------------|------|------|------|--------------------------------------------------------------------------------|
|                   | 0    | 0    | 0    | <div style="text-align: center;"> <b>Strong</b><br/> ↓<br/> <b>Weak</b> </div> |
|                   | 0    | 0    | 1    |                                                                                |
| Default           | 0    | 1    | 0    |                                                                                |
|                   | 0    | 1    | 1    |                                                                                |
|                   | 1    | 0    | 0    |                                                                                |
| Wireless Friendly | 1    | 0    | 1    |                                                                                |
|                   | 1    | 1    | 0    |                                                                                |
|                   | 1    | 1    | 1    |                                                                                |

**Byte 5: Control Register 5**

| Bit               | @Pup | Type | Name            | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|-------------------|------|------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|------|------|------|-----------------|--|---|---|---|------------------------------------------------|--|---|---|---|---------|---|---|---|--|---|---|---|--|---|---|---|-------------------|---|---|---|--|---|---|---|--|---|---|---|
| 7                 | 0    | R/W  | REF0_BIT2       | <div>Slew Rate Contorl for REF clocks</div> <table><tr><th>Mode</th><th>BIT2</th><th>BIT1</th><th>BIT0</th><th>Buffer Strength</th></tr><tr><td></td><td>0</td><td>0</td><td>0</td><td rowspan="9"><div>Strong</div><div>↓</div><div>Weak</div></td></tr><tr><td></td><td>0</td><td>0</td><td>1</td></tr><tr><td>Default</td><td>0</td><td>1</td><td>0</td></tr><tr><td></td><td>0</td><td>1</td><td>1</td></tr><tr><td></td><td>1</td><td>0</td><td>0</td></tr><tr><td>Wireless Friendly</td><td>1</td><td>0</td><td>1</td></tr><tr><td></td><td>1</td><td>1</td><td>0</td></tr><tr><td></td><td>1</td><td>1</td><td>1</td></tr></table> | Mode                                           | BIT2 | BIT1 | BIT0 | Buffer Strength |  | 0 | 0 | 0 | <div>Strong</div> <div>↓</div> <div>Weak</div> |  | 0 | 0 | 1 | Default | 0 | 1 | 0 |  | 0 | 1 | 1 |  | 1 | 0 | 0 | Wireless Friendly | 1 | 0 | 1 |  | 1 | 1 | 0 |  | 1 | 1 | 1 |
| Mode              | BIT2 | BIT1 | BIT0            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Buffer Strength                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 0    | 0    | 0               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | <div>Strong</div> <div>↓</div> <div>Weak</div> |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 0    | 0    | 1               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| Default           | 0    | 1    | 0               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 0    | 1    | 1               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 1    | 0    | 0               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| Wireless Friendly | 1    | 0    | 1               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 1    | 1    | 0               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 1    | 1    | 1               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 6                 | 1    | R/W  | REF0_BIT1       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 5                 | 0    | R/W  | REF0_BIT0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 4                 | 0    | R/W  | REF1_BIT2       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 3                 | 1    | R/W  | REF1_BIT1       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 2                 | 0    | R/W  | REF1_BIT0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 1                 | 0    | R/W  | TEST_MODE_ENTRY | Allows entry into test mode<br>0 = Normal Operation, 1 = Enter test mode(s)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 0                 | 0    | R/W  | TEST_MODE_SEL   | Test mode select either REF/N or tri-state<br>0 = All outputs tri-state, 1 = All output REF/N                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |

**Byte 6: Control Register 6**

| Bit               | @Pup | Type | Name                   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|-------------------|------|------|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|------|------|------|-----------------|--|---|---|---|------------------------------------------------|--|---|---|---|---------|---|---|---|--|---|---|---|--|---|---|---|-------------------|---|---|---|--|---|---|---|--|---|---|---|
| 7                 | 0    | R/W  | REF2_BIT2              | <div>Slew Rate Control for REF clocks</div> <table><tr><th>Mode</th><th>BIT2</th><th>BIT1</th><th>BIT0</th><th>Buffer Strength</th></tr><tr><td></td><td>0</td><td>0</td><td>0</td><td rowspan="8"><div>Strong</div><div>↓</div><div>Weak</div></td></tr><tr><td></td><td>0</td><td>0</td><td>1</td></tr><tr><td>Default</td><td>0</td><td>1</td><td>0</td></tr><tr><td></td><td>0</td><td>1</td><td>1</td></tr><tr><td></td><td>1</td><td>0</td><td>0</td></tr><tr><td>Wireless Friendly</td><td>1</td><td>0</td><td>1</td></tr><tr><td></td><td>1</td><td>1</td><td>0</td></tr><tr><td></td><td>1</td><td>1</td><td>1</td></tr></table> | Mode                                           | BIT2 | BIT1 | BIT0 | Buffer Strength |  | 0 | 0 | 0 | <div>Strong</div> <div>↓</div> <div>Weak</div> |  | 0 | 0 | 1 | Default | 0 | 1 | 0 |  | 0 | 1 | 1 |  | 1 | 0 | 0 | Wireless Friendly | 1 | 0 | 1 |  | 1 | 1 | 0 |  | 1 | 1 | 1 |
| Mode              | BIT2 | BIT1 | BIT0                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Buffer Strength                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 0    | 0    | 0                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | <div>Strong</div> <div>↓</div> <div>Weak</div> |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 0    | 0    | 1                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| Default           | 0    | 1    | 0                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 0    | 1    | 1                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 1    | 0    | 0                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| Wireless Friendly | 1    | 0    | 1                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 1    | 1    | 0                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
|                   | 1    | 1    | 1                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 6                 | 1    | R/W  | REF2_BIT1              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 5                 | 0    | R/W  | REF2_BIT0              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 4                 | 0    | R/W  | Wireless Friendly Mode | One-bit slew rate control. Set all SE clocks to 101 setting<br>0=Disabled; 1=Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 3                 | 1    | R/W  | PLL1_SS_EN             | Spread Enabled for PLL1<br>0=Spread Disabled; 1=Spread Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 2                 | 0    | R/W  | PLL1_SS_DC             | Spread Profile<br>0=-0.5%; 1=+/-0.25%                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 1                 | 0    | R/W  | CONF_SE2_FS            | CONF_SE2 Frequency Select<br>0=24.576MHz, 1=12MHz (Note: Byte 6<1> only applies when<br>Byte 6<0>=0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |
| 0                 | 0    | R/W  | CONF_SE2_PLL_SEL       | PLL source for CONF_SE2 output<br>0=PLL3; (Note: Byte6<0> = 0, Table 7 applies for<br>CONF_SE2)<br><br>1=PLL2; (Note: Byte6<0> = 1, Table 6 applies for<br>CONF_SE2)                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                |      |      |      |                 |  |   |   |   |                                                |  |   |   |   |         |   |   |   |  |   |   |   |  |   |   |   |                   |   |   |   |  |   |   |   |  |   |   |   |

**Byte 7: Control Register 7**

| Bit | @Pup | Type | Name           | Description                                                                                                                                                               |
|-----|------|------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | 0    | R/W  | PLL2_SS_EN     | Spread Enabled for PLL2<br>0=Spread Disabled; 1=Spread Enabled                                                                                                            |
| 6   | 0    | R/W  | CONFIG_SE1_FS2 | See Table 6 on page 7 for full configuraiton                                                                                                                              |
| 5   | 0    | R/W  | CONFIG_SE1_FS1 |                                                                                                                                                                           |
| 4   | 0    | R/W  | CONFIG_SE1_FS0 |                                                                                                                                                                           |
| 3   | 0    | R/W  | PLL1_PD        | Power Down PLL1<br>0=Enabled PLL1; 1=Disabled PLL1                                                                                                                        |
| 2   | 0    | R/W  | PLL2_PD        | Power Down PLL2<br>0=Enabled PLL2; 1=Disabled PLL2                                                                                                                        |
| 1   | 0    | R/W  | PLL3_PD        | Power Down PLL3<br>0=Enabled PLL3; 1=Disabled PLL3                                                                                                                        |
| 0   | 1    | R/W  | RESET#_SET     | RESET# Output setting<br>0=RESET# output goes low, but will not disabled SRC clocks<br>1=RESET# goes high after 100ms if device is not in power down or SRC_EN in not "0" |

## Input Pins Clarification

### SRC\_EN Clarification

SRC\_EN pin is a 3.3V active high input pin. When the SRC\_EN signal is a logic low, all SRC clocks will be disabled synchronously regardless of the CLKREQ# state. If SRC\_EN pin remains disabled it can be re-enabled through the SMBus register. The SRC\_EN signal will be asserted high whenever the SRC\_EN pin or the SRC\_EN bit is a logic high.

### CLKREQ# Clarification

The CLKREQ# signals are active low inputs used to cleanly enable and disable selected SRC outputs. If CLKREQ# pin remains disabled it can be re-enabled through the SMBus register. The CLKREQ# signal will be asserted high whenever the CLKREQ# pin or the CLKREQ# bit is a logic high.

### OE Clarification

The OE signals are active high inputs used to enable and disable single-ended outputs. If OE pin remains disabled it can be re-enabled through the SMBus register. The OE signal will be asserted high whenever the OE pin or the OE bit is a logic high. OE pins is required to be driven at all time.

### RESET# Clarification

The RESET# signal is 3.3V output signal with an internal 100k-ohm pull-down. The RESET# output is low during power up. When SRC\_EN is low and after all SRC clocks go low, RESET# will go low. If any of the SRCs is running when SRC\_EN is low, RESET# will not go low. When PD pin is de-asserted and SRC\_EN goes high, RESET# will remain low for 100ms then goes high. If PD is asserted, RESET# will be low.

**Table 4. CLKREQ# Table for SRC Clocks**

| CKPWRGD / PD# | SRC_EN Pin | SRC_EN Bit | CLKREQ# Pin | CLKREQ# Bit | SRC Clocks                   |
|---------------|------------|------------|-------------|-------------|------------------------------|
| 1             | 1          | X          | 0           | X           | Enabled                      |
| 1             | 1          | X          | X           | 0           | Enabled                      |
| 1             | X          | 1          | 0           | X           | Enabled                      |
| 1             | X          | 1          | X           | 0           | Enabled                      |
| 1             | 0          | 0          | 0           | 0           | Disabled if not free running |
| 1             | 0          | 0          | 0           | 1           | Disabled if not free running |
| 1             | 0          | 0          | 1           | 0           | Disabled if not free running |
| 1             | X          | X          | 1           | 1           | Disabled                     |
| 0             | X          | X          | X           | X           | Disabled                     |

**Table 5. Output Enable Table For Singled-Ended Clock**

| CKPWRGD / PD# | OE Pin | OE Bit | Singled Ended Clocks |
|---------------|--------|--------|----------------------|
| 1             | X      | 1      | Enabled              |
| 1             | 1      | X      | Enabled              |
| 1             | 0      | 0      | Disabled             |
| 0             | X      | X      | Disabled             |

**Table 6. Frequency and Spread Table for CONF\_SE1 (and CONF\_SE2 if Byte6<0> = 1)**

| Byte 7, bit 7 | Byte 7, bit 6 | Byte 7, bit 5 | Byte 7, bit 4 | CONF_SE1 Clock (Pin 44) | CONF_SE1 Spread | Note                                                                                                          |
|---------------|---------------|---------------|---------------|-------------------------|-----------------|---------------------------------------------------------------------------------------------------------------|
| 0             | 0             | 0             | 0             | 27MHz                   | no spread       | Default                                                                                                       |
| 0             | 0             | 0             | 1             | 12MHz                   | no spread       |                                                                                                               |
| 0             | 0             | 1             | 0             | 25MHz                   | no spread       | 25MHz REF output is used for CONF_SE1. PLL2 is disabled. This selection is not applicable to CONF_SE2 output. |
| 0             | 0             | 1             | 1             | 33MHz                   | no spread       |                                                                                                               |
| 0             | 1             | 0             | 0             | 24MHz                   | no spread       |                                                                                                               |
| 0             | 1             | 0             | 1             | 48MHz                   | no spread       |                                                                                                               |
| 0             | 1             | 1             | 0             | 30MHz                   | no spread       |                                                                                                               |
| 0             | 1             | 1             | 1             | 24.576MHz               | no spread       |                                                                                                               |
| 1             | 0             | 0             | 0             | 27MHz                   | -0.50%          |                                                                                                               |
| 1             | 0             | 0             | 1             | 27MHz                   | -0.75%          |                                                                                                               |
| 1             | 0             | 1             | 0             | 27MHz                   | -1.0%           |                                                                                                               |
| 1             | 0             | 1             | 1             | 27MHz                   | -1.5%           |                                                                                                               |
| 1             | 1             | 0             | 0             | 27MHz                   | +/-0.5%         |                                                                                                               |
| 1             | 1             | 0             | 1             | 27MHz                   | +/-0.25%        |                                                                                                               |
| 1             | 1             | 1             | 0             | 33MHz                   | -0.5%           |                                                                                                               |
| 1             | 1             | 1             | 1             | 33MHz                   | +/-0.25%        |                                                                                                               |

**Table 7. Frequency and Spread Table for CONF\_SE2 when Byte6<0> = 0**

| Byte 6, bit 1 | CONF_SE2 Clock (Pin 7) | CONF_SE2 Spread | Note    |
|---------------|------------------------|-----------------|---------|
| 0             | 24.576MHz              | no spread       | Default |
| 1             | 12MHz                  | no spread       |         |

### Absolute Maximum Conditions

| Parameter                   | Description                    | Condition                   | Min. | Max.  | Unit            |
|-----------------------------|--------------------------------|-----------------------------|------|-------|-----------------|
| V <sub>DD_3.3V</sub>        | Main Supply Voltage            | Functional                  | –    | 4.6   | V               |
| V <sub>DD_IO</sub>          | IO Supply Voltage              | Functional                  |      | 3.465 | V               |
| V <sub>IN</sub>             | Input Voltage                  | Relative to V <sub>SS</sub> | –0.5 | 4.6   | V <sub>DC</sub> |
| T <sub>S</sub>              | Temperature, Storage           | Non-functional              | –65  | 150   | °C              |
| T <sub>AI(INDUSTRIAL)</sub> | Temperature, Operating Ambient | Functional                  | –40  | 85    | °C              |
| T <sub>A(COMMERCIAL)</sub>  | Temperature, Operating Ambient | Functional                  | 0    | 85    | °C              |
| T <sub>J</sub>              | Temperature, Junction          | Functional                  | –    | 150   | °C              |
| θ <sub>JC</sub>             | Dissipation, Junction to Case  | JEDEC (JESD 51)             | –    | 20    | °C/W            |

**Absolute Maximum Conditions**

|                    |                                   |                        |      |    |      |
|--------------------|-----------------------------------|------------------------|------|----|------|
| $\theta_{JA}$      | Dissipation, Junction to Ambient  | JEDEC (JESD 51)        | –    | 60 | °C/W |
| ESD <sub>HBM</sub> | ESD Protection (Human Body Model) | JEDEC (JESD 22 - A114) | 2000 | –  | V    |
| UL-94              | Flammability Rating               | UL (Class)             | V-0  |    |      |

**Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**DC Electrical Specifications**

| Parameter                  | Description                   | Condition                                                  | Min.                  | Max.                  | Unit |
|----------------------------|-------------------------------|------------------------------------------------------------|-----------------------|-----------------------|------|
| VDD core                   | 3.3V Operating Voltage        | $3.3 \pm 5\%$                                              | 3.135                 | 3.465                 | V    |
| V <sub>IH</sub>            | 3.3V Input High Voltage (SE)  |                                                            | 2.0                   | V <sub>DD</sub> + 0.3 | V    |
| V <sub>IL</sub>            | 3.3V Input Low Voltage (SE)   |                                                            | V <sub>SS</sub> – 0.3 | 0.8                   | V    |
| V <sub>IHI2C</sub>         | Input High Voltage            | SDATA, SCLK                                                | 2.2                   | –                     | V    |
| V <sub>ILI2C</sub>         | Input Low Voltage             | SDATA, SCLK                                                | –                     | 1.0                   | V    |
| V <sub>IH_CTRL_INPUT</sub> | Input High Voltage            | Applies to all input and latched pins                      | 0.7                   | VDD+0.3               | V    |
| V <sub>IL_CTRL_INPUT</sub> | Input Low Voltage             | Applies to all input and latched pins                      | V <sub>SS</sub> – 0.3 | 0.35                  | V    |
| I <sub>IH</sub>            | Input High Leakage Current    | Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$ | –                     | 5                     | μA   |
| I <sub>IL</sub>            | Input Low Leakage Current     | Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$   | –5                    | –                     | μA   |
| V <sub>OH</sub>            | 3.3V Output High Voltage (SE) | I <sub>OH</sub> = –1 mA                                    | 2.4                   | –                     | V    |
| V <sub>OL</sub>            | 3.3V Output Low Voltage (SE)  | I <sub>OL</sub> = 1 mA                                     | –                     | 0.4                   | V    |
| I <sub>OZ</sub>            | High-impedance Output Current |                                                            | –10                   | 10                    | μA   |
| C <sub>IN</sub>            | Input Pin Capacitance         |                                                            | 1.5                   | 5                     | pF   |
| C <sub>OUT</sub>           | Output Pin Capacitance        |                                                            |                       | 6                     | pF   |
| L <sub>IN</sub>            | Pin Inductance                |                                                            | –                     | 7                     | nH   |
| V <sub>XIH</sub>           | Xin High Voltage              |                                                            | 0.7V <sub>DD</sub>    | V <sub>DD</sub>       | V    |
| V <sub>XIL</sub>           | Xin Low Voltage               |                                                            | 0                     | 0.3V <sub>DD</sub>    | V    |
| I <sub>DD_PWR_DW</sub>     | Power Down Current            |                                                            | –                     | 1                     | mA   |
| I <sub>DD_3.3V</sub>       | Dynamic Supply Current        | Default Power on, all clock active, C <sub>L</sub> =0      | –                     | 50                    | mA   |
| I <sub>DD_1.05V</sub>      | Dynamic Supply Current        | Default Power on, all clock active, C <sub>L</sub> =0      | –                     | 5                     | mA   |

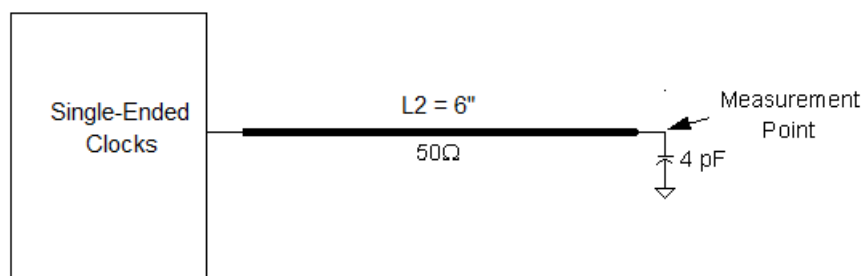
**AC Electrical Specifications**

| Parameter                               | Description                                       | Condition                                                                                         | Min. | Max.    | Unit |
|-----------------------------------------|---------------------------------------------------|---------------------------------------------------------------------------------------------------|------|---------|------|
| <b>Crystal</b>                          |                                                   |                                                                                                   |      |         |      |
| L <sub>ACC</sub>                        | Long-term Accuracy                                | Measured at VDD/2 differential                                                                    | –    | 250     | ppm  |
| <b>Clock Input</b>                      |                                                   |                                                                                                   |      |         |      |
| T <sub>DC</sub>                         | CLKIN Duty Cycle                                  | Measured at VDD/2                                                                                 | 47   | 53      | %    |
| T <sub>R</sub> /T <sub>F</sub>          | CLKIN Rise and Fall Times                         | Measured between 0.2V <sub>DD</sub> and 0.8V <sub>DD</sub>                                        | 0.5  | 4.0     | V/ns |
| T <sub>CCJ</sub>                        | CLKIN Cycle to Cycle Jitter                       | Measured at VDD/2                                                                                 | –    | 250     | ps   |
| T <sub>LTJ</sub>                        | CLKIN Long Term Jitter                            | Measured at VDD/2                                                                                 | –    | 350     | ps   |
| V <sub>IL</sub>                         | Input Low Voltage                                 | XIN / CLKIN pin                                                                                   | –    | 0.8     | V    |
| V <sub>IH</sub>                         | Input High Voltage                                | XIN / CLKIN pin                                                                                   | 2    | VDD+0.3 | V    |
| I <sub>IL</sub>                         | Input Low Current                                 | XIN / CLKIN pin, 0 < V <sub>IN</sub> < 0.8                                                        | –    | 20      | uA   |
| I <sub>IH</sub>                         | Input High Current                                | XIN / CLKIN pin, V <sub>IN</sub> = VDD                                                            | –    | 35      | uA   |
| <b>SRC at 0.7V</b>                      |                                                   |                                                                                                   |      |         |      |
| T <sub>DC</sub>                         | Duty Cycle                                        | Measured at 0V differential                                                                       | 45   | 55      | %    |
| T <sub>CCJ</sub>                        | Cycle to Cycle Jitter                             | Measured at 0V differential                                                                       | –    | 125     | ps   |
| RMS <sub>GEN1</sub>                     | Output PCIe* Gen1 REFCLK phase jitter             | BER = 1E-12 (including PLL BW 8 - 16 MHz, $\zeta$ = 0.54, Td=10 ns, Ftrk=1.5 MHz)                 | 0    | 108     | ps   |
| RMS <sub>GEN2</sub>                     | Output PCIe* Gen2 REFCLK phase jitter             | Includes PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, $\zeta$ = 0.54, Td=10 ns), Low Band, F < 1.5MHz | 0    | 3.0     | ps   |
| RMS <sub>GEN2</sub>                     | Output PCIe* Gen2 REFCLK phase jitter             | Includes PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, $\zeta$ = 0.54, Td=10 ns), Low Band, F < 1.5MHz | 0    | 3.1     | ps   |
| L <sub>ACC</sub>                        | Long Term Accuracy                                | Measured at 0V differential                                                                       | –    | 100     | ppm  |
| T <sub>R</sub> / T <sub>F</sub>         | Rising/Falling Slew Rate                          | Measured differentially from $\pm 150$ mV                                                         | 2.5  | 8       | V/ns |
| <b>CONF1_SE1 &amp; CONF_SE2 at 3.3V</b> |                                                   |                                                                                                   |      |         |      |
| T <sub>DC</sub>                         | Duty Cycle                                        | Measurement at 1.5V                                                                               | 45   | 55      | %    |
| T <sub>R</sub> / T <sub>F</sub> (48M)   | Rising and Falling Edge Rate                      | Measured between 0.8V and 2.0V                                                                    | 1.0  | 4.0     | V/ns |
| T <sub>CCJ</sub>                        | Cycle to Cycle Jitter                             | Measurement at 1.5V                                                                               | –    | 300     | ps   |
| L <sub>ACC</sub>                        | Long Term Accuracy                                | Measurement at 1.5V                                                                               | –    | 100     | ppm  |
| <b>25M at 3.3V</b>                      |                                                   |                                                                                                   |      |         |      |
| T <sub>DC</sub>                         | Duty Cycle                                        | Measurement at 1.5V                                                                               | 45   | 55      | %    |
| T <sub>R</sub> / T <sub>F</sub>         | Rising and Falling Edge Rate                      | Measured between 0.8V and 2.0V                                                                    | 1.0  | 4.0     | V/ns |
| T <sub>CCJ</sub>                        | Cycle to Cycle Jitter                             | Measurement at 1.5V                                                                               | –    | 300     | ps   |
| L <sub>ACC</sub>                        | Long Term Accuracy                                | Measured at 1.5V                                                                                  | –    | 100     | ppm  |
| <b>ENABLE/DISABLE and SET-UP</b>        |                                                   |                                                                                                   |      |         |      |
| T <sub>STABLE</sub>                     | Clock Stabilization from Power-up                 |                                                                                                   | –    | 1.8     | ms   |
| T <sub>STABLE</sub>                     | Clock Stabilization from CLKREQ and Output Enable |                                                                                                   | –    | 1.0     | ms   |
| T <sub>SS</sub>                         | Stopclock Set-up Time                             |                                                                                                   | 10.0 | –       | ns   |

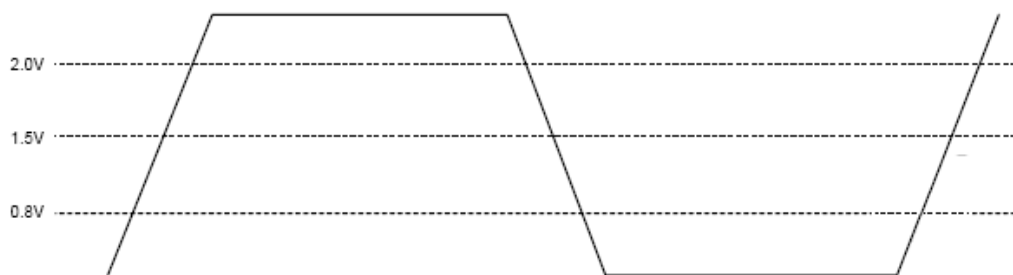
**Test and Measurement Set-up**

### For Single Ended Clocks

The following diagram shows the test load configurations for the single-ended output signals.



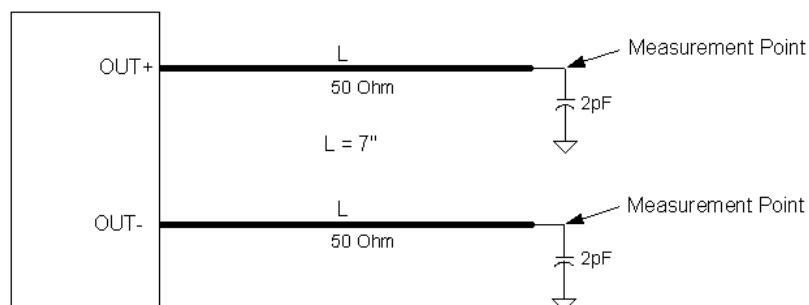
**Figure 1. Single-ended clocks Single Load Configuration**



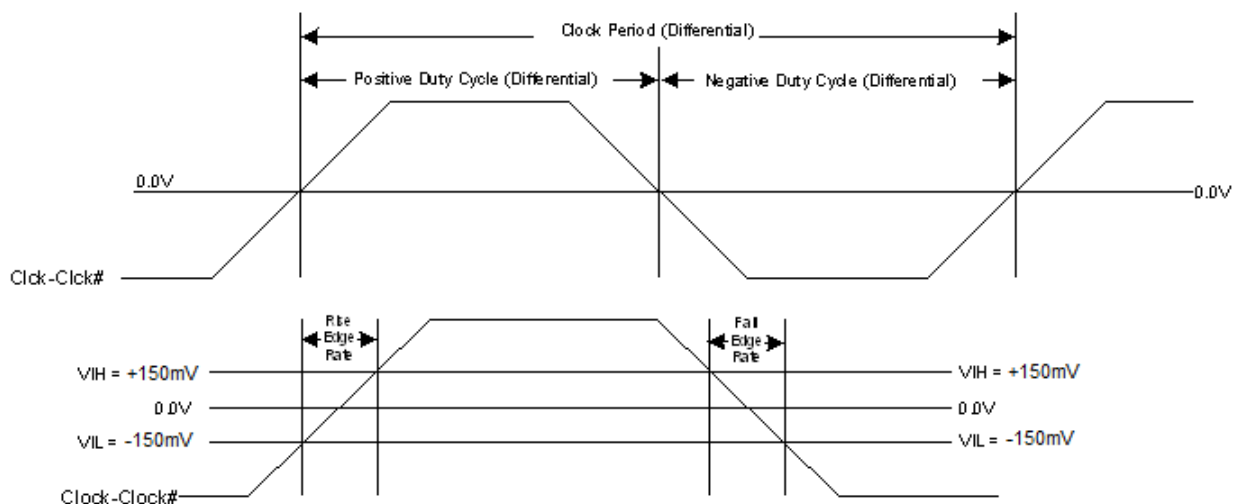
**Figure 2. Single-ended Output Signals (for AC Parameters Measurement)**

## For Differential Clock Signals

This diagram shows the test load configuration for the differential clock signals



**Figure 3. 0.7V Differential Load Configuration**



**Figure 4. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)**

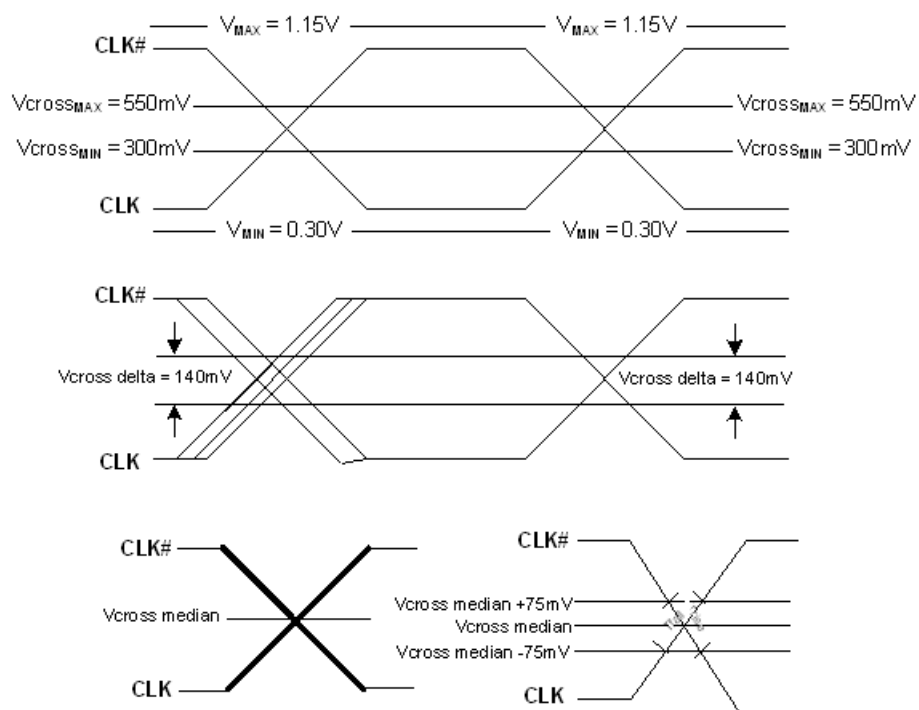


Figure 5. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

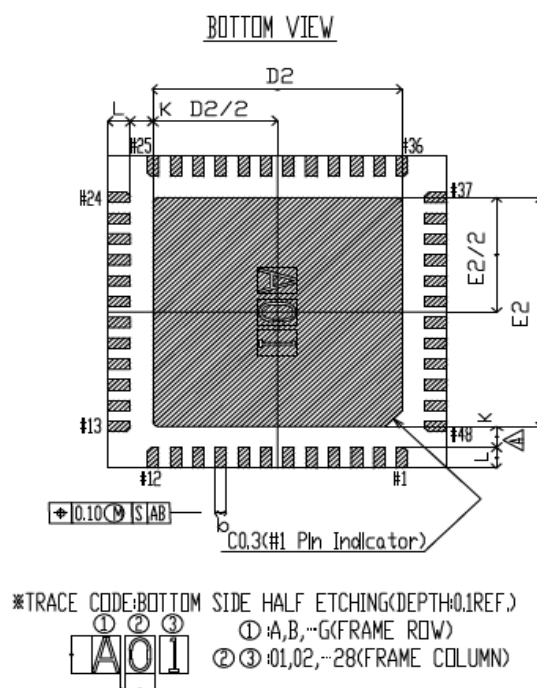
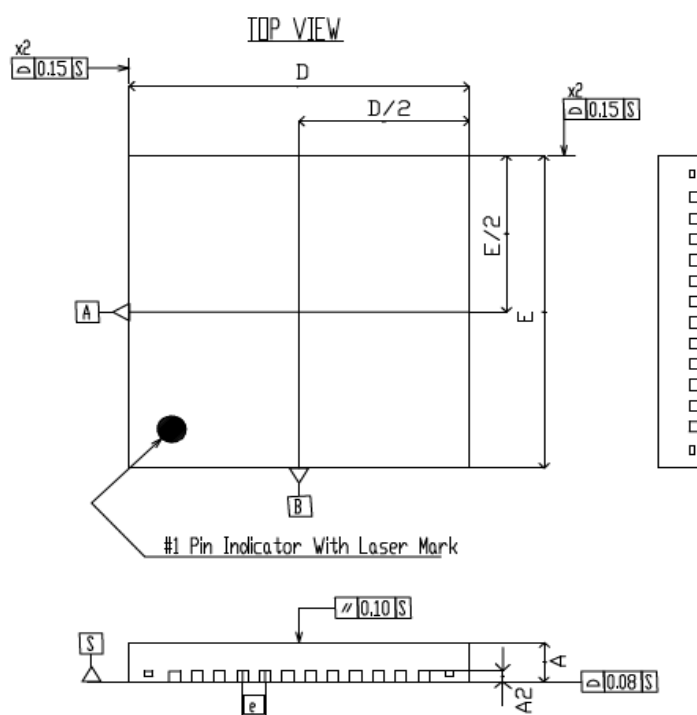
Document History Page

Ordering Information

| Part Number      | Package Type               | Product Flow             |
|------------------|----------------------------|--------------------------|
| <b>Lead-free</b> |                            |                          |
| SL28PCle50LC     | 48-pin QFN                 | Commercial, 0° to 85°C   |
| SL28PCle50LCT    | 48-pin QFN – Tape and Reel | Commercial, 0° to 85°C   |
| SL28PCle50LI     | 48-pin QFN                 | Industrial, -40° to 85°C |
| SL28PCle50LIT    | 48-pin QFN – Tape and Reel | Industrial, -40° to 85°C |

Package Diagrams

48-Lead QFN 6 x 6mm



| SYMBOL | COMMON DIMENSIONS |      |      |
|--------|-------------------|------|------|
|        | MIN               | NOM  | MAX  |
| A      | 0.70              | 0.75 | 0.80 |
| A2     | 0.20 REF.         |      |      |
| b      | 0.15              | 0.20 | 0.25 |
| D      | 5.90              | 6.00 | 6.10 |
| D2     | 4.25              | 4.40 | 4.55 |
| E      | 5.90              | 6.00 | 6.10 |
| E2     | 4.25              | 4.40 | 4.55 |
| e      | 0.40 BSC.         |      |      |
| k      | 0.36              | —    | —    |
| L      | 0.30              | 0.40 | 0.50 |

- NOTES)
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. DIMENSIONAL TOLERANCE UNLESS OTHERWISE SPECIFIED
  3. THE SURFACE OF THE PACKAGE SHALL BE RZ 4-8 $\mu$ m.
  4. PROTRUSIONS AT PKG. OUTLINE SHALL NOT EXCEED 0.10.

Document Title: SL28PCle50 PC EProClock® Generator  
DOC#: SP-AP-0758 (Rev. AA)

| REV. | Issue Date | Orig. of Change | Description of Change |
|------|------------|-----------------|-----------------------|
| AA   | 03/06/11   | JMA             | Initial Release       |

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