

Programmable Spread Spectrum Clock Generator (SSCG)

Key Features

- Wide 2.5V to 3.3V +/-10% power supply range
- 1.8V+/-5% Power Supply
- Programmable 3 outputs from 3 to 200MHz
- Low CCJ and LTJ
- Low power dissipation
- Programmable Center or Down Spread Modulation from 0.25 to 5.0%
- 8 to 48 MHz external crystal range
- 8 to 166 MHz external clock range
- Integrated internal voltage regulator
- Programmable PD#/OE/SSON#/FSEL functions
- Programmable CL at XIN and XOUT pins
- Programmable output rise and fall times
- Programmable spread spectrum modulation frequency from 30 to 120 kHz

Applications

- Printers, MFPs
- Digital Copiers
- NBPCs and LCD Monitors
- Routers, Servers and Switchers
- HDTV and DVD-R/W

Description

The SL15303 a programmable low power Spread Spectrum Clock Generator (SSCG) used for reducing Electromagnetic Interference (EMI).

The product is designed using SpectraLinear proprietary programmable **EProClock™** phase-locked loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and modulate the input clock. The modulated clock can significantly reduce the measured EMI levels, and leading to the compliance with regulatory agency requirements.

Up to 3 output clock frequencies, Spread %, output rise and fall times, crystal load, modulation frequency and PD#/OE/SSON#/FS functions can be programmed to meet the needs of wide range of applications.

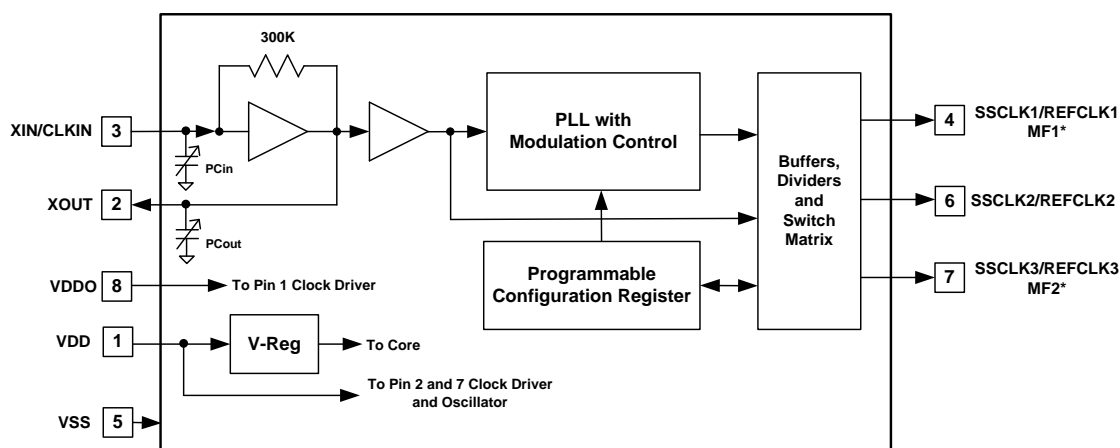
The SL15300 operates from 2.5V to 3.3V+/-10% or 1.8V+/-5% power supply voltage ranges. Contact SLI for 1.8+/-5% power supply operation specifications.

The product is offered in 8-pin TSSOP package with commercial and industrial grades.

Benefits

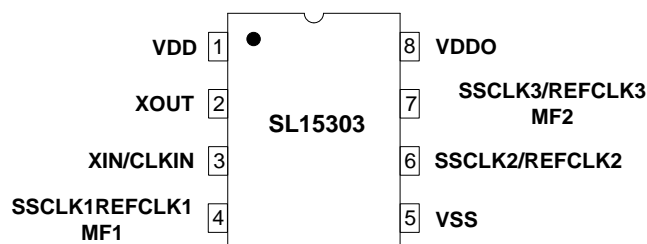
- Peak EMI reduction of 8 to 16 dB
- Fast time-to-market
- Cost Reduction
- Reduction of PCB layers
- Eliminates the need for higher order crystals (Xtals) and crystal oscillators (XOs)

Block Diagram



*MF: Programmable input control pin as PD#, OE, SSON# (Spread On/Off) or FSEL (Frequency Select)

Pin Configuration



8-Pin TSSOP

Pin Description

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|------------------------|-----------------|--|
| 1 | VDD | Power | Positive power supply pin for Pins 4 and 6 I/O (clock driver, PD#, OE, SSON# or FS), core and input oscillator. This pin can be powered as 3.3 to 2.5V or 1.8V as long as $VDDO \leq VDD$. |
| 2 | XOUT | Output | Crystal or ceramic resonator output pin. Leave this pin unconnected (floating) if external clock is used at Pin-3. |
| 3 | XIN/CLKIN | Input | Crystal, ceramic resonator or external clock input pin. |
| 4 | SSCLK1, REFCLK1 or MF1 | Output or Input | Programmable SSCLK1 or REFOUT1 clock pin or MF1 (PD#, OE, SSON# or FS control pin.) These input control pin can be programmed as Active Low or Active High) and pins can be internally programmed to have pull down (VSS), up (VDD) or no resistors. This pin is powered by VDD, Pin 1. |
| 5 | VSS | Power | Power supply ground for VDD and VSS. |
| 6 | SSCLK2, REFCLK2 | Output | This pin can be programmed as SSCLK2 or REFCLK2 clock pin and powered by VDD, Pin 1. |
| 7 | SSCLK3, REFCLK3 or MF2 | Output | Programmable SSCLK3 or REFOUT3 clock pin or MF2 (PD#, OE, SSON# or FS control pin.) These input control pin can be programmed as Active Low or Active High) and pins can be internally programmed to have pull down (VSS), up (VDD) or no resistors. This pin is powered by VDDO, Pin 8 as long as $VDDO \leq VDD$. |
| 8 | VDDO | Power | Power supply pin for Pin 7 clock driver. This pin can be powered as 3.3 to 2.5V or 1.8V as long as $VDDO \leq VDD$. |

Notes:

1. Pull-down/up resistors can be programmed to VDD or VSS as required.
2. Refer to DC electrical specifications tables for pull-down/up resistor values.

General Description

The primary source of EMI from digital circuits is the system clock and all the other synchronous clocks and control signals derived from the system clock. The well know techniques of filtering (suppression) and shielding (containment), while effective, can cost money, board space and longer development time.

A more effective and efficient technique to reduce EMI is Spread Spectrum Clock Generator (SSCG) technique. Instead of using constant clock frequency, the SSCG technique modulates (spreads) the system clock with a much smaller frequency, to reduce EMI emissions at its source: The System Clock.

The SL15303 is designed using SpectraLinear proprietary programmable **EProClock™** phase-locked loop (PLL) and Spread Spectrum Technologies (SST) to synthesize and modulate (spread) the system clock such that the energy is spread out over a wider bandwidth. This reduces the peak value of the radiated emissions at the fundamental and the harmonics.

Power Supply Operation

The SL15303 operates from 3.3V to 2.5V \pm 10% and 1.8 \pm 5% power supply ranges. Pins 7 driver is powered using VDDO where VDDO \leq VDD.

The SL15303 is available in 8-pin TSSOP package with Commercial Temperature range of 0 to 70°C and Industrial Temperature range of -40 to 85°C.

Input Frequency Range

The input frequency range is from 8.0 to 48.0 MHz for crystals and ceramic resonators. If an external clock is used, the input frequency range is from 3 to 166 MHz.

Output Frequency Range and Outputs

Up to four (3) outputs can be programmed as SSCLK, CLKOUT or REFCLK. SSCLK or CLKOUT output can be synthesized to any value from 3 to 200 MHz with spread based on valid input frequency. The spread at SSCLK pins can be stopped by SSON# input control pin. If SSON# pin is HIGH (VDD), the frequency at this pin is the synthesized to the nominal value of the input frequency and there is no spread.

REFOUT is the buffered output of the oscillator and is the same frequency as the input frequency without spread. However, REFOUT value can also be divided by using the output dividers from 2 to 32. The SSCLK is the programmed and synthesized value of the input clock. The remaining SSCLKs could be the same value providing fanout of up to 4 or the frequency can be divided from also 2 to 32. In this case, the spread % value is the same as the original programmed spread % value. By using only first order crystals, SL15300 can synthesize output frequency up to 200 MHz, eliminating the need for higher order Crystals (Xtals) and Crystal Oscillators (XOs). This reduces the cost while improving the system clock accuracy, performance and reliability.

Programmable CL (Crystal Load)

The SL15303 provides programmable on-chip capacitors at XIN/CLKIN (Pin-3) and XOUT (Pin-2). The resolution of this programmable capacitor is 6-bits with LSB value of 0.5pF. When all bits are off the pin capacitance is CXIN=CXOUT=8.5pF (minimum value). When all bits are on the pin capacitance is CXIN=CXOUT=40pF (maximum value). The values of CXIN and CXOUT based on the CL (Crystal Load Capacitor) can be calculated as: CXIN=CXOUT=2CL-CPCB. Refer to the Table 5 for additional information on crystal load (CL).

In addition, if an external clock is used, the capacitance at Pin-3 (CLKIN) can be programmed to control the edge rate of this input clock, providing additional EMI control.

Programmable Modulation Frequency

The Spread Spectrum Clock (SSC) modulation default value is 31.5 kHz. The higher values of up to 120 kHz can also be programmed. Less than 30 kHz modulation frequency is not recommended to stay out of the range audio frequency bandwidth since this frequency could be detected as a noise by the audio receivers within the vicinity.

Programmable Spread Percent (%)

The spread percent (%) value is programmable from \pm 0.25% to \pm 2.5% (center spread) or -0.5% to -5.0% (down spread) for all SSCLK frequencies. It is possible to program smaller or larger non-standard values of spread percent. Contact SLI if these non-standard spread percent values are required in the application.

SSON# or Frequency Select (FS)

The SL15303 Pin-4 can also be programmed as either SSON# to enable or disable the programmed spread percent value or as Frequency Select (FS). If SSON# is used, when this pin is pulled high (VDD), the spread is stopped and the frequency is the nominal value without spread. If low (GND), the frequency is the nominal value with the spread.

If FS function is used, the output pins can be programmed for different set of frequencies as selected by FS. SSCLK value can be any frequency from 3 to 200MHz, but the spread % is the same percent value. REFOUT is the same frequency as the input reference clock or divide by from 2 to 32 without spread. The set of frequencies in Table 1 is given as an example, using 48MHz crystal. The SL15300 also allows a fan-out of up to 4, meaning that Pins 4, 6, 7 and 8 can be programmed to the same frequencies with or without spread.

| FS (Pin-8) | SSCLK1/2 (Pins-4/7) | REFCLK4 (Pin-6) |
|---------------|------------------------|--------------------|
| 0 | 66MHz, \pm 2% | 48MHz |
| 1 | 33MHz, \pm 2% | 24MHz |

Table 1. Frequency Selection (FS)

Power Down (PD#) or Output Enable (OE)

The SL15300 Pin-4 can be programmed as either PD# or OE. PD# powers down the entire chip whereas OE only disables the output buffers to Hi-Z.

Absolute Maximum Ratings

| Description | Condition | Min | Max | Unit |
|----------------------------------|--------------------------------|--------|---------|------|
| Supply voltage, VDD | | -0.5 | 4.6 | V |
| All Inputs and Outputs | | -0.5 | VDD+0.5 | V |
| Ambient Operating Temperature | In operation, C-Grade | 0 | 70 | °C |
| Ambient Operating Temperature | In operation, I-Grade | -40 | 85 | °C |
| Storage Temperature | No power is applied | -65 | 150 | °C |
| Junction Temperature | In operation, power is applied | - | 125 | °C |
| Soldering Temperature | | - | 260 | °C |
| ESD Rating (Human Body Model) | JEDEC22-A114D | -4,000 | 4,000 | V |
| ESD Rating (Charge Device Model) | JEDEC22-C101C | -1,500 | 1,500 | V |
| ESD Rating (Machine Model) | JEDEC22-A115D | -250 | 250 | V |

DC Electrical Characteristics (C-Grade)

Unless Otherwise Stated VDD= VDDO= 3.3V to 2.5V+/- 10%, where VDDO≤VDD, CL=15pF and Ambient Temperature Range 0 to +70° C

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|---------------------------|--------|--|---------|-----|--------|------|
| Operating Voltage | VDD | VDD+/-10%, VDDO≤VDD | 2.25 | 3.3 | 3.63 | V |
| Operating Voltage | VDDO | VDD+/-10%, VDDO≤VDD | 2.25 | 3.3 | 3.63 | |
| Input Low Voltage | VIL | CMOS Level, if Pin 4 is programmed as PD#, OE, SSON# or FS | 0 | - | 0.3VDD | V |
| Input High Voltage | VIH | CMOS Level, if Pin 4 is programmed as PD#, OE, SSON# or FS | 0.7VDD | - | VDD | V |
| Output High Voltage | VOH | IOH=10mA, If Pins 4, 6, 7 and 8 are programmed as SSCLK/REFCLK | VDD-0.5 | - | - | V |
| Output Low Voltage | VOL | IOL=10mA, If Pins 4, 6 or 7 are programmed as SSCLK, CLKOUT or REFCLK | - | - | 0.5 | V |
| Input High Current | IIH | VIN=GND, Pin 4 is programmed as PD#, OE, SSON# or FS and no pull-up/down resistor used | -10 | - | 10 | μA |
| Input Low Current | IIL | VIN=GND, Pin 4 is programmed as PD#, OE, SSON# or FS and no pull-up/down resistor used | -10 | - | 10 | μA |
| Pull-up or Down Resistors | RPU/D | CMOS Level, if Pin is programmed as MF (PD#, OE, SSON# or FSEL) | 100 | 150 | 250 | kΩ |

| | | | | | | |
|--|---------------|---|-----|-----|-----|----|
| Operating Supply Current | IDD | FIN=30MHz and all 3 clocks are at 66MHz and +/-2.0% Spread and CL=0 | - | 7.8 | 9.4 | mA |
| Standby Current | ISBC | PD#=GND | - | 200 | 350 | μA |
| Output Leakage Current | IOL | Pins 4, 6 and 7 if programmed as SSCLK, CLKOUT or REFOUT | -10 | - | 10 | μA |
| Programmable Input Capacitance at Pins 2 and 3 | PCin PCout | Minimum setting value | - | 7 | - | pF |
| | | Maximum setting value | - | 40 | - | pF |
| | | Resolution (programming steps) | - | 0.5 | - | pF |
| Input Capacitance | CIN2 | Pins 4, 6 or 7 if programmed as MF (PD#, OE, SSON or FS) | - | 4 | 6 | pF |
| Load Capacitance | CL | Pins 4, 6 or 7 If programmed as SSCLK or REFCLK | - | - | 15 | pF |

AC Electrical Characteristics (C-Grade)

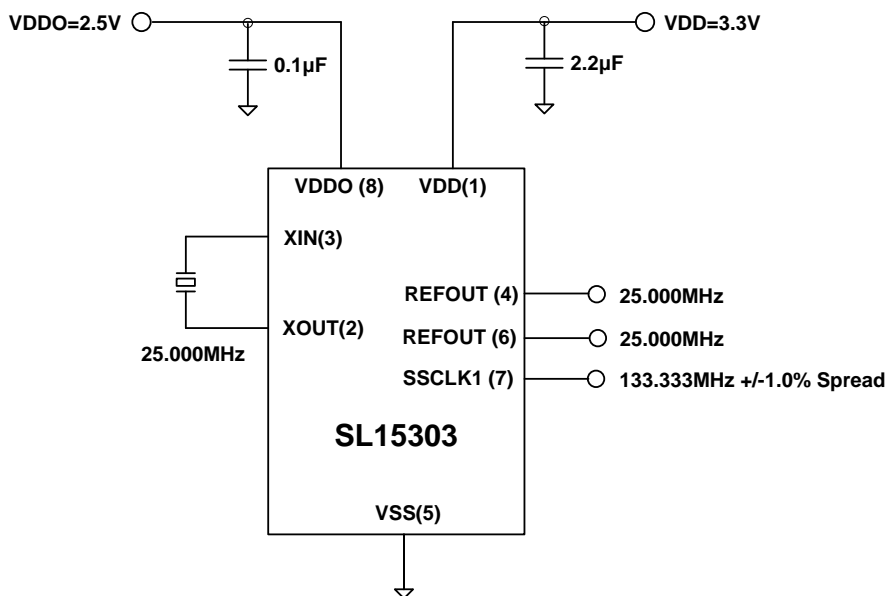
Unless Otherwise Stated VDD= VDDO= 3.3V to 2.5V+/- 10%, where VDDO≤VDD, CL=15pF and Ambient Temperature Range 0 to +70° C

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|------------------------|-----------|---|------|------|------|------|
| Input Frequency Range | FIN1 | Crystal or Ceramic Resonator | 8 | - | 48 | MHz |
| Input Frequency Range | FIN2 | External Clock | 3 | - | 166 | MHz |
| Output Frequency Range | FOUT1 | SSCLK or CLKOUT | 3 | - | 200 | MHz |
| Output Frequency Range | FOUT2 | REFCLK, crystal or resonator input | 0.25 | - | 48 | MHz |
| Output Frequency Range | FOUT3 | REFCLK, clock input | 0.25 | - | 166 | MHz |
| Output Duty Cycle | DC1 | SSCLK | 45 | 50 | 55 | % |
| Output Duty Cycle | DC2 | REFCLK , Xtal input | 45 | 50 | 55 | % |
| Output Duty Cycle | DC3 | REFCLK, clock input | 40 | 50 | 60 | % |
| Input Duty Cycle | DCIN | Clock Input, Pin 3 | 40 | 50 | 60 | % |
| Output Rise/Fall Time | tr/f1-3.3 | Programmable, VDD=VDDO=3.3V, CL=15pF, 20 to 80% of VDD/VDDO | - | 4.00 | 4.80 | ns |
| Output Rise/Fall Time | tr/f2-3.3 | Programmable, VDD=VDDO=3.3V, CL=15pF, 20 to 80% of VDD/VDDO | - | 2.00 | 2.40 | ns |
| Output Rise/Fall Time | tr/f3-3.3 | Programmable, VDD=VDDO=3.3V, CL=15pF, 20 to 80% of VDD/VDDO | - | 1.40 | 1.70 | ns |
| Output Rise/Fall Time | tr/f4-3.3 | Programmable, VDD=VDDO=3.3V, CL=15pF, 20 to 80% of VDD/VDDO | - | 1.10 | 1.35 | ns |
| Output Rise/Fall Time | tr/f5-3.3 | Programmable, VDD=VDDO=3.3V, CL=15pF, 20 to 80% of VDD/VDDO | - | 0.85 | 1.00 | ns |
| Output Rise/Fall Time | tr/f6-3.3 | Programmable, VDD=VDDO=3.3V, CL=15pF, 20 to 80% of VDD/VDDO | - | 0.70 | 0.85 | ns |

| | | | | | | |
|--|-----------|--|----------|------|--------|-----|
| Output Rise/Fall Time | tr/f7-3.3 | Programmable, VDD=VDDO=3.3V, CL=15pF, 20 to 80% of VDD/VDDO | - | 0.55 | 0.67 | ns |
| Output Rise/Fall Time | tr/f1-2.5 | Programmable, VDD=VDDO=2.5V, CL=15pF, 20 to 80% of VDD/VDDO | - | | | ns |
| Output Rise/Fall Time | tr/f2-2.5 | Programmable, VDD=VDDO=2.5V, CL=15pF, 20 to 80% of VDD/VDDO | - | | | ns |
| Output Rise/Fall Time | tr/f3-2.5 | Programmable, VDD=VDDO=2.5V, CL=15pF, 20 to 80% of VDD/VDDO | - | | | ns |
| Output Rise/Fall Time | tr/f4-2.5 | Programmable, VDD=VDDO=2.5V, CL=15pF, 20 to 80% of VDD/VDDO | - | | | ns |
| Output Rise/Fall Time | tr/f5-2.5 | Programmable, VDD=VDDO=2.5V, CL=15pF, 20 to 80% of VDD/VDDO | - | | | ns |
| Output Rise/Fall Time | tr/f6-2.5 | Programmable, VDD=VDDO=2.5V, CL=15pF, 20 to 80% of VDD/VDDO | - | | | ns |
| Output Rise/Fall Time | tr/f7-2.5 | Programmable, VDD=VDDO=2.5V, CL=15pF, 20 to 80% of VDD/VDDO | - | | | ns |
| Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8) | CCJ1 | FIN=25MHz, all 3 clocks are at 33MHz, +/-2.0% Spread. CL=15pF | - | 130 | - | ps |
| Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8) | CCJ2 | FIN=25MHz, all 3 clocks are at 66MHz, +/-2.0% Spread. CL=15pF | - | 100 | - | ps |
| Power-down Time | tPD | Time from PD# falling edge to Hi-Z at outputs (Asynchronous) | - | 150 | 350 | ns |
| Power-up Time (Crystal or Resonator) | tPU1 | Time from PD# rising edge to valid frequency at outputs (Asynchronous) | - | 3.5 | 5.0 | ms |
| Power-up Time (Clock) | tPU2 | Time from PD# rising edge to valid frequency at outputs (Asynchronous) | - | 2.0 | 3.0 | ms |
| Output Enable Time | tOE | Time from OE falling edge to Hi-Z at outputs (Asynchronous) | - | 180 | 350 | ns |
| Output Disable Time | tOD | Time from OE falling edge to Hi-Z at outputs (Asynchronous) | - | 180 | 350 | ns |
| Spread Percent Range | SPR-1 | Center Spread, SSCLK-1/2/3/4 | +/-0.125 | - | +/-2.5 | % |
| Spread Percent Range | SPR-2 | Down Spread, SSCLK-1/2/3/4 | -5.0 | - | -0.25 | % |
| Spread Percent Variation | ΔSS% | Variation of programmed Spread % | -15 | - | 15 | % |
| Modulation Frequency | FMOD | Programmable, 31.5 kHz standard | 30 | 31.5 | 120 | kHz |

External Components & Design Considerations

Typical Application Schematic



Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1µF must be used between VDD and VSS on the pins 1 and 5. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin.

Series Termination Resistor: A series termination resistor is recommended if the distance between the outputs (SSCLK or REFCLK pins) and the load is over 1 ½ inch. The nominal impedance of the SSCLK output is about 30 Ω. Use 20 Ω resistor in series with the output to terminate 50Ω trace impedance and place 20 Ω resistor as close to the SSCLK output as possible.

Crystal and Crystal Load: Use only parallel resonant fundamental crystals. DO NOT USE higher overtone crystals. To meet the crystal initial accuracy specification (in ppm); the internal on-chip programmable capacitors PCin and PCout must be programmed to match the crystal load requirement. These values are given by the formula below:

$$PCin(pF) = PCout(pF) = [(CL(pF) - Cp(pF)/2)] \times 2$$

Where CL is crystal load capacitor as given by the crystal datasheet and Cp(pF) is the compensation factor for the total parasitic capacitance at XIN or XOUT pin including PCB related parasitic capacitance.

As an example; if a crystal with CL=18pF is used and Cp=4pF, by using the above formula, PCin=PCout=[(18-(4/2))] x 2 = 32pF. Programming PCin and PCout to 32pF assures that this crystal sees an equivalent load of 18pF and no other external crystal load capacitor is needed. Deviating from the crystal load specification could cause an increase in frequency accuracy in ppm. Refer to the Table 5 for the recommended crystal specifications.

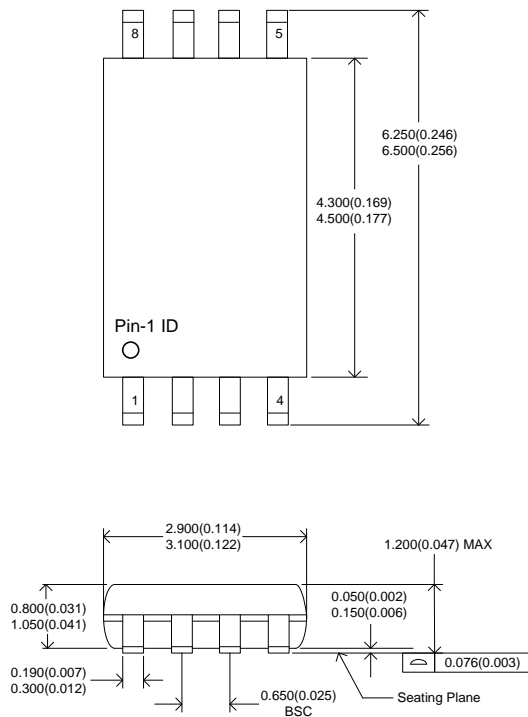
Recommended External Crystal Specifications

| Parameter | Description | Min | Typ | Max | Unit | Comments |
|-----------|---------------------------------|------|-----|-----|------|--------------------------------------|
| FNOM | Nominal Crystal Frequency Range | 8 | - | 48 | MHz | Fundamental Mode – AT Cut |
| CL | Nominal Crystal Load | 6 | 12 | 18 | pF | Load for +/-0 ppm Fo resonance value |
| R1,1 | Equivalent Series Resistance | 20 | 40 | 100 | Ohm | F-Range: 8.0 to 12.999 MHz |
| R1,2 | Equivalent Series Resistance | 12.5 | 25 | 60 | Ohm | F-Range: 13.0 to 19.999 MHz |
| R1,3 | Equivalent Series Resistance | 10 | 20 | 50 | Ohm | F-Range: 20.0 to 48.000 MHz |
| DL1,1 | Crystal Drive Level | - | - | 200 | μW | F-Range: 8.0 to 19.999 MHz |
| DL1,2 | Crystal Drive Level | - | - | 150 | μW | F-Range: 20.0 to 48.000 MHz |
| Co1 | Shunt Capacitance | - | 4 | 5.4 | pF | SMD Xtals |
| Co2 | Shunt Capacitance | - | 5 | 7.2 | pF | Through Hole (Leaded) Xtals |

Table 5. Recommended Crystal Specifications

Package Outline and Package Dimensions

8-Pin TSSOP Package (173 Mil)



Dimensions are in millimeters (inches)
Top line: (MIN) and Bottom line: (Max)

Thermal Characteristics

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---------------|-------------------------|-----|-----|-----|------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | - | 110 | - | °C/W |
| | θ_{JA} | 1m/s air flow | - | 100 | - | °C/W |
| | θ_{JA} | 3m/s air flow | - | 80 | - | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | Independent of air flow | - | 35 | - | °C/W |

Ordering Information ^[1]

| Ordering Number ^[2] | Marking | Shipping Package | Package | Temperature |
|--------------------------------|----------------|------------------|-------------|-------------|
| SL15303EZC-XXX | SL15303EZC-XXX | Tube | 8-pin TSSOP | 0 to 70°C |
| SL15303EZC-XXXT | SL15303EZC-XXX | Tape and Reel | 8-pin TSSOP | 0 to 70°C |
| SL15303EZI-XXX | SL15303EZI-XXX | Tube | 8-pin TSSOP | -40 to 85°C |
| SL15303EZI-XXXT | SL15303EZI-XXX | Tape and Reel | 8-pin TSSOP | -40 to 85°C |

Notes:

1. All SLI products are RoHS compliant.
2. "XXX" is "Dash" number will be assigned by SLI for the final programmed samples and production units based on the each customer programming requirements.

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