Quick start ADC1415S, ADC1215S, ADC1115S, ADC1015S series (F1 or F2 versions)

Demonstration board for ADC1415S, ADC1215S, ADC1115S, ADC1015S series

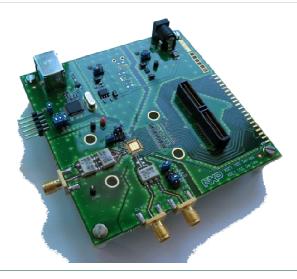
Rev. 5 — January 2011

Quick start

Document information

Info	Content
Keywords	PCB2122-2, Demonstration board, ADC, Converter
Abstract	This document describes how to use the demonstration board for the analog-to-digital converter ADC1415S, ADC1215S, ADC1115S, ADC1015S series.

Overview





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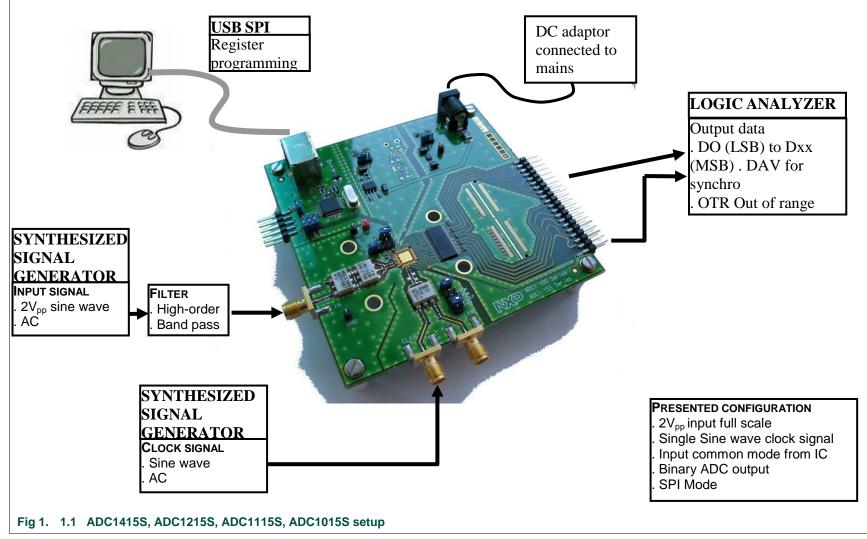
Revision history

Rev	Date	Description
1	20081001	Initial version.
2	20090518	Update
3	20090610	Add SPI software description.
4	20100519	Add HSDC extension module acquisition system description.
5	20110120	Update with latest software tool.



1.1 ADC1415S, ADC1215S, ADC1115S, ADC1015S F1 series (CMOS digital outputs)

Figure below presents the connections to measure ADC161xS.

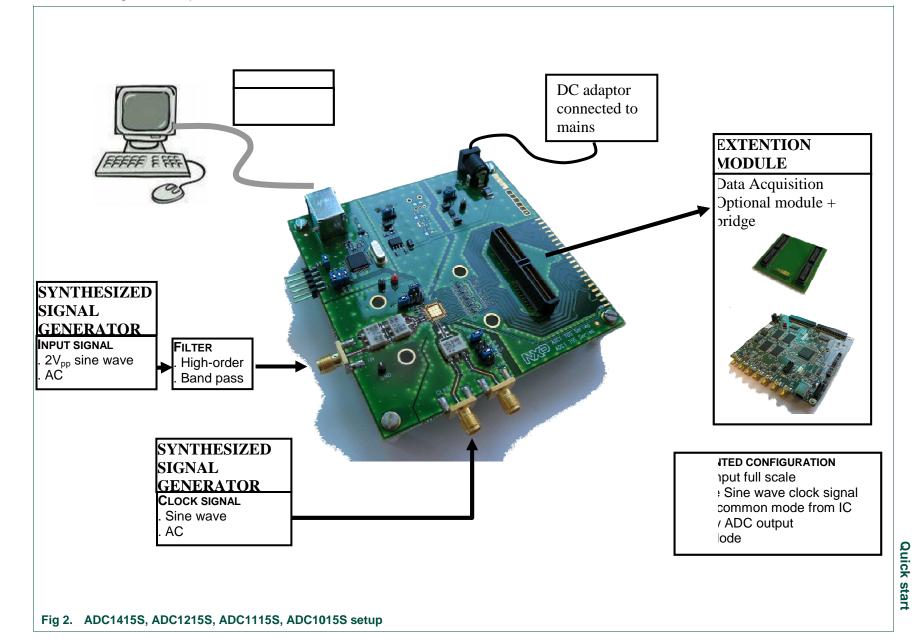


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Quick start ADC1415S, ADC1215S, ADC1115S, ADC1015S series (F1 or F2 versions)

1.2 ADC1415S, ADC1215S, ADC1115S, ADC1015S F2 series (LVDS/DDR digital outputs)

Figure below presents the connections to measure ADC1x15S.



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1.3 Power supply

The board is powered either with a 3 V_{DC} and 1.8/3 V_{DC} power supplies or a 5V DC adaptor.

Table 1	. Power supply	
Name	Function	View
J8	2.1 Jack connector – 5VDC	J10 / J11 1 1
	Change ST9 and ST10 position accordingly	
J10	+3V green connector – Power supply 3 V_{DC}	TP1
J11	Change ST9 and ST10 position accordingly	ST 9/10
	CMOS version	
	+1.8V green connector – Power supply 1.8 V_{DC}	
	LVDS DDR version	O POINT
	+3V green connector – Power supply 1.8 V_{DC}	ТЪЗ
TP1	GND test point	TP2
TP2	GND test point	

1.4 Input signals (IN, CLK)

The input clock signal can be either a sine wave or a LVCMOS signal.

To ensure a good evaluation of the device, the input signal and the input clock must be synchronized together.

Moreover, the input frequency (Fi, MHz) and the clock frequency (Fclk, Msps) should follow the formula:

$$\frac{Fi}{Fclk} = \frac{M}{N}$$

, where M is an odd number of period and N is the number of samples.

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J3

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Table 2. Input signals

Name	Function	View
J1	IN connector – Analog input signal (50 Ω matching)	
J2	CLKP connector – Single ended clock input signal (50 Ω matching), with a transformer.	
J3	CLKM connector – Grounded on that demoboard	

1.5 Output signals in CMOS version (D0 to D1x, DAV, OTR)

The digital output signal is available in binary, 2's complement or gray format. A Data Valid Output clock (DAV) is provided by the device for the data acquisition.

Table 3. Output signals

Name	Function	View
J6	Array connector – ADC digital output (D0 to D1x), OTR and Data Valid (DAV)	_
		1 6

1.6 Output signals in LVDS DDR version

The digital output signal is available in binary, 2's complement or gray format. A Data Valid Output clock (DAV) is provided by the device for the data acquisition.

Table 4. Output signals

Name	Function	View
J7	Samtec QTH connector – ADC digital output (D0 to D1x) and Data Valid (DAV)	

1.7 SPI Mode

The ADC1x15S can be **controlled** either by a Serial Peripheral Interface (SPI) or by PIN.

Table 5. SPI Interface

Name	Function	View
J12	USB connector – SPI interface	
		J12

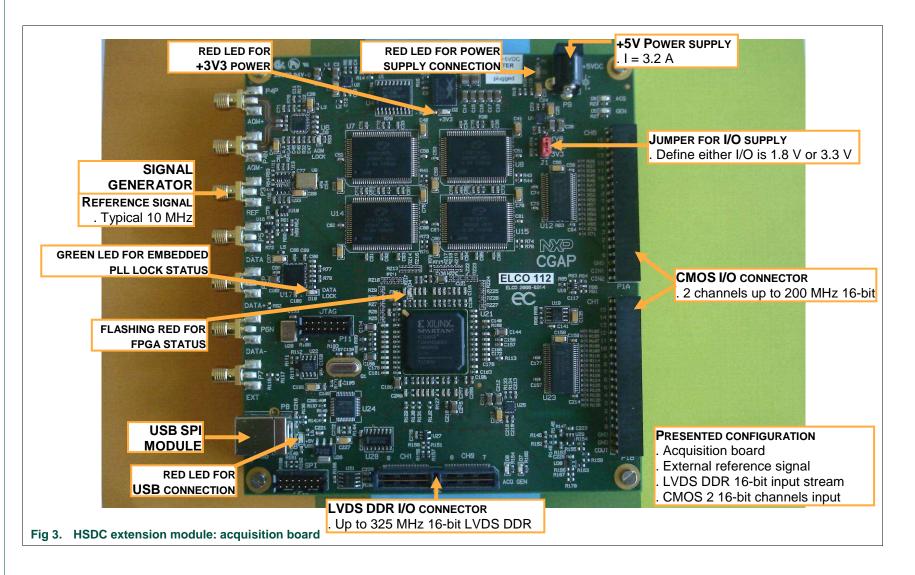
1.8 SPI program

For more details on how to control device with SPI, refer to section 3.3.

2.

HSDC extension module: acquisition board

The figure 4 shows an overview of the extension module HSDC-EXTMOD01/DB acquisition board:



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The HSDC extension module is intended for acquisition/generation and clock generation purpose. When connected to an ADC demo-board it is intended as an acquisition system for digital output bits delivered by ADC, either CMOS (HE14 P1 connector) or LVDS DDR (SAMTEC QTH_060_02 P2 connector).

The board brief specification is shown below:

- 32 MB memory size for acquisition pattern;
- 2 16-bit channels CMOS up to 200 MHz;
- 16-bit LVDS DDR input data stream up to 320 MHz;
- On-board or external reference for signal generation.

In this section the specific requirement for the use with ADC1x15S demo-board will be shown.

For more details on the HSDC-EXTMOD01/DB, please contact <u>dataconverter-</u> <u>support@nxp.com</u>.

2.1 HSDC extension module: hardware initialization

Before using the generation board, make sure that you connect the USB cable **prior to** the supply.

When USB and power cable are connected, the HSDC-EXTMOD will light 3 red LEDs.

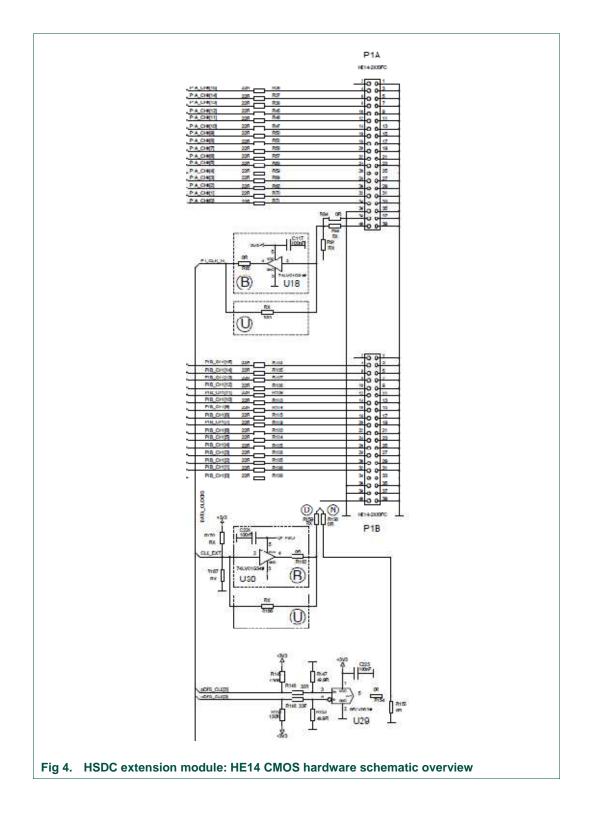
The green LED close to the PLL is only when it is locked (see section 3.3).

The red LED close to FPGA reports normal behavior when flashing $\frac{1}{4}$ on, $\frac{3}{4}$ off. Any other flashing behavior reports a failure at initialization (see section 3.3).

2.2 HSDC extension module: CMOS connector description

The <u>figure 5</u> shows a brief description of the hardware connection on the HE14 connector.

For proper use of the acquisition board, make sure that resistor R86 (0 Ω) is connected while R84 is removed.



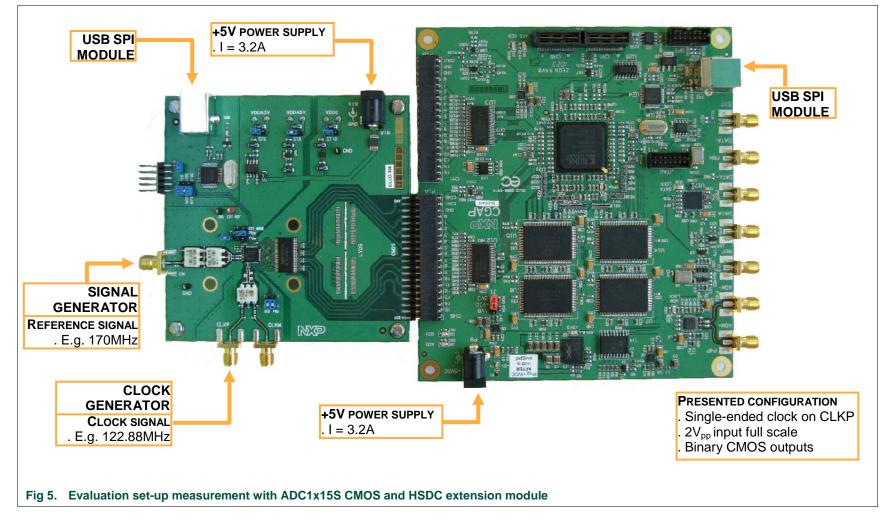
Quick start ADC1415S, ADC1215S, ADC1115S, ADC1015S series

or F2 versions

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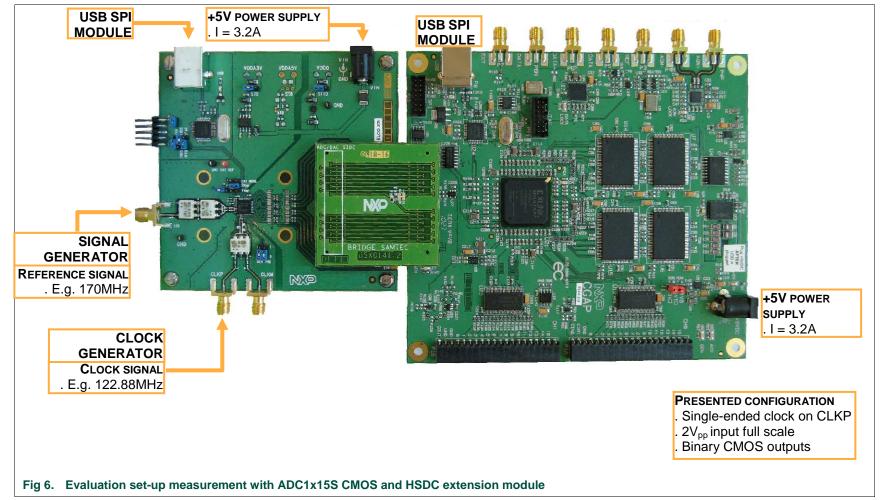
Quick start

3. Combo 1x15S and HSDC extension 3.1 ADC1415S, ADC1215S, ADC1115S, ADC1015S setup CMOS outputs at below shows an overview of the whole system ADC1x15S+HSDC extension in a cupply extension module (release A) for the The figure 24 below shows an overview of the whole system ADC1x15S+HSDC extension module with CMOS outputs configuration for which connection is straightforward, together with a supply extension module (release A) for the ADC1x15S demo-board:



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3.2 ADC1415S, ADC1215S, ADC1115S, ADC1015S setup LVDS/DDR outputs The figure 24 below shows an overview of the whole system ADC1x15S+HSDC extension module connection is straightforward, together with a supply extension module (release A) for the ADC1 The figure 24 below shows an overview of the whole system ADC1x15S+HSDC extension module with CMOS outputs configuration for which connection is straightforward, together with a supply extension module (release A) for the ADC1x15S demo-board:



Quick start ADC1415S, ADC1215S, ADC1115S, ADC1015S series (F1 or F2 versions) Quick start

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3.3 ADC Software tool

Run the application "SW_ADC_1_r02.exe". This application will allow:

- the user to control features on our high speed ADC through the SPI interface available on any ADC1415S, ADC1215S, ADC1115S, ADC1015S series;
- As well as performing any online data acquisition to evaluate the performances of the ADC1415S, ADC1215S, ADC1115S, ADC1015S series.

At start-up, the program will detect any board connected to your system and display information as can be seen on following window:

Number of sample: XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	pyright NXP semiconductors 2010	REFRESH Stop acquisition before any action. NXP HSDC ADC acquisition software		aa con	3 QUIT	.
Open and the processing of the proc	ADCI1155125 C esolution 11 122.88 22.88 22.99 22.90 frequency Fin (max. 600 MHz)	Acquisition Fin and Fs are: Fit coharent (Hc) Fi		ax. 255 trial		-
CPUCS Item AOC Unit INDS 0	65536					
OLVOS 20 OLVOS 20 OLVOS 20 OLVOS 20 INTIALIZATION 0 Output log 90 HOL CELTINOC found 00 HOC EXTINOC found 00 HOC EXTINO			Item	ADC	Unit	
Christer 5.000 Mre Amplitude -9.07 defs Output log -0.0 -0.0 Output log -0.0 -0.0 HEDCESTIMON Fund -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.0 -0.		20-				
Other Horizania Ho	OLVDS			5.000	MHz	
Initialization 390 Output log 40 HICC-EXTIMOD Fund 56.23 HOC-EXTIMOD Fund 56.23 HOC 570.8 HOC-EXTIMOD Fund 570.8 HOC-EXTIMOD Fund 56.23 HOC 570.8 HOC-EXTIMOD Fund 56.23 HOC 570.8 HOC-EXTIMOD Fund 58.10 HOC-EXTIMOD Fund 58.10 HOC-EXTIMOD Fund 58.10 HOC-EXTIMOD Fund 58.00 HOC-EXTIMOD Fund 58.00 HOC-EXTIMOD Fund 58.00 HOC-EXTIMOD Fund		0-	Amplitude	-0.937	dBFS	
Initialization -00-		H				
(4) INITIALIZATION Output log HSDC-EXTMOD Fund HSDC-EXTMOD Fun	-	-20 -		65.29	dBc	
INITIALIZATION 0 40 50 50 80 10.5 80 10.5 80 10.5 80 10.5 80 10.5 80 10.5 80 10.5 80 10.5 80 80 10.5 80 80 10.5 80 80 10.5 80	(4)		SNR		dBFS	
Output log 30 40 100 100.5 970.8 83.10 d85 HIGC-EXTINOD found HISC-EXTINOD is installed -100 -10			SINAD	65.19	dBc	
HEDC-EXTMOD is invalued -100- -120- -100-	INITIALIZATION		ENOB	10.54	bits	
HEDC-EXTMOD is invalued -100- -120- -100-	de dista	9 -60 -				
HEDC-EXTMOD is invalued -100- -120- -140-			SEDR	83.10	dBFS	
HEDC-EXTMOD is invalued -100- -120- -140-		5 -80 - 1				
-100 - -100 - -100 - -100 -			ADC Harmonics			
-120- -140-1				-104.107	dBc	
-100		-120-				
-140 - 112 - 560 dBc		the different lateration in a second reaction was a laterated and				
H6 -112.560 dBc			HS		dBc	
			H6	-112,560	dBc	
-160 - ADC Code excursion		-160 -	ADC Code excursion			
0 10M 20M 30M 40M 50M 61.43M Min 103 codes				103	codes	
Frequency (Hz) Max 1942 codes		Frequency (Hz)				
SAVE SETTINGS	SAVE SETTINGS	*1.(00) 1*				
	and the second se		A STOCKED (12510.0000.	(nonestrated)	
RESTORE SETTINGS	DESTORE SETTINGS					

①: "NXP Banner Button" will display your default internet browser to the NXP data converter home page;

②: "REFRESH" allows you to poll your system for any hardware change. It will reset any board connected to your system;

③: "QUIT" allows you quit the application;

④: "INITIALIZATION" allow you to initialize the HSDC-EXTMOD board prior to any acquisition task.

In the example above, the HSDC-EXTMOD has been detected, as well as ADC1115S125.

At this moment, make sure that 4 LEDs are visible on the HSDC-EXTMOD (2 close to power plug, 1 for USB and 1 close to FPGA).

The "Info" page gives more details on the current hardware configuration for the HSDC-EXTMOD board:

Quick start

Device detected: Constrained: Supplier size Fit: (max: 125 Mpc): Supplier size Fit: (max: 126 Mpc):	K# SW_ADC_1	REFRESH NXP HSDC ADC acquisition software QUIT	
	Device detected: ADC11155125 Recolution II Sampling rate F1 (max. 125 Mpz) 122.8 Input frequency Fin (max. 600 MHz) 5 Number of samples 65536 0 dMoS Output log Number of samples Output log Dub as thream Output log HSDC-EXTIMOD found HSDC-EXTIMOD is initialized	HSDC-EXTMOD serial number: 272 . software version HSDC-EXTMOD dilversion is 2.0. dil version HSDC-EXTMOD version is 71.1. vhd/ version HSDC-EXTMOD VHD. version is 3. HSDC-EXTMOD VHD. version is 3. HSDC-EXTMOD version is 3. HSDC-EXTMOD dock info Clock source is Port P1 (CMOS), active on rising edge. Synthetzer is LMK03001. memory info	

The HSDC-EXTMOD is not yet initialized, so the embedded PLL (LMK03001 in this example) is not locked. Initialization is only required for acquisition purpose.

Quick start

3.3.1 ADC SPI programming Functional Registers page

The page displays all SPI i	egisters for ADC1115S series:
-----------------------------	-------------------------------

pyright NXP semiconductors 2010	REFRESH NXP HSDC ADC acquisition software
Device detected: ADC1115512 tesolution 11 Sampling rate Fs (max. 125 Mpps) 122.88 Input frequency Fin (max. 600 MHz)	ADC - Functional Registers ADC - Read Registers ADC - Load Registers Tools Acquitation Tofo ADC1115S125 SPI registers access Reset and Operating Mode SWLRST OP_MODE normal (power-up)
s Number of samples 65536 V Jaka stream O CMOS D LVDS	Input Clock Internal Reference SE_SEL DIFF/SE CLKDIV DCS_EN Input Buffer Input Buffer Differential Differenti
INITIALIZATION	Output clock shifted (ahead) by 5/16Tek Image: Clock shifted (ahead) by 5/16Tek Test Pattern Fast OTR Test Pattern Fast OTR Off Image: Clock on led pattern Off Image: Clock on led pattern Off Image: Clock on led pattern OMOS Output DAV_DRV Dav_DRV DATA_DRV Very High T High T
SAVE SETTINGS	BIT WISE Send data to device

Perform any settings and then click on the "Send data to device" button to update the device registers.

3.3.2 ADC SPI programming Read Registers page

This page can be used to read all registers by clicking on the "Read all registers" button and will display the result in the table below:

pyright NXP semiconductors 2010	REFRESH	NXP HSDC ADC acquisition softw	are		QU	Π
ADC11155125	ADC - Functional Registers ADC - Read R ADC1115S125 SPI read register		·			
ampling rate Fs (max. 125 Msps)			Register name	Address	Value	
122.88 nput frequency Fin (max. 600 MHz)	Read all	registers	Reset and operating mode	5	×O	1001
5			Clock	<u>×</u> 6	1	
			Internal reference	8	×0	
umber of samples 65536 V	Save registe	ers read to file	Input buffer	10	×3	
ata stream			Output data standard	11	×0	
⊙ CMOS ○ LVDS	Data saved to file: C:\test.txt		Output clock	12	9	1
	8		Offset	13	×0	1
			Test pattern 1	14	×0	1
			Test pattern 2	15	×0	1
rutput log			Test pattern 3	× 16	×0	1
HSDC-EXTMOD found! Device ADC1115S125 found!			Fast OTR	17	×0	1
HSDC-EXTMOD is initialized!			CMOS output	20	E	1
			LVDS DDR O/P 1	21	0	1
			LVDS DDR 0/P 2	22	×0	1
			1	0	0	~
SAVE SETTINGS			<i>p</i>			

When all registers have been read, it is possible to save the data to a text file. The settings are saved in a table-like format as shown below:

Table 6.	Typical	saving	on	text file
----------	---------	--------	----	-----------

Content of file is shown as table format

Column 1	Column 2
Address	Value
05	00
06	01
08	00
10	03
11	00
12	09
13	00
14	00
15	00
16	00
17	00

Quick start

Column 1	Column 2
20	0e
21	00
22	00

Note that all data are saved in hexadecimal format.

Click on the "Save registers read to file" button to select the file to store data to. Make sure that you store your file with ".txt" extension, this will allow you to re-use the file on the "ADC - Load Registers" page.

3.3.3 ADC SPI programming Load Registers page

This page allows downloading configuration data to the device registers:

copyright NWP semiconductors 2010	REFRESH	NXP HSDC ADC acquisition soft	ware		QUI	
Device detected: ADC11155125 T Resolution	ADC - Functional Registers ADC - Read Registers ADC1115S125 SPI load registers Load data from text file (".stt"):	ADC - Load Registers Tools Acquisition	Info Register name) Address	Value	
Sampling rate Fs (max. 125 Msps)	G:\test.txt	2	Reset and operating mode	5	0	^
Input frequency Fin (max. 600 MHz)		0-	Clock	6	1	
			Internal reference	8	×0	
Number of samples 65536	Load data	2	Input buffer	10	3	
Data stream			Output data standard	11	0	
	download don		Output clock	12	9	
	j download dow	<u>* 3</u>	Offset	13	0	
			Test pattern 1	14	0	
			Test pattern 2	15	20	
Output log			Test pattern 3	16	0	
HSDC-EXTMOD found! Device ADC1115S125 found! HSDC-EXTMOD is initialized!			Fast OTR	17	0	
HSDC-EXTMOD IS Initialized			CMOS output	20	E	
			LVDS DDR O/P 1	21	0	
			LVDS DDR O/P 2	22	0	
			J.	0	0	~
SAVE SETTINGS RESTORE SETTINGS						

It is not necessary to have a file that has the whole set of registers listed. The only restriction is regarding the formatting of the file as given in <u>section 3.3.2</u>.

Note: this page cannot be used to download data saved during the comparison process.

To download settings onto device registers, follow the procedure below:

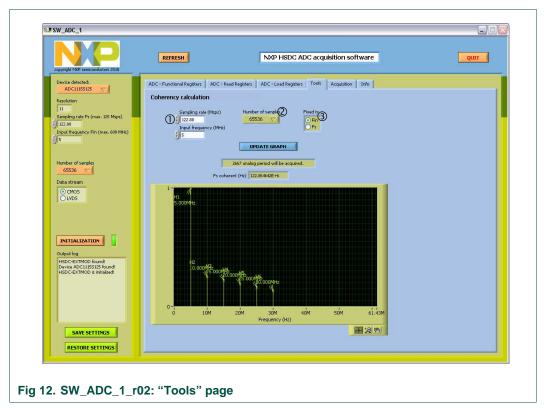
- Browse to select your file (button ①);
- Click on "Load data" button 2.

A message on field ③ and a progress bar will inform about the status of the operation until message "download done!" is seen. The table ④ is updated with the current values downloaded at the fly as can be seen on figure 13.

3.3.4 Tools page

This page allows the user to calculate the coherent frequencies values involved of the acquisition process. It gives an indication where the 6 first harmonics are located in the Nyquist zone.

Enter your analog and sampling frequencies in field^①. Indicate the number of samples to be acquired^②, as well as the fixed parameter for the coherency calculation (Fs in our example above^③). Press "UPDATE GRAPH" to look at the frequency plan, it gives also the real Fin frequency (Refer to <u>appendix A.1</u> for more details on coherency calculation):



Note: The level of the harmonics shown does not reproduce the behavior of the ADC; they are only given as indication for location.

3.3.5 Acquisition page

This page will acquire data to evaluate the high dynamic performance of the device:

copyright NXP semiconductors 2010	REFRESH	NXP HSDC ADC acquisition so	ftware.		QU	Π
Device detected:	ADC - Functional Registers ADC - Read F	Registers ADC - Load Registers Tools Acquisition	Info			
ADC11155125						
Resolution	Acquisition 5	herent (Hz) Select window type:	8			
11	Pitt and Ps are: Pitted is: Ps co			orr week		
Sampling rate Fs (max. 125 Msps)	coherent O Fin 122.4 non coherent Fs	864642E+6 No window T	inable FFT averaging 910 (m	57. 200 UNS		
Input frequency Fin (max. 600 MHz)	Store to file Line Header					
()s	Results file %					200
	6					all states
Number of samples	ACQUIRE	Display ADC0				
65536 - (2)	The second se	Autoscale	1			
	FFT Spectrum Reorganized Signal	Unreconstructed Signal Histogram	1	\bigcirc		
Data stream			Item	ADC	Unit	
OCMOS 3	20-		ADC Digitized signal		-	
OLVDS			Frequency	5.000	MHz	
	0 -		Amplitude	-0.938	dBFS	
	HD		ADC AC parameters			
(4)	-20 -		SNR	65.27	dBc	
	-40 -		SNR	66.21	dBFS	
INITIALIZATION			SINAD	65.15	dBc	
	(BP) 900- -60- - H3 - H2 H4		ENOB	10.53	bits	
Output log	3 H8		SFDR	81.35 82.29	dBc	
HSDC-EXTMOD found!	6 -80 -	H5	THD	-80.77	dBFS dBc	
Device ADC1115S125 found HSDC-EXTMOD is initialized		786	ADC Harmonics	-00.77	upc	
	-100	THE REAL PROPERTY AND A DESCRIPTION OF A DESCRIPTION OF	H2	-100.549	dBc	
	-120 -		H3	-82.292	dBc	
	-120 - La Male (1840 101	and a second of the second second	H4	-103.780		
	-140 -		H5	-91.571	dBc	
			H6	-106.814	dBc	
	-160 -		ADC Code excursion			
	0 10M 20		Min	104	codes	
SAVE SETTINGS		Frequency (Hz)	Max	1942	codes	
		+ 🗷 🤫	Mean	1022.84	codes	
RESTORE SETTINGS						
	1					

Before proceeding to any acquisition, the user needs to do the following entries:

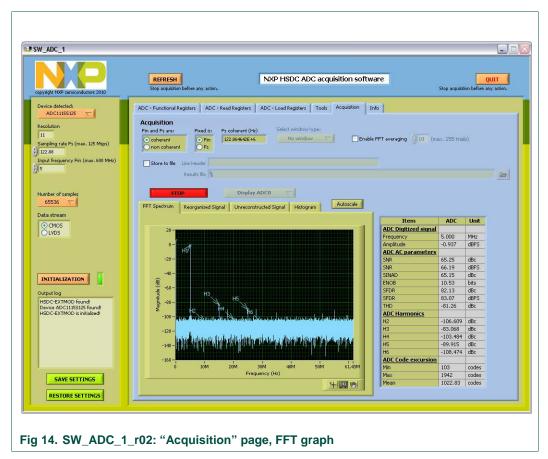
- the sampling frequency Fs: 122.88 Msps in our example (field ①);
- the input frequency Fin: 5 MHz in our example (field ①);
- the number of samples to be acquired 65536 in our example (field 2);
- indicate whether it is CMOS or LVDS DDR (field ③);
- Press the "INITIALIZATION" button. It will initialized the HSDC-EXTMOD board:
 - FPGA is ready (red LED is flashing ¼ on and ¾ off);
 - PLL embedded is locked (green LED is on);
- indicate whether Fin or Fs are coherent or not (field ⑤):
 - if signals are coherent, selected which Fin or Fs are fixed for the calculation (see <u>appendix</u> <u>A.1</u>);
 - If signals are not coherent, select the window for FFT processing to apply (the Blackman window gives better results).
- Press the "ACQUIRE" button (6) to display the results from the FFT processing. The results fields (2) will be updated automatically.
- press "STOP" ⑦ button to stop acquisition;
- field [®] allows to do FFT averaging over up to 255 trials, suitable for small signal analysis;
- Field (9) allows storing dynamic results to text file. Click on the check box, enter a header as a comment and browse to indicate where to store data file. <u>Table 7</u> shows how data are stored:

Coi	Tak	o <mark>le 7.</mark> s show	ın as ta			esults as	stored	in a tex	t file							
	Name	Fin	Fs	Vin	ENOB	SINAD_C	SNR_C	SNR_FS	SFDR_C	SFDR_FS	THD	H2	H3	H4	H5	H6
		(MHz)	(MHz)	(dBFS)	-	(dBc)	(dBc)	(dBFS)	(dBc)	(dBFS)	(dBc)	(dBc)	(dBc)	(dBc)	(dBc)	(dBc)
	ADC1115S test															
	ADC0	5.00	122.86	-0.93	10.53	65.30	65.18	66.23	81.82	82.75	-81.02	-98.65	-82.75	-102.16	-90.69	-108.62

Note that while acquisition is running, any other action (ADC SPI programming, quit or refresh) is not possible. Stop acquisition first before proceeding to any other task.

3.3.5.1 FFT spectrum

The first graph to be displayed is the FFT spectrum of the digital pattern acquired:



Press the "Autoscale" button to display the whole content.

3.3.5.2 Reorganized signal

The reorganized signal displays the reconstructed sine wave from coherency calculation corresponding to 1 period of the input signal:

pyright NKP semiconductors 2010	REFRESH NXP HSDC ADC acquisition softw Stop acquisiton hefore any action.		Stop acquisiti		UIT
vevice detected: ADC11155125 vesolution 11 ampling rate Ps (max. 125 Maps) 122.88 nput frequency Fin (max. 600 MHz) 5	Acquisition Fin and Fs are: Fixed is: Fs coherent (Hz) Select window type:	nfo	ox. 255 triak	=)	6
lumber of samples 65536 C Vata stream O CMOS UVDS	STOP Display ADC0 Autoscale FFT Spectrum Reorganized Signal Uhresconstructed Signal Histogram Autoscale 2000 - - - - - - -	Item ADC Digitized signal	ADC	Unit	
INITIALIZATION	1500 - 1500 - 1400 -	Frequency Amplitude ADC AC parameters SNR SNR SINR SINAD	5.000 -0.936 65.28 66.21 65.17	MHz dBFS dBc dBFS dBc	
Dutput log HSDC-EXTMOD found! Device ADC11155125 found! HSDC-EXTMOD is initialized!	- 1200	ENOB SFDR SFDR THD ADC Harmonics H2	10.53 82.02 82.96 -81.27 -102.508	bits dBc dBFS dBc dBc	
	400 -	H3 H4 H5 H6 ADC Code excursion	-82.955 -99.482 -91.065 -117.213	dBc dBc dBc dBc	
SAVE SETTINGS	<u>් 10000 20000 30000 40000 50000 60000 70000</u> Code 	Min Max Mean	103 1942 1022.79	codes codes codes	

Press the "Autoscale" button to display the whole content.

3.3.5.3 Unreconstructed signal

The unreconstructed signal displays the unreconstructed sine wave corresponding to the whole number of period being acquired following the coherency rule:

pyright NXP semiconductors 2010	REFRESH Stop acquisition before any action.	NXP HSDC ADC a	cquisition softwa		Stop acquisiti		UIT ny action.
evoice detected: ADCILISIZE C esculution 11 ampling rate Fs (mix. 125 Mips) 122:89 publifrequency Fin (max. 600 MHz) 5	ADC - Functional Registers ADC - Read Regist ACQuisition Fin and Fs are: Onon coherent Store to file Line Header Results file %	st (Hz) Select window type:		o	ox. 255 trial	s)	
iumber of samples 65536 😾	100 C	constructed Signal Histogram	Autoscale				
() CMOS				Item	ADC	Unit	
OLVDS	2000 -			ADC Digitized signal		1	
	1800 -			Frequency	5.000	MHz	
	1000 -			Amplitude	-0.936	dBFS	
	1600 -			ADC AC parameters	15.04	10	
				SNR	65.26 66.20	dBc dBFS	
	1400 -			SNR	65.15	dBc	
INITIALIZATION	au 1200 -			ENOB	10.53	bits	
	g			SFDR	81.96	dBc	
Dutput log	90 1000 -			SEDR	82.90	dBFS	
HSDC-EXTMOD found Device ADC1115S125 found				THD	-81.14	dBc	
HSDC-EXTMOD is initialized!	800 -			ADC Harmonics		dec	
	600 -			H2	-98.069	dBc	
				H3	-82.897	dBc	
	400 -			H4	-101.922	dBc	
	200 -			H5	-90.765	dBc	
	200-			H6	-108,493	dBc	
	0-			ADC Code excursion			
	0 10000 20000		60000 70000	Min	103	codes	
SAVE SETTINGS		Code		Max	1942	codes	
SHIESEITINGS			+ 2 1	Mean	1022.83	codes	
RESTORE SETTINGS		Zoom tool	and the second s				
NEW OKL SETTINGS	184m	Zoom tool					

Press the "Autoscale" button to display the whole content.

Use the zoom tool to observe in more details all the captured data.

3.3.5.4 Histogram

The histogram graph shows the distribution of output codes. This graph shows which code is present and if there is any missing code in the conversion range:

vright NXP semiconductors 2010	REFRESH NXP HSDC ADC acquisition softw Stop acquisition before any action.	are	Stop acquisit		UIT
vice detected; ADC11155125 C solution 1 mpling rate Fs (max. 125 Misps) 22.88 put frequency Fin (max. 600 MHz)	Acquisition Fin and Fs are: Fixed is: Fs coherent (Hz) Select window type:	nfo	ax. 255 trial	s)	
umber of samples 65536 T	STOP Display ADC0 FFT Spectrum Reorganized Signal Unreconstructed Signal Histogram Autoscale				
ata stream		Item	ADC	Unit	
⊙ CMOS ◯ LVDS	750	ADC Digitized signal			
JL#05	700 -	Frequency	5.000	MHz	
	650 -	Amplitude	-0.935	dBFS	
		ADC AC parameters			
	600 -	SNR	65.27	dBc	
		SNR	66.21	dBFS	
	500 -	SINAD	65.16	dBc	
INITIALIZATION	450 -	ENOB	10.53	bits	
utput log	8 400 - 2 350 -	SFDR	81.67	dBc	
ISDC-EXTMOD found	ਤੋਂ 350 –	SFDR	82.60	dBFS	
evice ADC1115S125 found!	Ö 300 -	THD	-80.91	dBc	
ISDC-EXTMOD is initialized!	250-	ADC Harmonics			
		H2	-97.376	dBc	
	200	H3	-82.605	dBc	
	150 -	H4	-105.907	dBc	
	100-	H5	-90.972	dBc	
	50-	H6	-103.965	dBc	
		ADC Code excursion			
	0 200 400 600 800 1000 1200 1400 1600 1800 2000 2200	Min	103	codes	
	Code	Max	1942	codes	
SAVE SETTINGS	+ 🔍 🕪	Mean	1022.81	codes	
RESTORE SETTINGS					

Press the "Autoscale" button to display the whole content.

The table shows the range of output codes.

3.3.6 Info page

This page will give practical information related to software and hardware settings:

pyright NXP semiconductors 2010	REFRESH NXP HSDC ADC acquisition software Step sequilition before any action. Step sequilition between any action.	QUIT one any action.
ADC1115S125	Functional Register: ADC - Load Register: Tools Acquisition Info DCC-EXTIMOD serial number: 272 Image: Constraint of the series	

The information visible on this page is:

- board serial number ①;
- HSDC software release number 2;
- HSDC-EXTMOD dll version 3;
- HSDC-EXTMOD vhdl version @;
- HSDC-EXTMOD supply status (5);
- HSDC-EXTMOD clock capability and status version 6;
- HSDC-EXTMOD memory capability .

4. Appendix A.1: coherency calculation

The coherency relies on the fact that clock and analog input signal are synchronized and the first and last samples being captured are adjoining samples: it ensures a continuous digitized time process for the FFT processing.

To achieve this, one has to

 $\frac{F_{in}}{F_{s}} = \frac{M}{N}$ follow the equation:

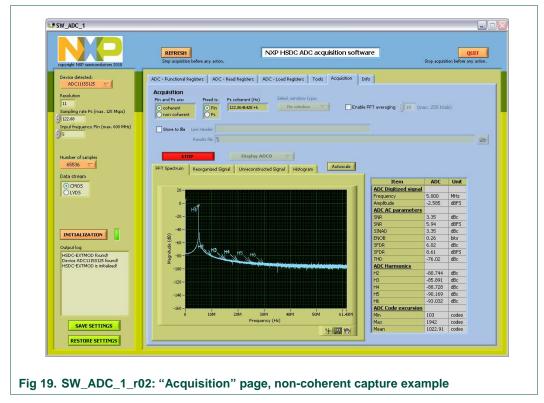
Where M is an odd integer equal to the number of periods being acquired and N the number of samples acquired.

With Fin, Fs and N known, M has to be chosen such that it follows the equation above. To do this iterative calculation, one has to decide whether Fin or Fs is fixed.

To illustrate this process, let's consider our current example with Fin = 5 MHz, Fs = 122.88Msps and N = 65536 samples acquired:

- if Fin is fixed, this leads to M = 2667 periods of input signal to be acquired and a real sampling frequency to be Fs = 122.864642 MHz;
- If Fs is fixed, this leads to M = 2667 periods of input signal to be acquired and a real input frequency to be Fin = 5.000625 MHz.

Those values needs to be programmed in the signal generator and clock generator before capture is done, otherwise the FFT calculation will lead to a non-coherent result as shown below:



The numbers given for SNR, SFDR are completely wrong if coherency is not respected.

5. Notes

For any question, feel free to contact us at the following e-mail <u>dataconverter-support@nxp.com</u>.

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