PI6C49S1510

High Performance Differential Fanout Buffer

Features

- 10 differential outputs with 2 banks
- User configurable output signaling standard for each bank: LVDS or LVPECL or HCSL
- LVCMOS reference output up to 200MHz
- Up to 1.5GHz output frequency for differential outputs
- Ultra low additive phase jitter: < 0.03 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Selectable reference inputs support either single-ended or differential or Xtal
- Low skew between outputs within banks (<40ps)
- Low delay from input to output (Tpd typ. < 1.5ns)
- Separate Input output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- TQFN-48 package

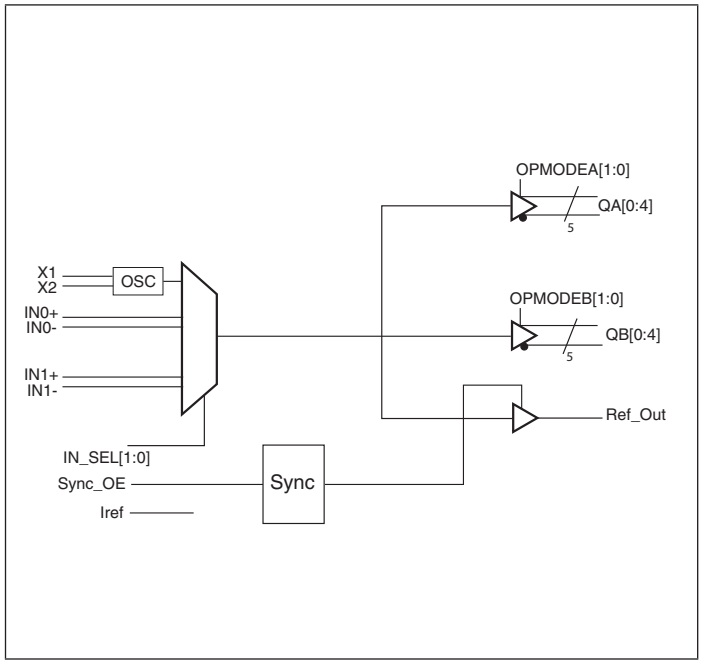
Description

The PI6C49S1510 is a high performance fanout buffer device-which supports up to 1.5GHz frequency. It also integrates a unique feature with user configurable output signaling standards on per bank basis which provide great flexibilities to users. The device also uses Pericom's proprietary input detection technique to make sure illegal input conditions will be detected and reflected by output states. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

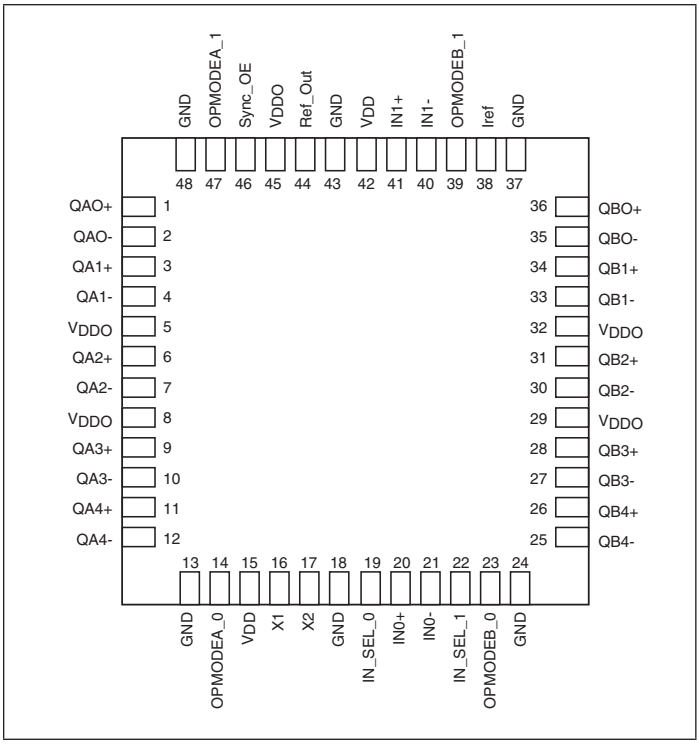
Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

Block Diagram



Pin Configuration (48-Pin TQFN)



Pinout Table

Pin #	Pin Name	Type		Description
1,2	QA0+ QA0-	Output		Bank A differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
3,4	QA1+ QA1-	Output		Bank A differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.
5,8,29,32,45	VDDO	Power		Power supply pins for IO
6,7	QA2+ QA2-	Output		Bank A differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
9,10	QA3+ QA3-	Output		Bank A differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
11,12	QA4+ QA4-	Output		Bank A differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
13,18,24,37,43,48	GND	Power		Power supply ground
14,47	OPMODEA	Input	Pulldown	Output mode select for Bank A. See Table 2 for functions, LVCMOS/LVTTL interface levels
15,42	V_{DD}	Power		Power supply pins
16	X1	Input		XTAL input
17	X2	Output		XTAL output
19,22	IN_SEL	Input	Pulldown	Input clock sele ct. See Table 1 for function. LVCMOS/LVTTL interface levels.
20	IN0+	Input	Pulldown	Reference input 0
21	IN0-	Input	Pull-up/ Pulldown	Inverted reference input 0, internal bias to $V_{DD/2}$
23,39	OPMODEB	Input	Pulldown	Output mode select for Bank B. See Table 2for functions, LVCMOS/LVTTL interface levels
26,25	QB4+ QB4-	Output		Bank B differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
28,27	QB3+ QB3-	Output		Bank B differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
31,30	QB2+ QB2-	Output		Bank B differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
34,33	QB1+ QB1-	Output		Bank B differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.

Pinout Table (Continued..)

Pin #	Pin Name	Type		Description
36,35	QB0+	Output		Bank B differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
	QB0-			
38	Iref	Output		A fixed precision resistor (475ohm) from this pin to ground provides a reference current.
40	IN1-	Input	Pull-up/ Pulldown	Inverted reference input, internal bias to $V_{DD/2}$
41	IN1+	Input	Pulldown	Reference input 1
44	Ref_Out	Output		Reference output, CMOS
46	Sync_OE	Input		Synchronous output enable for Ref_Out, see Table 3 for functions

Function Table

Table 1: Input select function

IN_SEL [1]	IN_SEL [0]	Function
0	0	IN0 is the selected reference input
0	1	IN1 is the selected reference input
1	X	XTAL is the selected input

Table 2: Output Mode select function

OPMODEA/B [1]	OPMODEA/B [0]	Output Bank A / Bank B Mode
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Hi-Z

Table 3: Reference output enable function

Sync_OE	Ref_Out
0	Hi-Z
1	Output enabled

Table 4: Illegal input level function

Input illegal status	Output status
Input open	Logic Low
Input both high	Logic Low
Input both low	Logic Low

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....-55 to +150°C
Supply Voltage to Ground Potential (V_{DD})..... -0.5 to +4.6V
Inputs (Referenced to GND) ..... -0.5 to V_{DD}+0.5V
Clock Output (Referenced to GND)..... -0.5 to V_{DD}+0.5V
Soldering Temperature (Max of 10 seconds) .....+260°C
Latch up.....200mA
ESD Protection (Input) .....2000 V min (HBM)

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		2.375		3.465	V
V_{DDO}	Output Supply Voltage		2.375		3.465	V
I_{DD}	Core Power Supply Current			90	120	mA
I_{DDO}	Output Power Supply Current	All LVPECL outputs unloaded		110	145	
		All LVDS outputs loaded		110	125	
		All HCSL outputs unloaded		70	90	
T_A	Ambient Operating Temperature		-40		85	°C

DC Electrical Specifications - Differential Inputs

Symbol	Parameter		Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			150	uA
I_{IL}	Input Low current	Input = GND	-150			uA
C_{IN}	Input capacitance			3		PF
V_{IH}	Input high voltage				V_{DD}+0.3	V
V_{IL}	Input low voltage		-0.3			V
V_{ID}	Input Differential Amplitude PK-PK		0.15		V_{DD}-0.85	V
V_{CM}	Common model input voltage		GND + 0.5		V_{DD}-0.85	V

DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			150	uA
I_{IL}	Input Low current	Input = GND	-150			uA
V_{IH}	Input high voltage	V_{DD}=3.3V	2.0		V_{DD}+0.3	V
V_{IL}	Input low voltage	V_{DD}=3.3V	-0.3		0.8	V
V_{IH}	Input high voltage	V_{DD}=2.5V	1.7		V_{DD}+0.3	V
V_{IL}	Input low voltage	V_{DD}=2.5V	-0.3		0.7	V

DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage		V_{DD}-1.4		V_{DD}-0.9	V
V_{OL}	Output Low voltage		V_{DD}-2.1		V_{DD}-1.7	V

DC Electrical Specifications- LVDS Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage			1.433		V
V_{OL}	Output Low voltage			1.064		V
Vocm	Output commode voltage			1.25		V
DVocm	Change in Vocm between completely output states				50	mV
Ro	Output impedance		85		140	Ω

DC Electrical Specifications – HCSL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage		520		900	mV
V_{OL}	Output Low voltage		0		150	mV

DC Electrical Specifications – LVCMOS Output

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage	V_{DD}=3.3V +/-5%, I_{OH} = 8mA	2.3			V
		V_{DD}=2.5V +/- 5%, I_{OH} = 8mA	1.5			V
V_{OL}	Output Low voltage	V_{DD}=3.3V +/-5%, I_{OL} = -8mA			0.5	V
		V_{DD}=2.5V +/- 5%, I_{OL} = -8mA			0.4	V

AC Electrical Specifications – Differential Outputs

Parameter	Description	Conditions		Min.	Typ.	Max.	Units
F_{OUT}	Clock output frequency	LVPECL, LVDS				1500	MHz
		HCSL				250	
T_r	Output rise time	From 20% to 80%	LVPECL	120	150	300	ps
			LVDS	120	150	300	
			HCSL	350		550	
T_f	Output fall time	From 80% to 20%	LVPECL	120	150	300	ps
			LVDS	120	150	300	
			HCSL	350		550	
T_{ODC}	Output duty cycle	Frequency<650MHz	LVPECL, HCSL	48		52	%
			LVDS	47		53	
V_{PP}	Output swing Single-ended	LVPECL outputs		400			mV
		LVDS outputs		250			
		HCSL outputs		520			
T_j	Buffer additive jitter RMS				0.03		ps
V_{CROSS}	Absolute crossing voltage	HCSL			460		mV
DV_{CROSS}	Total variation of crossing voltage	HCSL				140	mV
T_{SK}	Output Skew	10 outputs devices, outputs in same tank, with same load, at DUT.			40	70	ps
T_{PD}	Propagation Delay				1500		ps
T_{OD}	Valid to HiZ					200	ns
T_{OE}	HiZ to valid					200	ns
$T_{P2P\ Skew}$	Part to Part Skew[1]				200		ps

Notes:

1. This parameter is guaranteed by design

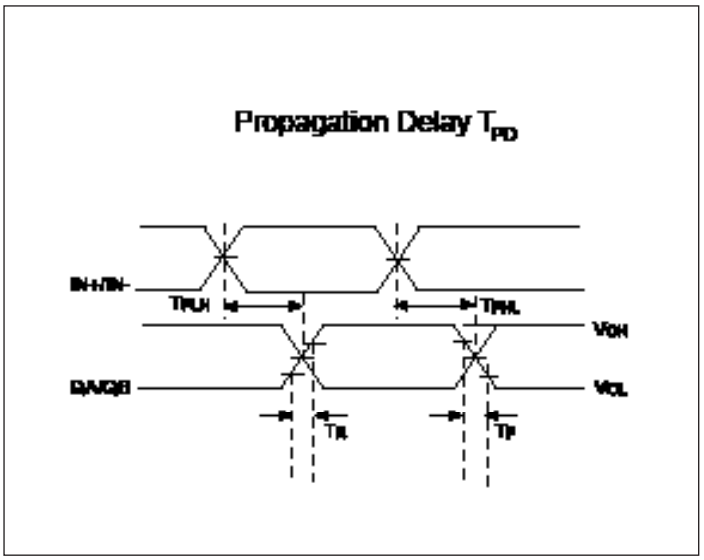
AC Electrical Specifications – CMOS

Parameter	Description	Conditions		Min.	Typ.	Max.	Units
F_{OUT}	Ref_Out frequency	XTAL input		10		50	MHz
		Reference input				200	MHz
T_j	Buffer additive jitter RMS	XTAL input			0.3		ps
		Reference input			0.03		ps
t_r/ t_f	Rise time, Fall time	C_L = 10pF			1.5		ns
T_{ODC}	Output duty cycle	C_L = 10pF		45		55	%
t_{PD}	Propagation delay			100		1500	ps
t_S	Setup time			300			ps
t_{SOD}	Clock edge to output disable	Ref_Out		2		4	cycles
t_{SOE}	Clock edge to output enable	Ref_Out		2		4	cycles

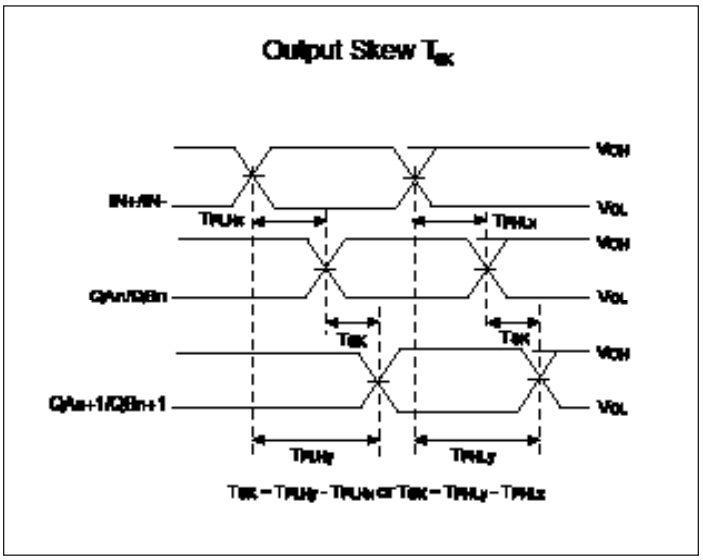
Crystal Characteristics

Parameter	Min.	Typ.	Max.	Units
Mode of Oscillation		Fundamental		
Frequency Range	10		50	MHz
Equivalent Series Resistance (ESR)			70	Ω
Shunt Capacitance			7	pF
Load Capacitance	10		18	pF

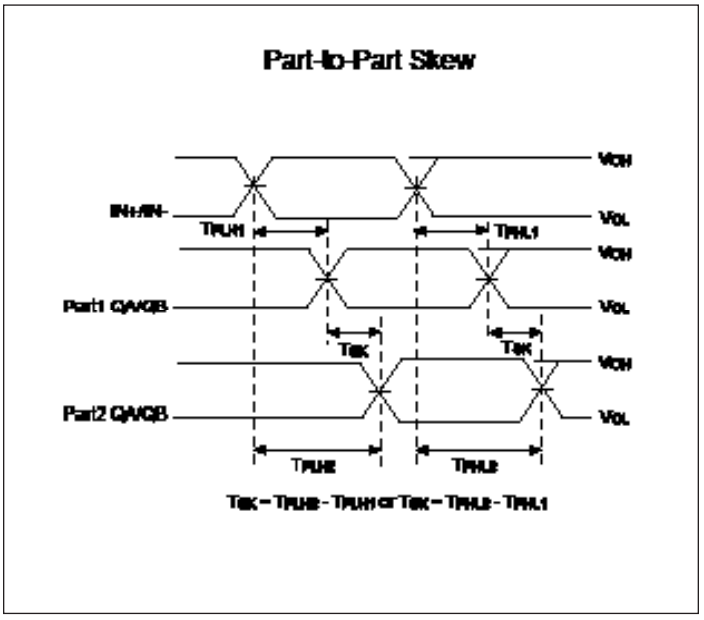
Propagation Delay



Output Skew



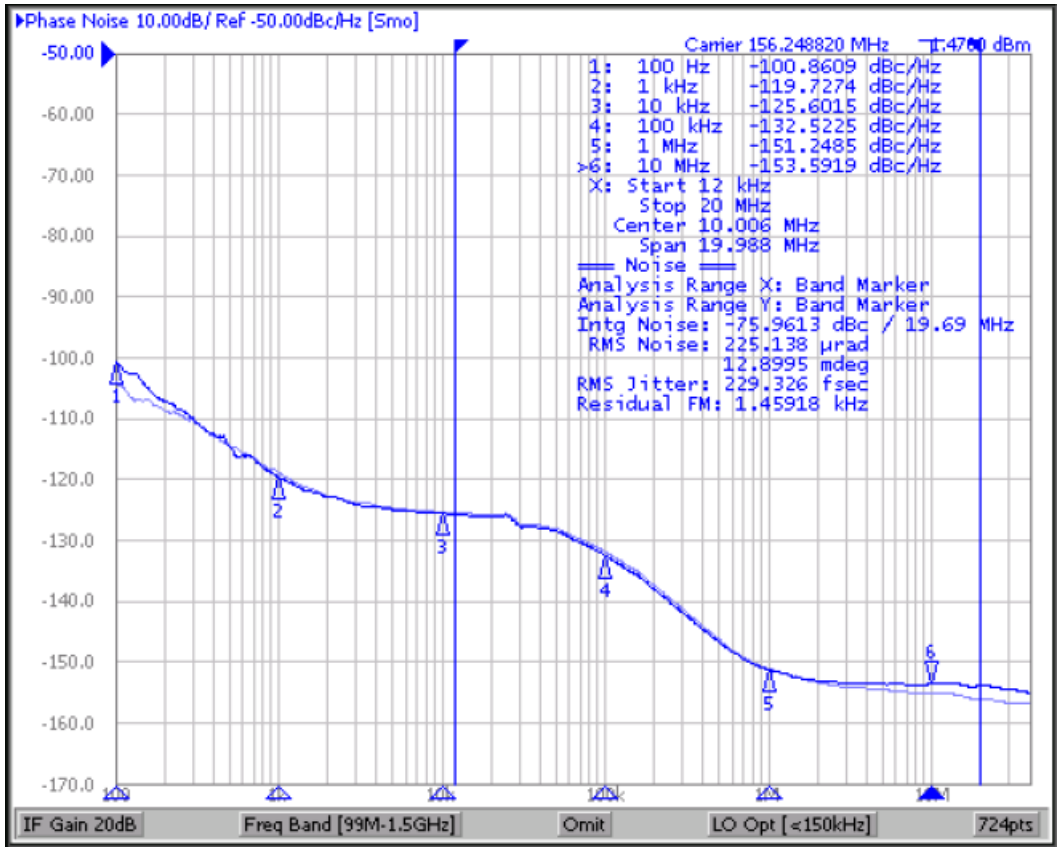
Part to Part Skew



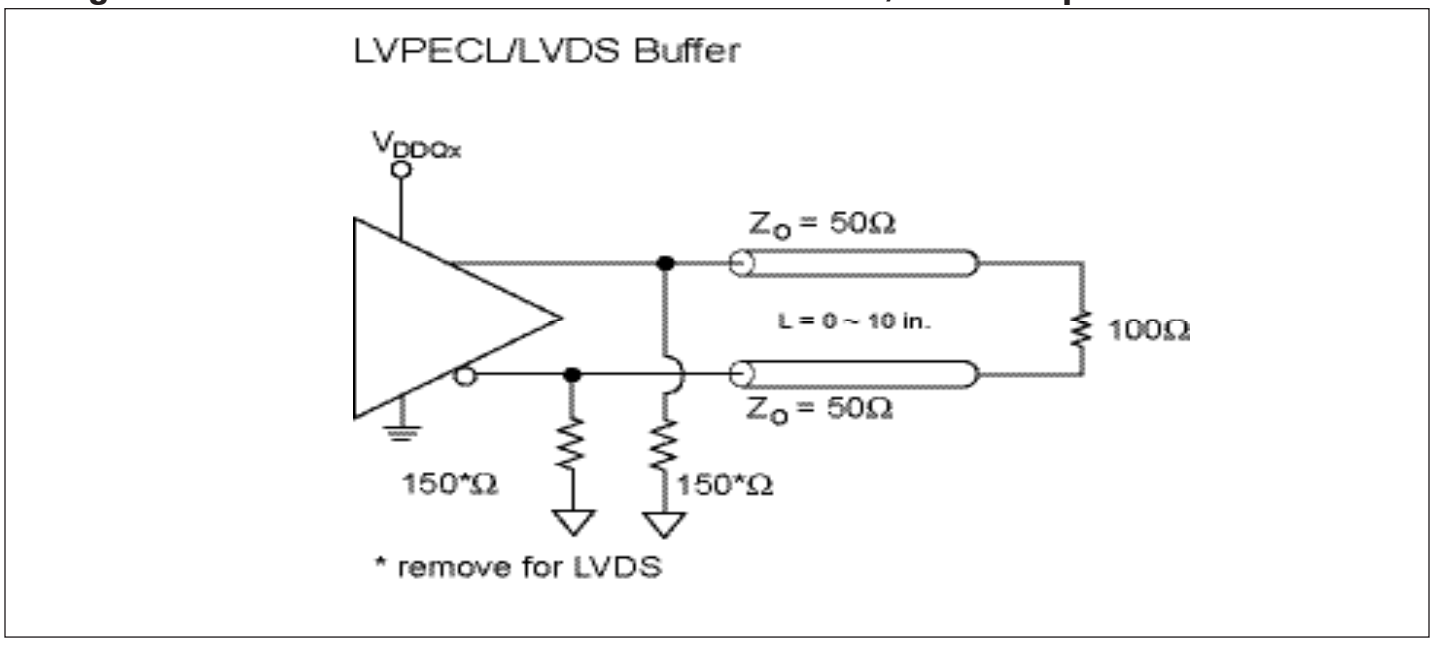
Phase Noise and Additive Jitter

Output phase noise (Dark Blue) vs Input Phase noise (light blue)

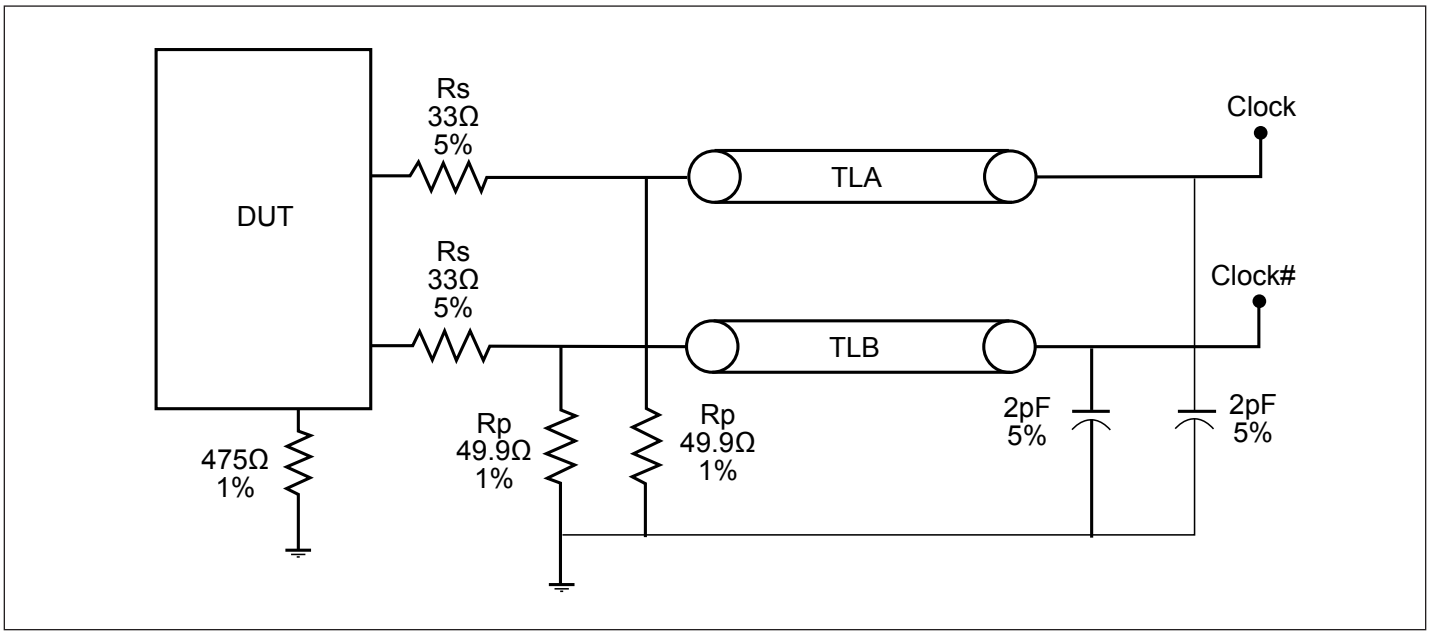
Additive jitter is calculated at ~27fs RMS (12kHz to 20MHz). Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$



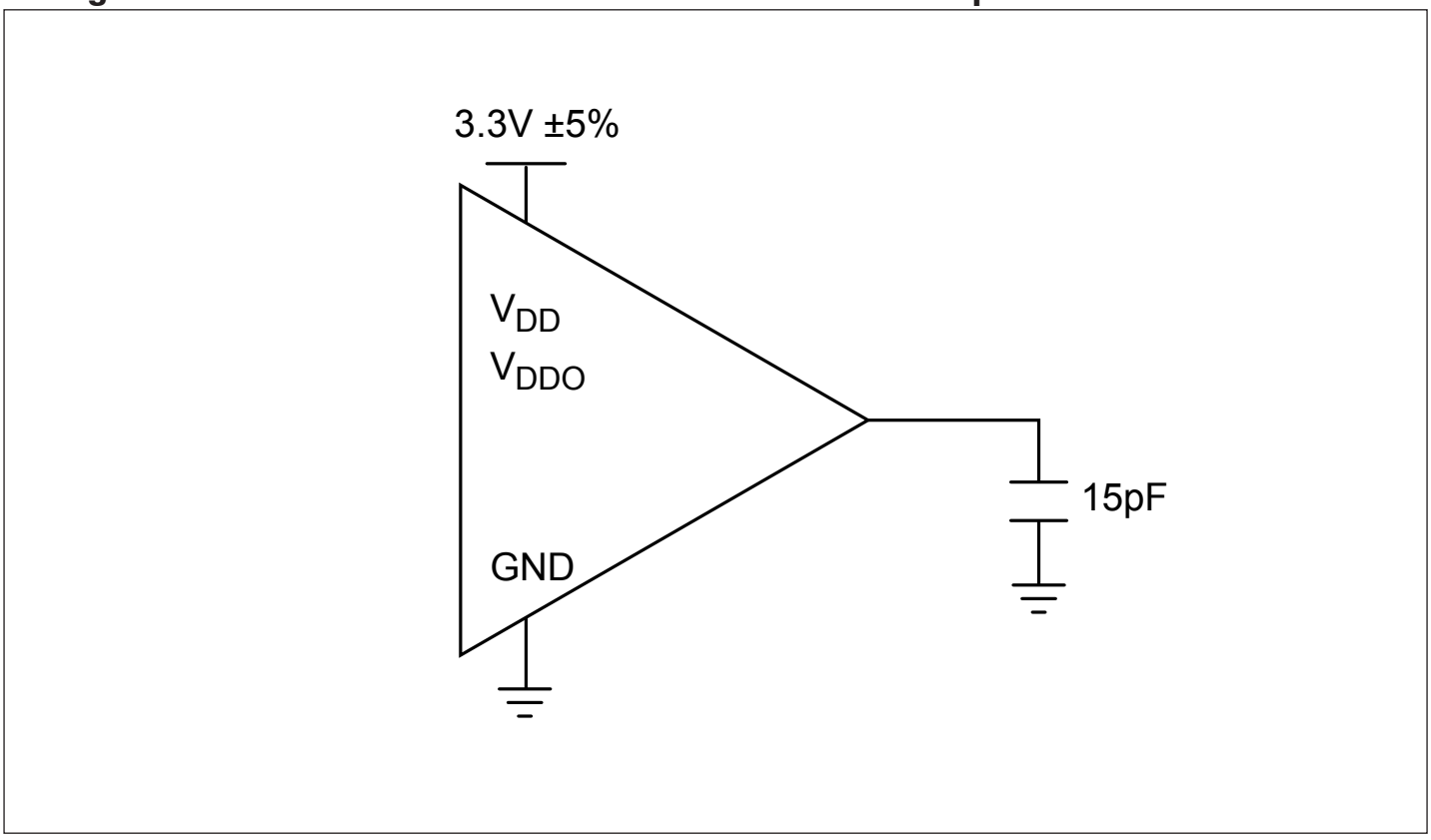
Configuration Test Load Board Termination for LVPECL/ LVDS Outputs



Configuration Test Load Board Termination for HCSL Outputs



Configuration Test Load Board Termination for LVCMOS Outputs



Application Information

Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to postion the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R1/R2 = 0.609.

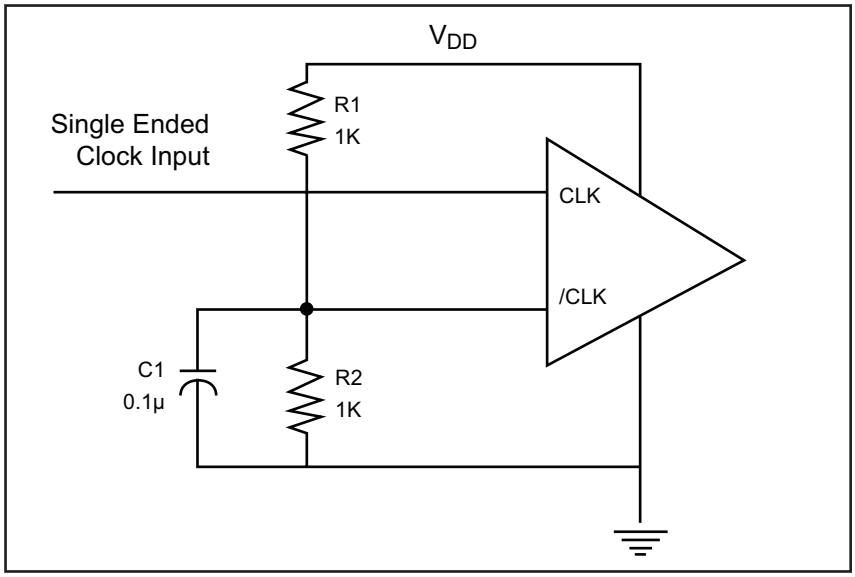
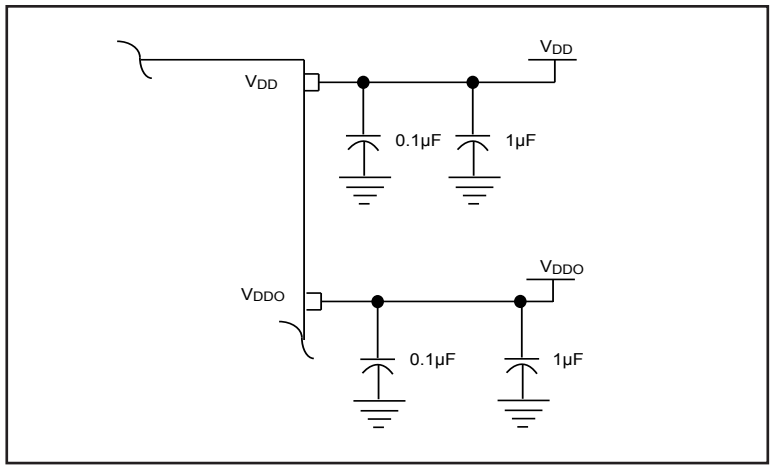


Figure 1. Single-ended input to Differential input device

Power Supply Filtering Techniques

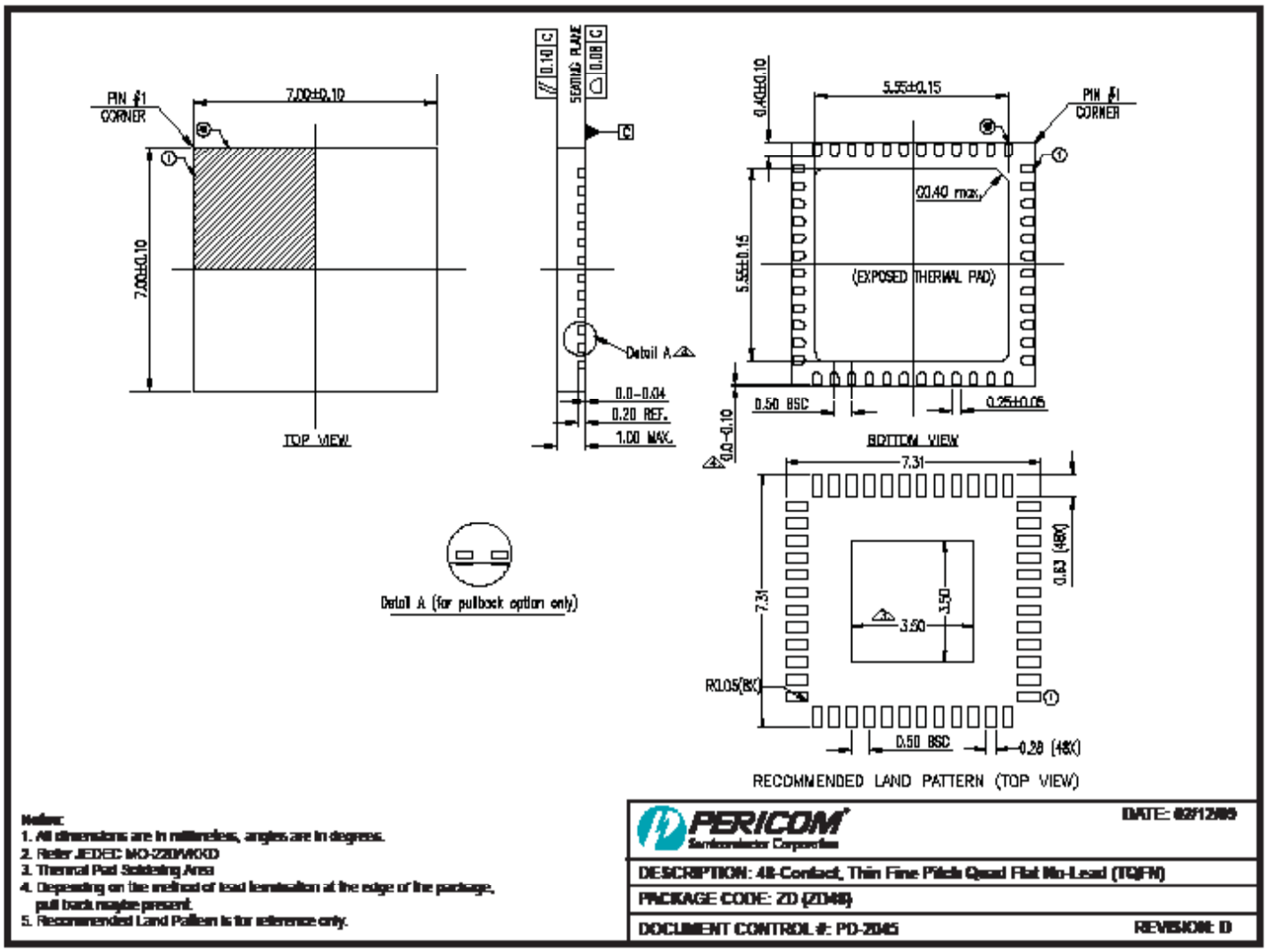
As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. All power pins should be individually connected to the power supply plane through vias, and 0.1µF an 1µF bypass capacitors should be used for each pin.



Thermal Information

Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	23.65 °C/W
Θ_{JC}	Junction-to-case thermal resistance		9.10 °C/W

Packaging Mechanical: 48-Pin TQFN (ZD)



Ordering Information

Ordering Code	Package Code	Package Type	Operating Temperature
PI6C49S1510ZDIE	ZD	Pb-free & Green, 48-pin TQFN	-40 °C to 85 °C

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. "E" denotes Pb-free and Green
3. Adding an "X" at the end of the ordering code denotes tape and Reel packaging