Power MOSFET

40 V, 75 A, 9.3 m Ω , Single N-Channel

Features

- Low R_{DS(on)}
- Low Capacitance
- Optimized Gate Charge
- NVMFS5834NLWF Wettable Flanks Product
- NVMFS Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	40	V
Gate-to-Source Volta	age		V _{GS}	±20	V
Continuous Drain		T _A = 25°C	I _D	14	Α
Current R _{θJA} (Note 1)		T _A = 100°C		12	
Power Dissipation		T _A = 25°C	P_{D}	3.6	W
R _{θJA} (Note 1)	Steady	T _A = 100°C		2.5	
Continuous Drain	State	T _C = 25°C	I _D	75	Α
Current R _{θJC} (Note 1)		T _C = 100°C		63	
Power Dissipation	1	T _C = 25°C	P_{D}	107	W
R _{θJC} (Note 1)		T _C = 100°C		75	
Pulsed Drain Current	t _p = 10 μs		I _{DM}	276	Α
Operating Junction and Storage Temperature			T _J , T _{STG}	-55 to +175	°C
Source Current (Body Diode)			IS	75	Α
Single Pulse Drain-to-Source Avalanche Energy (L = 0.1 mH)			EAS	48	mJ
			IAS	31	Α
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Bottom) (Note 1)	$R_{\theta JC}$	1.4	
Junction-to-Case (Top) (Note 1)	$R_{\theta JC}$	4.5	°C ///
Junction-to-Ambient Steady State (Note 1)	$R_{\theta JA}$	41	°C/W
Junction-to-Ambient Steady State (Note 2)	$R_{\theta JA}$	75	

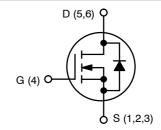
Surface-mounted on FR4 board using 1 sq-in pad (Cu area = 1.127 in sq [2 oz] including traces).



ON Semiconductor®

http://onsemi.com

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
40 V	9.3 mΩ @ 10 V	75 A
40 V	13.6 mΩ @ 4.5 V	73 A



N-CHANNEL MOSFET



S S S CASE 488AA STYLE 1

DIAGRAM D D XXXXXX **AYWZZ** D

MARKING

= Assembly Location

W = Work Week = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

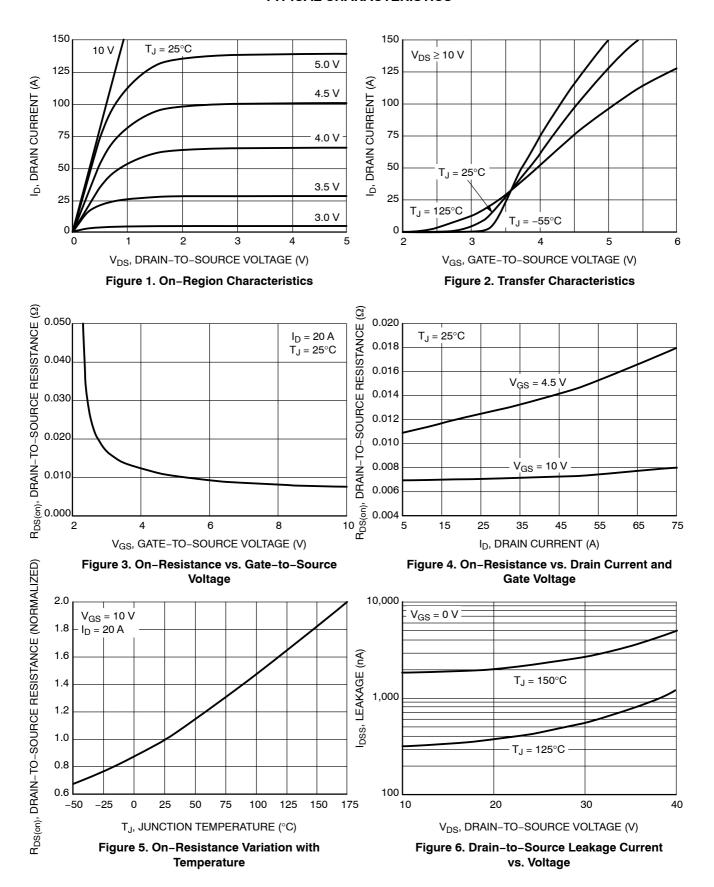
^{2.} Surface-mounted on FR4 board using 0.155 in sq (100mm²) pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /				34.7		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 40 V	T _J = 25 °C			1.0	μА
		V _{DS} = 40 V	T _J = 125°C			100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS}	= ±20 V			±100	nA
ON CHARACTERISTICS (Note 3)					•	•	•
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D = 250 \mu A$		1.0		3.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				5.7		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 20 A		7.1	9.3	
		V _{GS} = 4.5 V	I _D = 20 A		11.3	13.6	mΩ
Forward Transconductance	9FS	V _{DS} = 5 V, I _D = 20 A			29		S
CHARGES, CAPACITANCES & GATE RESIS	STANCE						•
Input Capacitance	C _{ISS}				1231		pF
Output Capacitance	C _{OSS}	V _{GS} = 0 V, f = 1 MH;	z, V _{DS} = 20 V		198		
Reverse Transfer Capacitance	C _{RSS}				141		1
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 20 V; I _D = 20 A			24		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 20 V; I _D = 20 A			12		nC
Threshold Gate Charge	Q _{G(TH)}				1.0		
Gate-to-Source Charge	Q _{GS}				4.2		
Gate-to-Drain Charge	Q_{GD}				6.3		1
Plateau Voltage	V _{GP}				3.4		V
Gate Resistance	R_{G}				0.7		Ω
SWITCHING CHARACTERISTICS (Note 4)					•	•	•
Turn-On Delay Time	t _{d(ON)}				10		
Rise Time	t _r	V_{GS} = 4.5 V, V_{DS} = 20 V, I_{D} = 20 A, R_{G} = 2.5 Ω			56.4		- ns
Turn-Off Delay Time	t _{d(OFF)}				17.4		
Fall Time	t _f				6.6		
DRAIN-SOURCE DIODE CHARACTERISTIC	s				<u>-</u>	<u>-</u>	
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 20 A	T _J = 25°C		0.84	1.2	.,
			T _J = 125°C		0.72		V
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, dIS/dt} = 100 \text{ A/}\mu\text{s,}$ $I_{S} = 20 \text{ A}$			18		
Charge Time	ta				10		ns
Discharge Time	t _b				8.0		1
Reverse Recovery Charge	Q _{RR}				108		nC

^{3.} Pulse Test: pulse width \leq 300 μ s, duty cycle \leq 2%. 4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

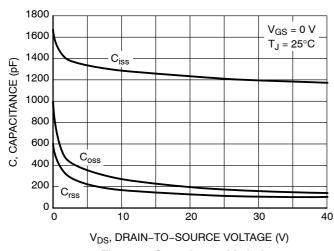


Figure 7. Capacitance Variation

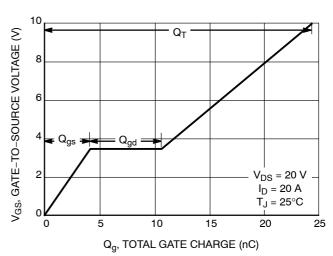


Figure 8. Gate-to-Source Voltage vs. Total Charge

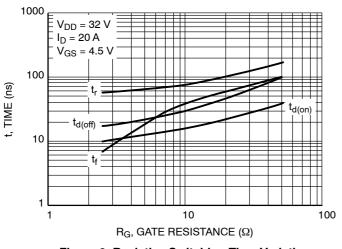


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

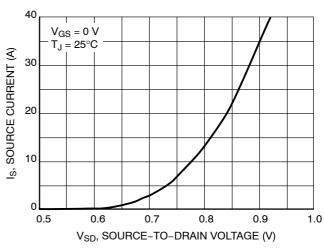


Figure 10. Diode Forward Voltage vs. Current

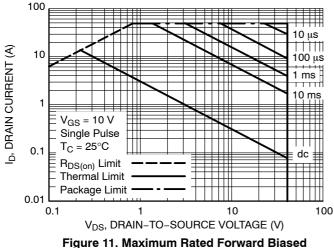


Figure 11. Maximum Rated Forward Biased
Safe Operating Area

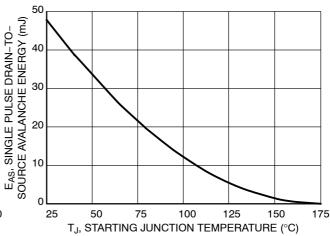


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS

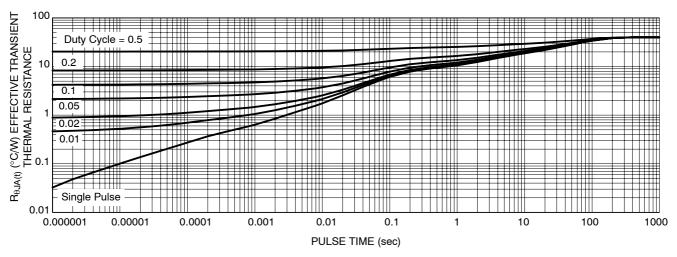


Figure 13. Thermal Response

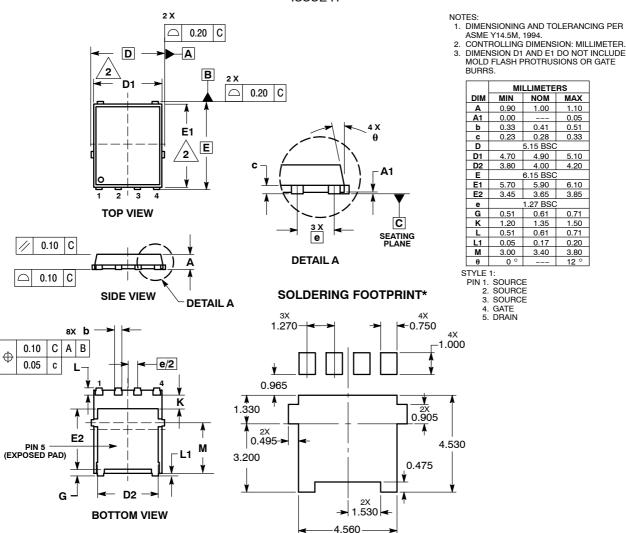
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NTMFS5834NLT1G	5834L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5834NLT1G	V5834L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5834NLWFT1G	5834LW	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5834NLT3G	V5834L	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5834NLWFT3G	5834LW	DFN5 (Pb-Free)	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DFN5 5x6, 1.27P (SO-8FL)CASE 488AA ISSUE H



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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