Reference Manual

DOC. REV. 11/19/2010

EBX-11 (Python)

AMD LX 800 Based SBC with Ethernet, Video, Audio, Industrial I/O, and SPI

PC/104
EMBEDDED-PC
MODULES

VERSALOGIC
CORPORATION

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Notice:

Product Release Notes

Rev 6 Release

- BIOS updated to Rev. 5.3.102 to add an option to turn off periodic System Management Interrupt.

- Reset circuit modified to address isolated booting issues.

- SPI interface improved in 6.00 PLD. SPI register set modified for ease of programming. Customers requiring previous SPI register configuration can retain 5.xx PLD. See VT1563 for a description of the differences between the 6.00 and 5.xx SPI interfaces.

- BIOS updated to Rev. 5.3.101 to correct the operation of the BIOS reflash utility.

Rev 5 Release

- Production release. See KnowledgeBase article VT1524 for a list of changes made for this release. See VT1527 for instructions on updating Rev. 4 boards with the Rev. 5 PLD code.

- EBX-11h Rev. 5.01 Released Nov. 2007.

Rev 4 Release

Beta release. Note: This release contained a nonstandard Digital I/O signaling on the J5 connector. See J5 I/O Connector on page 27 for details. The pinout will be corrected with the Rev. 5 release.

Rev 3 Release

Pre-production only. No customer releases.

Rev 2 Release

Pre-production only. No customer releases.

Rev 1 Release

Pre-production only. No customer releases.

Support

The EBX-11 support page, at **http://www.versalogic.com/private/pythonsupport.asp**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades
- Utility routines and benchmark software

This is a private page for EBX-11 users that can be accessed only be entering this address directly. It cannot be reached from the VersaLogic homepage.

The VersaTech KnowledgeBase is an invaluable resource for resolving technical issues with your VersaLogic product.

VersaTech KnowledgeBase

Contents

Introduction

Description

The EBX-11 is a feature-packed single board computer designed for OEM control projects requiring fast processing, industrial I/O, flexible memory options and designed-in reliability and longevity (product lifespan). Its features include:

- AMD LX 800 microcontroller with CS5536 companion chip
- Up to 1GB system RAM
- CompactFlash site
- 10/100 Ethernet interface (dual)
- Flat Panel Display support
- MMX™ + 3DNow!™ graphics
- PC/104-*Plus* expansion site
- IDE controller, one channel, ATA-5, UDMA66
- Four USB 2.0/1.1 ports
- TVS devices on user I/O connections (require connection to earth ground)
- Four COM ports (2 full serial ports, 2 4-pin with automatic handshake) and LPT port
- CPU temperature sensor

- PCI-based audio
- PS/2 keyboard and mouse ports
- Industrial I/O
  - 8-channel, 12-bit Analog inputs
  - 32-channel Digital I/O
  - Three PWM buffered TTL outputs
- SPI interface supports up to four (external) SPI devices either of user design or any of the SPX™ series of expansion boards, with clock frequencies from 1-8MHz
- Watchdog timer
- Vcc sensing reset circuit (all rails monitored, interrupt on fault)
- EBX-compliant 5.75" x 8.00" footprint
- Field upgradeable BIOS with OEM enhancements
- Latching I/O connectors
- Customizing available

The EBX-11 is compatible with popular operating systems such as Windows and Linux.

A full complement of standard I/O ports are included on-board. Additional I/O expansion is available through the high-speed PCI-based PC/104-*Plus* expansion site (which supports both PC/104 and PC/104-*Plus* expansion modules), and through the Serial Peripheral Interface (SPI).

System memory expansion is supported with one high-reliability latching 200-pin SODIMM socket. Up to 1 GB of low power, 333 MHz, PC2700 compatible DDR RAM is available.

The EBX-11 features high reliability design and construction, including latching I/O connectors. It also features a watchdog timer, voltage sensing reset circuits and self-resetting fuse on the 5V supply to the keyboard, mouse, and USB.

EBX-11 boards are subjected to 100% functional testing and are backed by a limited two-year warranty. Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service and product longevity for this exceptional SBC.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size: 5.75" x 8.00" x 1.75"; EBX compliant

Storage Temperature: -40° C to 85° C

Free Air Operating Temperature:
0° C to +60° C EBX-11g, gu
-40° C to +85° C EBX-11h

Power Requirements: *(with 1GB DDR SODIMMS, keyboard and mouse)*
EBX-11g, h – AMD CPU +5.0V ± 5% @ 0.90A (4.5W) typ.
+3.3V or ±12V may be required by some expansion modules

System Reset:
V_{cc} sensing, resets when the 3.3V, 2.5V, or Vcore power rails vary by more than +/- 10% of their optimal values.
Watchdog timeout

DRAM Interface:
One 200-pin SODIMM socket
Up to 1 GB 333 MHz, PC2700 compatible, DDR RAM

Video Interface:
Up to 1600 x 1200 (24 bits)
Standard analog output
MMX™ + 3DNow!™ graphics
LVDS output for TFT FPDs

IDE Interface:
One channel, 44-pin keyed 2mm header.
Supports up to and including UDMA5.
Supports up to two IDE devices (hard drives, CD-ROM, CompactFlash, etc.).

Ethernet Interface:
Two Intel 82551ER based Fast Ethernet 10/100 Controllers

Audio Interface:
AC '97 compatible Line Out and Line In support

Analog Input:
8-channel, 12-bit, single-ended, 500 kSPS, channel independent input range: 0 to +4.095V

COM1–2 Interface:
RS-232, 16C550 compatible, 115k baud max.

COM3–4 Interface:
RS-232/422/485, 16C550 compatible, 460k baud max.

LPT Interface:
Bi-directional/EPP/ECP compatible

Digital Interface:
32-channel, ±24 mA outputs, 3.3V signaling

SPX Interface:
Supports 4 external SPI chips either of user design or any of the SPX™ series of expansion boards

BIOS:
General Software Embedded BIOS© 2003 with OEM enhancements
Field-upgradeable with Flash BIOS Upgrade Utility

Bus Speed:
CPU Bus: 800 MHz (Celeron equiv.), 500 MHz actual
DRAM: 200 MHz/266 MHz/333 MHz
PC/104-*Plus* (PCI): 33MHz
PC/104 (ISA): 8MHz

Compatibility:
PC/104 – full compliance
Embedded-PCI (PC/104-*Plus*) – full compliance, 3.3V signaling
EBX – full compliance
SPX™ – full compliance

Weight:
EBX-11g – 0.394 lbs (0.179 kg)
EBX-11h – 0.414 lbs (0.188 kg)

Generated Frequencies:
266 MHz, 66 MHz, 48 MHz, 33 MHz, 25 MHz, 24.576 MHz, 14.318 MHz, 8 MHz, 4 MHz, 2 MHz, 1 MHz, 32.768 kHz

Specifications are subject to change without notice.

EBX-11 Block Diagram
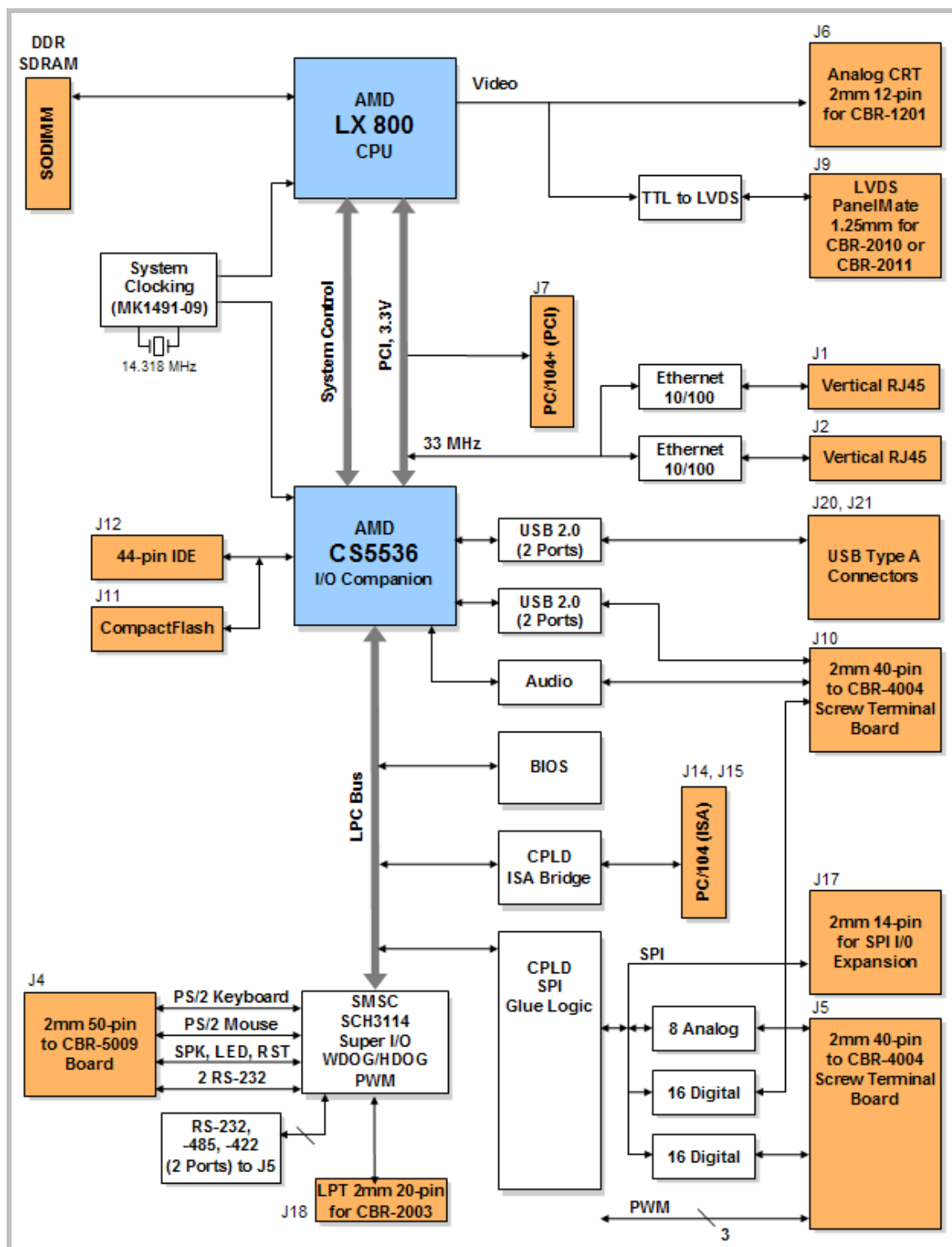
RoHS-Compliance

The EBX-11 is RoHS-compliant.

ABOUT ROHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corporation is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Warnings

ELECTROSTATIC DISCHARGE

Electrostatic discharge (ESD) can damage boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Note The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom-side of the EBX-11.

LITHIUM BATTERY

To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly.

MOUNTING SUPPORT

The single board computer must be supported at all eight mounting points to prevent excessive flexing when expansion modules are mated and demated. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty. See page 12 for more details.

TRANSIENT VOLTAGE SUPPRESSION (TVS) DEVICES

The EBX-11 circuitry is protected from spike and surge damage by on-board transient voltage suppression (TVS) devices on the user I/O signals. Figure 1 shows a typical example of TVS circuitry. In order for the TVS devices to function properly, they must be connected to earth ground. This connection is made at the board's lower right mounting hole, as shown in Figure 2. All other mounting holes are floating. Use metal standoffs or a grounding strap to connect the lower right mounting hole to the enclosure chassis, which should be connected to earth ground.
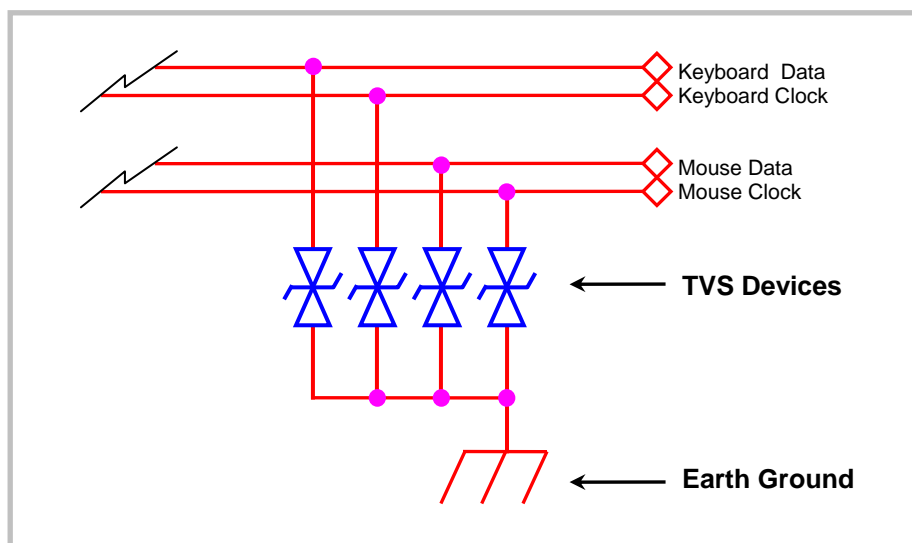
Figure 1. Schematic Showing Typical TVS Circuitry
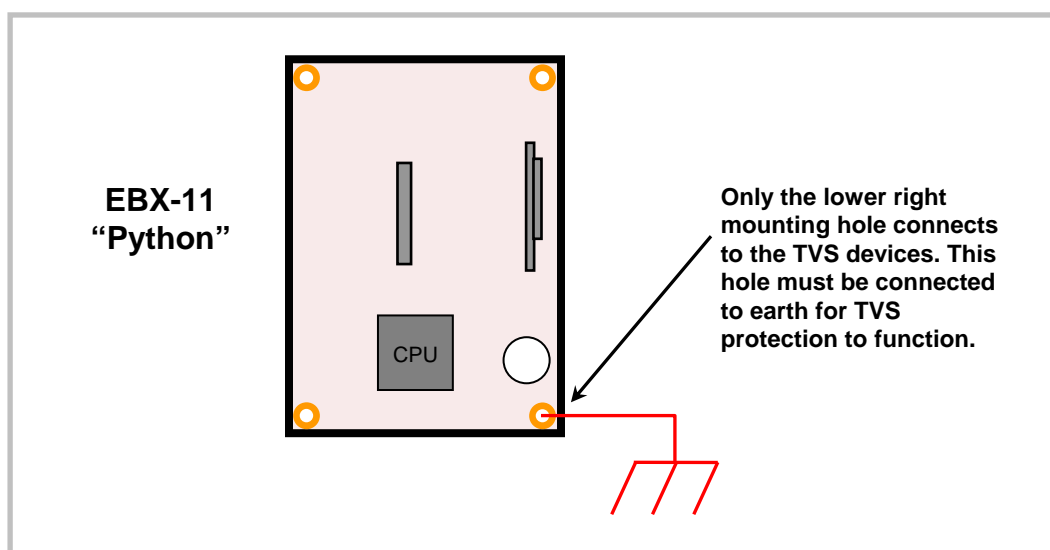
Figure 2. Attaching the EBX-11 to Earth Ground

Technical Support

If you are unable to solve a problem after reading this manual, please visit the EBX-11 product support web page below. The support page provides links to component datasheets, device drivers, and BIOS and PLD code updates.

<div style="border:1px solid;">

EBX-11 Support Page

http://www.versalogic.com/private/pythonsupport.asp

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The VersaTech KnowledgeBase contains a wealth of technical information about VersaLogic products, along with product advisories. Click the link below to see all KnowledgeBase articles related to the EBX-11.

<div style="border:1px solid;">

VersaTech KnowledgeBase

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If you have further questions, contact VersaLogic Technical Support at (503) 747-2261. VersaLogic support engineers are also available via e-mail at Support@VersaLogic.com.

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (503) 747-2261.

Please provide the following information:

- Your name, the name of your company, your phone number, and e-mail address
- The name of a technician or engineer that can be contacted if any questions arise
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note Please mark the RMA number clearly on the outside of the box before returning. Failure to do so can delay the processing of your return.

Initial Configuration

The following components are recommended for a typical development system.

- EBX-11 single board computer
- 200-pin SODIMM (memory module): DDR200, DDR266, or DDR333
- ATX power supply with motherboard and drive connectors
- SVGA video monitor
- Keyboard with PS/2 or USB connector
- Mouse with PS/2 or USB connector
- IDE hard drive
- IDE CD-ROM drive

The following VersaLogic cables are recommended.

- Video adapter cable (CBR-1201)
- Utility I/O cable (CBR-5009A) and accompanying board (CBR-5009B)
- IDE data cable (CBR-4406); may also require 2mm to 0.1" adapter (CBR-4405)
- Power adapter cable (CBR-2022)

You will also need a Windows (or other OS) installation CD.

Basic Setup

The following steps outline the procedure for setting up a typical development system. The EBX-11 should be handled at an ESD workstation or while wearing a grounded antistatic wrist strap.

Before you begin, unpack the EBX-11 and accessories. Verify that you received all the items you ordered. Inspect the system visually for any damage that may have occurred in shipping. Contact Support@VersaLogic.com immediately if any items are damaged or missing.

Gather all the peripheral devices you plan to attach to the EBX-11 and their interface and power cables.

It is recommended that you attach standoffs to the board (see 3) to stabilize the board and make it easier to work with.

Figure 3 shows a typical start-up configuration.
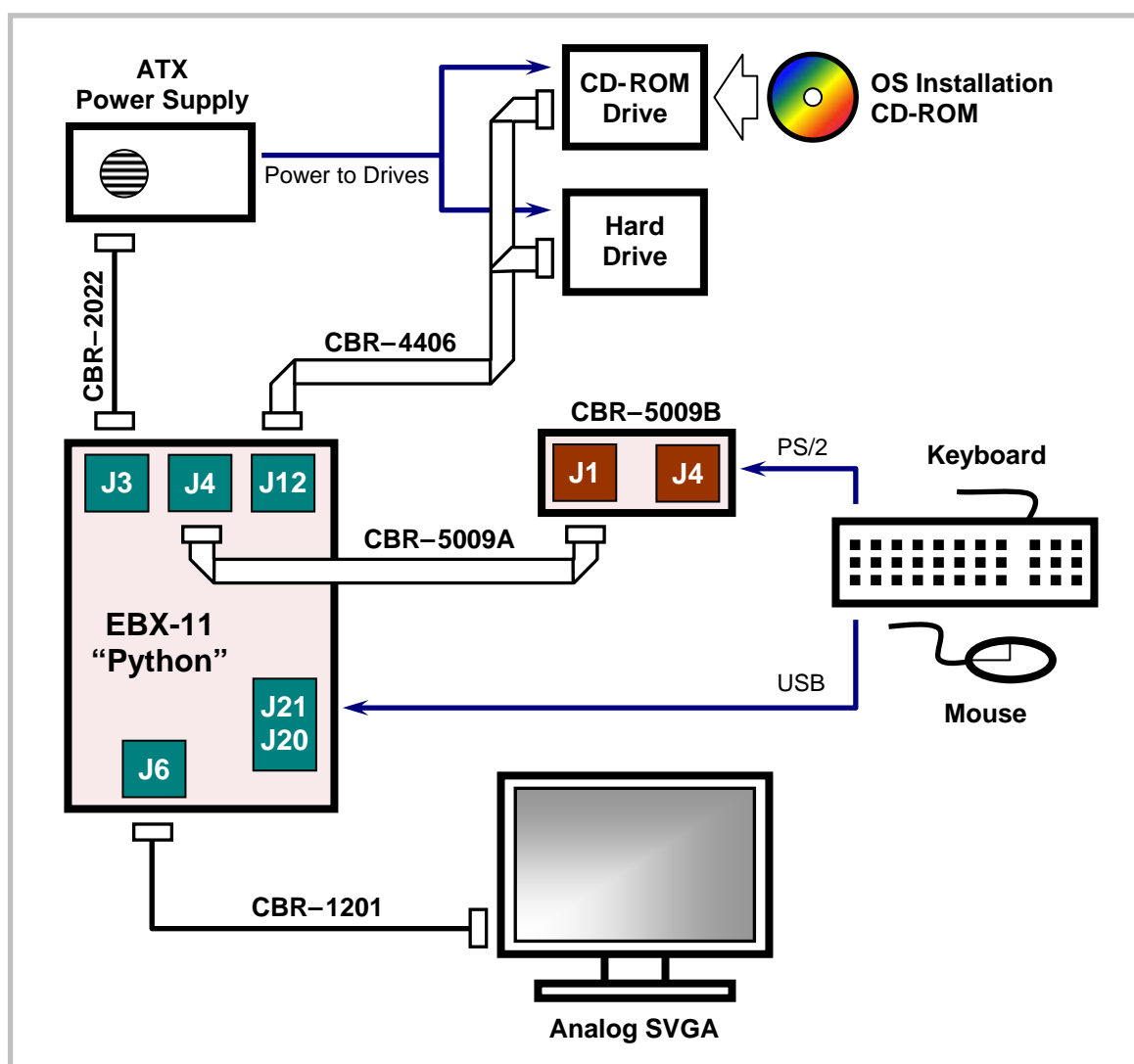
Figure 3. Typical Start-up Configuration

1. Install Memory

- Insert the DRAM module into the SODIMM socket and latch it into place.

2. Attach Power

- Plug the power adapter cable CBR-2022 into connector J3. Attach the motherboard connector of the ATX power supply to the adapter.

3. Attach Cables and Peripherals

- Plug the video adapter cable CBR-1201 into socket J6. Attach the video monitor interface cable to the video adapter.

- If you are using a PS/2 keyboard or mouse, plug the breakout cable CBR-5009A into socket J4. If necessary, attach the breakout board CBR-5009B to the cable. (The cable and board are shipped attached.) Plug the keyboard and/or mouse into connector J4 of breakout board.
- If you are using a USB keyboard or mouse, plug them into socket J20 or J21 of the EBX-11.
- Plug the hard drive data cable CBR-4404 into socket J12. Attach a hard drive and CD-ROM drive to the connectors on the cable. If the hard drive is 3.5", use the 2mm to 0.1" adapter CBR-4405 to attach the IDE cable.
- Attach an ATX power cable to any 3.5" drive (hard drive or CD-ROM drive).
- Set the hard drive jumper for master device operation and the CD-ROM drive jumper for slave device operation.

4. Review Configuration

- Before you power up the system, double check all the connections. Make sure all cables are oriented correctly and that adequate power will be supplied to the EBX-11 and peripheral devices.

5. Power On

- Turn on the ATX power supply and the video monitor. If the system is correctly configured, a video signal should be present.

6. Change CMOS Setup Settings

- Enter CMOS Setup by pressing Delete during the early boot cycle.
- Select Basic Configuration and set or verify the following settings (see CMOS Setup for a complete list of default settings):

```
DRIVE ASSIGNMENT ORDER │ Drive C: Ide 0/Pri Master

ATA DRV ASSIGNMENT │ Ide 0: 3 = AUTOCONFIG, LBA
ATA DRV ASSIGNMENT │ Ide 1: 5 = IDE CDROM

BOOT ORDER │ Boot 1st: CDROM
BOOT ORDER │ Boot 2nd: Drive C:
```

- Before saving the CMOS Setup settings, insert the Windows (or other OS) installation disk in the CD-ROM drive so it will be accessed when the system reboots.
- Press ESC and write the new parameters to CMOS RAM. The system will reboot.

7. Install Operating System

- Install the operating system according to the instructions provided by the OS manufacturer. (See Operating System Installation.)

Note   If you intend to operate the EBX-11 under Windows XP or Windows XP Embedded, be sure to use Service Pack 2 (SP2) for full support of the latest CS5536 I/O hub and its USB 2.0 features.

CMOS Setup

The default CMOS Setup parameters for the EBX-11 are shown below. See VersaLogic Knowledgebase article VT1528 – EBX-11 CMOS Setup Reference for more information about these parameters. Due to system configuration and changes between BIOS revisions, the information on your monitor may differ from that shown above. The date shown on the Basic CMOS Configuration screen is the BIOS build date.

Basic CMOS Configuration

```
+------------------------------------------------------------------------------+
|              System Bios Setup - Basic CMOS Configuration                     |
|           (C) 2005 General Software, Inc. All rights reserved                 |
+--------------------------+--------------------+------------------------------+
| DRIVE ASSIGNMENT ORDER:  | Date:>Nov 02, 2010 | Typematic Delay  : 250 ms    |
| Drive A: (None)          | Time: 00 : 00 : 00 | Typematic Rate   : 30 cps    |
| Drive B: (None)          | NumLock:  Disabled | Seek at Boot     : None      |
| Drive C: Ide 0/Pri Master +--------------------+ Show "Hit Del"   : Enabled   |
| Drive D: (None)          | BOOT ORDER:        | Config Box       : Enabled   |
| Drive E: (None)          | Boot 1st: Drive C: | F1 Error Wait    : Enabled   |
| Drive F: (None)          | Boot 2nd: (None)   | Parity Checking  : (Unused)  |
| Drive G: (None)          | Boot 3rd: (None)   | Memory Test Tick : Enabled   |
| Drive H: (None)          | Boot 4th: (None)   | Debug Breakpoints: (Unused)  |
| Drive I: (None)          | Boot 5th: (None)   | Debugger Hex Case: Upper     |
| Drive J: (None)          | Boot 6th: (None)   | Memory Test :StdLo FastHi    |
| Drive K: (None)          +--------------------+------------------+-----------+
| Boot Method: Boot Sector | ATA DRV ASSIGNMENT:  Sect  Hds  Cyls | Memory    |
+--------------------------+ Ide 0: 3 = AUTOCONFIG, LBA           |  Base:    |
| FLOPPY DRIVE TYPES:      | Ide 1: 3 = AUTOCONFIG, LBA            |   631KB   |
| Floppy 0: Not installed  | Ide 2: 3 = AUTOCONFIG, LBA           | Ext:      |
| Floppy 1: Not installed  | Ide 3: 3 = AUTOCONFIG, LBA           |   219MB   |
+--------------------------+--------------------------------------+-----------+
```

Features Configuration

```
+------------------------------------------------------------------------------+
|              System BIOS Setup - Advanced Configuration                       |
|           (C) 2005 General Software, Inc. All rights reserved                 |
+-------------------------------------+----------------------------------------+
| System Management Mode  : Enabled   | POST Memory Manager      : Disabled    |
| Splash Screen           : Disabled  | System Management BIOS   : Enabled     |
| Primary IDE UDMA        : Enabled   | Console Redirection      : Auto        |
| Firmbase Debug Console  : None      | UsbMassStorage           : Enabled     |
| Usb20                   : Enabled   |                                        |
+-------------------------------------+----------------------------------------+
```

Custom Configuration

```
+------------------------------------------------------------------------------+
|               System BIOS Setup - Custom Configuration                        |
|           (C) 2005 General Software, Inc. All rights reserved                 |
+-------------------------------------+----------------------------------------+
| PCI INT A Assignment  : IRQ 11      | ISA IRQ 3                : Disabled     |
| PCI INT B Assignment  : IRQ 5       | ISA IRQ 4                : Disabled     |
| PCI INT C Assignment  : IRQ 9       | ISA IRQ 5                : Disabled     |
| PCI INT D Assignment  : IRQ 9       | ISA IRQ 10               : Disabled     |
| Write protect BIOS    : Enabled     | COM 1 enable/IRQ         : IRQ4        |
| Video buffer size     : 32 MB       | COM 2 enable/IRQ         : IRQ3        |
| Flat panel display    : Disabled    | COM 3 enable/IRQ         : Disabled    |
| Video refresh rate    : 60 Hz       | COM 4 enable/IRQ         : Disabled    |
| Video data width      : 1 pix/clk   | COM 3 mode               : RS232 (4pin)|
| Primary video device  : Auto        | COM 4 mode               : RS232 (4pin)|
| Memory Timings        : Optimal     | LPT 1 enable/IRQ         : IRQ7       |
| CPU Temp threshold    : 80*C        | LPT 1 mode               : Printer    |
| CPU overtemp IRQ      : Disabled    | BIOS extension           : Disabled    |
| CPU/GLIU speed        : 500/333 MHz | USB OTG Device           : Disabled    |
| IDE cable type        : 40-Wire     | Legacy USB support       : Enabled     |
| Voltage Alert IRQ     : Disabled    | Periodic SMM IRQ         : Enabled     |
| Geode audio controller: Enabled     |                                        |
+-------------------------------------+----------------------------------------+
```

Shadow Configuration

```
+------------------------------------------------------------------------------+
|                   System BIOS Setup – Shadow/Cache Configuration             |
|              (C) 2005 General Software, Inc. All rights reserved             |
+-------------------------------------+----------------------------------------+
| Shadowing           : Chipset       | Shadow 16KB ROM at C000 : Enabled      |
| Shadow 16KB ROM at C400 : Enabled   | Shadow 16KB ROM at C800 : Disabled     |
| Shadow 16KB ROM at CC00 : Disabled  | Shadow 16KB ROM at D000 : Disabled     |
| Shadow 16KB ROM at D400 : Disabled  | Shadow 16KB ROM at D800 : Disabled     |
| Shadow 16KB ROM at DC00 : Enabled   | Shadow 16KB ROM at E000 : Enabled      |
| Shadow 16KB ROM at E400 : Enabled   | Shadow 16KB ROM at E800 : Enabled      |
| Shadow 16KB ROM at EC00 : Enabled   | Shadow 64KB ROM at F000 : Enabled      |
+-------------------------------------+----------------------------------------+
```

Note   Due to changes and improvements in the system BIOS, the information on your monitor may differ from that shown above. The factory default date will correspond to the BIOS build date.

Operating System Installation

The standard PC architecture used on the EBX-11 makes the installation and use of most of the standard x86 processor-based operating systems very simple. The operating systems listed on the VersaLogic OS Compatibility Chart use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular operating system, or a link to the drivers, are available at the EBX-11 Product Support web page at **http://www.versalogic.com/private/pythonsupport.asp.**

Note   An operating system installed on a different type of computer is not guaranteed to work on the EBX-11. This is referred to as a "foreign" installation. A hard disk that was used to boot a different computer cannot necessarily be moved to the EBX-11 and expected to boot. Even when porting an OS image from one revision of the EBX-11 to another, performance might fail or be impaired. For the best results, perform a fresh installation of the OS on each system. This restriction does not apply if you are producing multiple identical systems.

Physical Details

Dimensions and Mounting

The EBX-11 complies with all EBX standards which provide for specific mounting hole and PC/104-*Plus* stack locations as shown in the diagram below.
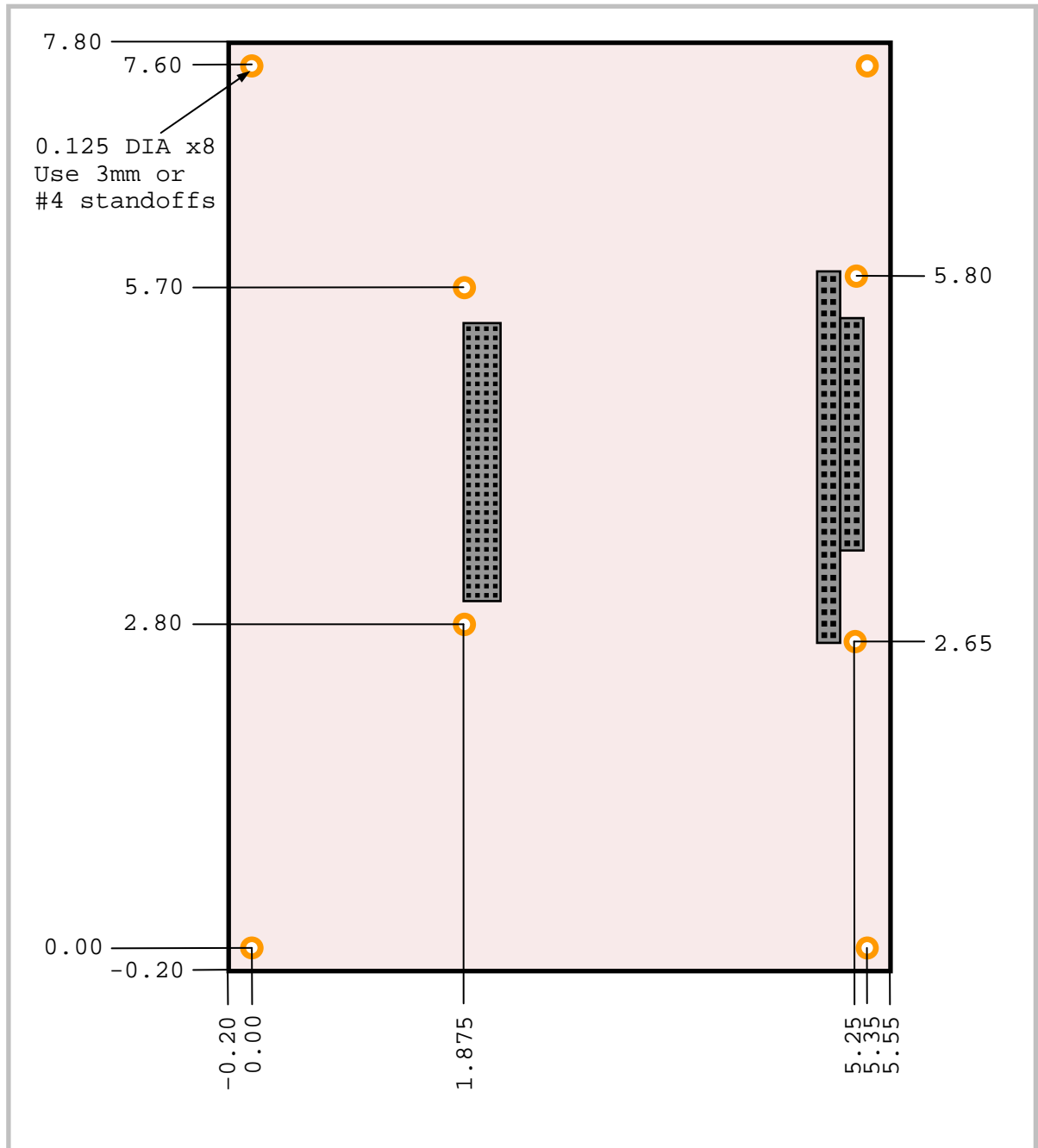
Figure 4. EBX-11 Dimensions and Mounting Holes

(Not to scale. All dimensions in inches.)

Caution   The single board computer must be supported at all eight mounting points to prevent excessive flexing when expansion modules are mated and demated. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty.
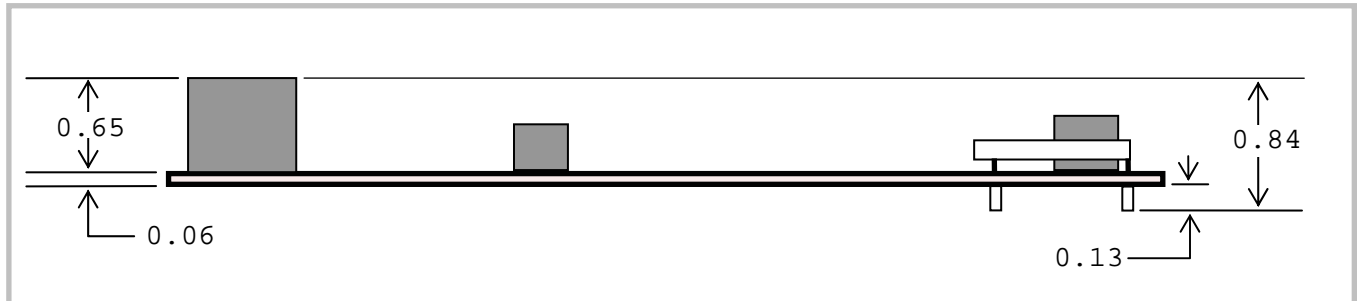
Figure 5. EBX-11 Height Dimensions
(Not to scale. All dimensions in inches.)
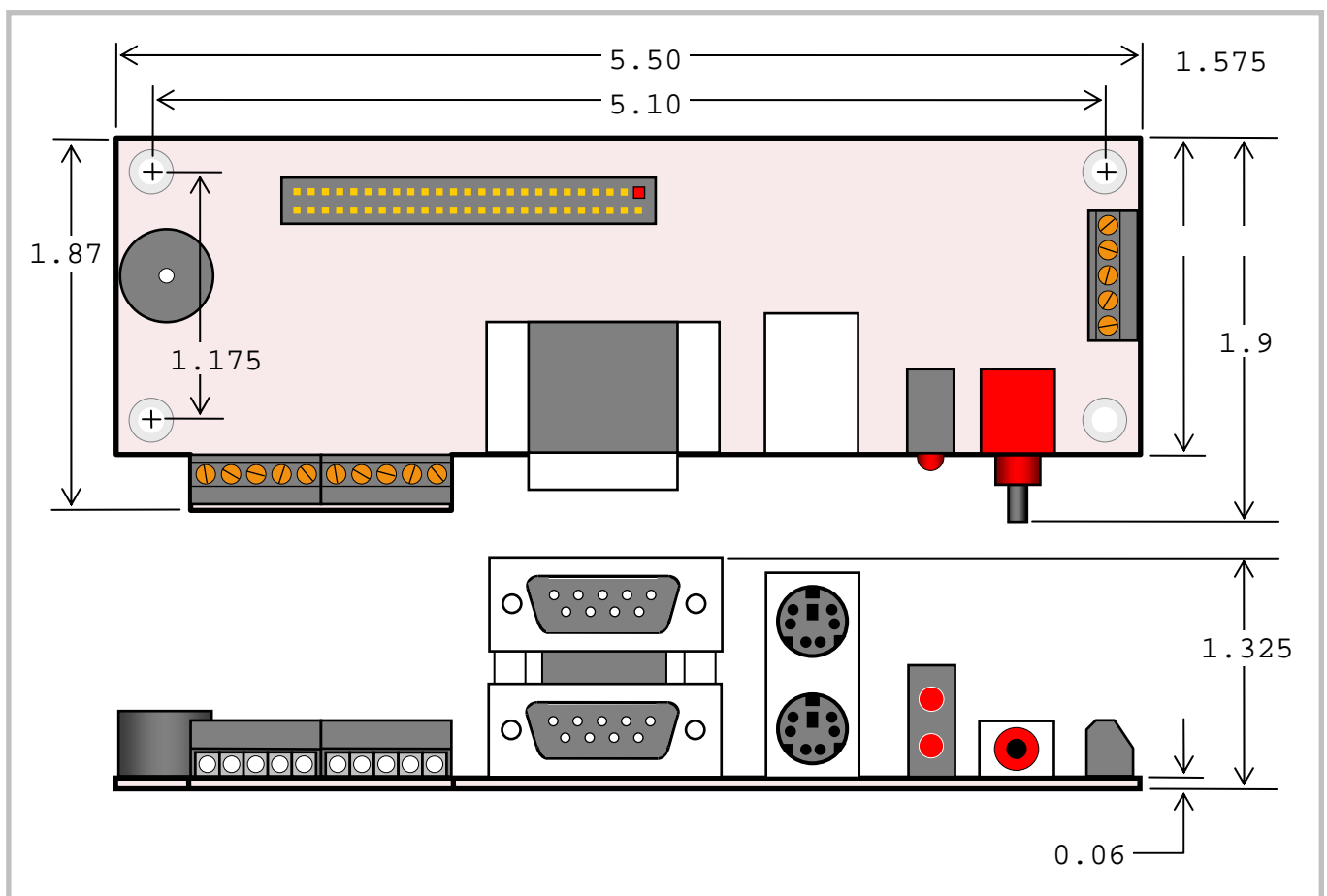
Figure 6. CBR-5009 Dimensions and Mounting Holes

Figure 7. CBR-4004 Dimensions and Mounting Holes
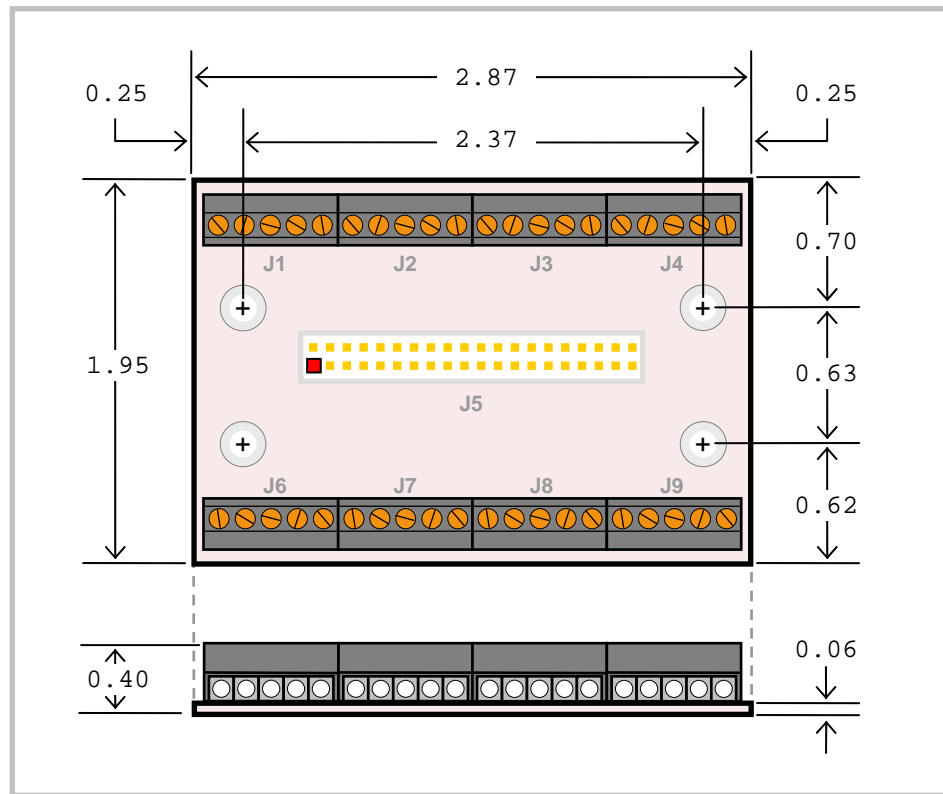
HARDWARE ASSEMBLY

The EBX-11 mounts on four hardware standoffs using the corner mounting holes (A). These standoffs are secured to the underside of the circuit board using pan head screws.

Four additional standoffs (B) must be used under the circuit board to prevent excessive flexing when expansion modules are mated and separated. These are secured with four male-female standoffs (C), threaded from the top side, which also serve as mounting struts for the PC/104 stack.

The entire assembly can sit on a table top or be secured to a base plate. When bolting the unit down, make sure to secure all eight standoffs (A and B) to the mounting surface to prevent circuit board flexing.

An extractor tool is available (part number VL-HDW-201) to separate the PC/104 modules from the stack.

Note   Standoffs and screws are available as part number VL-HDW-101.

STANDOFF LOCATIONS

Connect this mounting hole to earth to make TVS devices functional. See Transient Voltage Suppression (TVS) Devices.
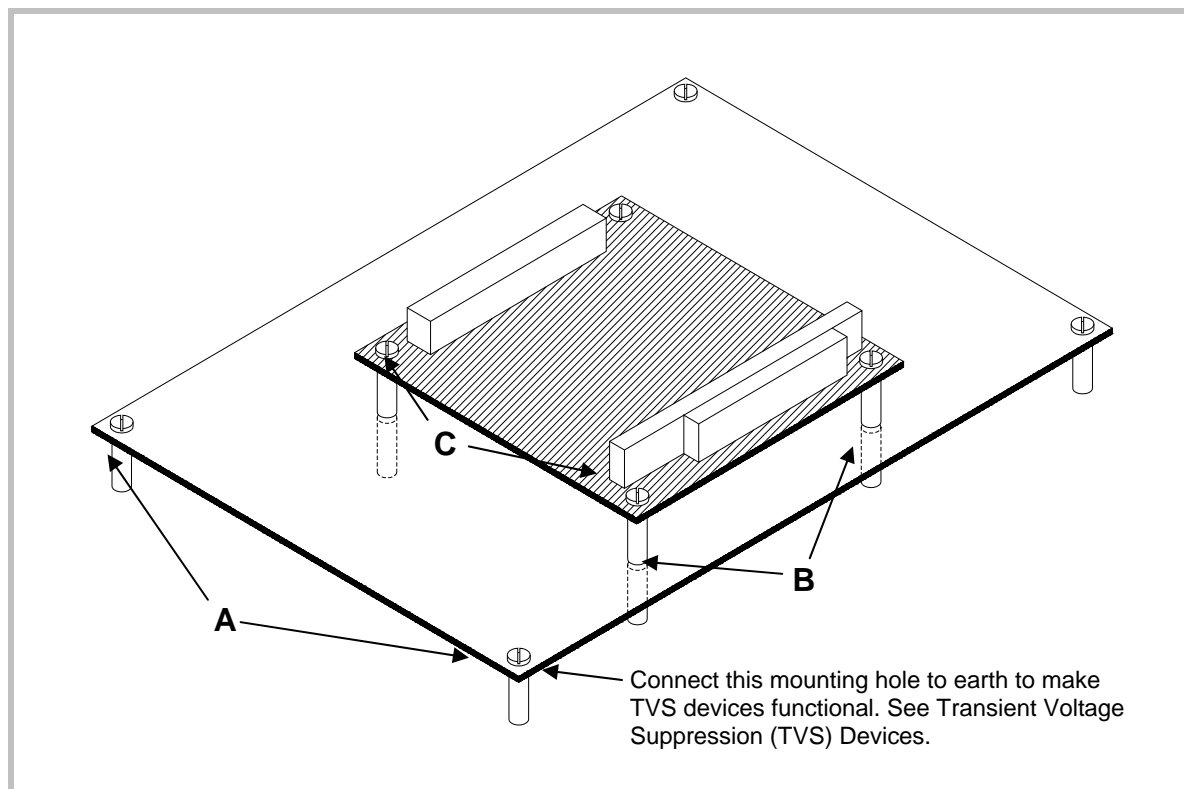
Figure 8. Standoff Locations

External Connectors

EBX-11 CONNECTORS

J5
Analog,
PWM, Digital

J4
COM 1-4,
PLED, PS/2
Keyboard and
Mouse, Reset
Button,
Speaker

J3
Power

J10
Audio, Digital
I/O, USB 0-1

J12
IDE

J18
LPT

J17
SPI

J16
Factory Use Only

V1

V2

■ = Pin 1

J2
Ethernet

J1
Ethernet

J7
PC/104-*Plus*

J11
CompactFlash

J14-J15
PC/104

SODIMM1
Memory

CPU

Battery

J21
USB 3

J20
USB 2

V3

J6
SVGA

J9
LVDS

Earth Ground
Reference Point

The lower right
mounting hole
(nearest to
jumper block
V3) must be
connected to
earth to make
TVS devices
functional. See
Transient
Voltage
Suppression
(TVS) Devices.

Figure 9. EBX-11 Connectors – Rev. 5.00 Boards and Later

EBX-11 CONNECTOR FUNCTIONS AND INTERFACE CABLES

The following table notes the function of each connector, as well as mating connectors and cables, and the page where a detailed pinout or further information is available.

Table 1: Connector Functions and Interface Cables

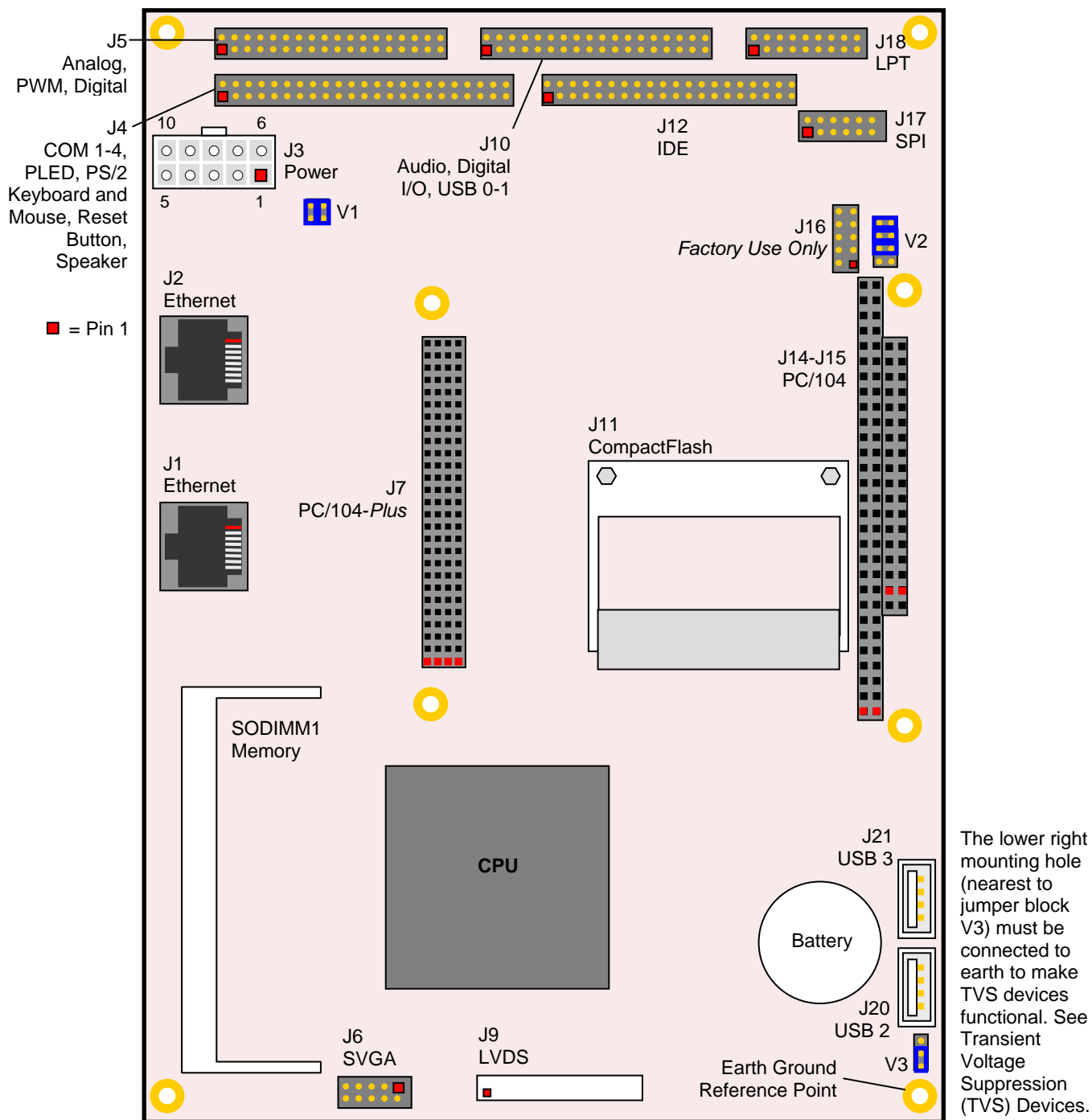| Connector	Function	Mating Connector	Transition Cable	Cable Description	Pin 1 Location[1] x coord.	y coord.	Page
J1	Ethernet 0	RJ45 Crimp-on Plug	–	–	0.425	4.200	42
J2	Ethernet 1	RJ45 Crimp-on Plug	–	–	0.425	5.500	42
J3	Main Power Input (EBX Compliant)	Molex 39-01-2100 Molex 39-00-0059 (10 ea.)	CBR-2022	6" ATX to EPIC power cable	0.625	6.600	22
J4	COM 1-4, PLED, PS/2 Keyboard and Mouse, Reset Button, Speaker	FCI 89361-350LF	CBR-5009A	18" 2mm 50-pin to 50-pin IDC to breakout board CBR-5009B	0.380	7.200	26
J5	Analog I/O, PWM I/O, Digital I/O	FCI 89361-340LF	CBR-4004A	12" 2mm 40-pin to 40-pin IDC to screw terminal board CBR-4004B	0.380	7.520	27
J6	SVGA Video Output	FCI 89361-712LF or FCI 89947-712LF	CBR-1201	1' 12-pin 2mm IDC to 15-pin HD D-Sub VGA	1.700	0.060	39
J7	PC-104-*Plus*	AMP 1375799-1	–	–	2.106	3.096	–
J9	LVDS	20-pin, PanelMate 1.25mm	CBR-2010 or CBR-2011	18-bit TFT FPD using 20-pin Hirose 18-bit TFT FPD using 20-pin JAE	2.400	0.190	40
J10	Audio, Digital I/O, USB 0-1	FCI 89361-340LF	CBR-4004A	12" 2mm 40-pin to 40-pin IDC to screw terminal board CBR-4004B	2.325	7.520	29
J11	CompactFlash	Type I or Type II Compact Flash	–	–	3.263	4.501	37
J12	IDE Hard Drive	FCI 89947-144LF	CBR-4406 CBR-4405[2]	18" 2mm IDE cable 2mm to 0.1" adapter	2.640	7.200	30
J14, J15	PC/104	AMP 1375795-2	–	–	5.050	2.700	–
J16	PLD Reprogram-ming Port *(Factory use Only)*	–	–	–	4.900	6.025	–
J17	SPX I/O	FCI 89361714LF	CBR-1401 or CBR-1402	2mm 14-pin IDC, 2 or 4 SPX device cable	4.280	6.950	55
J18	LPT	FCI 89361720LF	CBR-2003	12" 2mm 20-pin IDC LPT	4.270	7.520	33
J20[3]	USB 2	Standard USB Series A	–	–	5.320	0.642	35
J21	USB 3	Standard USB Series A	–	–	5.320	1.337	35

1. The PCB origin is the mounting hole to the lower left, as oriented in Figure 9.
2. CBR-4405 44-pin to 40-pin adapter required to connect to 3.5-inch IDE drives with 40-pin connectors.
3. On Rev. 4.01 and earlier boards, one connector (J13) provided the interface to both USB2 and USB3. The connector was a 2mm 10-pin header. See Table 15 for a pinout of this connector.

CBR-5009 CONNECTORS

= Pin 1
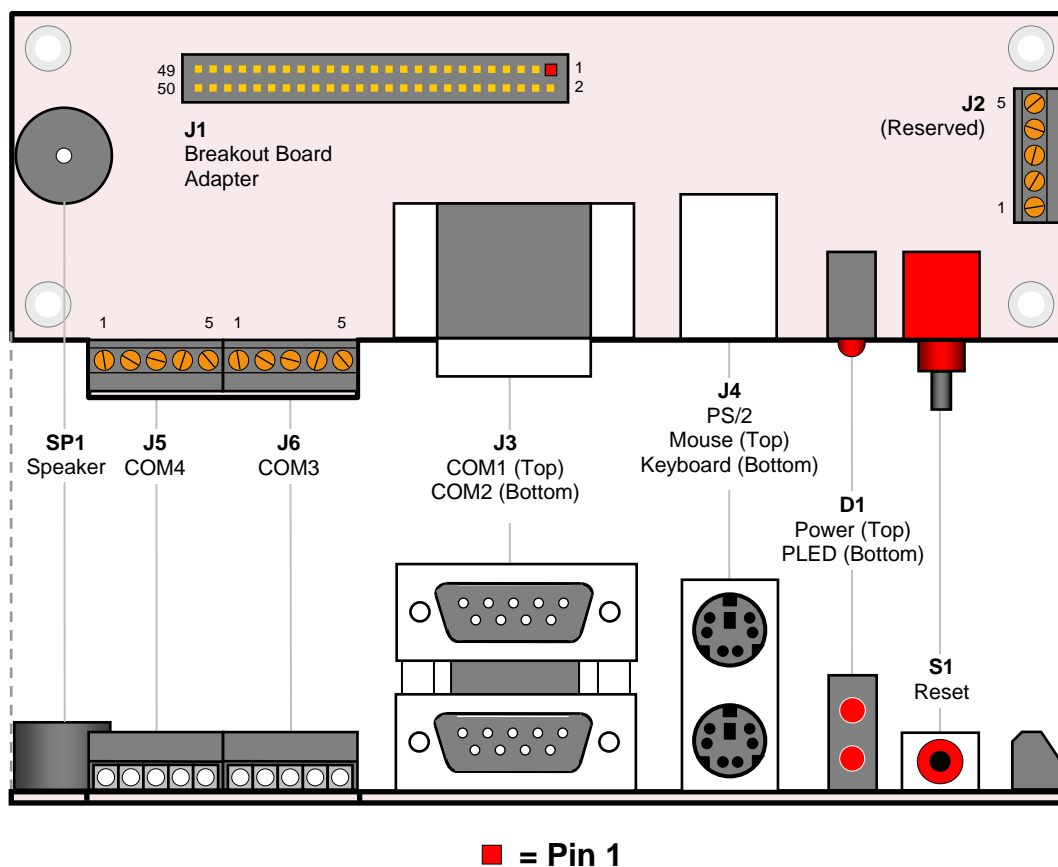
Figure 10. CBR-5009 Connectors

CBR-5009 CONNECTOR FUNCTIONS

Connector / Component	Function	Part Number	Description
D1	Power and Programmable LEDs	Dialight 552-0211	LEDx2 T1 3/4 PC Mount Red/Red
J1	High Density Connector	FCI 98414-F06-50U	2mm, 50 pins, keyed, latching header
J2	(Reserved)	–	–
J3	COM1, COM2	Kycon K42-E9P/P-A4N	Dual stacked DB-9 male
J4	PS/2 Keyboard and Mouse	Kycon KMDG-6S/6S-S4N	Dual stacked PS/2 female
J5	COM4	Conta-Clip 10250.4	5 pin screw terminal
J6	COM3	Conta-Clip 10250.4	5 pin screw terminal
S1	Reset Button	E-Switch 800SP9B7M6RE	Right angle momentary switch
SP1	Speaker	Challenge Electronics DBX05	Miniature speaker

CBR-4004 CONNECTORS
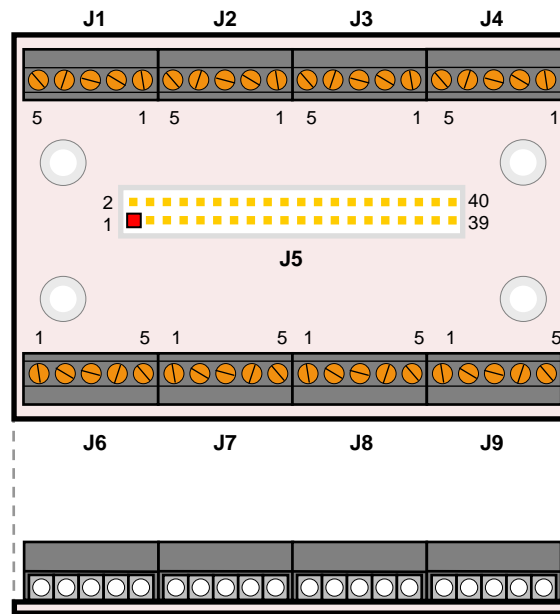
= Pin 1

Figure 11. CBR-4004 Connectors

CBR-4004 connector functions depend on the I/O connector to which it is attached, J5 or J10. See Table 5 (J5) or Table 7 (J10) for details.

Jumper Blocks

JUMPERS AS-SHIPPED CONFIGURATION
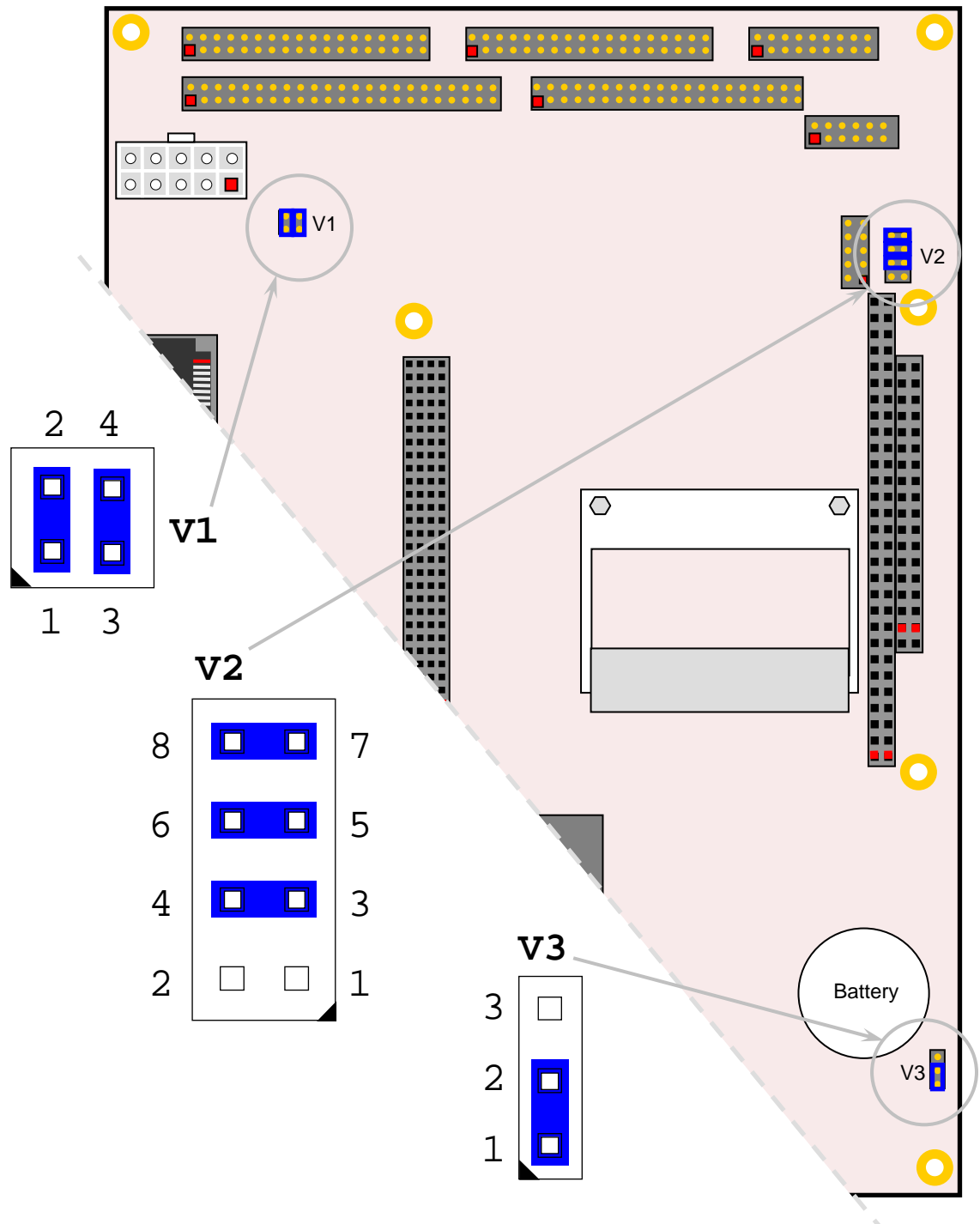
Figure 12. Jumper Block Locations

JUMPER SUMMARY

Table 2: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1[1-2]	**COM3 RS-485 Termination** In – 100 Ohm Termination Active Out – COM3 Unterminated	In	31
V1[3-4]	**COM4 RS-485 Termination** In – 100 Ohm Termination Active Out – COM4 Unterminated	In	31
V2[1-2]	**SD Master Selector** In – Compact FLASH Module is IDE Master Out – Compact FLASH Module is IDE Slave	Out	37
V2[3-4]	**General Purpose Input** In – CPU reads bit as 1 Out – CPU reads bit as 0	In	63
V2[5-6]	**Video BIOS Selector** In – Primary Video BIOS selected Out – Secondary Video BIOS selected The secondary video BIOS is field-upgradeable using the BIOS upgrade utility. See www.VersaLogic.com/private/pythonsupport.asp for more information.	In	39
V2[7-8]	**System BIOS Selector** In – Normal Operation Out – *Factory Use Only* This jumper should not be removed. If you hear a low-high beep tone and the EBX-11 appears to be failing to boot, verify that this jumper is properly installed.	In	–
V3[1-2-3]	**CMOS RAM and Real Time Clock Erase** [1-2] In – Normal [2-3] In – Erase CMOS RAM and Real-Time Clock	[1-2] In	23

4

Power Supply

POWER CONNECTORS

Main power is applied to the EBX-11 through an EPIC-style 10-pin polarized connector at location J3.

Warning!   To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors are wired correctly. Make sure to use both +5VDC pins and all ground pins to prevent excess voltage drop.
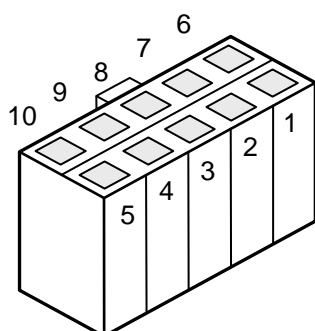
Table 3: Main Power Connector Pinout

J3 Pin	Signal Name	Description
1*	GND	Ground
2	GND	Ground
3	GND	Ground
4	+12VDC	Power Input
5	+3.3VDC	Power Input
6**	NC	Not Connected
7	+5VDC	Power Input
8	+5VDC	Power Input
9	-12VDC	Power Input
10	GND	Ground

* Pin 1 is typically used in EPIC-style power cables as a PS-ON signal. Since the EBX-11 does not support soft-off, pin 1 is internally connected to ground.

** Pin 6 is typically used in EPIC style power cables as a 5VSB (5V Stand By) signal. Since the EBX-11 does not support soft-off, pin 6 is an internal no connect.

Note   The +3.3VDC, +12VDC and -12VDC inputs on the main power connector are only required for PC/104-*Plus* and PC/104 expansion modules that require these voltages.

POWER REQUIREMENTS

The EBX-11 requires only +5 volts (±5%) for proper operation. The voltage required for the RS-232 ports and analog input sections are generated with a DC/DC converter. Low-voltage supply circuits provide power to the CPU and other on-board devices.

The exact power requirement of the EBX-11 depends on several factors, including memory configuration, CPU speed, peripheral connections, type and number of expansion modules and attached devices. For example, PS/2 keyboards typically draw their power directly from the EBX-11, and driving long RS-232 lines at high speed can increase power demand.

LITHIUM BATTERY

Warning!   To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly.

Normal battery voltage should be at least 3.0V. If the voltage drops below 3.0V, contact the factory for a replacement (part number HB3/0-1). The life expectancy under normal use is approximately 10 years.

CPU

The Geode LX 800 microcontroller has a 32-bit, low-voltage AMD x86 microprocessor at its core. The maximum clock rate is 500 MHz actual, with 800 MHz (Celeron equivalent) performance. The LX 800 features 64 kb of L1 cache, 128 kb of L2 cache, DDR SDRAM support, and an integrated display controller. The CPU operates without a heat sink and has a typical power consumption of 1.6W.

System RAM

COMPATIBLE MEMORY MODULES

The EBX-11 accepts one 200-pin SODIMM memory module with the following characteristics:

- Size   Up to 1GB
- Voltage   2.5V
- Type   PC2700 compatible (DDR 333 MHz)

Note   CMOS settings default to DDR 333 MHz. Settings to DDR 400 MHz are available, but VersaLogic only guarantees operation at the default settings.

CMOS RAM

CLEARING CMOS RAM

A jumper may be installed into V3[2-3] to erase the contents of the CMOS RAM and the Real-Time Clock. When clearing CMOS RAM: 1) Power off the EBX-11. 2) Remove the jumper from V3[1-2], install it on V3[2-3] and leave it for four seconds. 3) Move the jumper to back to V3[1-2]. 4) Power on the EBX-11.

CMOS Setup Defaults

The EBX-11 permits users to modify the CMOS Setup defaults. This allows the system to boot up with user-defined settings if CMOS RAM is cleared or corrupted. All CMOS setup defaults can be changed, except the time and date. The CMOS Setup defaults can be updated with the Flash BIOS Update (FBU) Utility, available from the General BIOS Information page.

Warning! If the CMOS Setup default settings make the system unbootable and prevent the user from entering CMOS Setup, the EBX-11 needs to be serviced by the factory.

DEFAULT CMOS RAM SETUP VALUES

After the CMOS RAM is cleared, the system will load default CMOS RAM parameters the next time the board is powered on. The default CMOS RAM setup values will be used in order to boot the system whenever the main CMOS RAM values are blank, or when the system battery is dead or has been removed from the board.

SAVING CMOS SETUP PARAMETERS AS CUSTOM DEFAULTS

To save CMOS Setup parameters to custom defaults, you will need a DOS bootable floppy with the FBU utility on it.

1. Boot the EBX-11 and enter CMOS Setup by pressing Delete during the early boot cycle.

2. Change the CMOS parameters as desired and configure the floppy drive as the first boot device:

    ```
    Basic CMOS Configuration | BOOT ORDER | Boot 1st: Drive A:
    ```

3. Save the settings and exit CMOS Setup.

4. Reboot the system from the DOS boot floppy.

5. Run FBU and select **Save CMOS contents**. A file named CMOS.BIN is created and saved to the floppy.

6. Select the FBU option **Load Custom CMOS defaults**. A directory of the floppy is displayed.

7. Select the CMOS.BIN file and press the **P** key to program the new CMOS defaults.

8. Reboot the system from the hard disk. The custom CMOS parameters are now saved as defaults.

Real Time Clock

The EBX-11 features a battery-backed 146818-compatible real-time clock/calendar chip. Under normal battery conditions, the clock maintains accurate timekeeping functions when the board is powered off.

SETTING THE CLOCK

The CMOS Setup utility (accessed by pressing the Delete key during a system boot) can be used to set the time/date of the real-time clock.

Interfaces and Connectors

Utility I/O Connectors

A number of interfaces on the EBX-11 are grouped together and made accessible through utility I/O connectors J4, J5, and J10. A number of cables and boards are available from VersaLogic that provide discrete connectors for each of the interfaces; however, you may wish to create custom cables that surface only the interfaces required by your application.

J4 I/O CONNECTOR

The 50-pin I/O connector (J4) incorporates the COM ports, keyboard and mouse, and the reset button and speaker interfaces. Table 4 illustrates the function of each pin.

Note: On Rev. 4 boards, the COM3 and COM4 connectors have a nonstandard pinout. The RxD+ and RxD- signals are transposed. The standard pinout is shown below. The nonstandard pinout is shown in Table 11.

Table 4: J4 I/O Connector Pinout – Rev. 5.00 and Later Boards

J4 Pin	CBR-5009B Connector	Pin	Signal		J4 Pin	CBR-5009B Connector	Pin	Signal	
1	**COM1**	1	Data Carrier Detect			**COM4**		RS-232	RS-422/485
2	**J3**	6	Data Set Ready		26	**J5**	1	Ground	Ground
3	Top DB9	2	Receive Data		27		5	RTS	TxD+
4		7	Request to Send		28		4	TXD	TxD-
5		3	Transmit Data		29		–	Ground	Ground
6		8	Clear to Send		30		2	RXD	RxD-
7		4	Data Terminal Ready		31		3	CTS	RxD+
8		9	Ring Indicator		32		–	Ground	Ground
9		5	Ground		33	**Mouse**	4	+5V (Protected)	
10	**COM2**	1	Data Carrier Detect		34	**J4**	1	Mouse Data	
11	**J3**	6	Data Set Ready		35	Top	3	Ground	
12	Bottom DB9	2	Receive Data		36		5	Mouse Clock	
13		7	Request to Send		37	**PBRESET**	1	Pushbutton Reset	
14		3	Transmit Data		38	**S1**	2	Ground	
15		8	Clear to Send		39	**(Reserved)**	1	Ground	
16		4	Data Terminal Ready		40		2	Not connected	
17		9	Ring Indicator		41		3	Ground	
18		5	Ground		42		4	Not connected	
	COM3		RS-232	RS-422/485	43	**Keyboard**	4	+5V (Protected)	
19	**J6**	1	Ground	Ground	44	**J4**	1	Keyboard Data	
20		5	RTS	TxD+	45	Bottom	3	Ground	
21		4	TXD	TxD-	46		5	Keyboard Clock	
22		–	Ground	Ground	47	**PLED**	1	+5V (Protected)	
23		2	RXD	RxD-	48	**D1**	2	Programmable LED	
24		3	CTS	RxD+	49	**Speaker**	1	+5V (Protected)	
25		–	Ground	Ground	50	**SP1**	2	Speaker Drive	

J5 I/O CONNECTOR

The 40-pin I/O connector (J5) incorporates the PWM interfaces, 16 digital I/O channels, and eight analog channels. Table 5 shows the function of each pin.

Note   On Rev. 4 boards, the TACH input, PWM output, and Digital I/O 0-10 signals were nonstandard. The signals were corrected in Rev. 5.00 boards. The standard pinout is shown below. The nonstandard pinout is shown in Table 6.

Table 5: J5 I/O Connector Pinout – Rev. 5.xx and Later Boards

J5 Pin	Signal	CBR-4004 Connector	CBR-4004 Pin (Label)*
1	TACH_IN 1	**J1**	5 (IO1)
2	TACH_IN 2	**TACH**	4 (IO2)
3	TACH_IN 3		3 (IO3)
4	NC		2 (IO4)
5	GND		1 (GND1)
6	PWM_OUT1	**J2**	5 (IO5)
7	PWM_OUT2	**PWM**	4 (IO6)
8	PWM_OUT3		3 (IO7)
9	NC		2 (IO8)
10	GND		1 (GND1)
11	Digital I/O 0	**J3**	5 (IO9)
12	Digital I/O 1	**Digital IO**	4 (IO10)
13	Digital I/O 2		3 (IO11)
14	Digital I/O 3		2 (IO12)
15	GND		1 (GND2)
16	Digital I/O 4	**J4**	5 (IO13)
17	Digital I/O 5	**Digital IO**	4 (IO14)
18	Digital I/O 6		3 (IO15)
19	Digital I/O 7		2 (IO16)
20	GND		1 (GND2)
21	Digital I/O 8	**J6**	1 (IO17)
22	Digital I/O 9	**Digital IO**	2 (IO18)
23	Digital I/O 10		3 (IO19)
24	Digital I/O 11		4 (IO20)
25	Pushbutton Reset		5 (GND3/PBRST#)
26	Digital I/O 12	**J7**	1 (IO21)
27	Digital I/O 13	**Digital IO**	2 (IO22)
28	Digital I/O 14		3 (IO23)
29	Digital I/O 15		4 (IO24)
30	GND		5 (GND3)
31	ADCH0	**J8**	1 (IO25)
32	ADCH1	**Analog**	2 (IO26)
33	ADCH2		3 (IO27)
34	ADCH3		4 (I028)
35	ADGND		5 (GND4)
36	ADCH4	**J9**	1 (IO29)
37	ADCH5	**Analog**	2 (IO30)
38	ADCH6		3 (IO31)
39	ADCH7		4 (IO32)
40	ADGND		5 (GND4)

Note: The CBR-4004 is a multipurpose board. The silkscreen label does not necessarily indicate pin function.

Table 6: J5 I/O Connector Pinout – Rev. 4.xx and Earlier Boards

J5 Pin	Signal	CBR-4004 J5 Pin	CBR-4004 Connector	CBR-4004 Pin (Label)*
1	TACH_IN 3	1	**J1**	5 (IO1)
2	GND	2	**PWM**	4 (IO2)
3	PWM_OUT1	3		3 (IO3)
4	TACH_IN 2	4		2 (IO4)
5	GND	5		1 (GND1)
6	PWM_OUT2	6	**J2**	5 (IO5)
7	TACH_IN 1	7	**PWM**	4 (IO6)
8	GND	8		3 (IO7)
9	PWM_OUT3	9		2 (IO8)
10	GND	10		1 (GND1)
11	GND	11	**J3**	5 (IO9)
12	Digital I/O 1	12	**Digital IO**	4 (IO10)
13	Digital I/O 0	13		3 (IO11)
14	Digital I/O 3	14		2 (IO12)
15	GND	15		1 (GND2)
16	Digital I/O 4	16	**J4**	5 (IO13)
17	Digital I/O 2	17	**Digital IO**	4 (IO14)
18	Digital I/O 6	18		3 (IO15)
19	Digital I/O 5	19		2 (IO16)
20	GND	20		1 (GND2)
21	Digital I/O 7	21	**J6**	1 (IO17)
22	Digital I/O 9	22	**Digital IO**	2 (IO18)
23	Digital I/O 8	23		3 (IO19)
24	Digital I/O 11	24		4 (IO20)
25	Digital I/O 10	25		5 (GND3/PBRST#)
26	Digital I/O 12	26	**J7**	1 (IO21)
27	Digital I/O 13	27	**Digital IO**	2 (IO22)
28	Digital I/O 14	28		3 (IO23)
29	Digital I/O 15	29		4 (IO24)
30	GND	30		5 (GND3)
31	ADCH0	31	**J8**	1 (IO25)
32	ADCH1	32	**Analog**	2 (IO26)
33	ADCH2	33		3 (IO27)
34	ADCH3	34		4 (I028)
35	ADGND	35		5 (GND4)
36	ADCH4	36	**J9**	1 (IO29)
37	ADCH5	37	**Analog**	2 (IO30)
38	ADCH6	38		3 (IO31)
39	ADCH7	39		4 (IO32)
40	ADGND	40		5 (GND4)

Note: The CBR-4004 is a multipurpose board. The silkscreen label does not necessarily indicate pin function.

J10 I/O CONNECTOR

The 40-pin I/O connector (J10) incorporates the USB0 and USB1 interfaces, 16 digital I/O channels, and the audio interface. Table 7 illustrates the function of each pin.

Table 7: J10 I/O Connector Pinout

J10 Pin	Signal	CB-4004 Connector	CBR-4004 Pin (Label)*
1	GND	**J1**	5 (IO1)
2	USBP0PWR	**USB0**	4 (IO2)
3	USPBP0+R		3 (IO3)
4	USBP0-R		2 (IO4)
5	GND		1 (GND1)
6	USBP1PWR	**J2**	5 (IO5)
7	USBP1+R	**USB1**	4 (IO6)
8	USBP1-R		3 (IO7)
9	GND		2 (IO8)
10	GND		1 (GND1)
11	Digital I/O 16	**J3**	5 (IO9)
12	Digital I/O 17	**Digital IO**	4 (IO10)
13	Digital I/O 18		3 (IO11)
14	Digital I/O 19		2 (IO12)
15	GND		1 (GND2)
16	Digital I/O 20	**J4**	5 (IO13)
17	Digital I/O 21	**Digital IO**	4 (IO14)
18	Digital I/O 22		3 (IO15)
19	Digital I/O 23		2 (IO16)
20	GND		1 (GND2)
21	Digital I/O 24	**J6**	1 (IO17)
22	Digital I/O 25	**Digital IO**	2 (IO18)
23	Digital I/O 26		3 (IO19)
24	Digital I/O 27		4 (IO20)
25	GND		5 (GND3/PBRST#)
26	Digital I/O 28	**J7**	1 (IO21)
27	Digital I/O 29	**Digital IO**	2 (IO22)
28	Digital I/O 30		3 (IO23)
29	Digital I/O 31		4 (IO24)
30	GND		5 (GND3)
31	NC	**J8**	1 (IO25)
32	AUDIOOUTR	**Audio Out**	2 (IO26)
33	NC		3 (IO27)
34	AUDIOOUTL		4 (I028)
35	AGND		5 (GND4)
36	NC	**J9**	1 (IO29)
37	AUDIOINR	**Audio In**	2 (IO30)
38	NC		3 (IO31)
39	AUDIOINL		4 (IO32)
40	AGND		5 (GND4)

Note: The CBR-4004 is a multipurpose board. The silkscreen label does not necessarily indicate pin function.

IDE

One IDE interface is available to connect up to two IDE devices, such as hard disks and CD-ROM drives. If the on-board CompactFlash is configured for use, only one other IDE device can be attached to the IDE controller. Connector J12 provides the interface to the IDE controller. Jumper V2[1-2] determines if the CompactFlash plugged into J11 is the master device or slave. Use CMOS Setup to specify the drive parameters of the attached drives.

Warning!   Cable length must be 18" or less to maintain proper signal integrity.

Table 8: IDE Hard Drive Connector Pinout

Pin	Signal Name	Function	Pin	Signal Name	Function
1	Reset-	Reset signal from CPU	23	DIOW	I/O write
2	Ground	Ground	24	Ground	Ground
3	DD7	Data bus bit 7	25	DIOR	I/O read
4	DD8	Data bus bit 8	26	Ground	Ground
5	DD6	Data bus bit 6	27	IORDY	I/O ready
6	DD9	Data bus bit 9	28	Ground	Ground
7	DD5	Data bus bit 5	29	DMACK-	DMA acknowledge
8	DD10	Data bus bit 10	30	Ground	Ground
9	DD4	Data bus bit 4	31	INTRQ	Interrupt request
10	DD11	Data bus bit 11	32	NC	No connection
11	DD3	Data bus bit 3	33	DA1	Device address bit 1
12	DD12	Data bus bit 12	34	CBLID-	Cable type identifier
13	DD2	Data bus bit 2	35	DA0	Device address bit 0
14	DD13	Data bus bit 13	36	DA2	Device address bit 2
15	DD1	Data bus bit 1	37	CS0	Chip select 0
16	DD14	Data bus bit 14	38	CS1	Chip select 1
17	DD0	Data bus bit 0	39	NC	No connection
18	DD15	Data bus bit 15	40	Ground	Ground
19	Ground	Ground	41	Power	+5.0 V
20	NC	Key	42	Power	+5.0 V
21	PDMARQ	DMA request	43	Ground	Ground
22	Ground	Ground	44	NC	No connection

Serial Ports

The EBX-11 features four on-board 16550-based serial channels located at standard PC I/O addresses. COM1 and COM2 are RS-232 (115.2K baud) serial ports. IRQ lines are chosen in CMOS Setup.

COM3 and COM4 can be operated in RS-232, RS-422 or RS-485 modes. Additional non-standard baud rates are also available (programmable in the normal baud registers) of up to 460k baud. IRQ lines are chosen in the CMOS Setup.

Each COM port can be independently enabled or disabled in CMOS Setup.

COM PORT CONFIGURATION

There are no configuration jumpers for COM1 and COM2 since they only operate in RS-232 mode. Use CMOS Setup to select between RS-232, RS-422, and RS485 operating modes for COM3 and COM4.

Jumper V1[1-2] is used to enable the RS-422/485 termination resistor for COM3. Jumper V1[3-4] is used to enable the RS-422/485 termination resistor for COM4. The termination resistor should be enabled for RS-422 and the RS-485 endpoint station. It should be disabled for RS-232 and the RS-485 intermediate station.

If RS-485 mode is used, the differential twisted pair (TxD+/RxD+ and TxD-/RxD-) is formed by connecting both transmit and receive pairs together. For example, on CBR-5009 connectors J6 and J5, the TxD+/RxD+ signal is formed by connecting pins 3 and 5, and the TxD-/RxD- signal is formed by connecting pins 2 and 4.

COM3 / COM4 RS-485 MODE LINE DRIVER CONTROL

The EBX-11 features automatic RS-485 direction control for COM ports 3 and 4. The purpose of this function is to save the effort of RS-485 direction control in software. The direction control signal RTS is used to tri-state the transmitter when no other data is available, so that other nodes can use the shared lines.

RS-485 direction control is set using the COM 3 Mode and COM 4 Mode parameters in CMOS Setup. To enable manual direction control, set the COM port mode to RS485 ManuFC; to enable auto direction control, set the parameter to RS485 AutoFC. Manual direction control is configured by asserting the RTS handshake line. Asserting the RTS handshake line puts the RS-485 port in transmit mode; de-asserting the line puts it in receive mode.

SERIAL PORT CONNECTORS

See the *Connector Location Diagrams* on pages 16 for connector and cable information. The pinouts of the DB9M connectors apply to the serial connectors on the VersaLogic breakout board CBR-5009.

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 9: COM1-2 Pinout – CBR-5009 Connector J3

COM1	COM2	
Top DB9 J3 Pin	Bottom DB9 J3 Pin	RS-232
1	10	DCD
2	11	RXD*
3	12	TXD*
4	13	DTR
5	14	Ground
6	15	DSR
7	16	RTS
8	17	CTS
9	18	RI

Note: On Rev. 4 boards, the COM3 and COM4 connectors have a nonstandard pinout. The RxD+ and RxD- signals are transposed, as shown in Table 11. The standard pinout is used on Rev. 5 boards, as shown in Table 10.

Table 10: COM3-4 Pinout – CBR-5009 Connectors J5-6 – Rev. 5 Boards

COM3	COM4			
J6 Pin	J5 Pin	RS-232	RS-422	RS-485
1	1	Ground	Ground	Ground
2	2	RXD	RxD-	RxD-
3	3	CTS	RxD+	RxD+
4	4	TXD	TxD-	TxD-
5	5	RTS	TxD+	TxD+

Table 11: COM3-4 Pinout – CBR-5009 Connectors J5-6 – Rev. 4 Boards

COM3	COM4			
J6 Pin	J5 Pin	RS-232	RS-422	RS-485
1	1	Ground	Ground	Ground
2	2	CTS	RxD+	RxD+
3	3	RXD	RxD-	RxD-
4	4	TXD	TxD-	TxD-
5	5	RTS	TxD+	TxD+

Parallel Port

The EBX-11 includes a standard bi-directional/EPP/ECP compatible LPT port (connector J18) which resides at the PC standard address of 378h. The port can be enabled or disabled and interrupt assignments can be made via the CMOS setup screen. The LPT mode is also set via the CMOS setup screen.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 12: LPT Parallel Port Pinout

J18 Pin	Centronics Signal	Signal Direction
1	Strobe	Out
2	Auto feed	Out
3	Data bit 0	In/Out
4	Printer error	In
5	Data bit 1	In/Out
6	Init	In/Out
7	Data bit 2	In/Out
8	Select input	Out
9	Data bit 3	In/Out
10	Data Bit 4	In/Out
11	Data Bit 5	In/Out
12	Data Bit 6	In/Out
13	Data Bit 7	In/Out
14	Ground	—
15	Acknowledge	In
16	Ground	—
17	Busy	In
18	Ground	—
19	Paper End	In
20	Printer Select	In

PS/2 Keyboard and Mouse

A standard PS/2 keyboard and mouse interface is accessible through connector J4 of the VersaLogic breakout board, CBR-5009. The breakout board is connected to connector J4 of the EBX-11. The 5V power provided to the keyboard and mouse is protected by a 1 Amp fuse.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 13: PS/2 Mouse and Keyboard

CBR-5009 J4 Top Pin	Signal	Description
1	MSDATA	Mouse Data
2	–	No Connection
3	GND	Ground
4	MKPWR	Protected +5V
5	MSCLK	Mouse Clock
6	–	No Connection
CBR-5009 J4 Bottom Pin	**Signal**	**Description**
1	KBDATA	Keyboard Data
2	–	No Connection
3	GND	Ground
4	MKPWR	Protected +5V
5	KBCLK	Keyboard Clock
6	–	No Connection

USB

The USB interface on the EBX-11 is OHCI (Open Host Controller Interface) and EHCI (Enhance Host Controller Interface) compatible, which provides a common industry software/hardware interface. There are four USB ports, one at connector J20, one at J21, and two at J10. The J20 and J21 connectors are standard USB Series A sockets. The USB interfaces at J10 are connected using the CBR-4004 screw terminal board (pinout below) or a custom cable.

BIOS CONFIGURATION

The USB controller can be enabled or disabled in CMOS Setup. The USB controller uses PCI interrupt "INTD#". CMOS Setup is used to select the IRQ line routed to each PCI interrupt line.

Table 14 USB Interface Connector J10

CBR-4004 J1 Pin	Signal Name	Function
1	GND	Ground
2	USBP0PWR	+5V (Protected)
3	USBP0+	Channel 0 Data +
4	USBP0−	Channel 0 Data −
5	GND	Ground
CBR-4004 J2 Pin	**Signal Name**	**Function**
6	USBP1PWR	+5V (Protected)
7	USBP1+	Channel 1 Data +
8	USBP1−	Channel 1 Data −
9	GND	Ground
10	GND	Ground

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

On revision 4.01 and earlier boards, one connector (J13) provided the interface to both USB2 and USB3. The connector was a 2mm 10-pin header. The pinout for this connector is shown below.

Table 15 USB2-3 Interface Connector J13 – Rev. 4.01 and Earlier

J13 Pin	Signal Name	Function
1	USBP2PWR	+5V (Protected)
3	USBP2–	Channel 2 Data –
5	USBP2+	Channel 2 Data +
7	GND	Ground
9	GND	Ground
2	USBP3PWR	+5V (Protected)
4	USBP3–	Channel 3 Data –
6	USBP3+	Channel 3 Data +
8	GND	Ground
10	GND	Ground

CompactFlash

Connector J11 provides a socket for a Type I or Type II CompactFlash (CF) module. This IDE based interface operates on the same channel than the IDE interface at connector J12. The CF interface supports operation in DMA mode.

The following CF modules have been tested and qualified as bootable devices by VersaLogic. Part numbers with a suffix of -3500 are RoHS-compliant.

Table 16. Qualified Bootable CF Modules

Manufacturer	Density	Mfg Part Number
Hagiwara	1 GB	CF1-1GMDG(H00AA)
Hagiwara	512 MB	CF1-512MDG(H00AA)
Silicon Systems	128 MB	SSD-C12M-3012
Silicon Systems	128 MB	SSD-C12M-3500
Silicon Systems	256 MB	SSD-C25M-3012
Silicon Systems	256 MB	SSD-C25MI-3012
Silicon Systems	256 MB	SSD-C25M-3500
Silicon Systems	256 MB	SSD-C25MI-3500
Silicon Systems	512 MB	SSD-C51M-3012
Silicon Systems	512 MB	SSD-C51MI-3012
Silicon Systems	512 MB	SSD-C51M-3500
Silicon Systems	512 MB	SSD-C51MI-3500
Silicon Systems	1 GB	SSD-C01G-3012
Silicon Systems	1 GB	SSD-C01G-3500
Silicon Systems	2 GB	SSD-C02G-3012
Silicon Systems	2 GB	SSD-C02GI-3012
Silicon Systems	2 GB	SSD-C02G-3500
Silicon Systems	4 GB	SSD-C04GI-3012

INSTALLING AN OPERATING SYSTEM ON COMPACTFLASH

On EBX-11 Rev. 5.02 and earlier boards, to install an operating system from a CD-ROM drive to the CF, the CF must be configured as the slave IDE device and the CD-ROM drive as the master. To ensure proper OS installation, do the following:

1. Verify that no jumper is installed at V2[1-2]. This is the default setting, which designates the CF as the slave IDE device.

2. Jumper the CD-ROM drive as the master IDE device.

3. Configure the following CMOS Setup parameters on the Basic CMOS Configuration screen:

```
DRIVE ASSIGNMENT ORDER | DRIVE C: Ide 1/Pri Slave
ATA DRV ASSIGNMENT | Ide 0: 5 = IDE CDROM
ATA DRV ASSIGNMENT | Ide 1: 3 = AUTOCONFIG,LBA
BOOT ORDER | Boot 1st: CDROM
```

After installing the OS, you may configure the CF to be the first boot device, which will reduce boot time.

This slave-only restriction does not apply to EBX-11 Rev. 5.03 or later boards.

Programmable LED

Connector J4 includes an output signal for attaching a software controlled LED. Connect the cathode of the LED to J4, pin 48; connect the anode to +5V. An on-board resistor limits the current to 15 mA when the circuit is turned on. A programmable LED is provided on the CBR-5009 breakout board.

To turn the LED on and off, set or clear bit D7 in I/O port 1D0h (or 1E0h). When changing the register, make sure not to alter the value of the other bits.

The following code examples show how to turn the LED on and off. Refer to page 59 for further information:

```
LED On                LED Off
MOV    DX,1D0H        MOV    DX,1D0H
IN     AL,DX          IN     AL,DX
OR     AL,80H         AND    AL,7FH
OUT    DX,AL          OUT    DX,AL
```

External Speaker

A miniature 8 ohm speaker can be connected between J4, pin 50 (SPKO*) and J4, pin 49 (MKPWR). A speaker is provided on the CBR-5009 breakout board.

Push-Button Reset

Connector J4 includes an input for a push-button reset switch. Shorting J4, pin 37 to ground causes the EBX-11 to reboot.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

A reset button is provided on the CBR-5009 breakout board.

Video Interface

An on-board video controller integrated into the chipset provides high performance video output for the EBX-11.

CONFIGURATION

The video interface uses PCI interrupt INTA*. CMOS Setup is used to select the IRQ line routed to INTA*.

The EBX-11 uses shared memory architecture. This allows the video controller to use variable amounts of system DRAM for video RAM. The amount of RAM used for video is set with a CMOS Setup option.

The EBX-11 supports two types of video output, SVGA and LVDS Flat Panel Display. A CMOS Setup option is used to select which output is enabled after POST.

VIDEO BIOS SELECTION

Jumper V2[5-6] can be removed to allow the system to boot off of the Secondary Video BIOS. Unlike the Primary Video BIOS, the Secondary Video BIOS can be reprogrammed in the field.

SVGA OUTPUT CONNECTOR

See the diagram on page 16 for the location of connector J6. An adapter cable, part number CBR-1201, is available to translate J6 into a standard 15-pin D-Sub SVGA connector.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 17: Video Output Pinout

J6 Pin	Signal Name	Function		Mini DB15 Pin
1	GND	Ground		6
2	RED	Red video		1
3	GND	Ground		7
4	GREEN	Green video		2
5	GND	Ground		8
6	BLU	Blue video		3
7	GND	Ground		5
8	HSYNC	Horizontal sync		13
9	GND	Ground		10
10	VSYNC	Vertical sync		14
11	CRT_SCL	DDC data clock line		15
12	CRT_SDA	DDC serial data line		12

LVDS FLAT PANEL DISPLAY CONNECTOR

The integrated LVDS Flat Panel Display in the EBX-11 is an ANSI/TIA/EIA-644-1995 specification-compliant interface. It can support up to 24 bits of RGB pixel data plus 3 bits of timing control (HSYNC/VSYNC/DE) on the 4 differential data output pairs. The LVDS clock frequency ranges from 25 MHz to 112 MHz.

CMOS Setup provides several options for standard LVDS Flat Panel types. If these options do not match the requirements of the panel you are attempting to use, contact Support@VersaLogic.com for a custom video BIOS.

The 3.3V power provided to pins 19 and 20 of J9 is protected by a 1 Amp fuse.

Table 18: LVDS Flat Panel Display Pinout

J9 Pin	Signal Name	Function
1	GND	Ground
2	NC	Not Connected
3	LVDSA3	Diff. Data (+)
4	LVDSA3#	Diff. Data 3 (−)
5	GND	Ground
6	LVFSCLK0	Differential Clock (+)
7	LVDSCLK0#	Differential Clock (−)
8	GND	Ground
9	LVDSA2	Diff. Data 2 (+)
10	LVDSA2#	Diff. Data 2 (−)
11	GND	Ground
12	LVDSA1	Diff. Data 1 (+)
13	LVDSA1#	Diff. Data 1 (−)
14	GND	Ground
15	LVDSA0	Diff. Data 0 (+)
16	LVDSA0#	Diff. Data 0 (−)
17	GND	Ground
18	GND	Ground
19	+3.3V	Protected Power Supply
20	+3.3V	Protected Power Supply

COMPATIBLE LVDS PANEL DISPLAYS

The following flat panel displays are reported to work properly with the integrated graphics video controller chip used on the EBX-11.

Table 19: Compatible Flat Panel Displays

Manufacturer	Model Number	Panel Size	Resolution	Interface	Panel Technology
eVision Displays	xxx084S01 series	8.4"	800 x 600 18-bit	LVDS	TFT
au Optronix	B084SN01	8.4"	800 x 600 18-bit	LVDS	TFT
eVision Displays	xxx104S01 series	10.4"	800 x 600 18-bit	LVDS	TFT
au Optronix	B104SN01	10.4"	800 x 600 18-bit	LVDS	TFT
eVision Displays	xxx141X01 series	14.1"	1024 x 768 18-bit	LVDS	TFT
Sharp	LQ121S1LG411	12.1"	800 x 600 18-bit	LVDS	TFT

CONSOLE REDIRECTION

The EBX-11 can be operated without using the on-board video output by redirecting the console to COM1. CMOS Setup and some operating systems such as DOS can use this console for user interaction.

In the Features Configuration screen, there is an option to control console redirection. This option can be set to Auto or Redirect. When set to Auto, the console will not be redirected to COM1 unless a signal is detected from the terminal by pressing and holding down CRTL-C. When set to Redirect, the console will be directed to COM1.

Notes on console redirection:

- When console redirection is enabled, you can access CMOS Setup by typing Ctrl-C.

- The decision to redirect the console is made early in BIOS execution and cannot be changed later.

- The redirected console uses 115200 baud, 8 data bits, 1 stop bit, no parity, and no flow control.

- The default console redirection setting is Auto. The default can be reloaded without entering BIOS setup by discharging CMOS contents.

Null Modem:

The following diagram illustrates a typical DB9 to DB9 RS-232 null modem adapter. Pins 7 and 8 are shorted together on each connector. Unlisted pins have no connection.

```
   System 1   <-->   System 2
   Name Pin         Pin Name
   -----------------------
   TX    3    <-->    2   RX
   RX    2    <-->    3   TX
   RTS   7    <-->    1   DCD
   CTS   8
   DSR   6    <-->    4   DTR
   DCD   1    <-->    7   RTS
                      8   CTS
   DTR   4    <-->    6   DSR
```

Ethernet Interface

The EBX-11 features two Intel 82551ER Fast Ethernet controllers on-board. While these controllers are not NE2000-compatible, they are widely supported. Drivers are readily available to support a variety of operating systems. See VersaLogic website for latest OS support.

BIOS CONFIGURATION

Each Ethernet controller can be enabled or disabled in CMOS Setup. Ethernet interface 0 (J1) uses PCI interrupt "INTA#" and Ethernet interface 1 (J2) uses PCI interrupt "INTB#". CMOS Setup is used to select the IRQ line routed to each PCI interrupt line.

STATUS LED

Each Ethernet controller has a two-colored LED located next to its RJ-45 connector to provide an indication of the Ethernet status as follows:

Green LED (Link):

- ON   Active Ethernet cable plugged in
- OFF   Active cable not plugged in
  or cable not plugged into active hub

Yellow LED (Activity):

- ON   Activity detected on cable
- OFF   No Activity detected on cable

ETHERNET CONNECTOR

Board-mounted RJ-45 connectors are provided to make connections with Category 5 Ethernet cables. The 82551ER Ethernet controller auto-detects 10BaseT/100Base-TX connectors.

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 20: RJ-45 Ethernet Connector

J1/J2 Pin	Fast Ethernet		Gigabit Ethernet	
	Signal Name	Function	Signal Name	Function
1	T+	Transmit Data +	MID0+	Media Dependent Interface [0]+
2	T−	Transmit Data −	MID0−	Media Dependent Interface [0]−
3	R+	Receive Data +	MID1+	Media Dependent Interface [1]+
4	IGND	Isolated Ground	MID2+	Media Dependent Interface [2]+
5	IGND	Isolated Ground	MID2−	Media Dependent Interface [2]−
6	R−	Receive Data −	MID1−	Media Dependent Interface [1]−
7	IGND	Isolated Ground	MID3+	Media Dependent Interface [3]+
8	IGND	Isolated Ground	MID3−	Media Dependent Interface [3]−

Audio

The audio interface on the EBX-11 is implemented using the Analog Devices AD1981B Audio Codec. This interface is AC'97 2.3 compatible. Drivers are available for most Windows-based operating systems. To obtain the most current versions, consult the EBX-11 product support page at **http://www.versalogic.com/private/pythonsupport.asp.**

J10 provides the line-level stereo input and line-level stereo output connection points. The outputs will drive any standard-powered PC speaker set.

SOFTWARE CONFIGURATION

The audio interface uses PCI interrupt "INTB#". The CMOS setup screen is used to select the IRQ line routed to INTB#.

The audio controller can be disabled within the CMOS setup.

Table 21: Audio Connector

CBR-4004 J10 Pin	Signal Name	Function
37	AUDINR	Line-In Right
39	AUDINL	Line-In Left
40	AGND	Ground
CBR-4004 J10 Pin	Signal Name	Function
32	AUDOUTR	Line-Out Right
34	AUDOUTL	Line-Out Left
35	AGND	Ground

CPU Temperature Monitor

A thermometer circuit constantly monitors the die temperature of the CPU. This circuit can be used to detect over-temperature conditions which can result from fan or heat sink failure or excessive ambient temperatures.

The system can be configured to generate an interrupt when the temperature exceeds the BIOS programmed threshold.

Contact the factory for information on reading and writing to the thermometer circuits.

Industrial I/O Functions and SPI Interface

The EBX-11 employs a set of I/O registers for controlling on-board analog input, digital I/O, and external serial peripheral interface (SPI) devices. These functions share control and data registers located at I/O addresses 1D8h through 1DDh.

The SPI bus specifies four logic signals:

- SCLK – Serial clock (output from master)
- MOSI – Master output, slave input (output from master)
- MISO – Master input, slave output (output from slave)
- SS – Slave select (output from master)

The EBX-11 SPI implementation adds additional features, such as hardware interrupt input to the master. The master initiates all SPI transactions. A slave device responds when its slave select is asserted and it receives clock pulses from the master.

Slave selects are controlled in one of two modes: manual or automatic. In automatic mode, the slave select is asserted by the SPI controller when the most significant data byte is written. This initiates a transaction to the specified slave device. In manual mode, the slave select is controlled by the user and any number of data frames can be sent. The user must command the slave select high to complete the transaction.

The SPI clock rate can be software configured to operate at speeds between 1 MHz and 8 MHz. All four common SPI modes are supported through the use of clock polarity and clock phase controls.

To initiate an SPI transaction, configure SPI registers SPICONTROL and SPISTATUS as shown in Table 23 and Table 24 for the desired I/O device. For additional information on communicating with specific SPI devices, please refer to their respective manufacturer's datasheets. Table 22 lists configuration values for on-board SPI devices.

Table 22: Analog Input and Digital I/O Register Values

Analog Input			Digital I/O		
I/O Port	Value	Description	I/O Port	Value	Description
1D8h	15h	Idle low, rising edge, 16-bit frame length, automatic slave select, ADC_SS	1D8h	26h	Idle low, rising edge, 24-bit frame length, auto slave select, DIO_0_SS
1D9h	30h	8 MHz, IRQ disabled, MSbit shift	1D9h	F8h	IRQ10, 8 MHz, hardware IRQ enabled, MSbit shift
1DAh	00h	Not used in 16-bit frame	1DAh	00h	Not used in 24-bit frame
1DBh	00h	Not used in 16-bit frame	1DBh	XXh	Data byte
1DCh	00h	Any value, data ignored	1DCh	XXh	Address byte
1DDh	XXh	XX = A/D channel (0-7), written to bits 5-3	1DDh	XXh	Command byte

SPI CONTROL REGISTERS

This section describes the SPI registers for the EBX-11 Rev. 6.00 and later. Appendix B – Legacy SPI Interface describes the SPI registers for Rev. 5.xx and earlier.

SPICONTROL (READ/WRITE) 1D8h

D7	D6	D5	D4	D3	D2	D1	D0
CPOL	CPHA	SPILEN1	SPILEN0	MAN_SS	SS2	SS1	SS0

Table 23: SPI Control Register Bit Assignments

Bit	Mnemonic	Description
D7	CPOL	**SPI Clock Polarity –** Sets the SCLK idle state. 0 = SCLK idles low 1 = SCLK idles high
D6	CPHA	**SPI Clock Phase –** Sets the SCLK edge on which valid data will be read. 0 = Data read on rising edge 1 = Data read on falling edge

D5-D4	SPILEN	**SPI Frame Length –** Sets the SPI frame length. This selection works in manual and auto slave select modes.
		
		SPILEN1 SPILEN0 Frame Length
		   0 0 8-bit
		   0 1 16-bit
		   1 0 24-bit
		   1 1 32-bit

D3	MAN_SS	**SPI Manual Slave Select Mode –** This bit determines whether the slave select lines are controlled through the user software or are automatically controlled by a write operation to SPIDATA3 (1DDh). If MAN_SS = 0, then the slave select operates automatically; if MAN_SS = 1, then the slave select line is controlled manually through SPICONTROL bits SS2, SS1, and SS0. 0 = Automatic, default 1 = Manual
D2-D0	SS	**SPI Slave Select –** These bits select which slave select will be asserted. The SSx# pin on the base board will be directly controlled by these bits when MAN_SS = 1. **SS2 SS1 SS0 Slave Select** 0 0 0 None, port disabled 0 0 1 SPX Slave Select 0, J17 pin-8 0 1 0 SPX Slave Select 1, J17 pin-9 0 1 1 SPX Slave Select 2, J17 pin-10 1 0 0 SPX Slave Select 3, J17 pin-11 1 0 1 On-Board A/D Converter Slave Select 1 1 0 On-Board Digital I/O Ch 0-Ch 15 Slave Select 1 1 1 On-Board Digital I/O Ch 16-Ch 31 Slave Select

SPISTATUS (READ/WRITE) 1D9h

D7	D6	D5	D4	D3	D2	D1	D0
IRQSEL1	IRQSEL0	SPICLK1	SPICLK0	HW_IRQ_EN	LSBIT_1ST	HW_INT	BUSY

Table 24: SPI Control and Status Register Bit assignments

Bit	Mnemonic	Description
D7-D6	IRQSEL	**IRQ Select** – These bits select which IRQ will be asserted when a hardware interrupt from a connected SPI device occurs. The HW_IRQ_EN bit must be set to enable SPI IRQ functionality. **IRQSEL1 IRQSEL0 IRQ** 0 0 IRQ3 0 1 IRQ4 1 0 IRQ5 1 1 IRQ10 **Note:** The on-board digital I/O chips must be configured for open-drain and mirrored interrupts in order for any SPI device to use hardware interrupts (see Digital I/O Interface).
D5-D4	SPICLK	**SPI SCLK Frequency –** These bits set the SPI clock frequency. **SPICLK1 SPICLK0 Frequency** 0 0 1.042 MHz 0 1 2.083 MHz 1 0 4.167 MHz 1 1 8.333 MHz
D3	HW_IRQ_EN	**Hardware IRQ Enable** – Enables or disables the use of the selected IRQ (IRQSEL) by an SPI device. 0 = SPI IRQ disabled, default 1 = SPI IRQ enabled **Note:** The selected IRQ is shared with PC/104 ISA bus devices. CMOS settings must be configured for the desired ISA IRQ.
D2	LSBIT_1ST	**SPI Shift Direction** – Controls the SPI shift direction of the SPIDATA registers. The direction can be shifted toward the least significant bit or the most significant bit. 0 = SPIDATA data is left-shifted (MSbit first), default 1 = SPIDATA data is right-shifted (LSbit first)
D1	HW_INT	**SPI Device Interrupt State –** This bit is a status flag that indicates when the hardware SPX signal SINT# is asserted. 0 = Hardware interrupt on SINT# is deasserted 1 = Interrupt is present on SINT# This bit is read-only and is cleared when the SPI device's interrupt is cleared.
D0	BUSY	**SPI Busy Flag** – This bit is a status flag that indicates when an SPI transaction is underway. 0 = SPI bus idle 1 = SCLK is clocking data in and out of the SPIDATA registers This bit is read-only.

SPI DATA REGISTERS

SPIDATA0 (READ/WRITE) 1DAh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA1 (READ/WRITE) 1DBh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA2 (READ/WRITE) 1DCh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 (READ/WRITE) 1DDh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 contains the most significant byte (MSB) of the SPI data word. A write to this register will initiate the SPI clock and, if the MAN_SS bit = 0, will also assert a slave select to begin an SPI bus transaction. Increasing frame sizes from 8-bit use the lowest address for the least significant byte of the SPI data word; for example, the LSB of a 24-bit frame would be SPIDATA1. Data is sent according to the LSBIT_1ST setting. When LSBIT_1ST = 0, the MSbit of SPIDATA3 is sent first, and received data will be shifted into the LSbit of the selected frame size set in the SPILEN field. When LSBIT_1ST = 1, the LSbit of the selected frame size is sent first, and the received data will be shifted into the MSbit of SPIDATA3.

Analog Input

The EBX-11 employs a multi-range, 12-bit A/D converter that accepts up to eight single-ended input signals. The converter features 500k samples per second, with input range of 0 to +4.095V.

The A/D converter is accessed through the SPI interface.

SOFTWARE CONFIGURATION

Configure the SPX registers for Analog Input as shown in Table 22. The EBX-11 cannot be configured to issue an interrupt upon completion of an A/D conversion, so the software must poll the BUSY bit to determine when the conversion is complete.

EXTERNAL CONNECTIONS

Single-ended analog voltages are applied to connectors J8 and J9 of the CBR-4004 board (connected to J5 of the EBX-11) as shown in the following table.

Table 25: Analog Input Connector

J5 Pin	Signal	CBR-4004 J5 Pin	CBR-4004 Connector	CBR-4004 Pin (Signal)
31	ADCH0	31	**J8** **Analog**	1 (IO25)
32	ADCH1	32		2 (IO26)
33	ADCH2	33		3 (IO27)
34	ADCH3	34		4 (I028)
35	ADGND	35		5 (GND4)
36	ADCH4	36	**J9** **Analog**	1 (IO29)
37	ADCH5	37		2 (IO30)
38	ADCH6	38		3 (IO31)
39	ADCH7	39		4 (IO32)
40	ADGND	40		5 (GND4)

CALIBRATION

There are no calibration adjustments. Calibration, if desired, is accomplished by mathematical transformation in software.

INITIATING AN ANALOG CONVERSION

The following procedure can be used to initiate an analog conversion.

1. Write 15h to the SPICONTROL register (I/O address 1D8h) – This value configures the SPI port to select the on-board A/D converter, 16-bit frame length, low SCLK idle state, rising edge SCLK edge, and automatic slave select.

2. Write 30h to the SPISTATUS register (I/O address 1D9h) – This value selects 8 MHz SCLK speed, hardware IRQ disable, and left-shift data.

3. Write any value to SPIDATA2 (I/O address 1DCh) – This data will be ignored by the A/D converter.

4. Write the analog input channel number to bits 5-3 of SPIDATA3 (1DDh) – Any write operation to this register triggers an SPI transaction.

5. Poll the BUSY bit until the conversion is completed.

6. Read the conversion data from SPIDATA2 (lower 8 bits) and SPIDATA3 (upper 4 bits).

Each analog conversion returns the conversion data from the previous conversion. The first analog conversion after power-up or reset returns the data from ADCH0. The second conversion returns the conversion data from the channel addressed in the first conversion. Each successive conversion returns conversion data from the previous conversion.

This means that multiple conversions on the same A/D channel return valid data after every conversion, starting with the second conversion. However, if a different channel is selected between analog reads, two conversions will be necessary to return valid data from the new channel. The analog input code example on page 50 shows how to use a 32bit SPI frame for an automatic second conversion when only one sample is desired.

ANALOG INPUT RANGE

Analog inputs are in binary format, 0 to +4.095V only.

The full analog input range is divided into 4096 steps. The output code (0000h) is associated with an analog input voltage of 0 Volts (ground). All codes are considered positive.

Sample values are shown in the following table:

Table 26: Binary Data Format

0 to +5V Input Voltage	Hex	Decimal	Comment
>+4.095	–	–	Out of range
+4.095	0FFFh	4095	Maximum voltage
+2.047	0800h	2048	Half scale
+1.023	0400h	1024	Quarter scale
+0.001	0001h	1	1 LSB
0.000	0000h	0	Zero (ground input)

ANALOG INPUT CODE EXAMPLE

The following code example illustrates the procedure for reading an analog voltage from the onboard ADC channel 3. A 32bit SPI frame is used to provide a valid single sample.

```
        MOV   DX, 1D8h
        MOV   AL, 35h      ;SPICONTROL: SPI Mode 00, 32bit, auto ADC_SS#
        OUT   DX, AL
        MOV   DX, 1D9h
        MOV   AL, 30h      ;SPISTATUS: 8MHz, no IRQ, left-shift
        OUT   DX, AL
                           ;SPIDATA2, SPIDATA1, SPIDATA0: don't care
        MOV   DX, 1DDh
        MOV   AL, 18h      ;SPIDATA3: ADC78H90 AIN4 = EBX-11 ADCH3
        OUT   DX, AL

BUSY:   MOV   DX, 1D9h     ;Get SPISTATUS
        IN    AL, DX
        AND   AL, 01h      ;Isolate the BUSY bit
        JNZ   BUSY         ;Loop back if SPI transaction not complete

        MOV   DX, 1DAh     ;Point to SPIDATA0 register
        IN    AX, DX       ;16bit input reads current conversion data
                           ;from SPIDATA1 into AH and from SPIDATA0 into
                           ;AL
```

For more detailed information on the EBX-11 A/D converter, please refer to the National Semiconductor ADC78H90 Datasheet.

Digital I/O Interface

The EBX-11 includes a 32-channel digital I/O interface. The digital lines are grouped as four 8-bit bi-directional ports. Data direction and output driver type are configurable by software.

Input data can be inverted through register settings. Any I/O pin(s) can generate an interrupt on change of state. All I/O pins use 3.3V signaling. As outputs, the I/O pins can source or sink 24 mA each.

Warning!   Damage will occur if the I/O pins are connected to 5V logic.

EBX-11 digital I/O ports are accessed through the SPI interface.

EXTERNAL CONNECTIONS

Digital I/O channels 0-15 are accessed via connector J5 on the EBX-11. Table 27 shows the pinout of these channels to the CBR-4004 expansion board connected to J5.

Digital I/O channels 16-31 are accessed via connector J10 on the EBX-11. Table 28 shows the pinout of these channels to the CBR-4004 expansion board connected to J10.

Note   Table 27 shows the pinout for Rev. 5.00 and later boards. See Table 6 for the pinout of Rev. 4.xx and earlier boards.

Table 27: Digital I/O Connections – Channels 0-15

J5 Pin	Signal	CBR-4004 J5 Pin	CBR-4004 Connector	CBR-4004 Pin (Label)*
11	Digital I/O 0	11	**J3** **Digital IO**	5 (IO9)
12	Digital I/O 1	12		4 (IO10)
13	Digital I/O 2	13		3 (IO11)
14	Digital I/O 3	14		2 (IO12)
15	GND	15		1 (GND2)
16	Digital I/O 4	16	**J4** **Digital IO**	5 (IO13)
17	Digital I/O 5	17		4 (IO14)
18	Digital I/O 6	18		3 (IO15)
19	Digital I/O 7	19		2 (IO16)
20	GND	20		1 (GND2)
21	Digital I/O 8	21	**J6** **Digital IO**	1 (IO17)
22	Digital I/O 9	22		2 (IO18)
23	Digital I/O 10	23		3 (IO19)
24	Digital I/O 11	24		4 (IO20)
25	Pushbutton Reset	25		5 (GND3/PBRST#)
26	Digital I/O 12	26	**J7** **Digital IO**	1 (IO21)
27	Digital I/O 13	27		2 (IO22)
28	Digital I/O 14	28		3 (IO23)
29	Digital I/O 15	29		4 (IO24)
30	GND	30		5 (GND3)

Note: The CBR-4004 is a multipurpose board. The silkscreen label does not necessarily indicate pin function.

Table 28: Digital I/O Connections – Channels 16-31

J10 Pin	Signal	CB-4004 Connector	CBR-4004 Pin (Label)*
11	Digital I/O 16	**J3** **Digital IO**	5 (IO9)
12	Digital I/O 17		4 (IO10)
13	Digital I/O 18		3 (IO11)
14	Digital I/O 19		2 (IO12)
15	GND		1 (GND2)
16	Digital I/O 20	**J4** **Digital IO**	5 (IO13)
17	Digital I/O 21		4 (IO14)
18	Digital I/O 22		3 (IO15)
19	Digital I/O 23		2 (IO16)
20	GND		1 (GND2)
21	Digital I/O 24	**J6** **Digital IO**	1 (IO17)
22	Digital I/O 25		2 (IO18)
23	Digital I/O 26		3 (IO19)
24	Digital I/O 27		4 (IO20)
25	GND		5 (GND3/PBRST#)
26	Digital I/O 28	**J7** **Digital IO**	1 (IO21)
27	Digital I/O 29		2 (IO22)
28	Digital I/O 30		3 (IO23)
29	Digital I/O 31		4 (IO24)
30	GND		5 (GND3)

Note: The CBR-4004 is a multipurpose board. The silkscreen label does not necessarily indicate pin function.

DIGITAL I/O PORT CONFIGURATION

Digital I/O channels 0-15 are accessed via SPI slave select 6 (writing 6h to the SS field of SPICONTROL). Channels 16-31 are accessed via SPI chip select 7 (writing 7h to the SS field). Each pair of I/O ports is configured by a set of paged I/O registers accessible through SPI. These registers control settings such as signal direction, input polarity, and interrupt source.

INTERRUPT GENERATION

The EBX-11 digital I/O can be configured to issue hardware interrupts on the transition (high to low or low to high) of any digital I/O pin. IRQ assignment is made in SPI control register SPISTATUS. Note that this IRQ is shared among all SPI devices on-board and externally connected to the EBX-11. The IRQ is also shared with the PC/104 bus and must be enabled in CMOS for ISA IRQx. Digital I/O port interrupt configuration is achieved through I/O port register settings. Please refer to the Microchip MCP23S17 datasheet for more information.

The on-board digital I/O chips must be configured for open-drain and mirrored interrupts in order for any SPI device to use hardware interrupts. The following code example illustrates how to do this.

```
MOV    DX, 1D8h
MOV    AL, 26h     ;SPICONTROL: SPI Mode 00, 24bit, auto DIO_0_SS#
OUT    DX, AL
MOV    DX, 1D9h
MOV    AL, 30h     ;SPISTATUS: 8MHz, no IRQ, left-shift
OUT    DX, AL
MOV    DX, 1DBh
MOV    AL, 44h     ;SPIDATA1: Mirror & Open-Drain interrupts
```

```
        OUT   DX, AL
        MOV   DX, 1DCh
        MOV   AL, 0Ah     ;SPIDATA2: MCP23S17 address 0x0A
        OUT   DX, AL
        MOV   DX, 1DDh
        MOV   AL, 40h     ;SPIDATA3: MCP23S17 write command
        OUT   DX, AL

BUSY:   MOV   DX, 1D9h
        IN    AL, DX      ;Get SPI status
        AND   AL, 01h     ;Isolate the BUSY bit
        JNZ   BUSY        ;Loop back if SPI transaction is not complete

        MOV   DX, 1D8h
        MOV   AL, 27h     ;SPICONTROL: SPI Mode 00, 24bit, auto DIO_1_SS#
        OUT   DX, AL
        MOV   DX, 1D9h
        MOV   AL, 30h     ;SPISTATUS: 8MHz, no IRQ, left-shift
        OUT   DX, AL
        MOV   DX, 1DBh
        MOV   AL, 44h     ;SPIDATA1: Mirror & Open-Drain interrupts
        OUT   DX, AL
        MOV   DX, 1DCh
        MOV   AL, 0Ah     ;SPIDATA2: MCP23S17 address 0x0A
        OUT   DX, AL
        MOV   DX, 1DDh
        MOV   AL, 40h     ;SPIDATA3: MCP23S17 write command
        OUT   DX, AL
```

WRITING TO A DIGITAL I/O PORT

The following code example initiates a write of 55h to Digital I/O port bits DIO15-DIO8.

```
        ;Write 44h to configure MCP23S17 register IOCON

        MOV   DX, 1D8h
        MOV   AL, 26h     ;SPICONTROL: SPI Mode 00, 24bit, DIO_0_SS#
        OUT   DX, AL
        MOV   DX, 1D9h
        MOV   AL, 30h     ;SPISTATUS: 8MHz, no IRQ, left-shift
        OUT   DX, AL
        MOV   DX, 1DBh
        MOV   AL, 44h     ;SPIDATA1: mirror and open-drain interrupts
        OUT   DX, AL
        MOV   DX, 1DCh
        MOV   AL, 0Ah     ;SPIDATA2: MCP23S17 IOCON register address 0Ah
        OUT   DX, AL
        MOV   DX, 1DDh
        MOV   AL, 40h     ;SPIDATA3: MCP23S17 write command
        OUT   DX, AL
        CALL  BUSY        ;Poll busy flag to wait for SPI transaction

        ;Configure MCP23S17 register IODIRA for outputs

        MOV   DX, 1DBh
        MOV   AL, 00h     ;SPIDATA1: 00h for outputs
        OUT   DX, AL
        MOV   DX, 1DCh
        MOV   AL, 00h     ;SPIDATA2: MCP23S17 register address 00h
        OUT   DX, AL
        MOV   DX, 1DDh
        MOV   AL, 40h     ;SPIDATA3: MCP23S17 write command
        OUT   DX, AL
        CALL  BUSY        ;Poll busy flag to wait for SPI transaction
```

```
        ;Write 55h to MCP23S17 register GPIOA

        MOV     DX, 1DBh
        MOV     AL, 55h         ;SPIDATA1: data to write
        OUT     DX, AL
        MOV     DX, 1DCh
        MOV     AL, 14h         ;SPIDATA2: MCP23S17 register address 00h
        OUT     DX, AL
        MOV     DX, 1DDh
        MOV     AL, 40h         ;SPIDATA3: MCP23S17 write command
        OUT     DX, AL
        CALL    BUSY            ;Poll busy flag to wait for SPI transaction

BUSY:   MOV     DX, 1D9h
        IN      AL, DX          ;Get SPISTATUS
        AND     AL, 01h         ;Isolate the BUSY flag
        JNZ     BUSY            ;Loop if SPI transaction not complete
```

SPX™ Expansion Bus

Up to four serial peripheral expansion (SPX) devices can be attached to the EBX-11 at connector J17 using the CBR-1401 or CBR-1402 cable. The SPX interface provides the standard SPI signals: SCLK, MISO, and MOSI, as well as four chip selects, SS0# to SS3#, and an interrupt input, SINT#.

Table 29: SPI Expansion Bus Connections

J17 Pin	Signal Name	Function
1	V5_0	+5.0V
2	SCLK	Serial Clock
3	GND	Ground
4	MISO	Serial Data In
5	GND	Ground
6	MOSI	Serial Data Out
7	GND	Ground
8	SS0#	Chip Select 0
9	SS1#	Chip Select 1
10	SS2#	Chip Select 2
11	SS3#	Chip Select 3
12	GND	Ground
13	SINT#	Interrupt Input
14	V5_0	+5.0V

VERSALOGIC SPX EXPANSION MODULES

VersaLogic offers a number of SPX modules that provide a variety of standard functions, such as analog input, digital I/O, CANbus controller, and others. These are small boards (1.2" x 3.775") that can mount on the PC/104 and PC/104-*Plus* stack, using standard PC/104 stand-offs, or up to two feet away from the base board. For more information, contact VersaLogic at info@VersaLogic.com.

Pulse Width Modulation Outputs and Tachometer Inputs

The EBX-11 incorporates three pulse width modulation (PWM) outputs and three tachometer (TACH) inputs which can be used, in a limited fashion, as general purpose frequency generators and counter/timers.

The PWM output frequency options are: 11.0 Hz, 14.6 Hz, 21.9 Hz, 29.3 Hz, 35.2 Hz, 44.0 Hz, 58.6 Hz, 87.7 Hz, 15 kHz, 20 kHz, 25 kHz, and 30 kHz. The PWM duty cycle is user definable from 0% (1/256) to 100% (255/256) and also invertible.

The SCH3114 Super I/O chip includes a fan speed monitoring feature, which uses TACH inputs. When the TACHs are set to manual mode, the inputs can be used as counter/timers instead of for fan speed monitoring. By default, the 16-bit tachometer registers hold the number of 90 kHz pulses that occur within five tachometer input edge-transitions (e.g., two TACH pulses).

In manual mode, the tachometer circuit begins monitoring the TACH inputs on the 1st edge detected and continues counting until the last edge is detected. If the counter overflows before the number of edges is detected, it sets the count to FFFFh. If no edges are detected, a "stalled-fan event" occurs and the counter is set to FFFFh.

Refer to the [SMSC SCH3114 Super I/O datasheet](#) for more information and detailed register descriptions.

EXTERNAL CONNECTIONS

Table 30: PWM and TACH Connections – Rev. 5.00 and Later Boards*

J5 Pin	Signal	CBR-4004 Connector	CBR-4004 Pin (Signal)
1	TACH_IN 1	**J1**	5 (IO1)
2	TACH_IN 2	**TACH**	4 (IO2)
3	TACH_IN 3		3 (IO3)
4	NC		2 (IO4)
5	GND		1 (GND1)
6	PWM_OUT 1	**J2**	5 (IO5)
7	PWM_OUT 2	**PWM**	4 (IO6)
8	PWM_OUT 3		3 (IO7)
9	NC		2 (IO8)
10	GND		1 (GND1)

*See Table 6 for the pinout of Rev. 4.xx and earlier boards.

PWM OUTPUT AND TACH INPUT CODE EXAMPLE

The following code provides guidelines for using PWM outputs and tachometer inputs as general purpose timers. Some steps are designated as required, but all steps are recommended.

```
;Controlling PWM outputs manually

;Pause the SCH3114 Hardware Monitor (optional)
MOV     DX, C70h     ;Hardware Monitor index port
MOV     AL, 40h      ;Ready,Lock,Start Register
OUT     DX, AL
MOV     DX, C71h     ;Hardware Monitor data port
IN      AL, DX       ;Read Current Value
AND     AL, FEh      ;Disable Start bit
OUT     DX, AL
```

```
        ;Set PWMs to manual mode (required)
        ;       PWM 1 Configuration Register = 5Ch
        ;       PWM 2 Configuration Register = 5Dh
        ;       PWM 3 Configuration Register = 5Eh
        ;
        MOV     DX, C70h
        MOV     AL, 5Ch      ;PWM 1 Configuration Register
        OUT     DX, AL
        MOV     DX, C71h
        IN      AL, DX       ;Read Current Value
        OR      AL, E0h      ;Set Manual Mode
        OUT     DX, AL

        ;Set Zone X Low Temp Limits to valid values (Required)
        ;All three must be set even if only one PWM is used...
        MOV     DX, C70h
        MOV     AL, 67h      ;Zone 1 Low Temp Limit Register
        OUT     DX, AL
        MOV     DX, C71h
        MOV     AL, 81h      ;any value other than default of 80h
        OUT     DX, AL

        MOV     DX, C70h
        MOV     AL, 68h      ;Zone 2 Low Temp Limit Register
        OUT     DX, AL
        MOV     DX, C71h
        MOV     AL, 81h      ;Any value other than default of 80h
        OUT     DX, AL

        MOV     DX, C70h
        MOV     AL, 69h      ;Zone 3 Low Temp Limit Register
        OUT     DX, AL
        MOV     DX, C71h
        MOV     AL, 81h      ;Any value other than default of 80h
        OUT     DX, AL

        ;Set PWM current duty cycle (optional)
        ;       PWM 1 Current Duty Cycle Register = 30h
        ;       PWM 2 Current Duty Cycle Register = 31h
        ;       PWM 3 Current Duty Cycle Register = 32h
        ;
        MOV     DX, C70h
        MOV     AL, 30h      ;PWM 1 Current Duty Cycle Register
        OUT     DX, AL
        MOV     DX, C71h
        MOV     AL, 80h      ;50% Duty Cycle, 40h = 25%, etc.
        OUT     DX, AL

        ;Set PWM Frequency (optional)
        ;       Zone 1 Range/PWM 1 Frequency Register = 5Fh
        ;       Zone 2 Range/PWM 2 Frequency Register = 60h
        ;       Zone 3 Range/PWM 3 Frequency Register = 61h
        ;
        ;       Frequency = low nibble
        ;       X0 = 11.0 Hz        X6 = 58.6Hz
        ;       X1 = 14.6Hz         X7 = 87.7Hz
        ;       X2 = 21.9Hz         X8 = 15 KHz
        ;       X3 = 29.3Hz         X9 = 20 KHz
        ;       X4 = 35.2Hz         XA = 30 KHz
        ;       X5 = 44.0Hz         XB = 25 KHz (default)
        ;
        MOV     DX, C70h
```

```
        MOV     AL, 5Fh       ;Zone 1 Range/PWM 1 Frequency
        OUT     DX, AL
        MOV     DX, C71h
        IN      AL, DX        ;Read Current Value
        AND     AL, F1h       ;Set to 14.6 Hz
        OUT     DX, AL

;Re-start the SCH3114 Hardware Monitor (required)
        MOV     DX, C70h      ;Hardware Monitor index port
        MOV     AL, 40h       ;Ready,Lock,Start Register
        OUT     DX, AL
        MOV     DX, C71h      ;Hardware Monitor data port
        IN      AL, DX        ;Read Current Value
        OR      AL, 1h        ;Enable Start bit
        OUT     DX, AL

;Reading FanTachs

;Read FanTach LSB first then read the latched MSB
;       fantach 1 LSB = 28h
;       fantach 1 MSB = 29h
;       fantach 2 LSB = 2Ah
;       fantach 2 MSB = 2Bh
;       fantach 3 LSB = 2Ch
;       fantach 3 MSB = 2Dh
;
        MOV     DX, C70h
        MOV     AL, 28h       ;FanTach 1 LSB
        OUT     DX, AL
        MOV     DX, C71h
        IN      BL, DX
        MOV     DX, C70h
        MOV     AL, 29h       ;FanTach 1 MSB
        IN      BH, DX

;BX now contains 16-bit number of 90KHz pulses that
;were counted within 5 edges (2 pulses) of the tach input.
;Input Frequency f = 1 / (BX * 11.11uS / 2), RPMs = f * 60
```

PC/104 Expansion Bus

EBX-11 has limited support of the PC/104 bus. Most PC/104 cards will work, but be sure to check the requirements of your PC/104 card against the list below.

PC/104 I/O SUPPORT

The ISA I/O ranges listed below are supported. The I/O ranges allocated to COM ports 1-4 are available to ISA when the on-board COM port function is disabled in CMOS Setup.

- 100h – 1CFh
  1DFh – 1EFh
  200h – 36Fh
  3E8h – 3EFh
  3F8h – 47Fh
  490h – 4CFh
  4D2h – AFFh

- When on-board COM ports are disabled in CMOS Setup: COM1 (0x3F8-0x3FF), COM2 (0x2F8-0x2FF), COM3 (0x3E8-0x3EF), COM4 (0x2E8-0x2EF).

PC/104 MEMORY SUPPORT

Memory ranges supported:

- D0000h-DBFFFh, 8-bit transfers only

IRQ SUPPORT

The following IRQs are available on the PC/104 bus:

- IRQ 3, IRQ 4, IRQ5, and IRQ 10

Each of the four IRQs must be enabled in CMOS Setup before they can be used on the ISA bus. Because ISA IRQ sharing is not supported, make sure that any IRQ channel used for an ISA device is not used elsewhere. For example, if ISA IRQ 4 is enabled, you must use a different IRQ for COM1.

DMA SUPPORT

The current revision of the board does not support PC/104 DMA.

6

System Resources and Maps

Memory Map

The lower 1 MB memory map of the EBX-11 is arranged as shown in the following table.

Various blocks of memory space between C0000h and FFFFFh can be shadowed. CMOS Setup is used to enable or disable this feature.

Table 31: Memory Map

Start Address	End Address	Comment
E0000h	FFFFFh	System BIOS
DC000h	DFFFFh	Reserved
D0000h	DBFFFh	PC/104
C0000h	CFFFFh	Video BIOS
A0000h	BFFFFh	Video RAM
00000h	9FFFFh	System RAM

I/O Map

The following table lists the common I/O devices in the EBX-11 I/O map. User I/O devices should be added using care to avoid the devices already in the map as shown in the following table.

Table 32: I/O Map

I/O Device	Standard I/O Addresses
Special Control Register	1D0h
Product ID and Revision Register	1D1h
Jumper and Status Register	1D2h
Reserved	1D3h – 1D7h
SPI Control and Data Registers	1D8h – 1DDh
COM/ISA IRQ Routing	1DEh
Primary Hard Drive Controller	1F0h – 1F7h
COM4 Serial Port	2E8h – 2EFh
LPT1 Parallel Port	378h – 37Fh
COM3 Serial Port	3E8h – 3EFh
COM2 Serial Port	2F8h – 2FFh
COM1 Serial Port	3F8h – 3FFh

Note   The I/O ports occupied by on-board devices are freed up when the device is disabled in the CMOS setup. This does not apply to SPI and Reserved registers.

Interrupt Configuration

The EBX-11 has the standard complement of PC type interrupts. Four non-shared interrupts are routed to the PC/104 bus, and up to four IRQ lines can be allocated as needed to PCI devices.

There are no interrupt configuration jumpers. All configuration is handled through CMOS Setup. The switches in Figure 11 indicate the various CMOS Setup options. Closed switches show factory default settings.

If your design needs to use interrupt lines on the PC/104 bus, IRQ10 is recommended. (IRQ3 and IRQ4 are normally used by COM ports on the main board.)
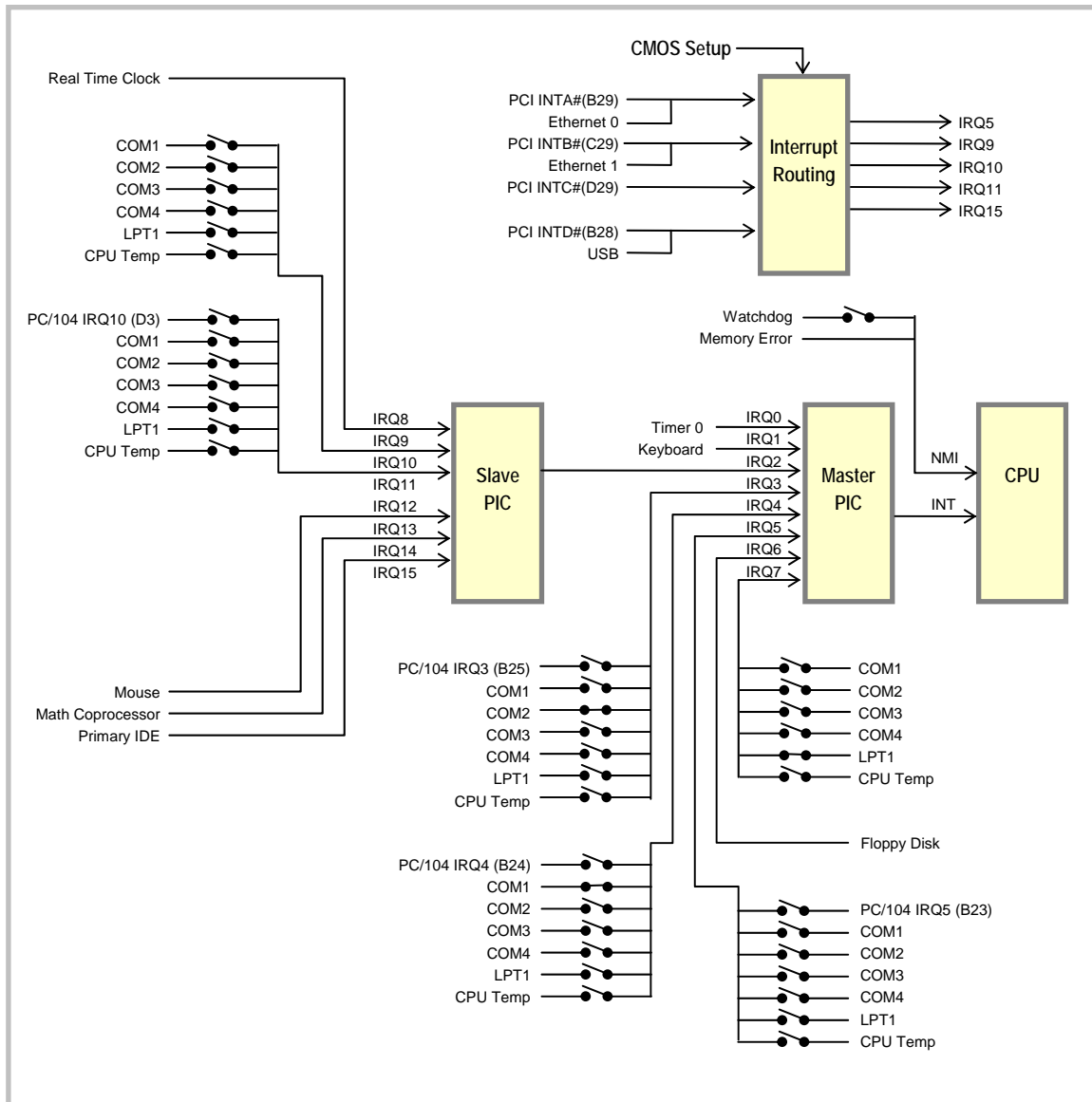
Figure 13. Interrupt Circuit Diagram

Special Registers 7

Special Control Register

SCR (READ/WRITE) 1D0h

D7	D6	D5	D4	D3	D2	D1	D0
PLED	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 33: Special Control Register Bit Assignments

Bit	Mnemonic	Description
D7	PLED	**Light Emitting Diode** — Controls the programmable LED on connector J4. 0 = Turns LED off 1 = Turns LED on
D6-D0	–	**Reserved** – These bits have no function.

Revision Indicator Register

REVIND (READ ONLY) 1D1h

D7	D6	D5	D4	D3	D2	D1	D0
PC4	PC3	PC2	PC1	PC0	REV2	REV1	REV0

This register is used to indicate the revision level of the EBX-11.

Table 34: Revision Indicator Register Bit Assignment

Bit	Mnemonic	Description
D7-D3	PC4-PC0	**Product Code** — These bits are hard-coded to represent the product type. The EBX-11 always reads as 00101. Other codes are reserved for future products. PC4　PC3　PC2　PC1　PC0　　　Product Code 　0　　　0　　　1　　　0　　　1　　　　EBX-11 *Note: These bits are read-only.*
D2-D0	REV1-REV0	**Revision Level** — These bits represent the EBX-11 circuit revision level. REV2　REV1　REV0　　Revision Level 　0　　　0　　　0　　　Rev. 1.xx through 3.xx 　0　　　0　　　1　　　Rev. 4.xx and 5.00 　0　　　1　　　0　　　EBX-11g, h Rev. 5.01 　0　　　1　　　1　　　EBX-11g, h PLD download only 　1　　　0　　　0　　　EBX-11g, h Rev. 6.xx *Note: These bits are read-only.*

Jumper and Status Register

JSR (READ/WRITE) 1D2h (or 1E2h via the CMOS setup)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	GPI	VB_SEL	BRM_SEL	Reserved	Reserved	Reserved	Reserved

Table 35: Jumper and Status Register Bit Assignments

Bit	Mnemonic	Description
D7	–	**Reserved** — This bit has no function.
D6	GPI	**General Purpose Input** — Indicates the status of V2[3-4]. 0 = Jumper out 1 = Jumper in *Note: This bit is read-only.*
D5	VB_SEL	**Video BIOS Selection –** Indicates the status of jumper V2[5-6] 0 = Jumper out, Secondary Video BIOS selected 1 = Jumper in, Primary Video BIOS selected *Note: This bit is read-only.*
D4	BRM_SEL	**BIOS Recovery Mode –** Indicates the status of jumper V2[7-8] 0 = Jumper out, BIOS recovery Mode selected 1 = Jumper in, Runtime System BIOS selected *Note: This bit is read-only. Consult factory for use of this function*
D3-D0	–	**Reserved** — These bits have no function.

Appendix A – References

A

PC Chipset *LX 800 Chipset*	Advanced Micro Devices (http://amd.com/us-en/)
Ethernet Controller *Intel 82551ER*	Intel Corporation (http://developer.intel.com/sites/developer)
PC/104 Specification *PC/104 Resource Guide*	PC/104 Consortium (www.controlled.com/pc104)
PC/104-*Plus* Specification *PC/104 Resource Guide*	VersaLogic Corporation (www.versalogic.com)
General PC Documentation *The Programmer's PC Sourcebook*	Microsoft Press (www.microsoft.com/learning/books)
General PC Documentation *The Undocumented PC*	Powell's Books (www.powells.com)

Appendix B – Legacy SPI Interface

B

Improvements to the SPI interface were incorporated into the EBX-11 Revision 6.00 and later boards. The SPI registers and functions of the SPI controller were redesigned for better performance and ease of use. This appendix contains the SPI registers for the EBX-11 Revision 5.xx and earlier boards. See SPI Control Registers and SPI Data Registers for a description of Rev. 6.xx registers.

SPICON1 (READ/WRITE) 1D8h

D7	D6	D5	D4	D3	D2	D1	D0
INT0	BUSY	CP	CLK1	CLK0	CS2	CS1	CS0

Table 36: SPI Control Register 1 Bit Assignments

Bit	Mnemonic	Description
D7	INT0	**SPI Interrupt on Completion Enable –** Setting this bit enables the SPI controller to generate an interrupt on completion of every SPI transaction. 0 = SPI interrupts disabled 1 = SPI interrupts enabled This IRQ is shared among all SPI devices on-board and connected to the EBX-11.
D6	BUSY	**SPI Busy Flag –** Set by hardware on the start of every SPI bus transaction and cleared upon completion of a new transaction. 0 = Transaction complete 1 = Transaction in progress ***Note:*** *This bit is read-only.*
D5	CP	**SPI Master Clock Polarity –** CP along with CI in SPICON2 combine to set the SCLK behavior. **CI CP SCLK** 1 0 Idle low, rising edge active 1 1 Idle low, falling edge active 0 1 Idle high, rising edge active 0 0 Idle high, falling edge active
D4-D3	CLK1-CLK0	**SPI Master Clock Frequency –** These bits set the SPI Master clock frequency. **CLK1 CLK0 Frequency** 0 0 1MHz 1 0 2MHz 0 1 4MHz 1 1 8MHz
D2-D0	CS2-CS0	**SPI Master Chip Select –** These bits select which of the EBX-11's seven chip selects will be asserted during an SPI transaction. **CS2 CS1 CS0 Chip Select** 0 0 0 None, port disabled 0 0 1 External Chip Select 0 0 1 0 External Chip Select 1 0 1 1 External Chip Select 2 1 0 0 External Chip Select 3 1 0 1 On-Board A/D Converter Chip Select 1 1 0 On-Board Digital I/O Chip Select Chan 0-15 1 1 1 On-Board Digital I/O Chip Select Chan 16-31

SPICON2 (READ/WRITE) 1D9h

D15	D14	D13	D12	D11	D10	D9	D8
INT1	Reserved	SPISET1	SPISET0	Reserved	DONE	CI	Reserved

Table 37: SPI Control Register 2 Bit assignments

Bit	Mnemonic	Description
D15	INT1	**SPI Hardware Interrupt Enable –** Setting this bit enables SPI devices with a hardware interrupt feature to generate an interrupt request. 0 = SPI device interrupts disabled 1 = SPI device interrupts enabled This IRQ is shared among all SPI devices on-board and connected to the EBX-11.
D14	–	**Reserved** – This bit is unused and read as 1.
D13-D12	SPISET	**SPI Frame Length Control –** These bits set the SPI cycle frame length. SPISET1 SPISET0 **Frame Length** 0 0 8 Bit 0 1 16 Bit 1 0 Invalid 1 1 24 Bit
D11	–	**Reserved** – This bit is unused and read as 1.
D10	DONE	**SPI Cycle Complete Flag –** Set by hardware on completion of every SPI bus transaction. Cleared by writing a 0 to this bit or by hardware on initiation of a new SPI transaction.
D9	CI	**SPI Clock Idle –** CI along with CP in SPICON1 combine to set the SCLK behavior. **CI CP SCLK** 1 0 Idle low, rising edge active 1 1 Idle low, falling edge active 0 1 Idle high, rising edge active 0 0 Idle high, falling edge active
D8	–	**Reserved** – This bit is unused and read as 1.

SPIDATA1 (READ/WRITE) 1DAh

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

SPIDATA2 (READ/WRITE) 1DBh

D15	D14	D13	D12	D11	D10	D9	D8
D15	D14	D13	D12	D11	D10	D9	D8

SPIDATA3 (READ/WRITE) 1DCh

D23	D22	D21	D20	D19	D18	D17	D16
D23	D22	D21	D20	D19	D18	D17	D16

Note   Writing any value to SPIDATA3 will initiate an SPI transaction based on current SPICON1 and SPICON2 settings.

SPICON3 (WRITE ONLY) 1DDh

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	SPIINT3	SPIINT2	SPIINT1	SPIINT0

Table 38: SPI Control Register 3 Bit Assignments

Bit	Mnemonic	Description
D7-D4	–	**Reserved** – These bits are unused and read as 1.
D3-D0	SPIINT	**SPI IRQ Routing –** These bits control which IRQ the SPI interrupt is routed to. **SPIINT3 SPIINT2 SPIINT1 SPIINT0 IRQ Selection** 0 0 0 0 No IRQ 0 0 0 1 IRQ3 0 0 1 0 IRQ4 0 1 0 0 IRQ5 1 0 0 0 IRQ10