

MC74HC151A

8-Input Data Selector/Multiplexer

High-Performance Silicon-Gate CMOS

The MC74HC151 is identical in pinout to the LS151. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Strobe pin must be at a low level for the selected data to appear at the outputs. If Strobe is high, the Y output is forced to a low level and the \bar{Y} output is forced to a high level.

The HC151 is similar in function to the HC251 which has 3-state outputs.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- These are Pb-Free Devices

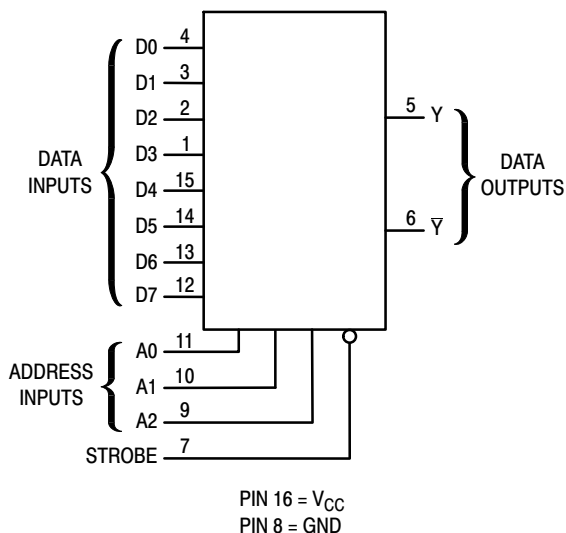
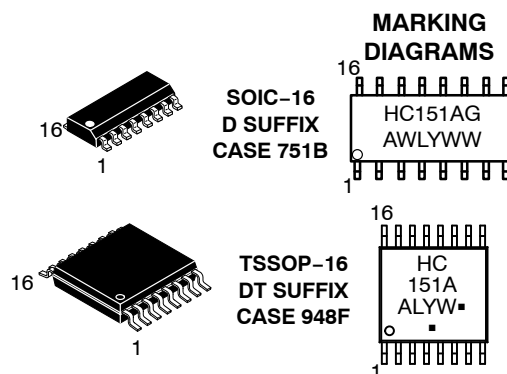


Figure 1. Logic Diagram



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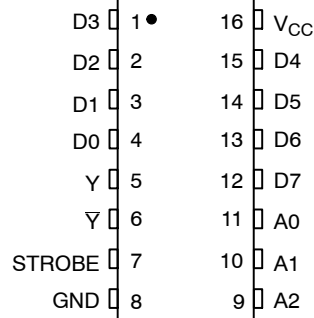
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A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



FUNCTION TABLE

| Inputs | | | | Outputs | |
|--------|----|----|--------|---------|------------|
| A2 | A1 | A0 | Strobe | Y | \bar{Y} |
| X | X | X | H | L | H |
| L | L | L | L | D0 | $\bar{D0}$ |
| L | L | H | L | D1 | $\bar{D1}$ |
| L | H | L | L | D2 | $\bar{D2}$ |
| L | H | H | L | D3 | $\bar{D3}$ |
| H | L | L | L | D4 | $\bar{D4}$ |
| H | L | H | L | D5 | $\bar{D5}$ |
| H | H | L | L | D6 | $\bar{D6}$ |
| H | H | H | L | D7 | $\bar{D7}$ |

D0, D1, ..., D7 = the level of the respective D input.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|---|------------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V_{in} | DC Input Voltage (Referenced to GND) | -1.5 to $V_{CC} + 1.5$ | V |
| V_{out} | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| I_{in} | DC Input Current, per Pin | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 50 | mA |
| P_D | Power Dissipation in Still Air SOIC Package TSSOP Package | 500 TBD | mW |
| T_{stg} | Storage Temperature | -65 to +150 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit | |
|------------------------------------|--|---|-----------------|--------------------|----|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V | |
| V _{in} , V _{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V | |
| T _A | Operating Temperature, All Package Types | −55 | +125 | °C | |
| t _r , t _f | Input Rise and Fall Time (Figure 2) | V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V | 0 0 0 | 1000 500 400 | ns |

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V_{CC} V | Guaranteed Limit | | | Unit |
|----------|--|--|-------------------|--------------------|--------------------|--------------------|---------------|
| | | | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V_{IH} | Minimum High-Level Input Voltage | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$ | 2.0 4.5 6.0 | 1.5 3.15 4.2 | 1.5 3.15 4.2 | 1.5 3.15 4.2 | V |
| V_{IL} | Maximum Low-Level Input Voltage | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$ | 2.0 4.5 6.0 | 0.3 0.9 1.2 | 0.3 0.9 1.2 | 0.3 0.9 1.2 | V |
| V_{OH} | Minimum High-Level Output Voltage | $V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$ | 2.0 4.5 6.0 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | V |
| | | $V_{in} = V_{IH}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$ | 4.5 6.0 | 3.98 5.48 | 3.84 5.34 | 3.70 5.20 | |
| V_{OL} | Maximum Low-Level Output Voltage | $V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$ | 2.0 4.5 6.0 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V |
| | | $V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$ | 4.5 6.0 | 0.26 0.26 | 0.33 0.33 | 0.40 0.40 | |
| I_{in} | Maximum Input Leakage Current | $V_{in} = V_{CC} \text{ or GND}$ | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| I_{CC} | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$ | 6.0 | 8 | 80 | 160 | μA |

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|---|----------------------|------------------|-----------------|-----------------|------|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input D to Output Y (Figures 2 and 7) | 2.0 4.5 6.0 | 170 34 29 | 215 43 37 | 255 51 43 | ns |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input D to Output \bar{Y} (Figures 4 and 7) | 2.0 4.5 6.0 | 185 37 31 | 230 46 39 | 280 56 48 | ns |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input D to Output Y (Figures 3 and 7) | 2.0 4.5 6.0 | 185 37 31 | 230 46 39 | 280 56 48 | ns |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A to Output \bar{Y} (Figures 3 and 7) | 2.0 4.5 6.0 | 205 41 35 | 255 51 43 | 310 62 53 | ns |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input D to Output Y (Figures 5 and 7) | 2.0 4.5 6.0 | 125 25 21 | 155 31 26 | 190 38 32 | ns |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Strobe to Output \bar{Y} (Figures 6 and 7) | 2.0 4.5 6.0 | 125 25 21 | 155 31 26 | 190 38 32 | ns |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 2, 4 and 7) | 2.0 4.5 6.0 | 75 15 13 | 95 19 16 | 110 22 19 | ns |
| C _{in} | Maximum Input Capacitance | – | 10 | 10 | 10 | pF |

| | | | |
|-----------------|---|---|----|
| C _{PD} | Power Dissipation Capacitance (Per Package) | Typical @ 25°C, V _{CC} = 5.0 V | pF |
| | | 36 | |

PIN DESCRIPTIONS

INPUTS

D0, D1, ... , D7 (Pins 4, 3, 2, 1, 15, 14, 13, 12)

Data inputs. Data on any one of these eight binary inputs may be selected to appear on the output.

CONTROL INPUTS

A0, A1, A2 (Pins 11, 10, 9)

Address inputs. The data on these pins are the binary address of the selected input (see the Function Table).

Strobe (Pin 7)

Strobe. This input pin must be at a low level for the selected data to appear at the outputs. If the Strobe pin is high, the Y output is forced to a low level and the \bar{Y} output is forced to a high level.

OUTPUTS

Y, \bar{Y} (Pins 5, 6)

Data outputs. The selected data is presented at these pins in both true (Y output) and complemented (\bar{Y} output) forms.

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SWITCHING WAVEFORMS

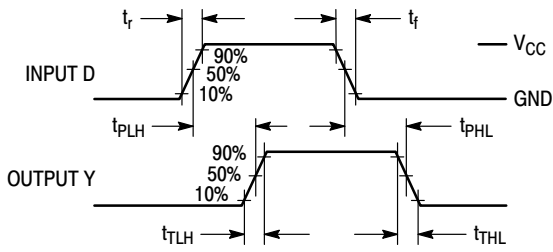


Figure 2.

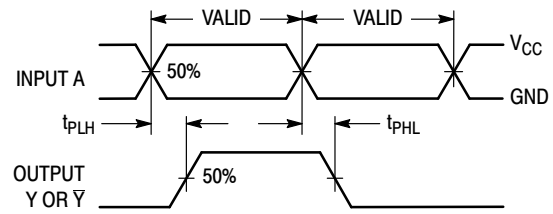


Figure 3.

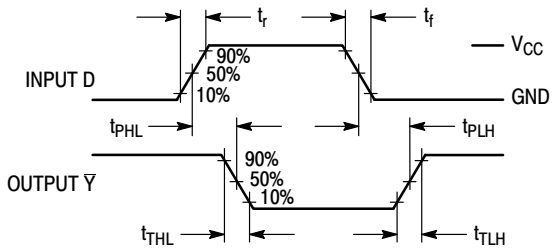


Figure 4.

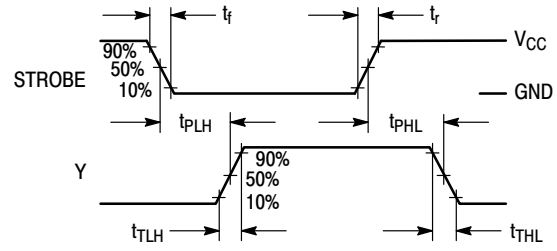


Figure 5.

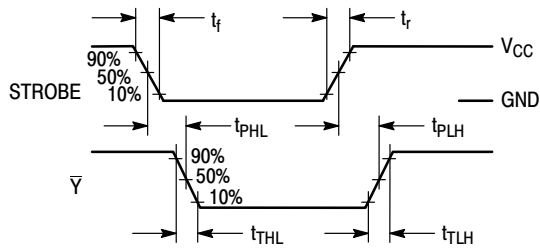
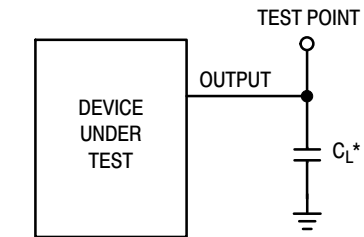


Figure 6.



*Includes all probe and jig capacitance

Figure 7. Test Circuit

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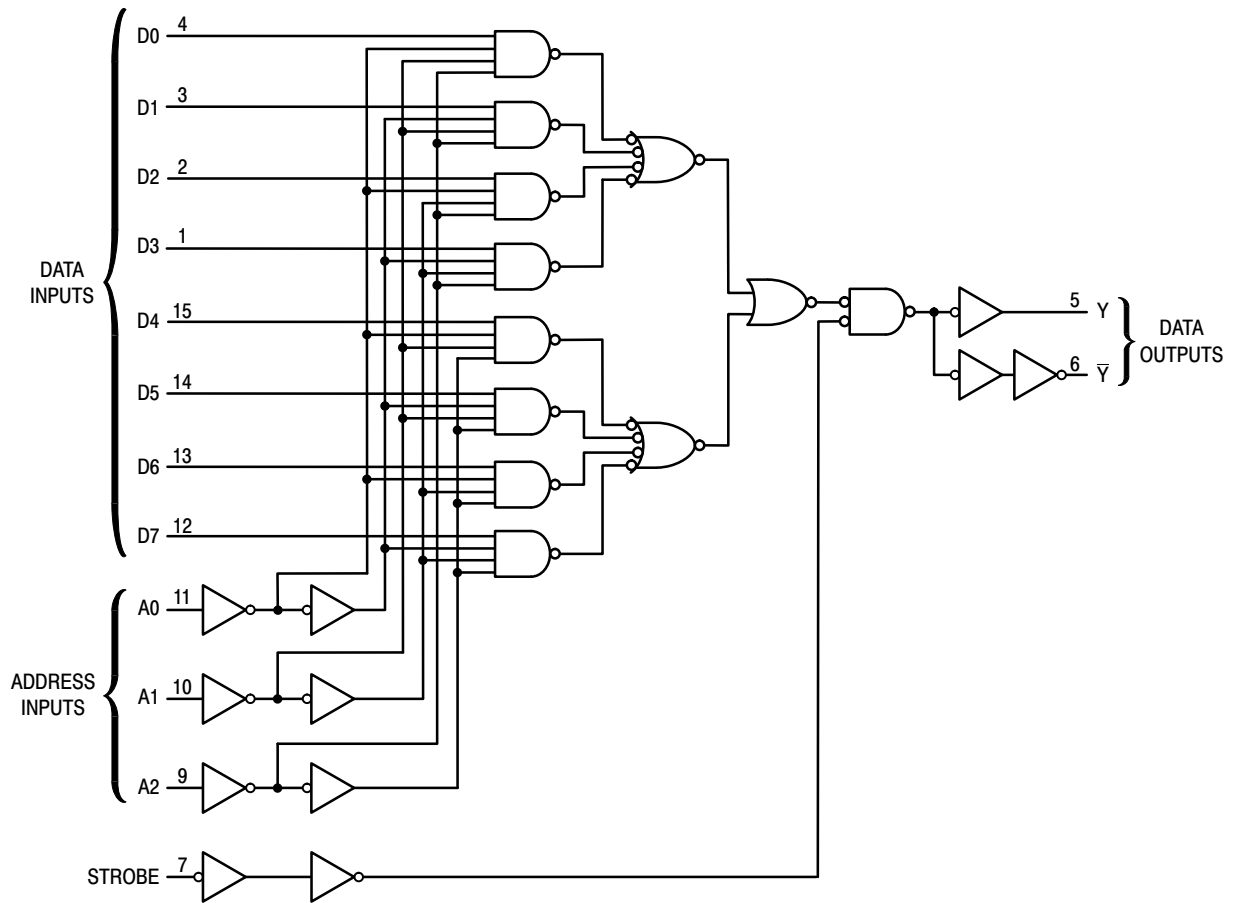


Figure 8. Expanded Logic Diagram

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------|----------------------|------------------|
| MC74HC151ADG | SOIC–16 (Pb–Free) | 48 Units / Rail |
| MC74HC151ADR2G | SOIC–16 (Pb–Free) | 2500 Tape & Reel |
| MC74HC151ADTR2G | TSSOP–16* | 2500 Tape & Reel |
| MC74HC151ADTG | TSSOP–16* | 96 Units / Tube |

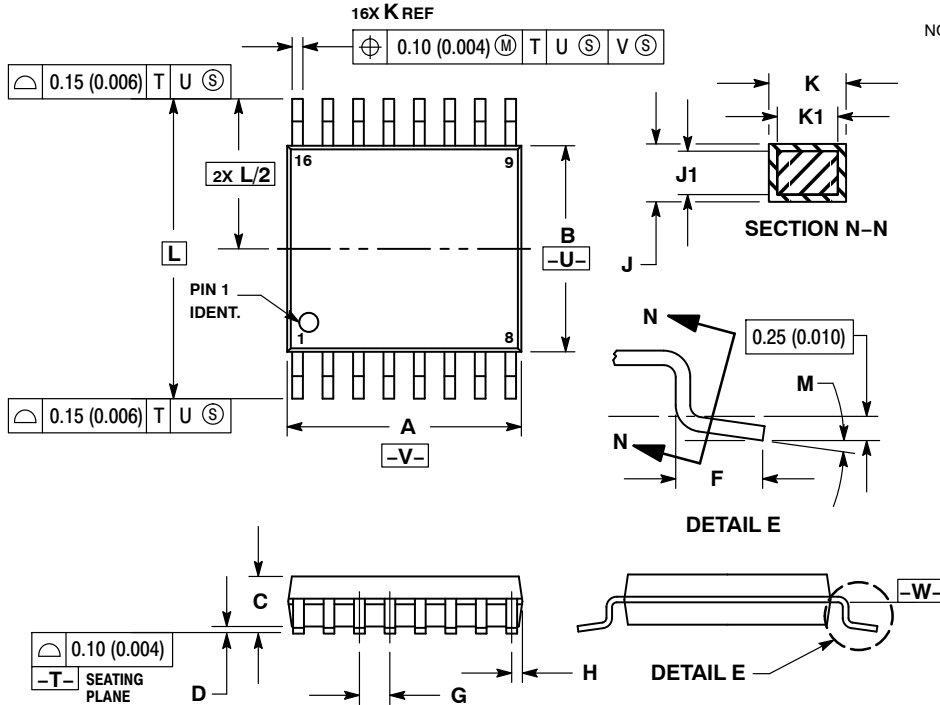
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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PACKAGE DIMENSIONS

TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE B

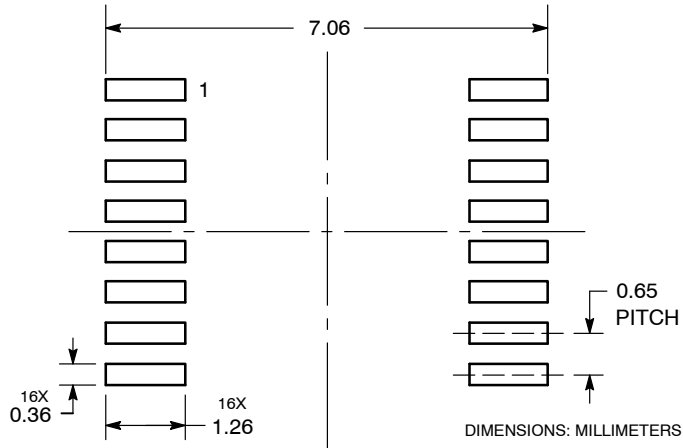


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT*

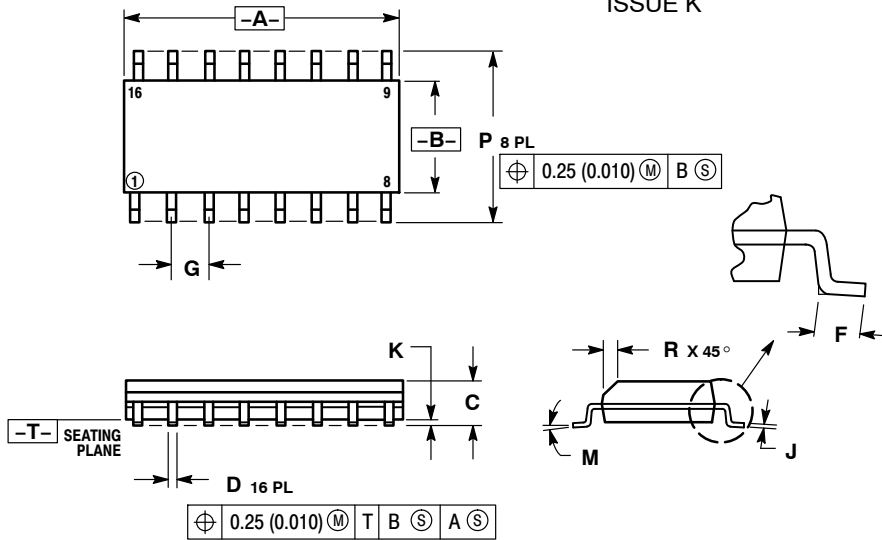


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

SOIC-16
CASE 751B-05
ISSUE K

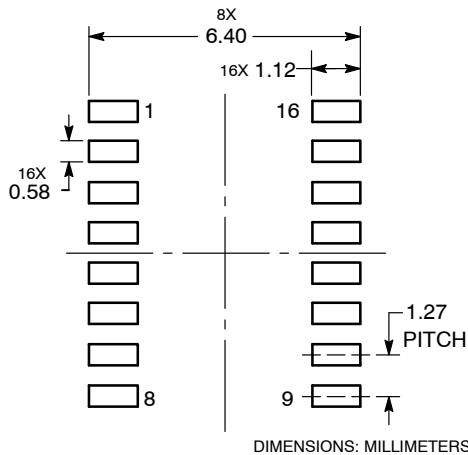


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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