M58BW16F, M58BW32F

16Mb or 32Mb (x32, Boot Block, Burst) 3.3V Supply Flash Memory

Features

- Supply voltage
  - V_{DD} = 2.7–3.6V (45ns) or V_{DD} = 2.5–3.3V (55ns)
  - V_{DDQ} = V_{DDQIN} = 2.4V to VDD for I/O buffers
- High performance
  - Access times: 45 and 55ns
  - Synchronous burst reads
  - 75 MHz effective zero wait-state burst read
  - Asynchronous page reads (4 double words)
- M58BW32F memory organization:
  - Eight 64 Kbit small parameter blocks
  - Four 128 Kbit large parameter blocks
  - Sixty-two 512 Kbit main blocks
- M58BW16F memory organization:
  - Eight 64 Kbit parameter blocks
  - Thirty-one 512 Kbit main blocks
- Hardware block protection
  - WP# pin to protect any block combination from Program and Erase operations
  - PEN signal for Program/Erase Enable
- Irreversible modify protection (OTP like) on 128 Kbits:
  - Block 1 (bottom device) or block 72 (top device) in the M58BW32F
  - Blocks 2 and 3 (bottom device) or blocks 36 and 35 (top device) in the M58BW16F
- Security
  - 64-bit unique device identifier (UID)
- Fast programming
  - Write to buffer and program capability (8 double words)
- Optimized for FDI drivers
  - Common flash interface (CFI)
  - Fast Program/Erase Suspend feature in each block
- Low power consumption
  - 100µA typical Standby current
- Electronic signature
- Manufacturer code: 0020h
  - Top device codes: M58BW32FT: 8838h
    M58BW16FT: 883Ah
  - Bottom device codes: M58BW32FB: 8837h
    M58BW16FB: 8839h
- Automotive device grade 3:
  - Temperature: –40 to 125 °C
- Automotive grade certified

Part Numbering Information

Devices are shipped from the factory with memory content bits erased to 1. For available options, such as packages or speed, or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Table 1: Part Number Information Scheme

Part Number Category	Category Details
Device type	M58 = Parallel Flash memory
Architecture	B = Burst mode
Operating voltage	W = [2.7 V to 3.6 V] V_{DD} range for 45 ns speed class [2.5 V to 3.3 V] V_{DD} range for 55 ns speed class [2.4 V to V_{DD}] V_{DDQ} range for 45 ns and 55 ns speed classes
Device function/density	32F = 32 Mbit (x 32), boot block, burst, 0.11 µm technology
	16F = 16 Mbit (x 32), boot block, burst, 0.11 µm technology
Array matrix	T = Top boot B = Bottom boot
Speed	4 = 45 ns 5 = 55 ns
Package	T = PQFP80
	ZA = LBGA80, 1.0 mm pitch
Temperature range	3 = Automotive grade certified[1] , –40 to 125 °C
Packing Option	Blank = Standard packing
	T = Tape and reel packing
	F = ECOPACK® package, tape & reel 24 mm packing

Note: 1. Qualified & characterized according to AEC Q100 & Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

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Description

The M58BW16F and M58BW32F are 16 and 32Mbit non-volatile Flash memories, respectively. They can be erased electrically at block level and programmed in-system on a double-word basis using a 2.7–3.6V or 2.5–3.3V V_{DD} supply for the circuit and a VDDQ supply voltage (2.4V to VDD) for the input and output buffers.

In the rest of the document the M58BW16F and M58BW32F will be referred to as M58BWxxF unless otherwise specified.

The devices support asynchronous (latch controlled READ and page READ) and synchronous bus operations. The synchronous burst read interface allows a high data transfer rate controlled by the burst clock signal, K. It is capable of bursting fixed or unlimited lengths of data. The burst type, latency and length are configurable and can be easily adapted to a large variety of system clock frequencies and microprocessors. All write operations are asynchronous. On power-up the memory defaults to read mode with an asynchronous bus.

The device features an asymmetrical block architecture:

- The M58BW32F has an array of 62 main blocks of 512Kb each, plus 4 large parameter blocks of 128Kb each and 8 small parameter blocks of 64Kb each. The large and small parameter blocks are located either at the top (M58BW32FT) or at the bottom (M58BW32FB) of the address space. The first large parameter block is referred to as boot block and can be used either to store a boot code or parameters. The memory array organization is detailed in the M58BW32F top boot block addresses table and the M58BW32F bottom boot block addresses table.
- The M58BW16F has an array of 8 parameter blocks of 64Kb each and 31 main blocks of 512Kb each. In the M58BW16FT the parameter blocks are located at the top of the address space whereas in the M58BW16FB, they are located at the bottom. The memory array organization is detailed in the M58BW16F top boot block addresses table and the M58BW16F bottom boot block addresses table.

PROGRAM and ERASE commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a PROGRAM or ERASE operation can be detected and any error conditions identified in the status register. The command set required to control the memory is consistent with JEDEC standards.

An ERASE operation can be suspended in order to perform either READ or PROGRAM in any other block, and then resumed. The PROGRAM operation can be suspended to read data in any other block, and then resumed. Each block can be programmed and erased over 100,000 cycles.

All blocks are protected during power-up. The M58BWxxF features the following levels of hardware and software block protection to avoid unwanted Program/Erase operations:

- Write/protect enable input, WP#, hardware protects a combination of blocks from PROGRAM and ERASE operations. The blocks to be protected are configured individually by issuing a SET BLOCK PROTECTION CONFIGURATION REGISTER or a CLEAR BLOCK PROTECTION CONFIGURATION REGISTER command.
- All PROGRAM or ERASE operations are blocked when RP#, is held LOW.

- A program/erase enable input, PEN, is used to protect all blocks, preventing PROGRAM and ERASE operations from affecting their data.
- A permanent user-enabled protection against Modify operations is available:

  on one specific 128Kb parameter block in the M58BW32F – block 1 for bottom devices or block 72 for top devices

  on two specific 64Kb parameter blocks in the M58BW16F – blocks 2 and 3 for bottom devices or blocks 36 and 35 for top devices.

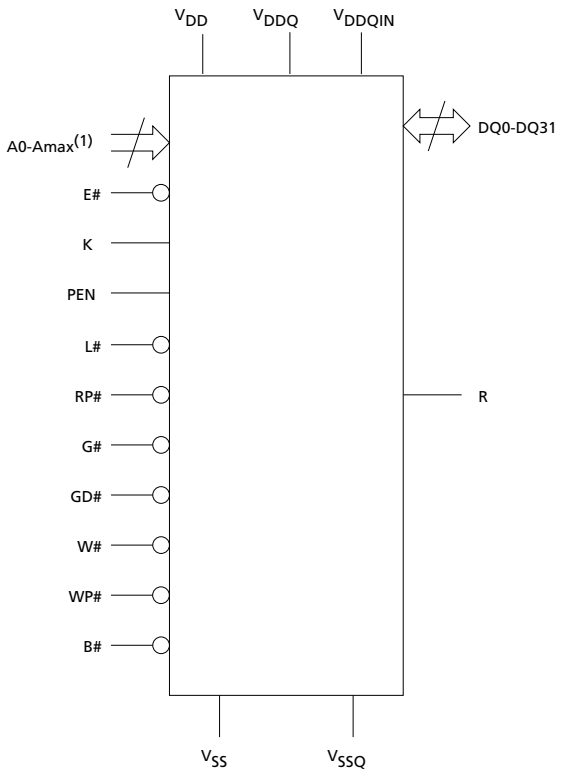
A reset/power-down mode is entered when the RP# input is LOW. In this mode the power consumption is reduced to the standby level, the device is write protected and both the status and burst configuration registers are cleared. A recovery time is required when the RP# input goes HIGH.

A manufacturer code and a device code are available. They can be read from the memory allowing programming equipment or applications to automatically match their interface to the characteristics of the memory.

Finally, the M58BWxxF features a 64-bit unique device identifier (UID) which is programmed by Micron on the production line. It is unique for each die and can be used to implement cryptographic algorithms to improve security. Information is available in the CFI area (see the M58BW16F extended query information table).

The memory is offered in PQFP80 (14 x 20mm) and LBGA80 (1.0mm pitch) packages and it is supplied with all the bits erased (set to '1').

Figure 1: Logic Diagram



Note: 1. Amax is equal to A18 in the M58BW16F, and to A19 in the M58BW32F.

Table 2: Signal Names

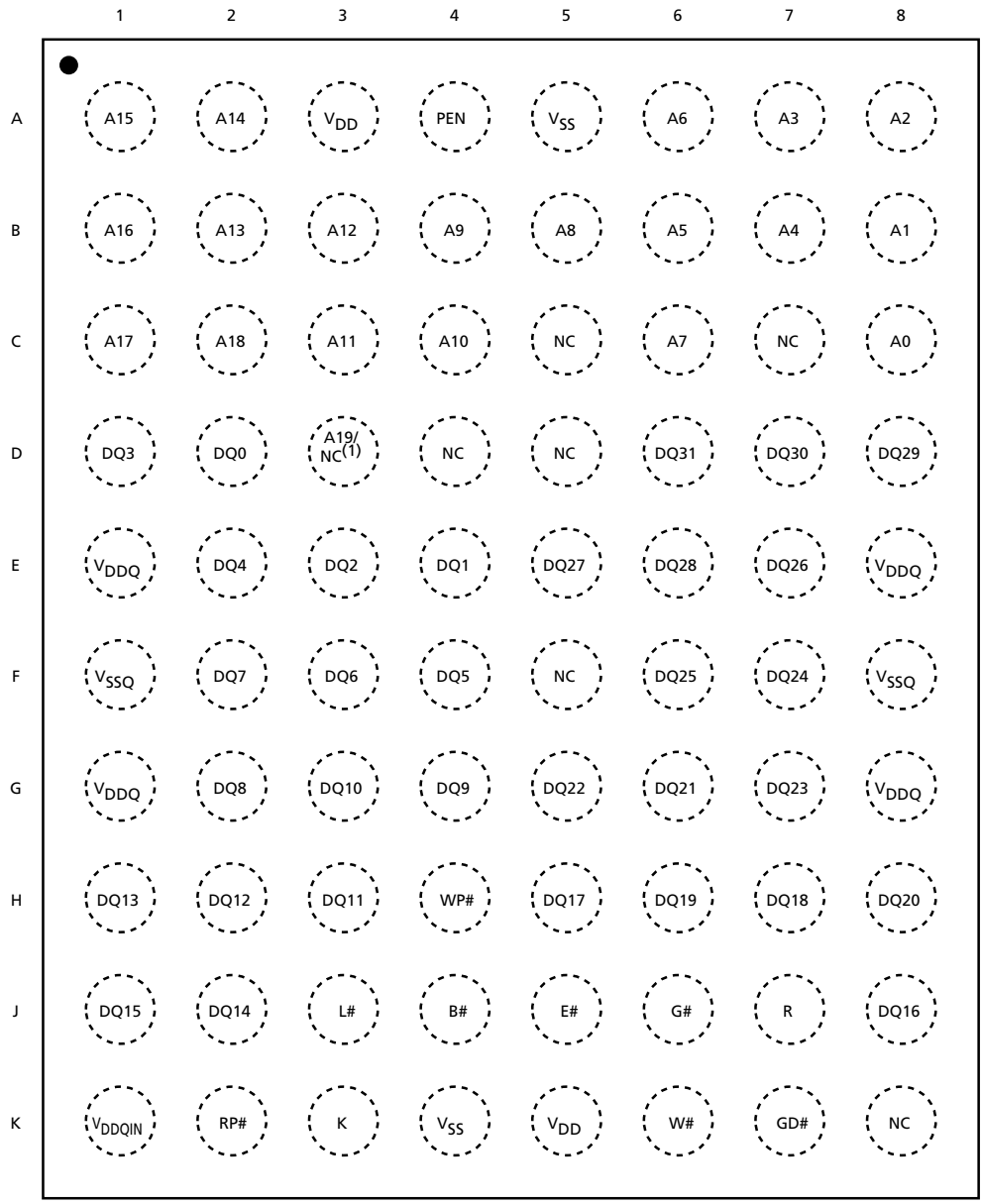
Signal name	Function	Direction
A[MAX:0][1]	Address inputs	Inputs
DQ[7:0]	Data input/output, command input	I/O
DQ[15:8]	Data input/output, Burst Configuration Register	I/O
DQ[31:16]	Data input/output	I/O
B#	Burst Address Advance	Input
E#	Chip Enable	Input
G#	Output Enable	Input
K	Burst Clock	Input
L#	Latch Enable	Input
R	Valid Data Ready	Output
RP#	Reset/Power-down	Input
W#	Write Enable	Input
GD#	Output Disable	Input

Table 2: Signal Names (Continued)

Signal name	Function	Direction
WP#	Write Protect	Input
V_{DD}	Supply voltage	
V_{DDQ}	Power supply for output buffers	
V_{DDQIN}	Power supply for input buffers only	
PEN	Program/Erase Enable	Input
V_{SS}	Ground	
V_{SSQ}	Input/output ground	
NC	Not connected internally	
DNU	Don't use as internally connected	

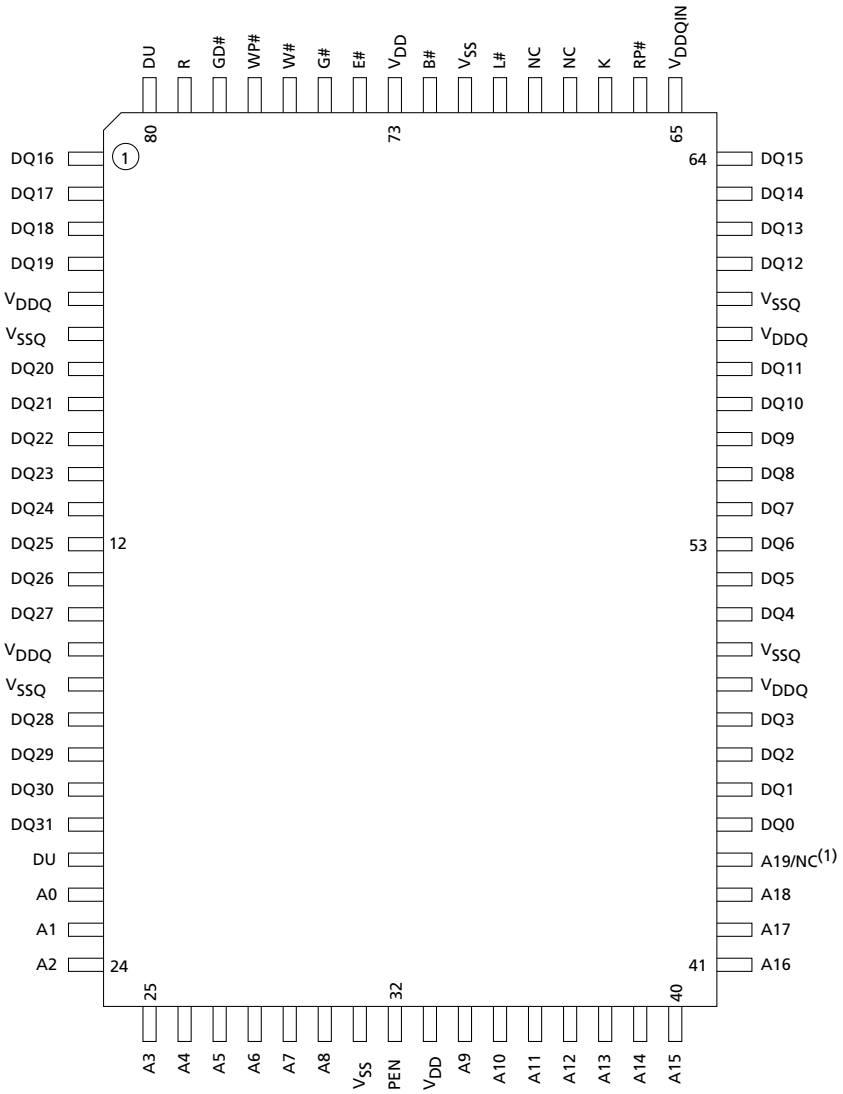
Note: 1. A[MAX] is equal to A18 in the M58BW16F, and to A19 in the M58BW32F.

Figure 2: LBGA Connections (Top View through Package)



Note: 1. Ball D3 is NC in the M58BW16F and A19 in the M58BW32F.

Figure 3: PQFP Connections (Top View through Package)



Note: 1. Pin 44 is NC in the M58BW16F and A19 in the M58BW32F.

Block Protection

The M58BWxxF features four different levels of block protection.

- **Write Protect pin,** WP#, - When WP# is Low, V_{IL}, the protection status that has been configured in the Block Protection Configuration Register is activated. The Block Protection Configuration Register is volatile. Any combination of blocks is possible. Any attempt to program or erase a protected block will return an error in the Status Register (see the Status Register bits table).

- **Reset/Power-down pin,** RP#, - If the device is held in reset mode (RP# at V_{IL}), no Program or Erase operation can be performed on any block.
- **Program/Erase Enable (PEN),-** The Program/Erase Enable input, PEN, protects all blocks by preventing Program and Erase operations from modifying the data. Prior to issuing a Program or Erase command, the Program/Erase Enable must be set to High (V_{IH}). If it is Low (V_{IL}), the Program or Erase operation is not accepted and an error is generated in the Status Register.
- **Permanent protection against modify operations** - specific OTP-like blocks can be permanently protected against modify operations (Program/Erase):

  in the M58BW32F, a unique 128-Kbit parameter block – block 1 (01000h-01FFFh) for bottom devices or block 72 (FE000h-FEFFFh) for top devices

  in the M58BW16F, two 64-Kbit parameter blocks – blocks 2 and 3 (01000h-01FFFh) for bottom devices or blocks 36 and 35 (7E000h-7EFFFh) for top devices

  This protection is user-enabled. Details of how this protection is activated are provided in a dedicated application note.

After a device reset the first two kinds of block protection (WP#, RP#) can be combined to give a flexible block protection. All blocks are protected at power-up.

OTP Protection

The OTP protection is an user-enabled feature that permanently protects specific blocks, so called OTP blocks, against modify operations (program/erase). It is available:

- On one specific 128-kbit parameter block in the M58BW32F- block 1 (01000h-01FFFh) for bottom devices or block 72 (FE000h-FEFFFh) for top devices
- On two specific 64-kbit parameter blocks in the M58BW16F- block 2 and 3 (01000h-01FFFh) for bottom devices or block 36 and 35 (7E000h-7EFFFh) for top devices.

The default state is unprotected. However, once the protection has been enabled, it is impossible to disable it and the OTP blocks will remain “modify protected” permanently.

Obviously, this information is stored in internal nonvolatile registers.

Activation Sequence

If the user wants to make the OTP protection effective on a part, he has to issue the Lock OTP protection command.

The Lock OTP protection requires 2 write cycles:

- write (ADD=000AAh, DATA=49h) - Lock OTP Protection command 1
- write (ADD=00003h, DATA=0000 0000h) - Lock OTP Protection command 2

This sequence of commands has to be given with Write Protect Enable WP_N=’1’. The user can check its execution polling on the SR in the same way as a normal Program command.

The program duration lasts about 35 µs like for a standard Program command. It is also possible to detect the end of the operation by polling the Status Register.

Any Erase attempt returns A3h in the Status Register while any Program attempt returns 93h.

Once the first write cycle of the Lock OTP protection command is issued, a wrong address on second write cycle will cause the activation sequence to fail. The Status Register allows detecting this event and its value is then B1h (invalid sequence).

As a consequence, the protection is not active and the sequence must be restarted after a Clear Status Register command.

The Lock OTP Protection command cannot be suspended.

Memory Map Addresses

Table 3: M58BW32F Top Boot Block Addresses

Block Number	Size (Kbit)	Address Range[1]
73	128	FF000h-FFFFFh
72	128	FE000h-FEFFFh[2]
71	128	FD000h-FDFFFh
70	128	FC000h-FCFFFh
69	64	FB800h-FBFFFh
68	64	FB000h-FB7FFh
67	64	FA800h-FAFFFh
66	64	FA000h-FA7FFh
65	64	F9800h-F9FFFh
64	64	F9000h-F97FFh
63	64	F8800h-F8FFFh
62	64	F8000h-F87FFh
61	512	F4000h-F7FFFh
60	512	F0000h-F3FFFh
59	512	EC000h-EFFFFh
58	512	E8000h-EBFFFh
57	512	E4000h-E7FFFh
56	512	E0000h-E3FFFh
55	512	DC000h-DFFFFh
54	512	D8000h-DBFFFh
53	512	D4000h-D7FFFh
52	512	D0000h-D3FFFh
51	512	CC000h-CFFFFh
50	512	C8000h-CBFFFh
49	512	C4000h-C7FFFh
48	512	C0000h-C3FFFh
47	512	BC000h-BFFFFh
46	512	B8000h-BBFFFh
45	512	B4000h-B7FFFh
44	512	B0000h-B3FFFh

Table 3: M58BW32F Top Boot Block Addresses (Continued)

Block Number	Size (Kbit)	Address Range[1]
43	512	AC000h-AFFFFh
42	512	A8000h-ABFFFh
41	512	A4000h-A7FFFh
40	512	A0000h-A3FFFh
39	512	9C000h-9FFFFh
38	512	98000h-9BFFFh
37	512	94000h-97FFFh
36	512	90000h-93FFFh
35	512	8C000h-8FFFFh
34	512	88000h-8BFFFh
33	512	84000h-87FFFh
32	512	80000h-83FFFh
31	512	7C000h-7FFFFh
30	512	78000h-7BFFFh
29	512	74000h-77FFFh
28	512	70000h-73FFFh
27	512	6C000h-6FFFFh
26	512	68000h-6BFFFh
25	512	64000h-67FFFh
24	512	60000h-63FFFh
23	512	5C000h-5FFFFh
22	512	58000h-5BFFFh
21	512	54000h-57FFFh
20	512	50000h-53FFFh
19	512	4C000h-4FFFFh
18	512	48000h-4BFFFh
17	512	44000h-47FFFh
16	512	40000h-43FFFh
15	512	3C000h-3FFFFh
14	512	38000h-3BFFFh
13	512	34000h-37FFFh
12	512	30000h-33FFFh
11	512	2C000h-2FFFFh
10	512	28000h-2BFFFh
9	512	24000h-27FFFh
8	512	20000h-23FFFh
7	512	1C000h-1FFFFh
6	512	18000h-1BFFFh

Table 3: M58BW32F Top Boot Block Addresses (Continued)

Block Number	Size (Kbit)	Address Range[1]
5	512	14000h-17FFFh
4	512	10000h-13FFFh
3	512	0C000h-0FFFFh
2	512	08000h-0BFFFh
1	512	04000h-07FFFh
0	512	00000h-03FFFh

Notes: 1. Addresses are indicated in 32-bit addressing.
2. OTP block.

Table 4: M58BW32F Bottom Boot Block Addresses

#	Size (Kbit)	Address Range[1]
73	512	FC000h-FFFFFh
72	512	F8000h-FBFFFh
71	512	F4000h-F7FFFh
70	512	F0000h-F3FFFh
69	512	EC000h-EFFFFh
68	512	E8000h-EBFFFh
67	512	E4000h-E7FFFh
66	512	E0000h-E3FFFh
65	512	DC000h-DFFFFh
64	512	D8000h-DBFFFh
63	512	D4000h-D7FFFh
62	512	D0000h-D3FFFh
61	512	CC000h-CFFFFh
60	512	C8000h-CBFFFh
59	512	C4000h-C7FFFh
58	512	C0000h-C3FFFh
57	512	BC000h-BFFFFh
56	512	B8000h-BBFFFh
55	512	B4000h-B7FFFh
54	512	B0000h-B3FFFh
53	512	AC000h-AFFFFh
52	512	A8000h-ABFFFh
51	512	A4000h-A7FFFh
50	512	A0000h-A3FFFh
49	512	9C000h-9FFFFh
48	512	98000h-9BFFFh
47	512	94000h-97FFFh

Table 4: M58BW32F Bottom Boot Block Addresses (Continued)

#	Size (Kbit)	Address Range[1]
46	512	90000h-93FFFh
45	512	8C000h-8FFFFh
44	512	88000h-8BFFFh
43	512	84000h-87FFFh
42	512	80000h-83FFFh
41	512	7C000h-7FFFFh
40	512	78000h-7BFFFh
39	512	74000h-77FFFh
38	512	70000h-73FFFh
37	512	6C000h-6FFFFh
36	512	68000h-6BFFFh
35	512	64000h-67FFFh
34	512	60000h-63FFFh
33	512	5C000h-5FFFFh
32	512	58000h-5BFFFh
31	512	54000h-57FFFh
30	512	50000h-53FFFh
29	512	4C000h-4FFFFh
28	512	48000h-4BFFFh
27	512	44000h-47FFFh
26	512	40000h-43FFFh
25	512	3C000h-3FFFFh
24	512	38000h-3BFFFh
23	512	34000h-37FFFh
22	512	30000h-33FFFh
21	512	2C000h-2FFFFh
20	512	28000h-2BFFFh
19	512	24000h-27FFFh
18	512	20000h-23FFFh
17	512	1C000h-1FFFFh
16	512	18000h-1BFFFh
15	512	14000h-17FFFh
14	512	10000h-13FFFh
13	512	0C000h-0FFFFh
12	512	08000h-0BFFFh
11	64	07800h-07FFFh
10	64	07000h-077FFh
9	64	06800h-06FFFh

Table 4: M58BW32F Bottom Boot Block Addresses (Continued)

#	Size (Kbit)	Address Range[1]
8	64	06000h-067FFh
7	64	05800h-05FFFh
6	64	05000h-057FFh
5	64	04800h-04FFFh
4	64	04000h-047FFh
3	128	03000h-03FFFh
2	128	02000h-02FFFh
1	128	01000h-01FFFh[2]
0	128	00000h-00FFFh

Notes: 1. Addresses are indicated in 32-bit word addressing.
2. OTP block.

Table 5: M58BW16F Top Boot Block Addresses

#	Size (Kbit)	Address Range
38	64	7F800h-7FFFFh
37	64	7F000h-7F7FFh
36[1]	64	7E800h-7EFFFh
35[1]	64	7E000h-7E7FFh
34	64	7D800h-7DFFFh
33	64	7D000h-7D7FFh
32	64	7C800h-7CFFFh
31	64	7C000h-7C7FFh
30	512	78000h-7BFFFh
29	512	74000h-77FFFh
28	512	70000h-73FFFh
27	512	6C000h-6FFFFh
26	512	68000h-6BFFFh
25	512	64000h-67FFFh
24	512	60000h-63FFFh
23	512	5C000h-5FFFFh
22	512	58000h-5BFFFh
21	512	54000h-57FFFh
20	512	50000h-53FFFh
19	512	4C000h-4FFFFh
18	512	48000h-4BFFFh
17	512	44000h-47FFFh
16	512	40000h-43FFFh
15	512	3C000h-3FFFFh

Table 5: M58BW16F Top Boot Block Addresses (Continued)

#	Size (Kbit)	Address Range
14	512	38000h-3BFFFh
13	512	34000h-37FFFh
12	512	30000h-33FFFh
11	512	2C000h-2FFFFh
10	512	28000h-2BFFFh
9	512	24000h-27FFFh
8	512	20000h-23FFFh
7	512	1C000h-1FFFFh
6	512	18000h-1BFFFh
5	512	14000h-17FFFh
4	512	10000h-13FFFh
3	512	0C000h-0FFFFh
2	512	08000h-0BFFFh
1	512	04000h-07FFFh
0	512	00000h-03FFFh

Note: 1. OTP block.

Table 6: M58BW16F Bottom Boot Block Addresses

#	Size (Kbit)	Address Range
38	512	7C000h-7FFFFh
37	512	78000h-7BFFFh
36	512	74000h-77FFFh
35	512	70000h-73FFFh
34	512	6C000h-6FFFFh
33	512	68000h-6BFFFh
32	512	64000h-67FFFh
31	512	60000h-63FFFh
30	512	5C000h-5FFFFh
29	512	58000h-5BFFFh
28	512	54000h-57FFFh
27	512	50000h-53FFFh
26	512	4C000h-4FFFFh
25	512	48000h-4BFFFh
24	512	44000h-47FFFh
23	512	40000h-43FFFh
22	512	3C000h-3FFFFh
21	512	38000h-3BFFFh
20	512	34000h-37FFFh

Table 6: M58BW16F Bottom Boot Block Addresses (Continued)

#	Size (Kbit)	Address Range
19	512	30000h-33FFFh
18	512	2C000h-2FFFFh
17	512	28000h-2BFFFh
16	512	24000h-27FFFh
15	512	20000h-23FFFh
14	512	1C000h-1FFFFh
13	512	18000h-1BFFFh
12	512	14000h-17FFFh
11	512	10000h-13FFFh
10	512	0C000h-0FFFFh
9	512	08000h-0BFFFh
8	512	04000h-07FFFh
7	64	03800h-03FFFh
6	64	03000h-037FFh
5	64	02800h-02FFFh
4	64	02000h-027FFh
3[1]	64	01800h-01FFFh
2[1]	64	01000h-017FFh
1	64	00800h-00FFFh
0	64	00000h-007FFh

Note: 1. OTP block.

Signal Descriptions

See the Logic Diagram figure and the Signal Names table for an overview of the signals connected to this device.

Address Inputs (A[MAX:0])

Amax is equal to A18 in the M58BW16F, and to A19 in the M58BW32F.

The address inputs are used to select the cells to access in the memory array during bus operations. During WRITE operations they control the commands sent to the command interface of the Program/Erase controller. E# must be LOW when selecting the addresses.

The address inputs are latched on the rising edge of L#, or on the active edge of K, whichever occurs first, in a READ operation. The address inputs are latched on the rising edge of E#, W#, or L#, whichever occurs first in a WRITE operation. The address latch is transparent when L# is LOW. The address is internally latched in an ERASE or PROGRAM operation.

Data Inputs/Outputs (DQ[31:0])

The data inputs/outputs output the data stored at the selected address during a bus READ operation, or are used to input the data during a PROGRAM operation. During bus WRITE operations they represent the commands sent to the command interface of the program/erase controller. When used to input data or WRITE commands they are latched on the rising edge of W# or E#, whichever occurs first.

When E# and G# are both LOW and GD# is HIGH, the data bus outputs data from the memory array, the electronic signature, the block protection configuration register, the CFI information, or the contents of the burst configuration register or status register. The data bus is high impedance when the device is deselected with E# and G# both HIGH, and either GD# or RP# LOW. The status register content is output on DQ0-DQ7 and DQ8-DQ31 are LOW.

Chip Enable (E#)

The chip enable, E#, input activates the memory control logic, input buffers, decoders and sense amplifiers. E# at HIGH deselects the memory and reduces the power consumption to the standby level.

Output Enable (G#)

The output enable, G#, gates the outputs through the data output buffers during a READ operation, when GD# is HIGH. When G# is HIGH, the outputs are high impedance independently of G#.

Output Disable (GD#)

The output disable, GD#, deactivates the data output buffers. When GD#, is HIGH, the outputs are driven by G#. When GD#, is LOW, the outputs are high impedance independently of GD#. The GD# pin must be connected to an external pull-up resistor as there is no internal pull-up resistor to drive the pin.

Write Enable (W#)

The write enable, W#, input controls writing to the command interface, input address, and data latches. Both addresses and data can be latched on the rising edge of W# (also see Latch Enable, L#).

Reset/Power-Down (RP#)

The reset/power-down, RP#, is used to apply a hardware reset to the memory. A hardware reset is achieved by holding RP# LOW for at least t_{PLPH}. Writing is inhibited to protect data, and the command interface and program/erase controller are reset. The status register information is cleared and power consumption is reduced to the standby level (I_{DD1}). The device acts as deselected; that is, the data outputs are high impedance.

After RP# goes HIGH, the memory will be ready for bus READ operations after a delay of t_{PHEL} or bus WRITE operations after t_{PHWL}.

If Reset/Power-down goes Low, V_{IL}, during a Block Erase or a Program operation, the internal state machine handles the operation as a Program/Erase Suspend, so the maximum time defined in the Program, Erase times and endurance cycles table must be applied.

During power-up, power should be applied simultaneously to V_{DD} and V_{DDQIN} with RP# held LOW. When the supplies are stable RP# is taken to HIGH. G#, E#, and W#, should be held HIGH during power-up.

In an application, it is recommended to associate RP# with the reset signal of the microprocessor. Otherwise, if a RESET operation occurs while the memory is performing an ERASE or PROGRAM operation, the memory may output the status register information instead of being initialized to the default asynchronous random read mode.

See the Reset, Power-down and Power-up AC characteristics table and the Reset, Power-down and Power-up AC waveforms - Control pins Low figure for more details.

Program/Erase Enable (PEN)

The program/erase enable input, PEN, protects all blocks by preventing PROGRAM and ERASE operations from modifying the data. Prior to issuing a PROGRAM or ERASE command, PEN must be set to HIGH. If it is LOW, the PROGRAM or ERASE operation is not accepted and an error is generated in the status register.

Latch Enable (L#)

The bus interface can be configured to latch the address inputs on the rising edge of Latch Enable, L#, for asynchronous latch enable controlled READ or WRITE operations or synchronous burst READ operations. In synchronous burst READ operations, the address is latched on the active edge of the clock when L# is LOW. Once latched, the addresses may change without affecting the address used by the memory. When L# is LOW, the latch is transparent. L# can remain LOW for asynchronous random READ and WRITE operations.

Burst Clock (K)

The Burst Clock, K, is used to synchronize the memory with the external bus during synchronous burst READ operations. Bus signals are latched on the active edge of the K. In synchronous burst read mode, the address is latched on the first active clock edge

when L# is LOW, or on the rising edge of L#, whichever occurs first. During asynchronous bus operations the clock is not used.

Burst Address Advance (B#)

The burst address advance, B#, controls the advancing of the address by the internal address counter during synchronous burst READ operations.

B# is only sampled on the active clock edge of K when the X-latency time has expired. If B# is LOW, the internal address counter advances. If B# is HIGH, the internal address counter does not change; the same data remains on the data inputs/outputs and B# is not sampled until the Y-latency expires. B# may be tied to V_{IL}.

Valid Data Ready (R)

The Valid Data Ready output, R, can be used during synchronous burst READ operations to identify if the memory is ready to output data or not. The R pin output can be configured to be active on the clock edge of the invalid data read cycle or one cycle before that. The R pin HIGH indicates that new data is or will be available. When R is LOW, the previous data outputs remain active.

Write Protect (WP#)

The Write Protect, WP#, provides protection against PROGRAM or ERASE operations. When WP# is LOW, the protection status that has been configured in the block protection configuration register is activated. PROGRAM and ERASE operations to protected blocks are disabled. When WP# is HIGH, all the blocks can be programmed or erased, if no other protection is used.

Supply Voltage (V_{DD})

The supply voltage, V_{DD}, is the core power supply. All internal circuits draw their current from the V_{DD} pin, including the program/erase controller.

Output Supply Voltage (V_{DDQ})

The output supply voltage, V_{DDQ}, is the output buffer power supply for all operations (Read, Program and Erase) used for DQ0-DQ31 when used as outputs.

Input Supply Voltage (V_{DDQIN})

The input supply voltage, V_{DDQIN}, is the power supply for all input signal. Input signals are: K, B#, L#, W#, GD#, G#, E#, A0-Amax and DQ0-DQ31, when used as inputs.

Ground ($V_{SS}$and V_{SSQ})

The ground V_{SS} is the reference for the internal supply voltage V_{DD}. The ground V_{SSQ} is the reference for the output and input supplies $V_{DDQ,}$ and V_{DDQIN}. It is essential to connect V_{SS} and V_{SSQ} together.

Note: A 0.1 µF capacitor should be connected between the supply voltages, V_{DD}, V_{DDQ}, and V_{DDQIN}, and the grounds, V_{SS} and V_{SSQ} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during all operations of the parts, see the DC Characteristics table, for maximum current supply requirements.

Don't Use (DNU)

The DNU pin should not be used as it is internally connected. Its voltage level can be between V_{SS} and V_{DDQ} or leave it unconnected.

Not Connected (NC)

The NC pin is not physically connected to the device.

Bus Operations

Each bus operation that controls the memory is described in this section, see the Asynchronous Bus Operations table and the Synchronous Burst Read Bus Operations table for a summary. The bus operation is selected through the burst configuration register; the bits in this register are described at the end of this section.

On power-up or after a hardware reset the memory defaults to asynchronous bus read and asynchronous bus write. No synchronous operation can be performed until the burst configuration register has been configured. The electronic signature, block protection configuration, CFI, or status register will be read in asynchronous mode regardless of the burst configuration register settings.

Typically glitches of less than 5 ns on CE# or WE# are ignored by the memory and do not affect bus operations.

Asynchronous Bus Operations

For asynchronous bus operations refer to the Asynchronous Bus Operations table together with the following text. The read access will start at whichever of the three following events occurs last: valid address transition, E# going LOW, or L# going LOW.

Asynchronous Bus Read

Asynchronous bus READ operations read from the memory cells, or specific registers (electronic signature, block protection configuration register, status register, CFI ,and burst configuration register) in the command interface. A valid bus operation involves setting the desired address on the address inputs, applying a LOW signal to E# and G# and keeping W# and GD# HIGH. The data inputs/outputs will output the value, see the Asynchronous Bus Read AC Waveforms figure and the Asynchronous Bus Read AC Characteristics table for details of when the output becomes valid.

Asynchronous read is the default read mode which the device enters on power-up or on return from reset/power-down.

Asynchronous Latch Controlled Bus Read

Asynchronous latch controlled bus READ operations read from the memory cells or specific registers in the command interface. The address is latched in the memory before the value is output on the data bus, allowing the address to change during the cycle without affecting the address that the memory uses.

A valid bus operation involves setting the desired address on the address inputs, setting E# and L# LOW and keeping W# and GD# HIGH; the address is latched on the rising edge of L#. Once latched, the address inputs can change. To read data on the data inputs/outputs, G# must be set LOW; see the Asynchronous Latch Controlled Bus Read AC Waveforms figure and the Asynchronous Bus Read AC Characteristics table for details on when the output becomes valid.

Note that, since the L# input is transparent when set LOW, asynchronous bus READ operations can be performed when the memory is configured for asynchronous latch enable bus operations by holding L# LOW throughout the bus operation.

Asynchronous Page Read

Asynchronous page READ operations are used to read from several addresses within the same memory page. Each memory page is 4 double-words and is addressed by the address inputs A0 and A1.

Data is read internally and stored in the page buffer. Valid bus operations are the same as asynchronous bus READ operations but with different timings. The first read operation within the page has identical timings, while subsequent reads within the same page have much shorter access times. If the page changes, then the normal, longer timings apply again. A page READ does not support latched controlled READ.

See the Asynchronous Page Read AC Waveforms figure and the Asynchronous Page Read AC Characteristics table for details on when the outputs become valid.

Asynchronous Bus Write

Asynchronous bus WRITE operations write to the command interface in order to send commands to the memory or to latch addresses and input data for programming. Bus WRITE operations are asynchronous, and K is don't care during bus WRITE operations.

A valid asynchronous bus WRITE operation begins by setting the desired address on the address inputs, and setting E#, W#, and L# LOW and G# HIGH. The address inputs are latched by the command interface on the rising edge of E#, W#, or L# whichever occurs first. Commands and input data are latched on the rising edge of E# or W#, whichever occurs first. G# must remain HIGH during the entire asynchronous bus WRITE operation.

See DC and AC Parameters for details of the timing and waveforms requirements.

Output Disable

The data outputs are high impedance when the G# is HIGH or GD# is LOW.

Standby

When E# is HIGH, and the program/erase controller is idle, the memory enters standby mode, the power consumption is reduced to the standby level (I_{DD1}) and the data inputs/output pins are placed in the high impedance state regardless of G#, W#, or GD# inputs.

The standby mode can be disabled by setting the standby disable bit (M14) of the burst configuration register to '1' (see the DC Characteristics table).

Reset/Power-Down

The memory is in Reset/Power-down mode when Reset/Power-down (RP#) is LOW. The power consumption is reduced to the standby level (I_{DD1}) and the outputs are high impedance, independent of the E#, G#, GD#, or W# inputs. In this mode the device is write protected and both the status and the burst configuration registers are cleared. A recovery time is required when the RP# input goes HIGH.

Table 7: Asynchronous Bus Operations[1]

Bus operation	Step	E#	G#	GD#	W#	RP#	L#	A[MAX:0]	DQ[31:0]
Asynchronous Bus Read[2]		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Address	Data output
Asynchronous Latch Controlled Bus Read	Address Latch	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Address	High Z
	Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	Data output
Asynchronous Page Read		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Address	Data output
Asynchronous Bus Write		V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	Address	Data input
Output Enable, G#		V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X	High Z
Output Disable, GD#		V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z
Standby		V_{IH}	X	X	X	V_{IH}	X	X	High Z
Reset/Power-down, RP#		X	X	X	X	V_{IL}	X	X	High Z

Notes: 1. X = Don't care.
2. Data, Manufacturer code, Device code, Burst Configuration Register, Standby Status and Block Protection Configuration Register are read using the Asynchronous Bus Read command.

Synchronous Bus Operations

Synchronous Burst Read

Synchronous burst READ operations are used to read from the memory at specific times synchronized to an external reference clock. The valid edge of the clock signal is the rising edge for M58BW32F, while for M58BW16F it is determined by setting M6 bit of the burst configuration register. Once the Flash memory is configured in burst mode, it is mandatory to have an active clock signal since the switching of the output buffer databus is synchronized to the active edge of the clock. In the absence of clock, no data is output.

The burst type, length and latency can be configured. The different configurations for synchronous burst READ operations are described in the Burst Configuration Register. Refer to the Example Burst Configuration X-1-1-1 figure for examples of synchronous burst operations.

In continuous burst read, one burst READ operation can access the entire memory sequentially by keeping B# LOW for the appropriate number of clock cycles. At the end of the memory address space, the burst read restarts from the beginning at address 000000h.

A valid synchronous burst READ operation begins when the burst clock is active and E# and L# are LOW. The burst start address is latched and loaded into the internal burst address counter on the valid edge of K or on the rising edge of L#, whichever occurs first.

After an initial memory latency time, the memory outputs data at each clock cycle (or two clock cycles depending on the value of bit M9 of Burst Configuration Register). The B# input controls the memory burst output. The second burst output is on the next clock valid edge after the B# has been pulled LOW.

Valid data ready, R, monitors if the memory burst boundary is exceeded and the burst controller of the microprocessor needs to insert wait states. When R is LOW on the ac-

tive clock edge, no new data is available and the memory does not increment the internal address counter at the active clock edge even if B# is LOW. R may be configured (by bit M8 of Burst Configuration Register) to be valid immediately at the active clock edge.

A synchronous burst READ operation will be suspended if B# goes HIGH. If G# is LOW and GD# is HIGH, the last data is still valid. If G# is HIGH or GD#, is LOW, but B# is LOW, the internal burst address counter is incremented at each active edge of K.

The synchronous burst read timing diagrams and AC characteristics are described in the AC and DC Parameters. See Figures Synchronous Burst Read, Latch Enable Controlled (data valid from 'n' clock rising edge), Synchronous Burst Read (data valid from 'n' clock rising edge), Synchronous Burst Read - valid data ready output, and Synchronous Burst Read - Burst Address Advance and the Synchronous Burst Read AC Characteristics table.

Synchronous Burst Read Suspend

During a synchronous burst READ operation, it is possible to suspend the operation, freeing the data bus for other higher priority devices.

A valid synchronous burst READ operation is suspended when both G# and B# are HIGH. The B# going HIGH stops the burst counter, and the G# going HIGH inhibits the data outputs. The synchronous burst READ operation can be resumed by setting G# LOW.

Table 8: Synchronous Burst Read Bus Operations[1]

Bus operation	Step	E#	G#	GD#	RP#	K	L#	B#	A[MAX:0] DQ[31:0]
Synchronous Burst Read[2]	Address Latch	V_{IL}	V_{IH}	X	V_{IH}	A[3]	V_{IL}	X	Address input
	Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A[3]	V_{IH}	V_{IL}	Data output
	Read Suspend	V_{IL}	V_{IH}	X	V_{IH}	X	V_{IH}	V_{IH}	High Z
	Read Resume	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A[3]	V_{IH}	V_{IL}	Data output
	Burst Address Advance	V_{IL}	V_{IH}	X	V_{IH}	A[3]	V_{IH}	V_{IL}	High Z
	Read Abort, E#	V_{IH}	X	X	V_{IH}	X	X	X	High Z
	Read Abort, RP#	X	X	X	V_{IL}	X	X	X	High Z

Notes:
1. X = Don't care, V_{IL} or V_{IH}.
2. M15 = 0, Bit M15 is in the Burst Configuration Register.
3. A = Active edge (See bit M6 in the burst configuration register for further details on the active edge of K).

Burst Configuration Register

The burst configuration register is used to configure the type of bus access that the memory will perform.

The burst configuration register is set through the command interface and will retain its information until it is re-configured, the device is reset, or the device goes into reset/power-down mode. The burst configuration register bits are described in the Burst Configuration Register table. They specify the selection of the burst length, burst type, burst X and Y latencies and the READ operation. Refer to the Example Burst Configuration X-1-1-1 figure for examples of synchronous burst configurations.

Read Select Bit M15

The read select bit, M15, is used to switch between asynchronous and synchronous bus READ operations. When the read select bit is set to 1, bus READ operations are asynchronous; when the read select bit is set to 0, bus READ operations are synchronous. On reset or power-up, the read select bit is set to 1 for asynchronous accesses.

Standby Disable Bit M14

The standby disable bit, M14, is used to disable the standby mode. When the standby bit is 1, the device will not enter standby mode when E# goes HIGH.

X-Latency Bits M13-M11

The X-latency bits M13-M11 are used during synchronous bus READ operations to set the number of clock edges between the address being latched and the edge where the first data become available. For correct operation the X-latency bits can only assume the values in the burst configuration register table.

Y-Latency Bit M9

The Y-latency bit is used during synchronous bus READ operations to set the number of clock cycles between consecutive reads. When the Y-latency bit is 1, the data changes each clock cycle. When the Y-latency is 2, the data changes every second clock cycle.

Valid Data Ready Bit M8

The valid data ready bit controls the timing of pin R. When the valid data ready bit is 0, pin R output is driven LOW for the active clock edge when invalid data is output on the bus. When the valid data ready bit is 1, pin R output is driven LOW one clock cycle prior to invalid data being output on the bus.

Valid Clock Edge Bit (M6)

For M58BW16F, the valid clock edge bit, M6, is used to configure the active edge of K during synchronous burst READ operations. When the valid clock edge bit is 0, the falling edge of K is the active edge; when the valid clock edge bit is 1, the rising edge of K is active. For M58BW32F, bit M6 is "Don't Care." Only rising edge of K is available.

Burst Wrap Bit M3

The burst READ operations can be confined inside the 4 or 8 double-word boundary (wrap) or overcome the boundary (no wrap). The wrap burst bit is used to select between wrap and no wrap. When the wrap burst bit is set to 0, the burst READ operation wraps; when it is set to 1, the burst READ operation does not wrap.

Burst Length Bits M2-M0

The burst length bits set the maximum number of double-words that can be output during a synchronous burst READ operation. Burst lengths of 4, 8, or continuous burst are available. The Burst Configuration Register table gives the valid combinations of the burst length bits that the memory accepts.

If either a continuous or a no wrap burst READ operation has been initiated, the device will output data synchronously. Depending on the starting address, the device asserts the pin R to communicate that some wait states are needed before the data valid appearance. As shown in the WAIT States table, the bits ADD[4:0] of the starting address

will determine the number of WAIT states that the device is going to drive in the data bus lines. Elsewhere, the burst mode will run without activating the pin R output.

Table 9: Burst Configuration Register

Note 1 applies to the entire table.

Bit	Description	Value	Description	Notes
M15	Read select	0	Synchronous burst read	
		1	Asynchronous read (default at power-up)	
M14	Standby disable	0	Standby mode enabled (default at power-up)	
		1	Standby mode disabled	
M13-M11	X-latency	000	Reserved (default value)	2
		001	3, 3-1-1-1, 3-2-2-2	
		010	4, 4-1-1-1, 4-2-2-2	
		011	5, 5-1-1-1, 5-2-2-2	
		100	6, 6-1-1-1, 6-2-2-2	
		101	7, 7-1-1-1, 7-2-2-2	
		110	8, 8-1-1-1, 8-2-2-2	
		111	Reserved	
M10		0	Reserved (default value)	
		1	Reserved	
M9	Y-latency	0	One burst clock cycle (default value)	3
		1	Two burst clock cycles	
M8	Valid data ready	0	R valid LOW during valid burst clock edge (default value)	
		1	R valid LOW 1 data cycle before valid burst clock edge	
M7		0	Reserved (default value)	
		1	Reserved	
M6	Valid clock edge	0	Falling burst clock edge (default value)	4
		1	Rising burst clock edge	
M5-M4		00	Reserved (default value)	
		01	Reserved	
		10	Reserved	
		11	Reserved	
M3	Wrapping	0	Wrap (default value)	
		1	No Wrap	

Table 9: Burst Configuration Register (Continued)

Note 1 applies to the entire table.

Bit	Description	Value	Description	Notes
M2-M0	Burst length	000	Reserved (default value)	
		001	4 double-words	
		010	8 double-words	
		011	Reserved	
		100	Reserved	
		101	Reserved	
		110	Reserved	
		111	Continuous	

Notes:
1. M10, M7, M5, and M4 are reserved for future use.
2. X latencies can be calculated as: $(t_{AVQV} - t_{LLKH} + t_{QVKH}) + t_{SYSTEM\ MARGIN} < (X - 1)\ t_K$. X is an integer number from 4 to 8, t_K is the clock period and $t_{SYSTEM\ MARGIN}$ is the time margin required for the calculation.
3. Y latencies can be calculated as: $t_{KHQV} + t_{SYSTEM\ MARGIN} + t_{QVKH} < Y\ t_K$.
4. M6 bit is Don't Care in the M58BW32F and the device has the rising burst clock edge set. To maintain the compatibility this could be modified and read.

Table 10: WAIT States

ADD[4:0]	Number of Clock WAIT States
11101	1
11110	2
11111	3

Table 11: Burst Type Definition

M3	Starting Address	X4	X8	Continuous
0	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10
0	1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11
0	2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12
0	3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13
0	4	–	4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14
0	5	–	5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15
0	6	–	6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-16
0	7	–	7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-16-17
0	8	–	-	8-9-10-11-12-13-14-15-16-17-18
1	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10
1	1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8-9-10-11
1	2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-9-10-11-12
1	3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10-11-12-13

Table 11: Burst Type Definition (Continued)

M3	Starting Address	X4	X8	Continuous
1	4	4-5-6-7	4-5-6-7-8-9-10-11	4-5-6-7-8-9-10-11-12-13-14
1	5	5-6-7-8	5-6-7-8-9-10-11-12	5-6-7-8-9-10-11-12-13-14-15
1	6	6-7-8-9	6-7-8-9-10-11-12-13	6-7-8-9-10-11-12-13-14-15-16
1	7	7-8-9-10	7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-15-16-17
1	8	10-11-12-13	8-9-10-11-12-13-14-15	8-9-10-11-12-13-14-15-16-17-18

Figure 4: Example Burst Configuration X-1-1-1

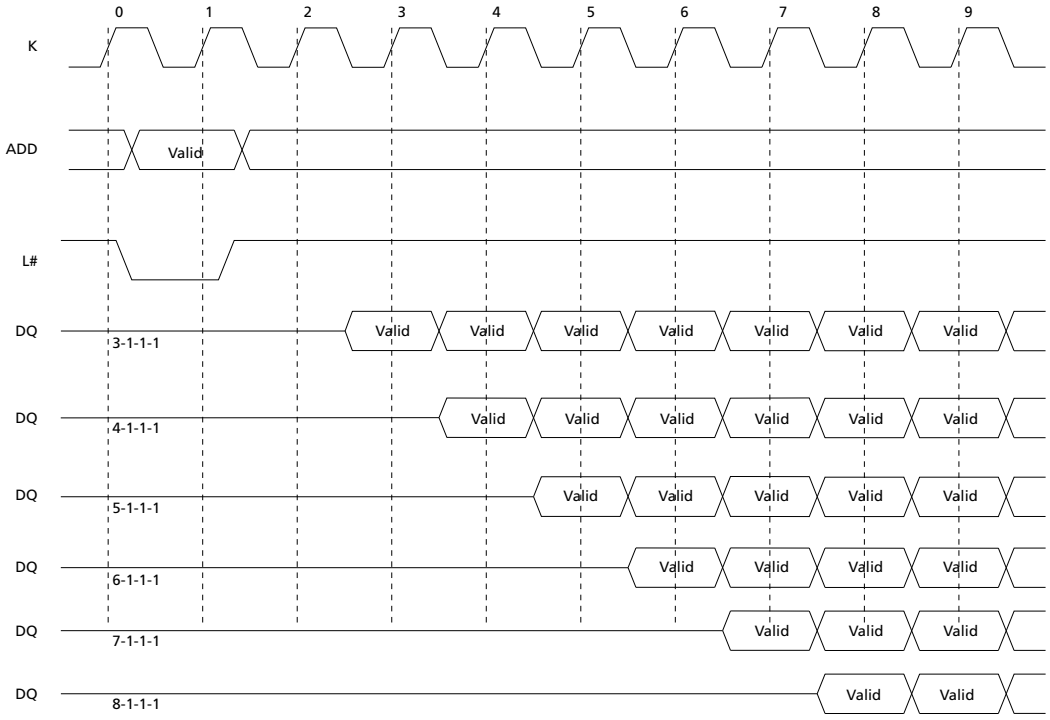
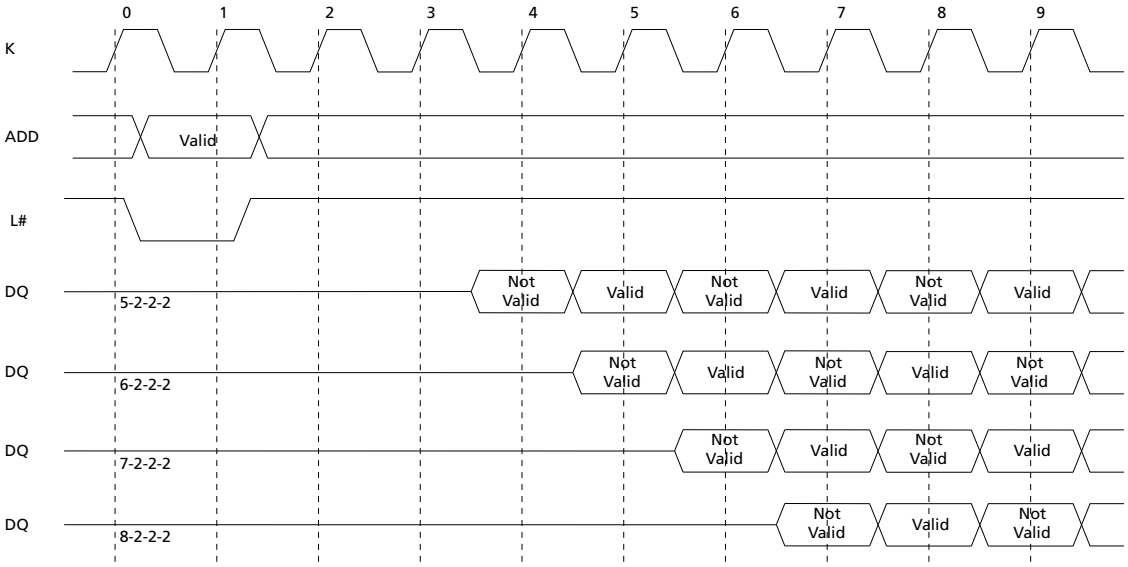


Figure 5: Example Burst Configuration X-2-2-2



Device Commands

All bus WRITE operations to the memory are interpreted by the command interface. Commands consist of one or more sequential bus write operations. The commands are summarized in the Commands table.

Table 12: Commands[1]

Command		Cycles	Bus operations											
			1st cycle			2nd cycle			3rd cycle			4th cycle		
			Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data
READ MEMORY ARRAY		≥ 2	Write	X	FFh	Read	RA	RD						
READ ELECTRONIC SIGNATURE[2]		≥ 2	Write	X	90h	Read	IDA	IDD						
READ STATUS REGISTER		1	Write	X	70h									
READ QUERY		≥ 2	Write	X	98h	Read	RA	RD						
CLEAR STATUS REGISTER		1	Write	X	50h									
BULK ERASE		2	Write	55h	20h	Write	BA	D0h						
ERASE ALL MAIN BLOCKS		2	Write	55h	80h	Write	AAh	D0h						
PROGRAM	any block	2	Write	AAh	40h 10h	Write	PA	PD						
	OTP block	2	Write	AAh	40h	Write	PA	PD						
WRITE TO BUFFER AND PROGRAM		N+4	Write	AAh	E8h	Write	BA	N	Write	PA	PD	Write	X	D0h
PROGRAM/ERASE SUSPEND		1	Write	X	B0h									
PROGRAM/ERASE RESUME		1	Write	X	D0h									
SET BURST CONFIGURATION REGISTER		3	Write	X	60h	Write	BCRh	03h	Read	RA	RD			
SET BLOCK PROTECTION CONFIGURATION REGISTER		2	Write	X	60h	Write	BA	01h						
CLEAR BLOCK PROTECTION CONFIGURATION REGISTER		2	Write	X	60h	Write	BA	D0h						
LOCK OTP PROTECTION		2	Write	AAh	49h	Write	03h	00h						

Notes:
1. X Don't care; RA Read Address, RD Read Data, ID Device Code, IDA Identifier Address, IDD Identifier Data, SRD Status Register Data, PA Program Address; PD Program Data, QA Query Address, QD Query Data, BA Any address in the Block, BCR Burst Configuration Register value, N+1 number of Words to program, BA Block address.
2. Manufacturer code, device code, burst configuration register, and block protection configuration register of each block are read using the Read Electronic Signature command.

READ MEMORY ARRAY Command

The READ MEMORY ARRAY command returns the memory to read mode. One bus write cycle is required to issue the command and return the memory to read mode. Subsequent READ operations will output the addressed memory array data. Once the command is issued, the memory remains in read mode until another command is issued. From read mode, READ commands will access the memory array.

READ ELECTRONIC SIGNATURE Command

The READ ELECTRONIC SIGNATURE command is used to read the manufacturer code, the device code, the block protection configuration register and the burst configuration register. One bus write cycle is required to issue the command. Once the command is issued, subsequent bus READ operations, depending on the address specified, read the manufacturer code, the device code, the block protection configuration or the burst configuration register until another command is issued.

Table 13: Read Electronic Signature

Code	Device	A[MAX:0]	DQ[31:0]
Manufacturer	All	00000h	00000020h
Device	M58BW16FT	00001h	0000883Ah
	M58BW16FB	00001h	00008839h
	M58BW32FT	00001h	00008838h
	M58BW32FB	00001h	00008837h
Burst Configuration Register	All	00005h	BCR[1]
Block Protection Configuration Register	All	SBA+02h[2]	00000000h (Unprotected)
			00000001h (Protected)

Notes: 1. BCR = Burst Configuration Register.
2. SBA is the start address of each block.

READ QUERY Command

The READ QUERY command is used to read data from the common flash interface (CFI) memory area. One bus write cycle is required to issue the command. Once the command is issued, subsequent bus READ operations read from the CFI memory area, depending on the address specified.

READ STATUS REGISTER Command

The READ STATUS REGISTER command is used to read the status register. One bus write cycle is required to issue the command. Once it is issued, subsequent bus READ operations read the status register until another command is issued.

The status register information is present on DQ0-DQ7 when E# and G# are LOW and GD# is at HIGH.

An interactive update of the status register bits is possible by toggling G# or GD#. This update is also possible during PROGRAM, ERASE, or WRITE TO BUFFER and PROGRAM operations by performing the following: deactivate the device with E# LOW and then reactivate the device with E# and G# LOW and GD# HIGH.

The content of the status register may also be read at the completion of PROGRAM, ERASE, SUSPEND, or WRITE TO BUFFER and PROGRAM operations. During PROGRAM, ERASE, or WRITE TO BUFFER and PROGRAM commands, DQ7 indicates the program/erase controller status. It is valid until the operation is completed or suspended.

See the Status Register and Status Register Bits tables for details on the definitions of the status register bits.

CLEAR STATUS REGISTER Command

The CLEAR STATUS REGISTER command can be used to reset to 0 bits 1, 3, 4 and 5 in the status register. One bus write cycle is required to issue this command. Once the command is issued, the memory returns to its previous mode, and subsequent bus READ operations continue to output the same data.

The bits in the status register do not automatically return to 0 when a new PROGRAM, ERASE, BLOCK PROTECT, BLOCK UNPROTECT, or WRITE TO BUFFER and PROGRAM commands are issued. If an error occurs, it is essential to clear any error bits in the status register by issuing a CLEAR STATUS REGISTER command before attempting a new PROGRAM, ERASE, RESUME, or WRITE TO BUFFER and PROGRAM commands.

BLOCK ERASE Command

The BLOCK ERASE command can be used to erase a block. It sets all of the bits in the block to '1'. All previous data in the block is lost. If the block is protected then the ERASE operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two bus write cycles are required to issue the command; the first write cycle sets up the command, the second confirms the command, latches the block address in the program/erase controller, and starts the program/erase controller. The sequence is aborted if the CONFIRM command is not given, and the device will output the status register data with bits 4 and 5 set to 1.

Once the command is issued, subsequent bus READ operations read the status register. See the section on the status register for details on the definitions of the status register bits. During the ERASE operation, the memory will accept only the READ STATUS REGISTER command and the PROGRAM/ERASE SUSPEND command. All other commands are ignored.

If PEN is HIGH, the operation can be performed. If PEN goes below HIGH, the operation aborts and the PEN status bit in the status register is set to 1. The status register should be cleared before reissuing the command.

Typical erase times are given in the Program and Erase Times and Endurance Cycles table. See the Block Erase Flowchart and Pseudocode figure for a suggested flowchart on using the BLOCK ERASE command.

ERASE ALL MAIN BLOCKS Command

The ERASE ALL MAIN BLOCKS command is used to erase all main blocks (62 main blocks for M58BW32F and 31 main blocks for M58BW16F).

without affecting the parameter blocks. Issuing the command sets every bit in each main block to 1. All data previously stored in the main blocks are lost.

Two bus write cycles are required to issue this command. The first cycle sets up the command, and the second cycle confirms the command and starts the program/erase controller. If the CONFIRM command is not given, the sequence is aborted, and status register bits 4 and 5 are set to 1. If the address given in the second cycle is located in a protected block, the ERASE ALL MAIN BLOCKS operation aborts. The data remains unchanged in all blocks and the status register outputs the error.

Once the command has been issued, subsequent bus READ operations output the status register. See the Status Register for details.

During an ERASE ALL MAIN BLOCKS operation, only the READ STATUS REGISTER command is accepted by the memory; any other command are ignored. The ERASE ALL MAIN BLOCKS command cannot be suspended once it has begun.

If PEN is HIGH, the operation will be performed. Otherwise, the operation aborts and the status register PEN bit (bit 3) is set to 1. The status register should be cleared before reissuing the command.

PROGRAM Command

The PROGRAM command is used to program the memory array. Two bus write operations are required to issue the command; the first write cycle sets up the PROGRAM command, and the second write cycle latches the address and data to be programmed and starts the program/erase controller. A PROGRAM operation can be aborted by writing FFFFFFFFh to any address after the program set-up command has been given.

The PROGRAM command is also used to program the OTP block. Refer to the Commands table for details of the address.

Once the command is issued, subsequent bus READ operations read the status register. See the Status Register table for details on the definitions of the status register bits. During the PROGRAM operation, the memory will accept only the READ STATUS REGISTER command and the PROGRAM/ERASE SUSPEND command. All other commands will be ignored.

If RP#, falls to LOW during programming, the operation will be aborted.

If PEN is HIGH, the operation can be performed. Otherwise, the operation aborts, and the PEN status bit in the status register is set to 1. The status register should be cleared before reissuing the command. See also the Program Flowchart and Pseudocode figure.

WRITE TO BUFFER AND PROGRAM Command

The WRITE TO BUFFER AND PROGRAM command makes use of the device's double word (32 bit) write buffer to speed up programming. Up to eight double words can be loaded into the write buffer and programmed into the memory. The following successive steps are required to issue the command.

1. One bus write operation is required to set up the WRITE TO BUFFER AND PROGRAM command. Any bus read operations will start to output the status register after the 1st cycle.
2. Use one bus write operation to write the selected memory block address (any address in the block where the values will be programmed can be used) along with the value N on the data inputs/outputs, where N+1 is the number of words to be programmed. The maximum value of N+1 is 8 words.

3. Use N+1 bus write operations to load the address and data for each word into the write buffer. The address must be between Start address and Start address plus N, where start address is the first word address.
4. Finally, use one bus write operation to issue the final cycle to confirm the command and start the PROGRAM operation.

If any address is outside the block boundaries or if the correct sequence is not followed, status register bits 4 and 5 are set to 1 and the operation will abort without affecting the data in the memory array. A protected block must be unprotected using the BLOCKS UNPROTECT command.

During a WRITE TO BUFFER AND PROGRAM operation, the memory will accept only the READ STATUS REGISTER and the PROGRAM/ERASE SUSPEND commands. All other commands are ignored. If PEN is HIGH, the operation executes. Otherwise, the operation aborts and the status register PEN bit (bit 3) is set to 1. The status register should be cleared before reissuing the command.

PROGRAM/ERASE SUSPEND Command

The PROGRAM/ERASE SUSPEND command is used to pause a PROGRAM, ERASE, or WRITE TO BUFFER AND PROGRAM operation. The command will be accepted only during a PROGRAM, ERASE, or WRITE TO BUFFER AND PROGRAM operation. It can be issued at any time during a PROGRAM, ERASE, or WRITE TO BUFFER AND PROGRAM operation. The command is ignored if the device is already in suspend mode.

One bus write cycle is required to issue the command and pause the program/erase controller. Once the command is issued, it is necessary to poll the program/erase controller status bit (bit 7) to find out when the program/erase controller has paused. No other commands will be accepted until the program/erase controller has paused, after which the memory will continue to output the status register until another command is issued.

During the polling period between issuing the PROGRAM/ERASE SUSPEND command and the program/erase controller pausing, it is possible for the operation to complete. Once the program/erase controller status bit (bit 7) indicates that the program/erase controller is no longer active, the program suspend status bit (bit 2) or the erase suspend status bit (bit 6) can be used to determine if the operation has completed or is suspended. For timing on the delay between issuing the PROGRAM/ERASE SUSPEND command and the program/erase controller pausing, see the Program and Erase Times and Endurance Cycles table.

During execution of a PROGRAM/ERASE SUSPEND command, the READ MEMORY ARRAY, READ STATUS REGISTER, READ ELECTRONIC SIGNATURE, READ QUERY, and PROGRAM/ERASE SUSPEND commands will be accepted by the command interface. Additionally, if the suspended operation was an ERASE operation, the PROGRAM, WRITE TO BUFFER AND PROGRAM, SET/CLEAR BLOCK PROTECTION CONFIGURATION REGISTER, and PROGRAM SUSPEND commands will also be accepted. When a PROGRAM operation is completed inside a BLOCK ERASE SUSPEND operation, the READ MEMORY ARRAY command must be issued to reset the device in read mode. Then, the ERASE RESUME command can be issued to complete the whole sequence. Only the blocks not being erased may be read or programmed correctly.

ERASE operations can be suspended in a systematic and periodical way; however, to ensure the effectiveness of ERASE operations and avoid infinite erase times, it is imperative to wait a minimum time between successive ERASE RESUME and ERASE SUS-

PEND commands. This time, called the minimum effective erase time, is given in the Program and Erase Times and Endurance Cycles table.

See the Program Suspend & Resume Flowchart and Pseudocode figure and the Erase Suspend and Resume Flowchart and Pseudocode figure for suggested flowcharts on using the PROGRAM/ERASE SUSPEND command.

PROGRAM/ERASE RESUME Command

The PROGRAM/ERASE RESUME command can be used to restart the program/erase controller after a PROGRAM/ERASE SUSPEND operation has paused it. One bus write cycle is required to issue the PROGRAM/ERASE RESUME command.

See the Program Suspend and Resume Flowchart and Pseudocode figure, and the Erase Suspend and Resume Flowchart and Pseudocode figure for information on using the PROGRAM/ERASE RESUME command.

SET BURST CONFIGURATION REGISTER Command

The SET BURST CONFIGURATION REGISTER command is used to write a new value to the burst configuration register. This register defines the burst length, type, X and Y latencies, and synchronous/asynchronous read mode. For M58BW16F only, it also defines the valid clock edge configuration.

Two bus write cycles are required to issue the SET BURST CONFIGURATION REGISTER command. The first cycle writes the setup command. The second cycle writes the address where the new burst configuration register content is to be written and then confirms the command. If the command is not confirmed, the sequence is aborted and the device outputs the status register with bits 4 and 5 set to 1. Once the command is issued, the memory returns to read mode as if a READ MEMORY ARRAY command had been issued.

The value for the burst configuration register is always presented on A0-A15. M0 is on A0, M1 on A1, etc.; address bits A16-Amax are ignored.

SET BLOCK PROTECTION CONFIGURATION REGISTER Command

The SET BLOCK PROTECTION CONFIGURATION REGISTER command is used to configure the block protection configuration register to ‘protected’, for a specific block. Protected blocks are fully protected from program or erase when WP# pin is LOW. The status of a protected block can be changed to ‘unprotected’ by using the CLEAR BLOCK PROTECTION CONFIGURATION REGISTER command. At power-up, all blocks are configured as ‘protected’.

Two bus operations are required to issue a Set Block Protection Configuration Register command:

- The first cycle writes the setup command
- The second write cycle specifies the address of the block to protect and confirms the command. If the command is not confirmed, the sequence is aborted and the device outputs the status register with bits 4 and 5 set to 1.

To protect multiple blocks, the SET BLOCK PROTECTION CONFIGURATION REGISTER command must be repeated for each block. Any attempt to reprotect a block already protected does not change its status.

CLEAR BLOCK PROTECTION CONFIGURATION REGISTER Command

The CLEAR BLOCK PROTECTION CONFIGURATION REGISTER command is used to configure the block protection configuration register to 'unprotected', for a specific block thus allowing PROGRAM/ERASE operations to this block, regardless of the WP# pin status.

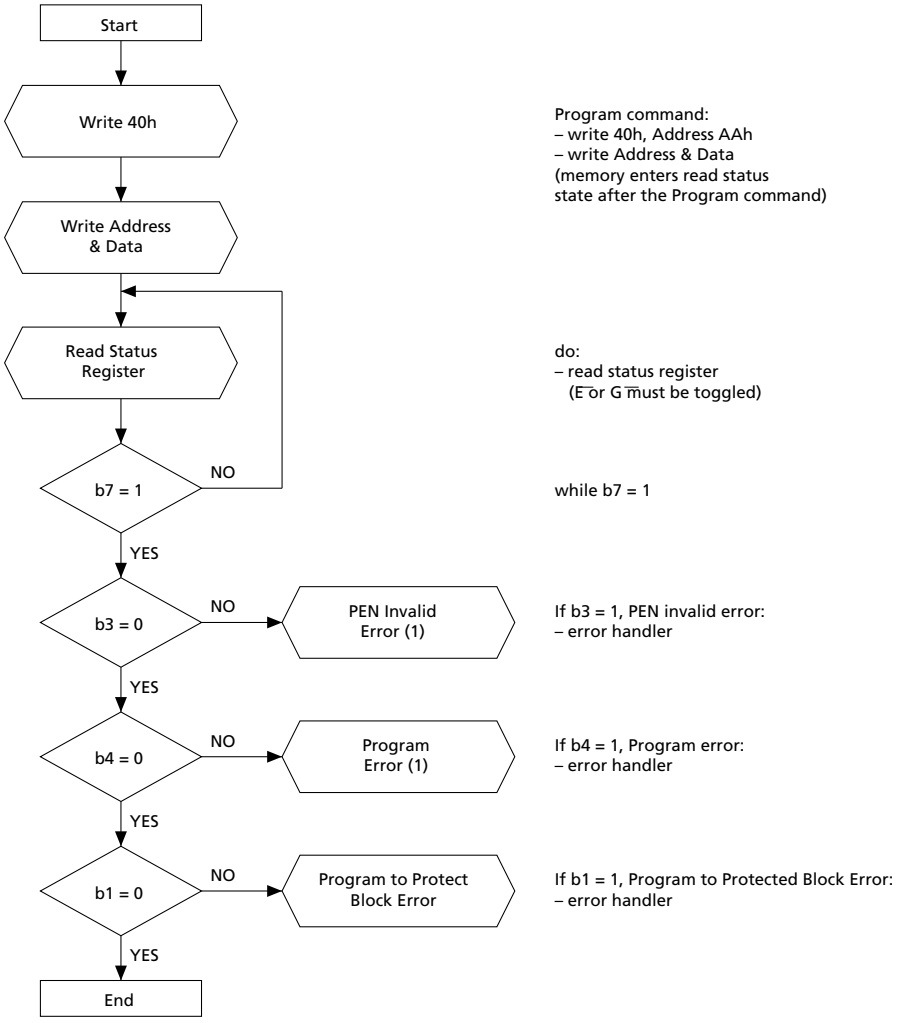
Two bus operations are required to issue a CLEAR BLOCK PROTECTION CONFIGURATION REGISTER command:

- The first cycle writes the setup command
- The second write cycle specifies the address of the block to unprotect and confirms the command. If the command is not confirmed, the sequence is aborted and the device outputs the status register with bits 4 and 5 set to 1.

To unprotect multiple blocks, the CLEAR BLOCK PROTECTION CONFIGURATION REGISTER command must be repeated for each block. Any attempt to unprotect a block already unprotected does not affect its status.

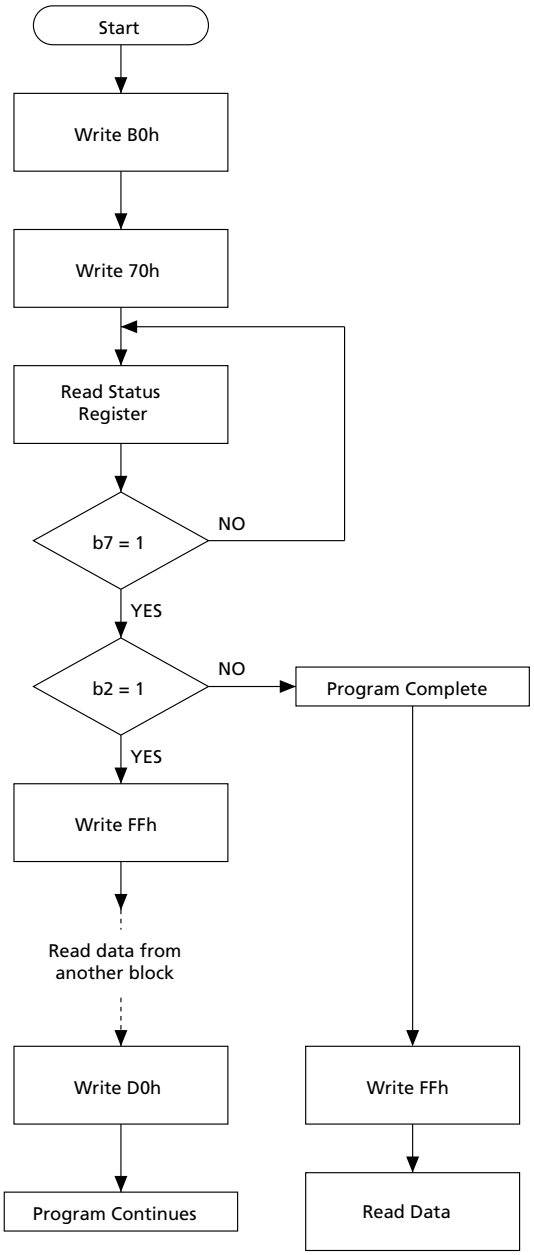
Flowcharts

Figure 6: Program Flowchart and Pseudocode



Note: 1. If an error is found, the Status Register must be cleared before further P/E operations.

Figure 7: Program Suspend & Resume Flowchart and Pseudocode



Program/Erase Suspend command:
– write B0h
– write 70h

do:
– read status register

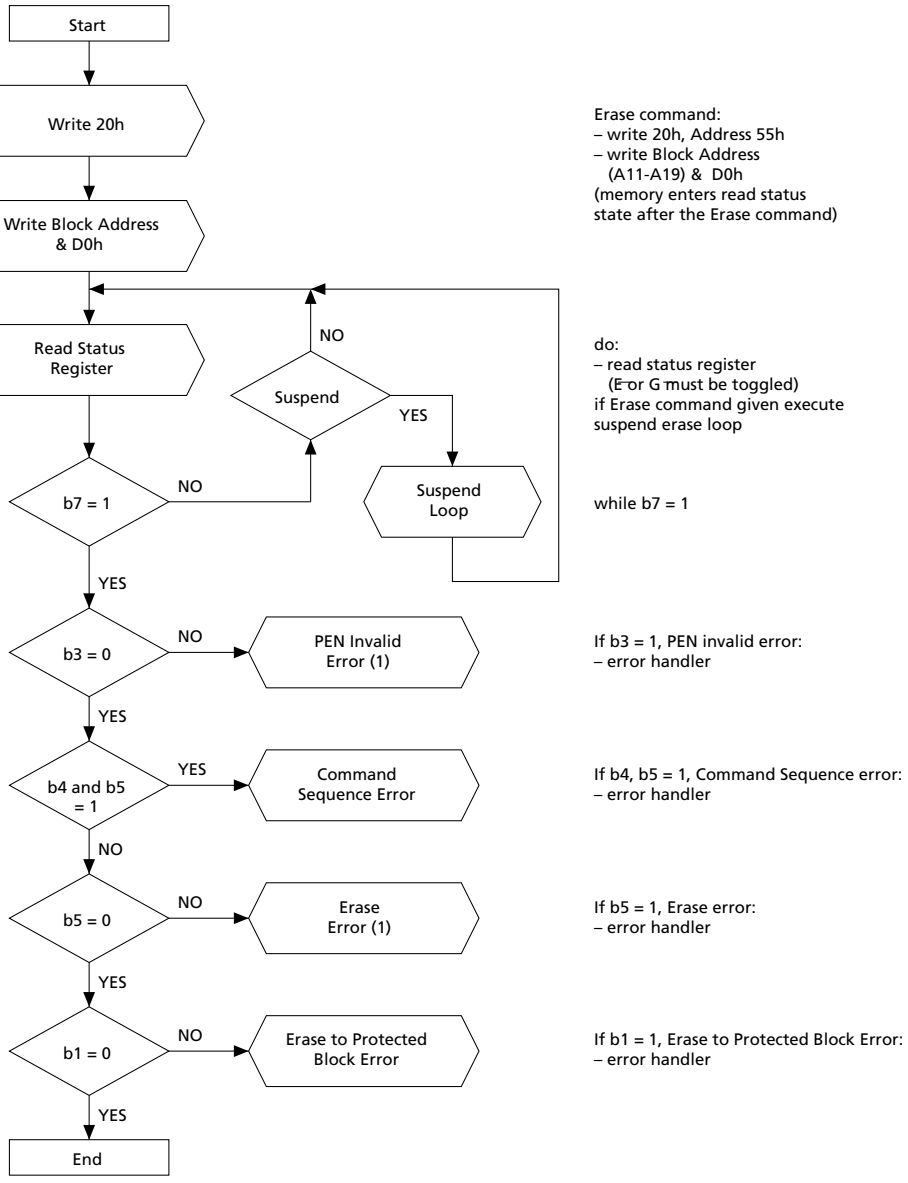
while b7 = 1

If b2 = 0, Program completed

Read Memory Array command:
– write FFh
– one or more data reads from other blocks

Program Erase Resume command:
– write D0h to resume programming
– if the program operation completed then this is not necessary. The device returns to Read Array as normal (as if the Program/Erase Suspend command was not issued).

Figure 8: Block Erase Flowchart and Pseudocode



Note: 1. If an error is found, the Status Register must be cleared before further Program/Erase operations.

Figure 9: Erase Suspend & Resume Flowchart and Pseudocode

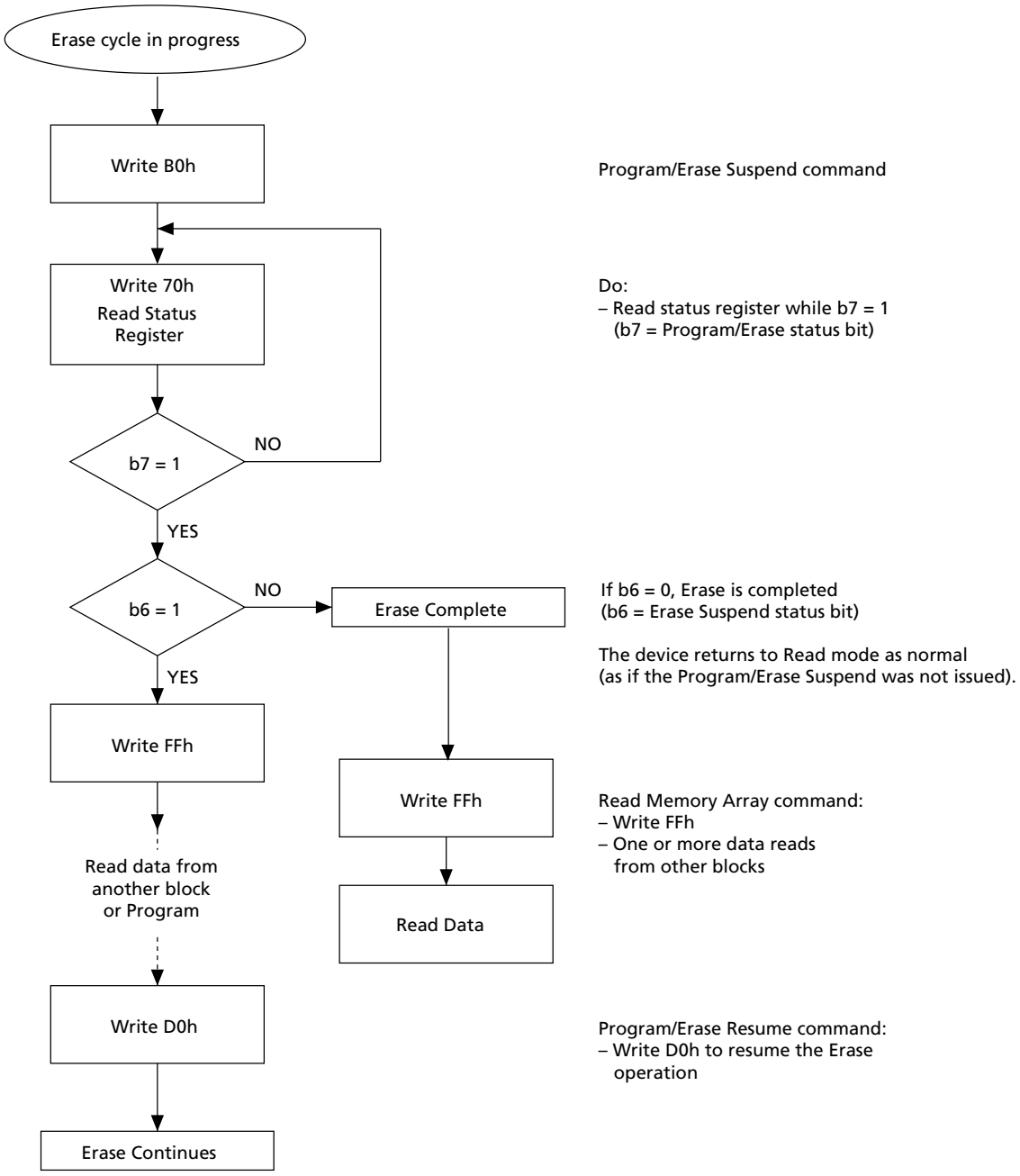


Figure 10: Power-up Sequence followed by Synchronous Burst Read

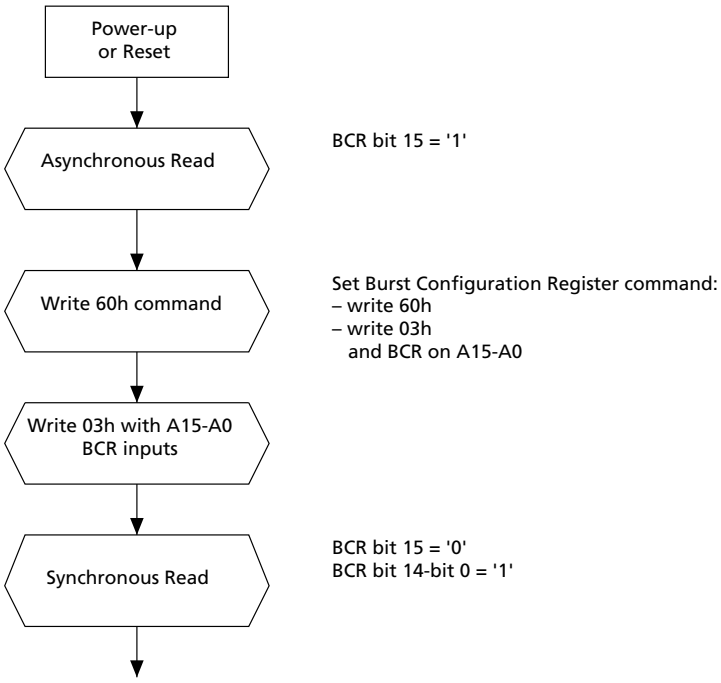


Figure 11: Command Interface and Program/Erase Controller Flowchart (A)

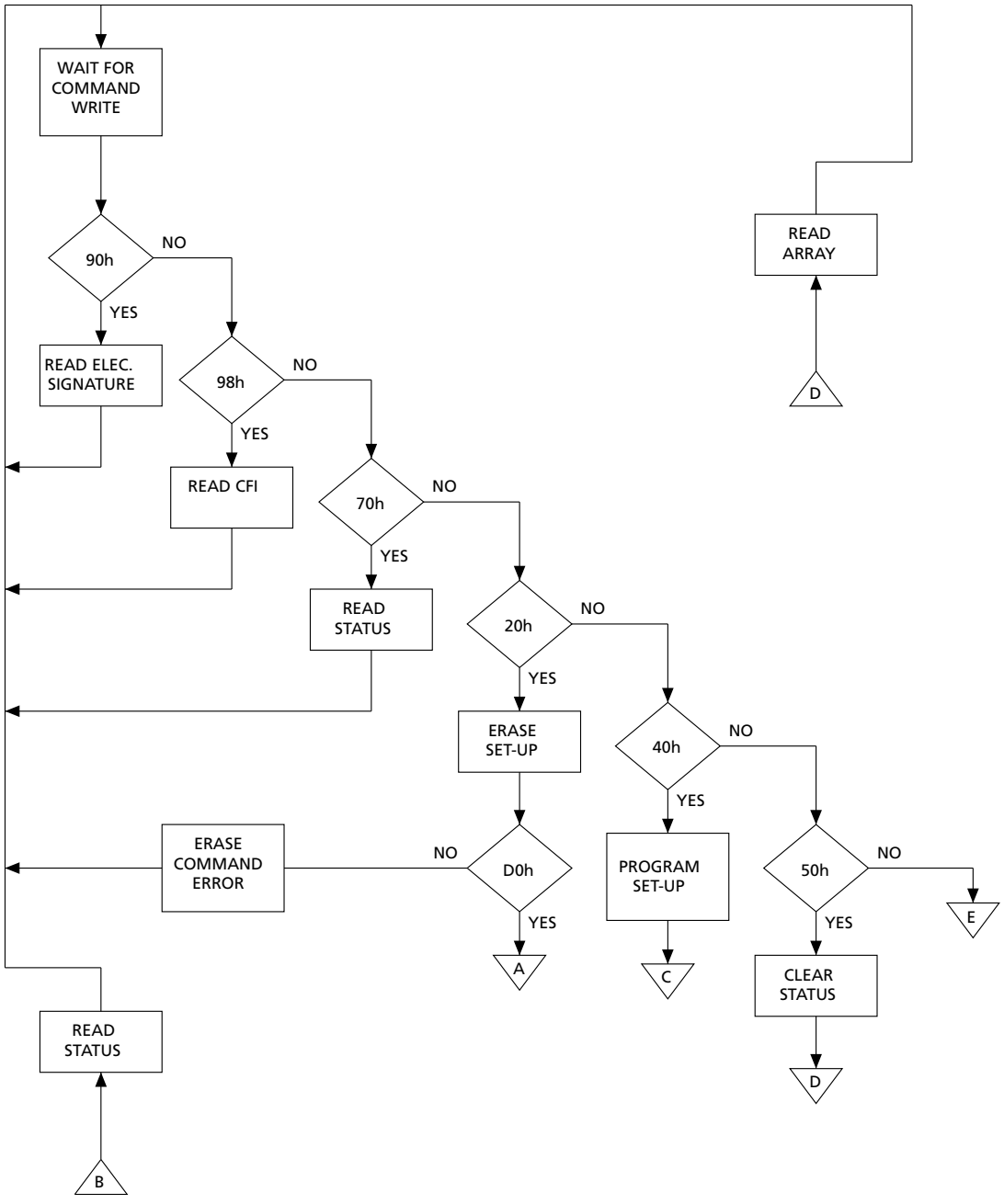


Figure 12: Command Interface and Program/Erase Controller Flowchart (B)

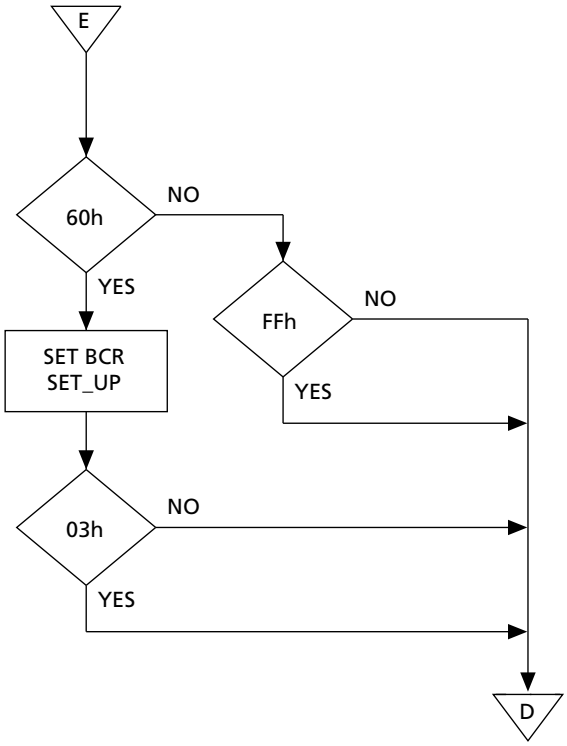


Figure 13: Command Interface and Program/Erase Controller Flowchart (C)

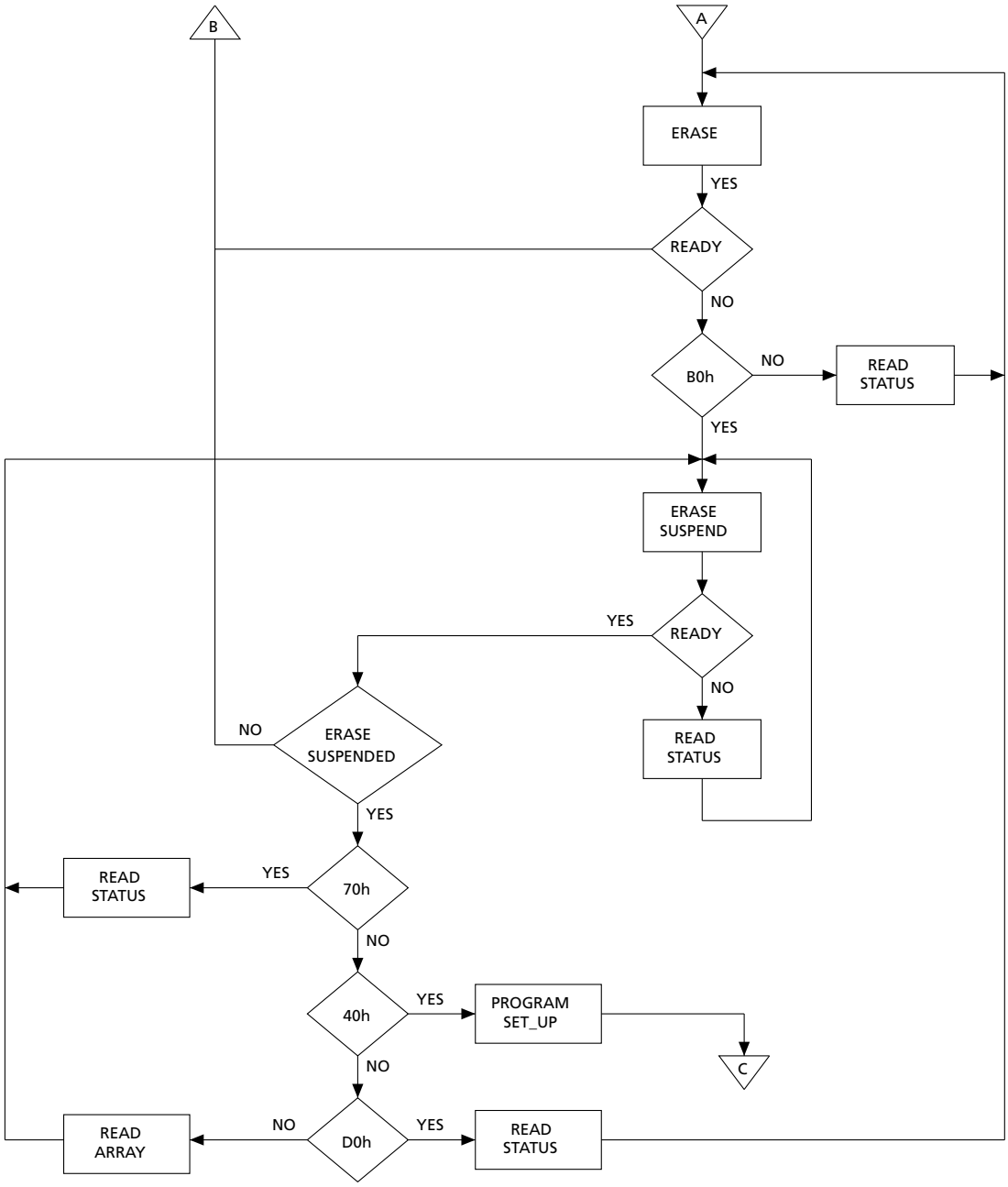
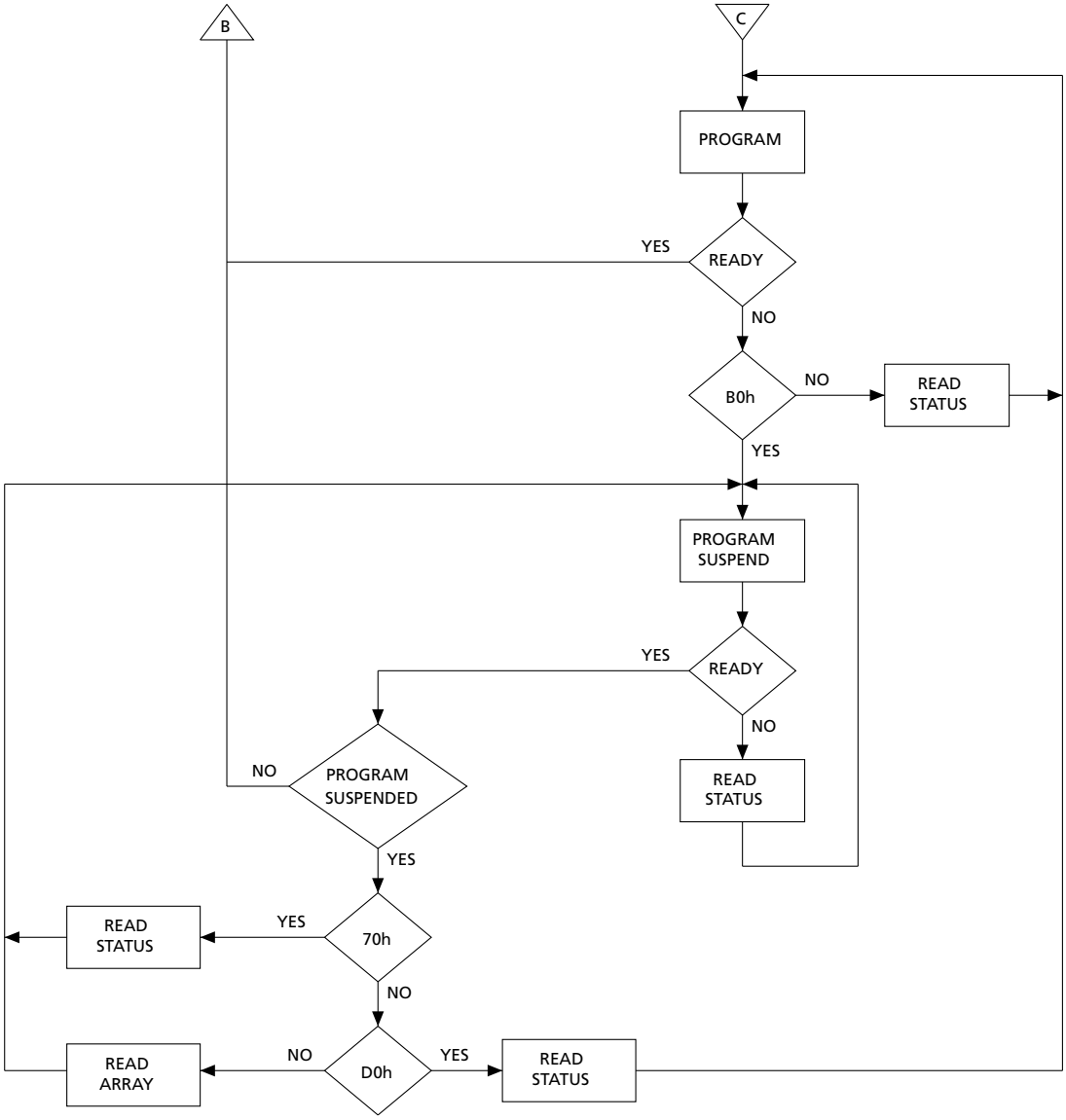


Figure 14: Command Interface and Program/Erase Controller Flowchart (D)



Status Register

The Status Register provides information on the current or previous PROGRAM, ERASE, WRITE TO BUFFER AND PROGRAM, or BLOCK PROTECT operation. The various bits in the Status Register convey information and errors on the operation. They are output on DQ[7:0].

To read the Status Register the Read Status Register command can be issued. The Status Register is automatically read after PROGRAM, ERASE, WRITE TO BUFFER AND PROGRAM, BLOCK PROTECT, PROGRAM/ERASE RESUME commands. The Status Register can be read from any address.

The contents of the Status Register can be updated during a PROGRAM, ERASE, OR WRITE TO BUFFER AND PROGRAM operation by toggling the Output Enable or Output Disable pins or by de-activating (Chip Enable, V_{IH}) and then reactivating (Chip Enable and Output Enable, V_{IL}, and Output Disable, V_{IH}.) the device.

The Status Register bits are summarized in the Status Register bits table. Refer to the Status Register bits table in conjunction with the following text descriptions.

Table 14: Status Register Bits

Bit	Name	Logic level	Definition
7	Program/Erase Controller Status	'1'	Ready
		'0'	Busy
6	Erase Suspend Status	'1'	Suspended
		'0'	In progress or completed
5	Erase Status	'1'	Erase error
		'0'	Erase success
4	Program Status,	'1'	Program error
		'0'	Program success
3	PEN Status bit	'0'	No program or erase attempted
		'1'	Program or erase attempted
2	Program Suspend Status	'1'	Suspended
		'0'	In progress or completed
1	Erase/Program in a protected block	'1'	Program/erase on protected block, abort
		'0'	No operations to protected blocks
0	Reserved	'1'	Reserved

Program/Erase Controller Status (bit 7)

The program/erase controller status bit indicates whether the program/erase controller is active or inactive. When the program/erase controller status bit is set to '0', the program/erase controller is active; when bit 7 is set to 1, the program/erase controller is inactive.

The program/erase controller status is set to 0 immediately after a PROGRAM/ERASE SUSPEND command is issued and until the program/erase controller pauses. After the program/erase controller pauses, the bit is set to 1.

During PROGRAM, ERASE, and WRITE TO BUFFER AND PROGRAM operations, the program/erase controller status bit can be polled to find the end of the operation. The other bits in the status register should not be tested until the program/erase controller completes the operation and the bit is set to ‘.

After the program/erase controller completes its operation, the erase status (bit 5) and program status (bit 4) should be tested for errors.

Erase Suspend Status (bit 6)

The Erase Suspend Status bit indicates that an Erase operation has been suspended and is waiting to be resumed. The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is set to ‘1’ (Program/Erase controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Erase Suspend Status bit is set to ‘0’, the Program/Erase controller is active or has completed its operation; when the bit is set to ‘1’, a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns to ‘0’.

Erase Status (Bit 5)

The Erase Status bit can be used to identify if the memory has failed to verify that the block has erased correctly. The Erase Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase controller inactive).

When the Erase Status bit is set to ‘0’, the memory has successfully verified that the block has erased correctly. When the Erase Status bit is set to ‘1’, the Program/Erase controller has applied the maximum number of pulses to the block and still failed to verify that the block has erased correctly.

Once set to ‘1’, the Erase Status bit can only be reset to ‘0’ by a Clear Status Register command or a hardware reset. If set to 1 it should be reset before a new PROGRAM, ERASE, or WRITE TO BUFFER AND PROGRAM command is issued, otherwise the new command will appear to fail.

Program/Write to Buffer and Program Status (Bit 4)

The Program/Write to Buffer and Program Status bit is used to identify a Program failure or a Write to Buffer and Program failure. Bit 4 should be read once the Program/Erase Controller Status bit is High (Program/Erase controller inactive).

When bit 4 is set to ‘0’ the memory has successfully verified that the device has programmed correctly. When bit 4 is set to ‘1’ the device has failed to verify that the data has been programmed correctly.

Once set to ‘1’, the Program Status bit can only be reset to ‘0’ by a Clear Status Register command or a hardware reset. If set to 1 it should be reset before a new PROGRAM, ERASE, or WRITE TO BUFFER AND PROGRAM command is issued, otherwise the new command will appear to fail.

PEN Status (Bit 3)

The PEN Status bit can be used to identify when a PROGRAM, ERASE, or WRITE TO BUFFER AND PROGRAM operation has been attempted when PEN is LOW.

When bit 3 is set to 0, no PROGRAM, ERASE, or WRITE TO BUFFER AND PROGRAM operation has been attempted with PEN LOW since the last CLEAR STATUS REGISTER command or hardware reset.

When bit 3 is set to 1, a PROGRAM, ERASE, or WRITE TO BUFFER AND PROGRAM operation has been attempted with PEN LOW.

Once set to 1, bit 3 can only be reset by a CLEAR STATUS REGISTER command or a hardware reset. If set to 1, it should be reset before a new PROGRAM, ERASE, or WRITE TO BUFFER AND PROGRAM command is issued. Otherwise the new command will appear to fail.

Program Suspend Status (Bit 2)

The program suspend status bit indicates that a PROGRAM or WRITE TO BUFFER AND PROGRAM operation has been suspended and is waiting to be resumed. The program suspend status should be considered valid only when the program/erase controller status bit is set to 1 (program/erase controller inactive). After a PROGRAM/ERASE SUSPEND command is issued, the memory may still complete the operation rather than entering the suspend mode.

When the program suspend status bit is set to '0', the program/erase controller is active or has completed its operation. When the bit is set to 1, a PROGRAM/ERASE SUSPEND command has been issued and the memory is waiting for a PROGAM/ERASE RESUME command.

When a PROGRAM/ERASE RESUME command is issued the program suspend status bit returns to 0.

Block Protection Status (Bit 1)

The block protection status bit can be used to identify if a PROGRAM, ERASE, or WRITE TO BUFFER AND PROGRAM operation has tried to modify the contents of a protected block.

When the block protection status bit is set to 0, no PROGRAM, ERASE, or WRITE TO BUFFER AND PROGRAM operation has been attempted to protected blocks since the last CLEAR STATUS REGISTER command or hardware reset. When the block protection status bit is set to 1, a PROGRAM, ERASE, or WRITE TO BUFFER AND PROGRAM operation has been attempted on a protected block.

Once set to 1, the block protection status bit can only be reset LOW by a CLEAR STATUS REGISTER command or a hardware reset. If set to 1, it should be reset before a new PROGRAM, ERASE, or WRITE TO BUFFER AND PROGRAM command is issued. Otherwise the new command will appear to fail.

Reserved (Bit 0)

This bit is reserved for future use.

Common Flash Interface (CFI)

The common Flash interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query command (RCFI) is issued the device enters CFI Query mode and the data structure is read from the memory. The following tables show the addresses used to retrieve the data.

Table 15: Query Structure Overview

Offset	Sub-section name	Description	
00h	0020h	Manufacturer code	Micron
01h	883A 8839 8838 8837	Device code	M58BW16FT (top) M58BW16FB (bottom) M58BW32FT (top) M58BW32FB (bottom)
10h	CFI query identification string	Command set ID and algorithm data offset	
1Bh	System interface information	Device timing and voltage information	
27h	Device geometry definition	Flash memory layout	
P(h)[1]	Primary algorithm-specific extended query table	Additional information specific to the primary algorithm (optional)	
A(h)[2]	Alternate algorithm-specific extended query table	Additional information specific to the alternate algorithm (optional)	

Notes:
1. Offset 15h defines P which points to the primary algorithm extended query address table.
2. Offset 19h defines A which points to the alternate algorithm extended query address table.

Table 16: CFI - Query Address and Data Output

Address A0-Amax	Data		Instruction
10h	51h	"Q"	51h; "Q" Query ASCII string 52h; "R" 59h; "Y"
11h	52h	"R"	
12h	59h	"Y"	
13h	03h		Primary vendor: Command set and control interface ID code
14h	00h		
15h	35h (M58BW16F) 39h (M58BW32F)		Primary algorithm extended query address table: P(h)
16h	00h		
17h	00h		Alternate vendor: Command set and control interface ID code
18h	00h		

Table 16: CFI - Query Address and Data Output (Continued)

Address A0-Amax	Data	Instruction
19h	00h	Alternate algorithm extended query address table
1Ah	00h	

Notes: 1. The x 8 or byte address and the x 16 or word address mode are not available.
2. Query data are always presented on DQ7-DQ0. DQ31-DQ8 are set to '0'.

Table 17: CFI - Device Voltage and Timing Specification

Address A0-Amax	Data	Description	Value
1Bh	27h[1]	V_{DD} min	2.7 V
1Ch	36h[1]	V_{DD} max	3.6 V
1Dh	xxxx xxxxh	Reserved	
1Eh	xxxx xxxxh	Reserved	
1Fh	04h	2^n µs typical for word, double word program	16 µs
20h	xxxx xxxxh	Reserved	
21h	0Ah	2^n ms, typical time-out for Erase Block	1 s
22h	xxxx xxxxh	Reserved	
23h	xxxx xxxxh	Reserved	
24h	xxxx xxxxh	Reserved	
25h	xxxx xxxxh	Reserved	
26h	xxxx xxxxh	Reserved	

Note: 1. 1 Bits are coded in binary code decimal, bit7 to bit4 are scaled in Volts and bit3 to bit0 in mV.

Table 18: M58BW16F Device Geometry Definition

Address A0-Amax	Data	Description	Value
27h	15h	2^n number of bytes memory size	2 Mbytes
28h	03h	Device interface sync./async.	x 32
29h	00h	Organization sync./async.	Asynchronous
2Ah	00h	Maximum number of byte in multi-byte program = 2^n	32 bytes
2Bh	00h		
2Ch	02h	Bit7-0 = number of Erase Block regions in device	2
2Dh	1Eh	Number (n-1) of Erase Blocks of identical size; n=31	31 blocks
2Eh	00h		
2Fh	00h	Erase Block region information x 256 bytes per Erase Block (64 Kbytes)	512 Kbits
30h	01h		
31h	07h	Number (n-1) of Erase Blocks of identical size; n=8	8 blocks
32h	00h		
33h	20h	Erase Block region information x 256 bytes per Erase Block (8 Kbytes)	64 Kbits
34h	00h		

Note: 1. This table is valid for top configuration. For bottom configuration, refer to the M58BW16F Bottom Boot Block Addresses table.

Table 19: M58BW16F Extended Query Information

Address 0ffset	Address Amax-A0	Data (hex)		Description
(P)h	35h	50	P	Query ASCII string - extended table
(P+1)h	36h	52	R	
(P+2)h	37h	49	Y	
(P+3)h	38h	31h		Major revision number
(P+4)h	39h	31h		Minor revision number
(P+5)h	3Ah	86h		Optional feature: (1=yes, 0=no) bit0, Chip Erase supported (0= no) bit1, Suspend Erase supported (1=yes) bit2, Suspend Program supported (1=yes) bit3, Lock/Unlock supported (0=no) bit4, Queue Erase supported (0=no) bit5, Instant individual block locking (0=no) bit6, Protection bits supported (0=no) bit7, Page Read supported (1=yes) bit8, Synchronous Read supported (1=yes) Bit9, Reserved
(P+6)h	3Bh	01h		Synchronous Read supported
(P+7)h	3Ch	00h		
(P+8)h	3Dh	00h		
(P+9)h	3Eh	01h		Function allowed after Suspend: Program allowed after Erase Suspend (1=yes) Bit 7-1 reserved for future use
(P+A)h-(P+D)h	3Fh-42h	Reserved		
(P+13)h-(P+40)h	48h-7Fh	Reserved		
(P+41)h	80h	xxxx xxxxh		Unique device ID - 1 (16 bits)
(P+42)h	81h	xxxx xxxxh		Unique device ID - 2 (16 bits)
(P+43)h	82h	xxxx xxxxh		Unique device ID - 3 (16 bits)
(P+44)h	83h	xxxx xxxxh		Unique device ID - 4 (16 bits)

Table 20: M58BW32F Device Geometry Definition

Address A0-Amax	Data	Description	Value
27h	16h	2^n number of bytes memory size	4 Mbytes
28h	03h	Device interface sync./async.	x 32
29h	00h	Organization sync./async.	Asynchronous
2Ah	05h	Maximum number of byte in multi-byte program = 2^n	32 bytes
2Bh	00h		
2Ch	03h	Bit7-0 = number of Erase Block regions in device	3
2Dh	3Dh	Number (n-1) of Erase Block regions of identical size; n = 61	62 blocks
2Eh	00h		
2Fh	00h	Erase Block region information x 256 bytes per Erase Block (64 Kbytes)	512 Kbits
30h	01h		
31h	07h	Number (n-1) of Erase blocks of identical size; n = 8	8 blocks
32h	00h		
33h	20h	Erase Block region information x 256 bytes per Erase Block (8 Kbytes)	64 Kbits
34h	00h		
35h	03h	Number (n-1) of Erase Block of identical size; n = 8	8 blocks
36h	00h		
37h	40h	Erase Block region information x 256 bytes per Erase block (16 Kbytes)	128 Kbits
38h	00h		

Note: 1. This table is valid for top configuration. For bottom configuration, refer to the M58BW32F Bottom Boot Block Addresses table.

Table 21: M58BW32F Extended Query Information

Address Offset	Address Amax-A0	Data (hex)		Description
(P)h	39h	50	P	Query ASCII string - extended table
(P+1)h	3Ah	52	R	
(P+2)h	3Bh	49	Y	
(P+3)h	3Ch	31h		Major revision number
(P+4)h	3Dh	31h		Minor revision number
(P+5)h	3Eh	86h		Optional feature: (1=yes, 0=no) bit0, Chip Erase supported (0= no) bit1, Suspend Erase supported (1=yes) bit2, Suspend Program supported (1=yes) bit3, Lock/Unlock supported (0=no) bit4, Queue Erase supported (0=no) bit5, Instant individual block locking (0=no) bit6, Protection bits supported (0=no) bit7, Page Read supported (1=yes) bit8, Synchronous Read supported (1=yes) Bit 9, Reserved
(P+6)h	3Fh	01h		Synchronous Read supported
(P+7)h	40h	00h		
(P+8)h	41h	00h		
(P+9)h	42h	01h		Function allowed after Suspend: Program allowed after Erase Suspend (1=yes) Bit 7-1 reserved for future use
(P+A)h-(P+D)h	43h-46h	Reserved		
(P+13)h-(P+40)h	4Ch-7Fh	Reserved		
(P+41)h	80h	xxxx xxxxh		Unique device ID - 1 (16 bits)
(P+42)h	81h	xxxx xxxxh		Unique device ID - 2 (16 bits)
(P+43)h	82h	xxxx xxxxh		Unique device ID - 3 (16 bits)
(P+44)h	83h	xxxx xxxxh		Unique device ID - 4 (16 bits)

Table 22: Protection Register Information

Address A0-Amax	Data		Instruction	Value	
	M58BW16FT M58BW16FB	M58BW32FT M58BW32FB		M58BW16FT M58BW16FB	M58BW32FT M58BW32FB
(P+E)h	0x02 0x02	0x01 0x01	Number of Protection register field in JEDEC ID space, Block region information X256 bytes	2 x 64 Kb 2 x 64 Kb	1 x 128 Kb 1 x 128 Kb
(P+F)h	0x01 0xFE	0x01 0xFE	Protection field: this field describes user-available OTP Protection Register bytes. Bits 7-0=physical low address Bits 15-8=physical high address Bits 23-16='n', 2n=Factory pre-programmed bytes Bits 31-24='n', 2n=user programmable bytes	-	-
(P+10)h	0x01 0xFE	0x01 0xFE		-	-
(P+11)h	0x0 0x0	0x0 0x0		-	-
(P+12)h	0x12 0x12	0x12 0x12		2 x 64 Kb 2 x 64 Kb	1 x 128 Kb 1 x 128 Kb

Maximum Rating

Stressing the device above the ratings listed in the Absolute maximum ratings table, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 23: Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_{BIAS}	Temperature under bias	–40	125	°C
T_{STG}	Storage temperature	–55	155	°C
V_{IO}	Input or output voltage	–0.6	V_{DDQ} + 0.6 V_{DDQIN} + 0.6	V
V_{DD}, V_{DDQ}, V_{DDQIN}	Supply voltage	–0.6	4.2	V

Table 24: Data Retention

Power Supply V_{DD}	Unit	External Temperature		Unit
		25 °C	125 °C	
0	V	20	7	Years
2.5	V	–	25	Years
2.7	V	–	15	Years

Program and Erase Times and Endurance Cycles

Table 25: Program and Erase Times and Endurance Cycles[1]

Parameters	M58BW16F			M58BW32F			Unit
	Min	Typ	Max	Min	Typ	Max	
Full Chip Program		15	20		15	20	s
Double Word Program		15	35		15	35	µs
512 Kbit Block Erase		1	2		1	2	s
128 Kbit Block Erase		0.8	1.6		0.8	1.6	s
64 Kbit Block Erase		0.6	1.2		0.6	1.2	s
Erase all main blocks		45	60		30	50	s
Program Suspend Latency time			10			10	µs
Erase Suspend Latency time			30			30	µs
Minimum effective erase time[2]			40			40	µs
Program/Erase cycles (per block)			100,000			100,000	cycles

Notes:
1. T_A = –40 to 125 °C, V_{DD} = 2.7 V to 3.6 V, V_{DDQ} = 2.6 V to V_{DD}.
2. The minimum effective erase time is defined as the minimum time required between the last Erase Resume command and the next Erase Suspend command for the internal Flash memory Program/Erase controller to be able to execute its algorithm.

DC and AC Parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in Operating and AC measurement conditions table. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

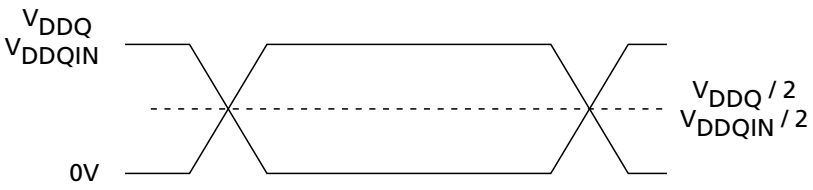
Operating Conditions and Capacitance

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in Operating and AC measurement conditions table. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 26: Operating and AC Measurement Conditions

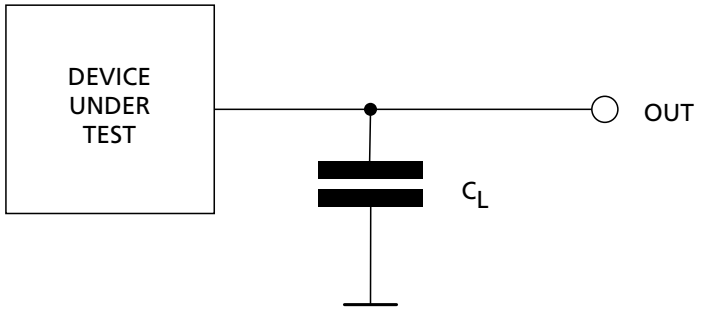
Parameter	M58BW16F, M58BW32F				Units
	45 ns		55 ns		
	Min	Max	Min	Max	
Supply voltage (V_{DD})	2.7	3.6	2.5	3.3	V
Input/output supply voltage (V_{DDQ})	2.4	3.6	2.4	3.3	V
Ambient temperature (T_A) Grade 3	–40	125	–40	125	°C
Load capacitance (C_L)	30		30		pF
Clock rise and fall times		3		3	ns
Input rise and fall times		3		3	ns
Input pulses voltages	0 to V_{DDQ}		0 to V_{DDQ}		V
Input and output timing ref. voltages	$V_{DDQ/2}$		$V_{DDQ/2}$		V

Figure 15: AC Measurement Input/Output Waveform



Note: 1. $V_{DD} = V_{DDQ}$.

Figure 16: AC Measurement Load Circuit



C_L includes JIG capacitance

Table 27: Device Capacitance

Symbol	Parameter	Test condition	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V	6	8	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V	8	12	pF

Notes: 1. T_A = 25 °C, f = 1 MHz.
2. Sampled only, not 100% tested.

DC Characteristics

Symbol	Parameter	Test Condition	Typ	Max	Unit	Notes
I_{LI}	Input Leakage current	0 V≤ V_{IN} ≤ V_{DDQIN}		±1	µA	
I_{LO}	Output Leakage current	0 V ≤ V_{OUT} ≤ V_{DDQ}		±5	µA	
I_{DD}	Supply current (Random Read)	E# = V_{IL}, G# = V_{IH}, f_{add} = 6 MHz		25	mA	
I_{DDP-UP}	Supply current (power-up)			20	mA	1
I_{DDB}	Supply current (Burst Read)	E# = V_{IL}, G# = V_{IH}, f_{clock} = 75 MHz		50	mA	
I_{DD1}	Supply current (Standby)	E# = RP# = V_{DD} ± 0.2 V		150	µA	2
I_{DD2}	Supply current (Program or Erase)	Program, Erase in progress		30	mA	
I_{DD3}	Supply current (Erase/Program Suspend)	E# = V_{IH}		150	µA	
I_{DD4}	Supply current (Standby Disable)		5	10	mA	
V_{IL}	Input Low voltage			$0.2V_{DDQIN}$	V	
V_{IH}	Input High voltage (for DQ lines)			V_{DDQ} + 0.3	V	
V_{IH}	Input High voltage (for input only lines)			3.6	V	
V_{OL}	Output Low voltage	I_{OL} = 100 µA		0.1	V	
V_{OH}	Output High voltage CMOS	I_{OH} = –100 µA			V	
V_{LKO}	V_{DD} supply voltage (Erase and Program lockout)			2.2	V	

Notes:
1. I_{DDP-UP} is the current needed from the device until RP goes to its logic high level when the power supply is stable (t_{VDHPH}). See the Reset, Power-down and Power-up AC waveforms - Control pins Low figure and the Reset, Power-down and Power-up AC waveforms - Control pins toggling.
2. The Standby mode can be disabled by setting the Standby Disable bit (M14) of the Burst Configuration Register to ‘1’.

Asynchronous Bus Read AC Characteristics

Figure 17: Asynchronous Bus Read AC Waveforms

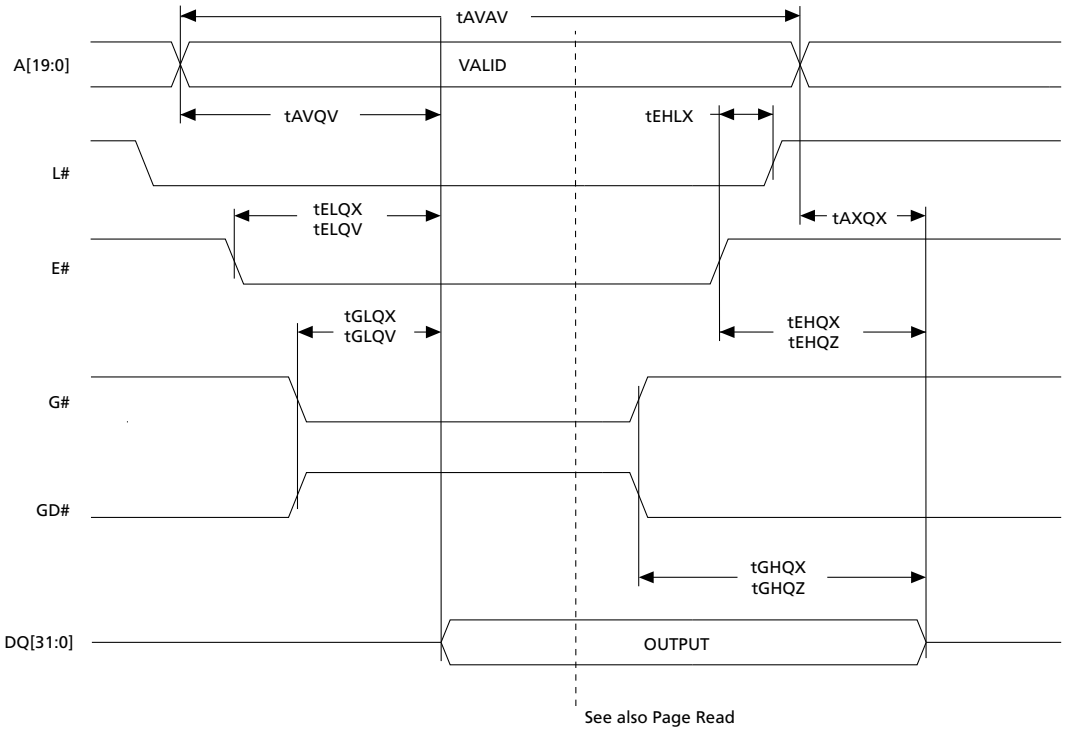


Figure 18: Asynchronous Latch Controlled Bus Read AC Waveforms

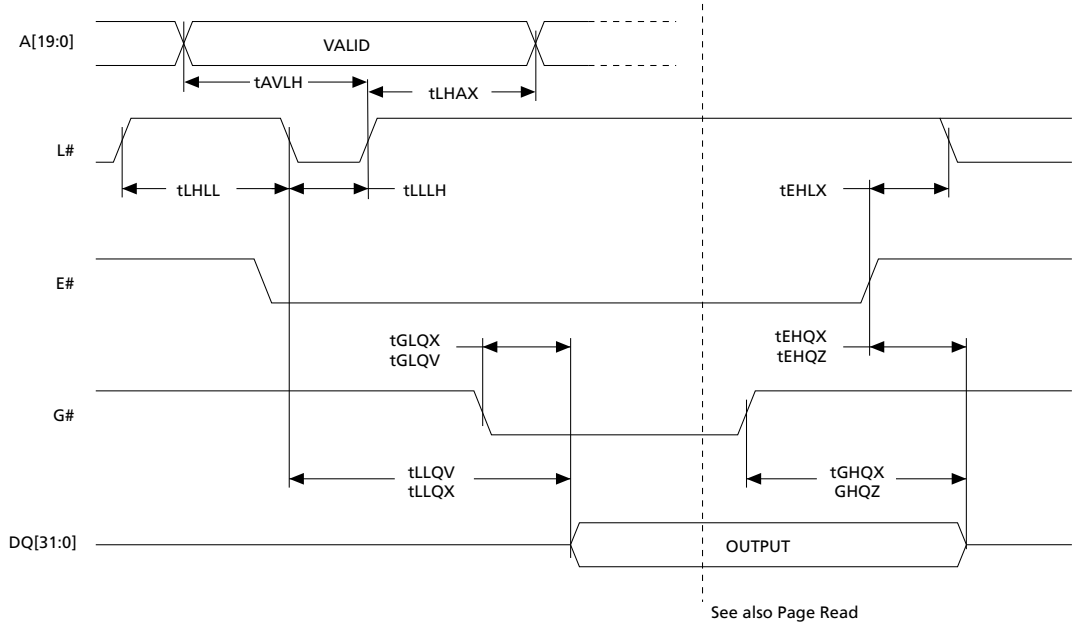


Figure 19: Asynchronous Chip Enable Controlled Bus Read AC Waveforms

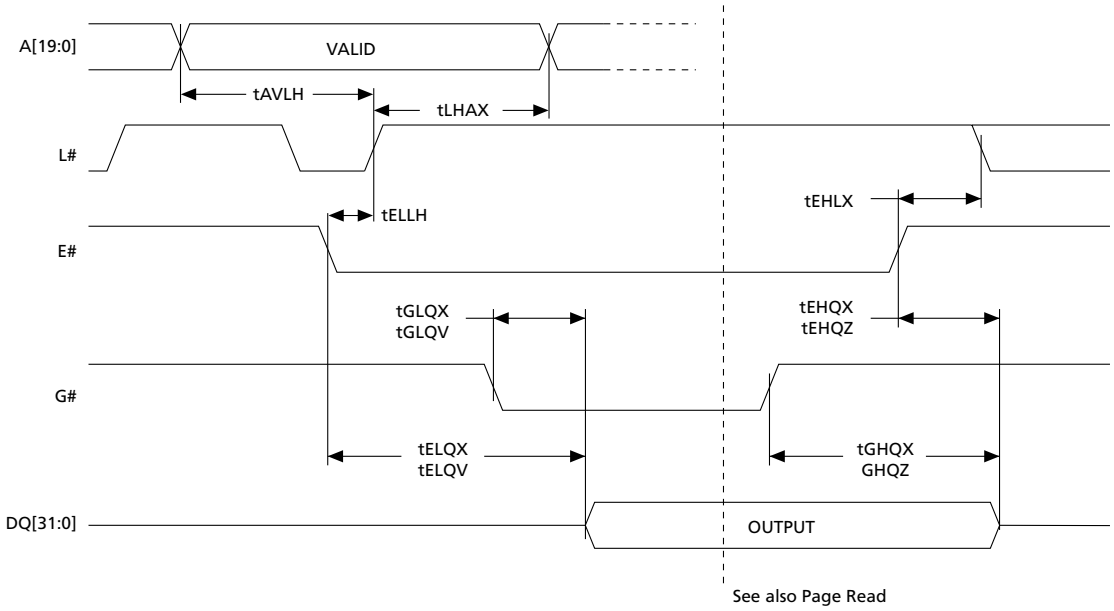


Figure 20: Asynchronous Address Controlled Bus Read AC Waveforms

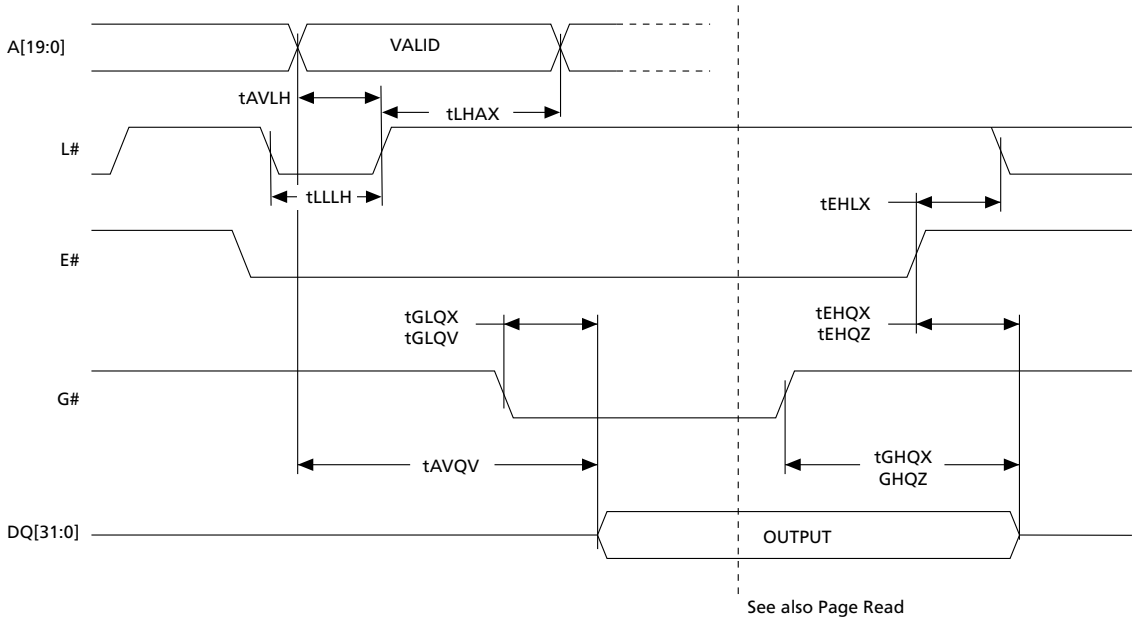


Table 28: Asynchronous Bus Read AC Characteristics

Symbol	Parameter	Test condition	Min/Max	M58BWxxF		Unit	Notes
				45	55		
t_{AVAV}	Address Valid to Address Valid	E# = V_{IL}, G# = V_{IL}	Min	45	55	ns	
t_{AVQV}	Address Valid to Output Valid	E# = V_{IL}, G# = V_{IL}	Max	45	55	ns	
t_{AXQX}	Address Transition to Output Transition	L# = V_{IL}, G# = V_{IL}	Min	0	0	ns	
t_{EHLX}	Chip Enable HIGH to Latch Enable Transition		Min	0	0	ns	
t_{EHQX}	Chip Enable HIGH to Output Transition	G# = V_{IL}	Min	0	0	ns	
t_{EHQZ}	Chip Enable HIGH to Output Hi-Z	G# = V_{IL}	Max	20	20	ns	
t_{ELQV}	Chip Enable LOW to Output Valid	G# = V_{IL}	Max	45	55	ns	1
t_{GHQX}	Output Enable HIGH to Output Transition	E# = V_{IL}	Min	0	0	ns	
t_{GHQZ}	Output Enable HIGH to Output Hi-Z	E# = V_{IL}	Max	15	15	ns	
t_{GLQV}	Output Enable LOW to Output Valid	E# = V_{IL}	Max	15	15	ns	
t_{GLQX}	Output Enable LOW to Output Transition	E = V_{IL}	Min	0	0	ns	
t_{LHAX}	Latch Enable HIGH to Address Transition	E# = V_{IL}	Min	5	5	ns	
t_{LHLL}	Latch Enable HIGH to Latch Enable LOW		Min	10	10	ns	
t_{LLLH}	Latch Enable LOW to Latch Enable HIGH	E# = V_{IL}	Min	10	10	ns	
t_{LLQV}	Latch Enable LOW to Output Valid Chip Enable LOW to Output Valid	E# = V_{IL}, G# = V_{IL}	Max	45	55	ns	
t_{LLQX}	Latch Enable LOW to Output Transition	E# = V_{IL}, G# = V_{IL}	Min	0	0	ns	
t_{ELQX}	Chip Enable LOW to Output Transition	L# = V_{IL}, G# = V_{IL}	Min	0	0	ns	
t_{AVLH}	Address Valid to Latch Enable LOW		Min	10	10	ns	
t_{ELLH}	Chip Enable LOW to Latch Enable HIGH		Min	10	10	ns	

Note: 1. Output Enable G# may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of Chip Enable E# without increasing t_{ELQV}.

Asynchronous Page Read AC Characteristics

Figure 21: Asynchronous Page Read AC Waveforms

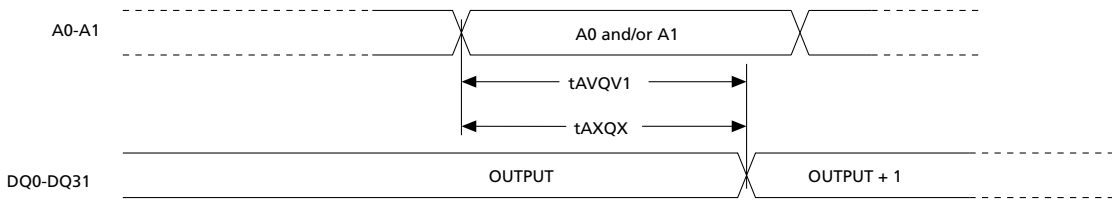


Table 29: Asynchronous Page Read AC Characteristics

Symbol	Parameter	Test Conditions	Max/Min	M58BWxxF		Unit
				45	55	
t_{AVQV1}	Address Valid to Output Valid	E# = V_{IL}, G# = V_{IL}	Max	25	25	ns
t_{AXQX}	Address Transition to Output Transition	E# = V_{IL}, G# = V_{IL}	Min	0	0	ns

Note: 1. For other timings see the Asynchronous Bus Read AC characteristics table.

Asynchronous Write AC Characteristics

Figure 22: Asynchronous Write E# - Controlled AC Waveforms

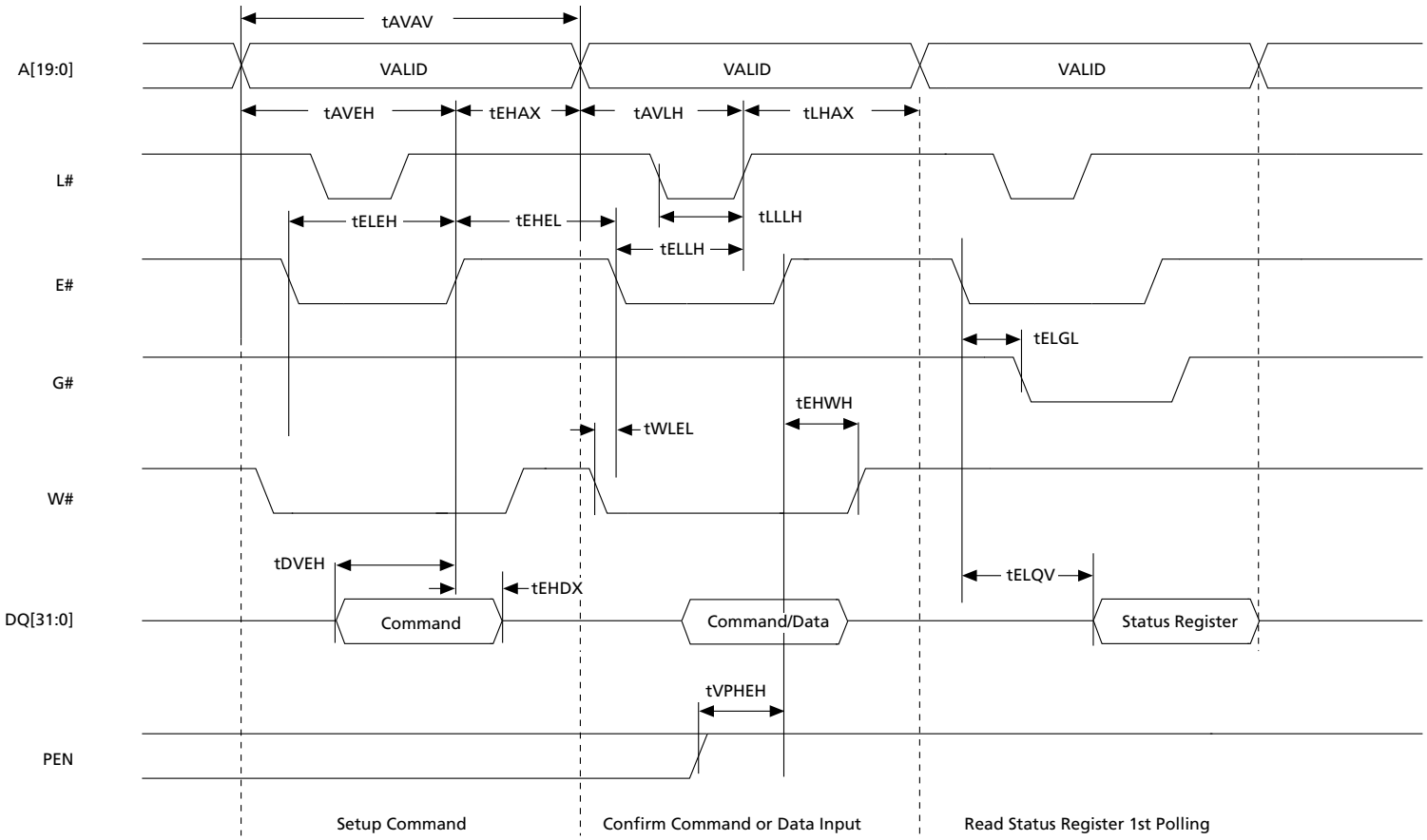


Table 30: Asynchronous Write E# - Controlled AC Characteristics

Symbol	Parameter	Test condition	Max/Min	M58BWxxF		Unit
				45	55	
t_{AVAV}	Address Valid to Address Valid		Min	45	55	ns
t_{AVEH}	Address Valid to Chip Enable High		Min	25	30	ns
t_{EHAX}	Chip Enable High to Address Transition		Min	0	0	ns
t_{ELEH}	Chip Enable Low to Chip Enable High	W# = V_{IL}	Min	25	30	ns
t_{EHEL}	Chip Enable High to Chip Enable Low		Min	20	20	ns
t_{DVEH}	Data Input Valid to Chip Enable High	W# = V_{IL}	Min	25	30	ns
t_{EHDX}	Chip Enable High to Input Transition	W# = V_{IL}	Min	0	0	ns
t_{AVLH}	Address Valid to Latch Enable High		Min	10	10	ns
t_{LHAX}	Latch Enable High to Address Transition		Min	5	5	ns
t_{LLLH}	Latch Enable Low to Latch Enable High		Min	10	10	ns
t_{ELLH}	Chip Enable Low to Latch Enable High		Min	10	10	ns
t_{EHGL}	Chip Enable High to Output Enable Low		Min	150	150	ns
t_{WLEL}	Write Enable Low to Chip Enable Low		Min	0	0	ns
t_{EHWH}	Chip Enable High to Write Enable High		Min	0	0	ns
t_{ELQV}	Chip Enable Low to Output Valid	G# = V_{IL}	Max	45	55	ns
t_{VPHEH}	PEN High to Chip Enable High		Min	0	0	ns

Figure 23: Asynchronous Write W# - Controlled AC Waveforms

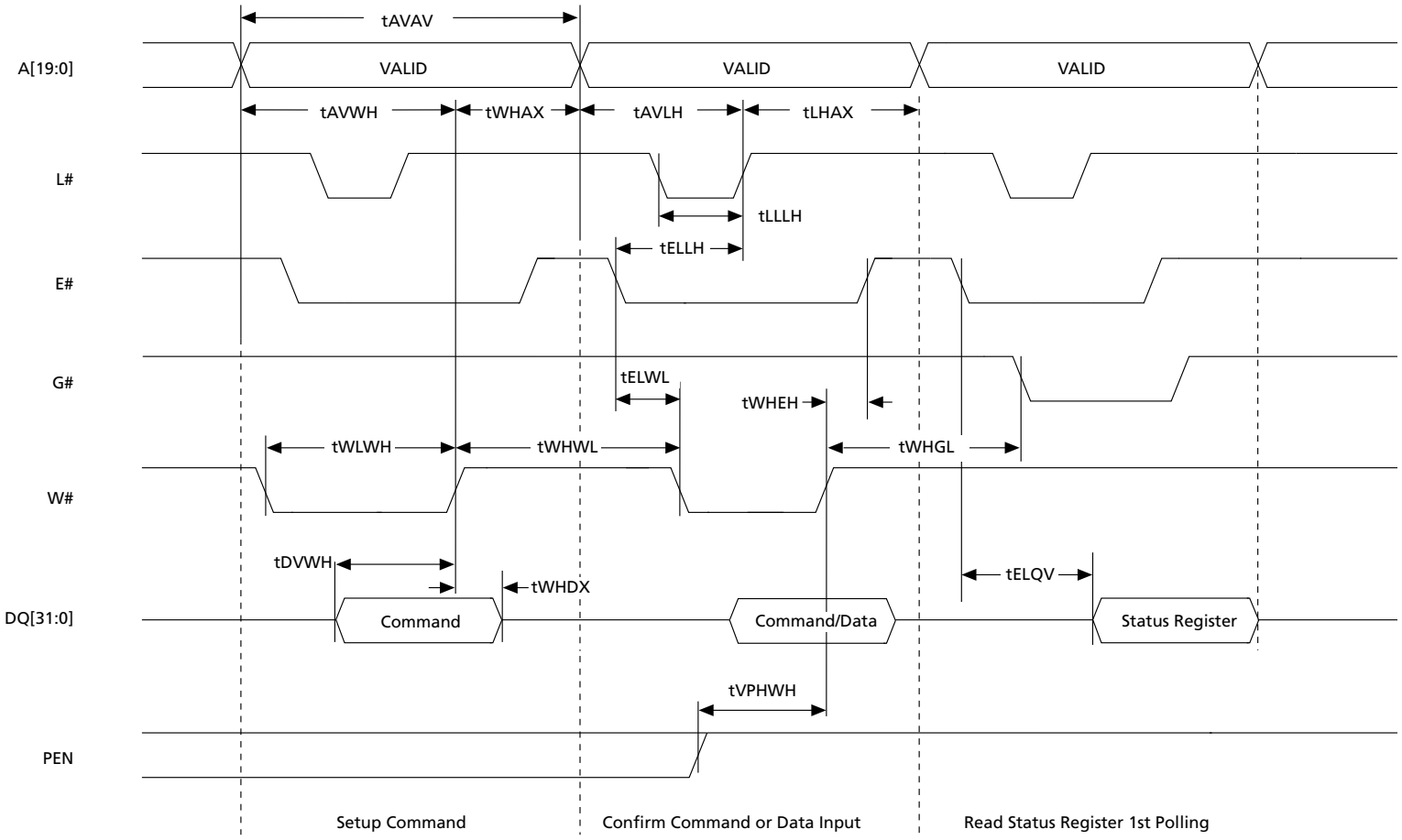
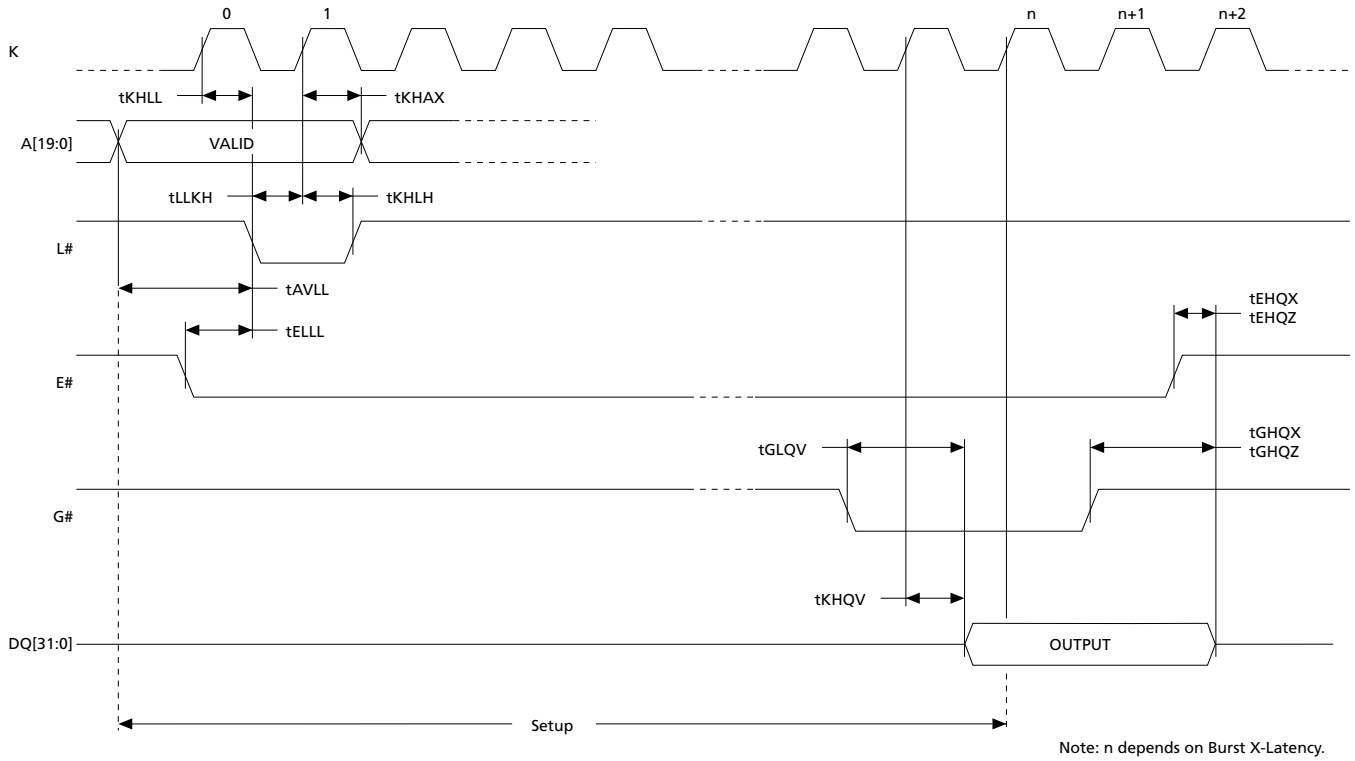


Table 31: Asynchronous Write E# - Controlled AC Characteristics

Symbol	Parameter	Test condition	Max/Min	M58BWxxF		Unit
				45	55	
t_{AVAV}	Address Valid to Address Valid		Min	45	55	ns
t_{AVWH}	Address Valid to Write Enable High	E# = V_{IL}	Min	25	30	ns
t_{WHAX}	Write Enable High to Address Transition		Min	0	0	ns
t_{WLWH}	Write Enable Low to Write Enable High	E# = V_{IL}	Min	25	30	ns
t_{WHWL}	Write Enable High to Write Enable Low		Min	20	20	ns
t_{DVWH}	Data Input Valid to Write Enable High	E# = V_{IL}	Min	25	30	ns
t_{WHDX}	Write Enable High to Input Transition	E# = V_{IL}	Min	0	0	ns
t_{AVLH}	Address Valid to Latch Enable High	E# = V_{IL}	Min	10	10	ns
t_{LHAX}	Latch Enable High to Address Transition	E# = V_{IL}	Min	5	5	ns
t_{LLLH}	Latch Enable Low to Latch Enable High		Min	10	10	ns
t_{ELLH}	Chip Enable Low to Latch Enable High		Min	10	10	ns
t_{ELWL}	Chip Enable Low to Write Enable Low		Min	0	0	ns
t_{WHEH}	Write Enable High to Chip Enable High		Min	0	0	ns
t_{WHGL}	Write Enable High to Output Enable Low		Min	150	150	ns
t_{ELQV}	Chip Enable Low to Output Valid	G# = V_{IL}	Max	45	55	ns
t_{VPHWH}	PEN High to Write Enable High		Min	0	0	ns

Synchronous Burst Read AC Characteristics

Figure 24: Synchronous Burst Read, Latch Enable Controlled (data valid from 'n' clock rising edge)



Note: n depends on Burst X-Latency.

Figure 25: Synchronous Burst Read, Chip Enable Controlled (data valid from 'n' clock rising edge)

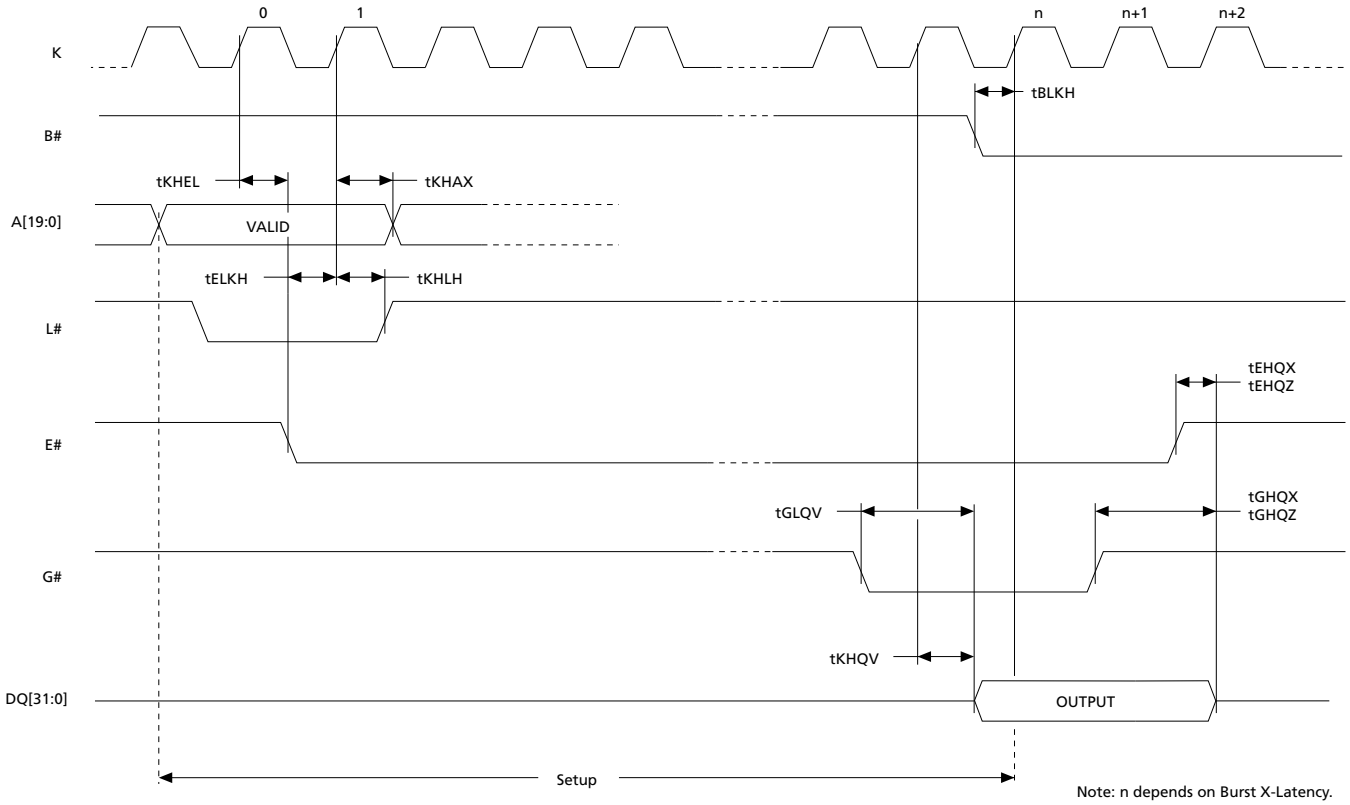


Figure 26: Synchronous Burst Read, Valid Address Transition Controlled (data valid from 'n' clock rising edge)

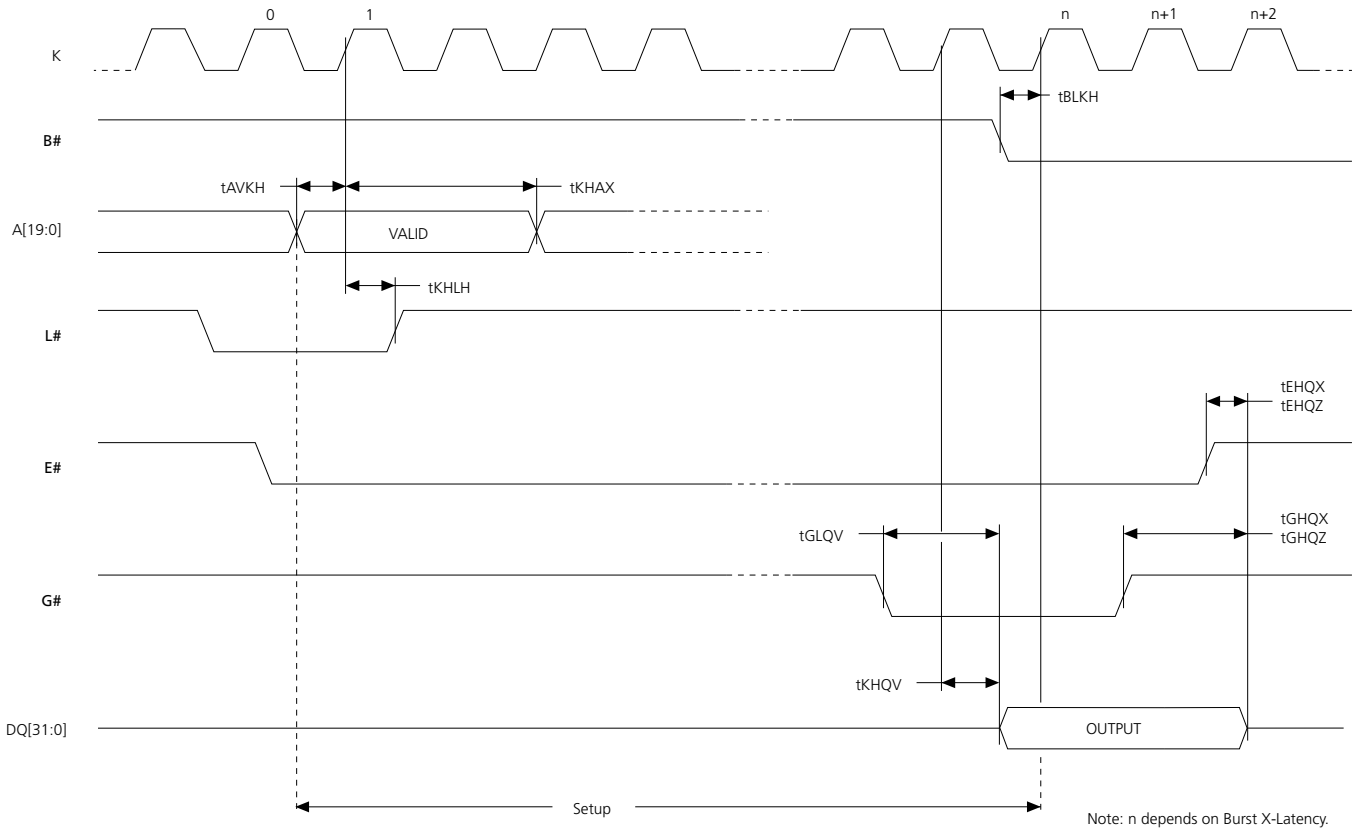
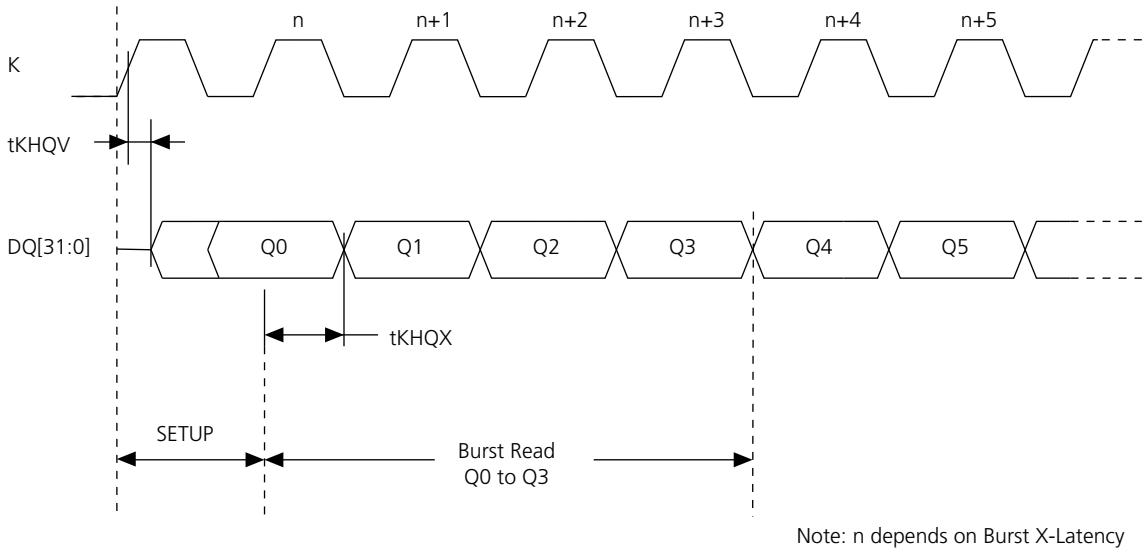
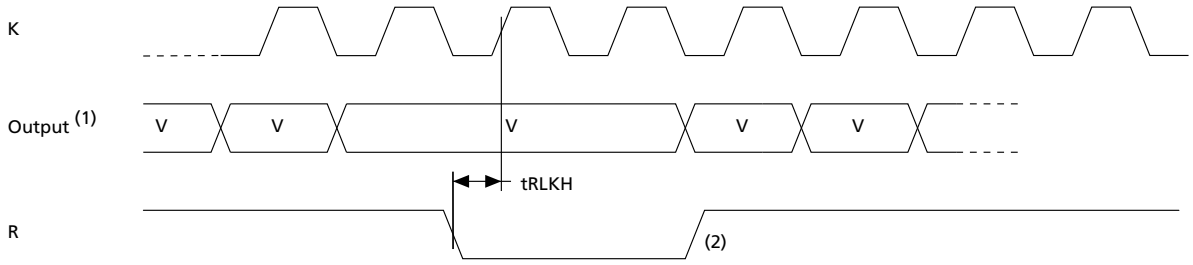


Figure 27: Synchronous Burst Read (data valid from 'n' clock rising edge)



Note: 1. For set up signals and timings see Synchronous Burst Read.

Figure 28: Synchronous Burst Read (valid data ready output)



Notes: 1. Valid Data Ready = Valid Low during valid clock edge.
2. V= Valid output.
3. The internal timing of R follows DQ.

Figure 29: Synchronous Burst Read (Burst Address Advance)

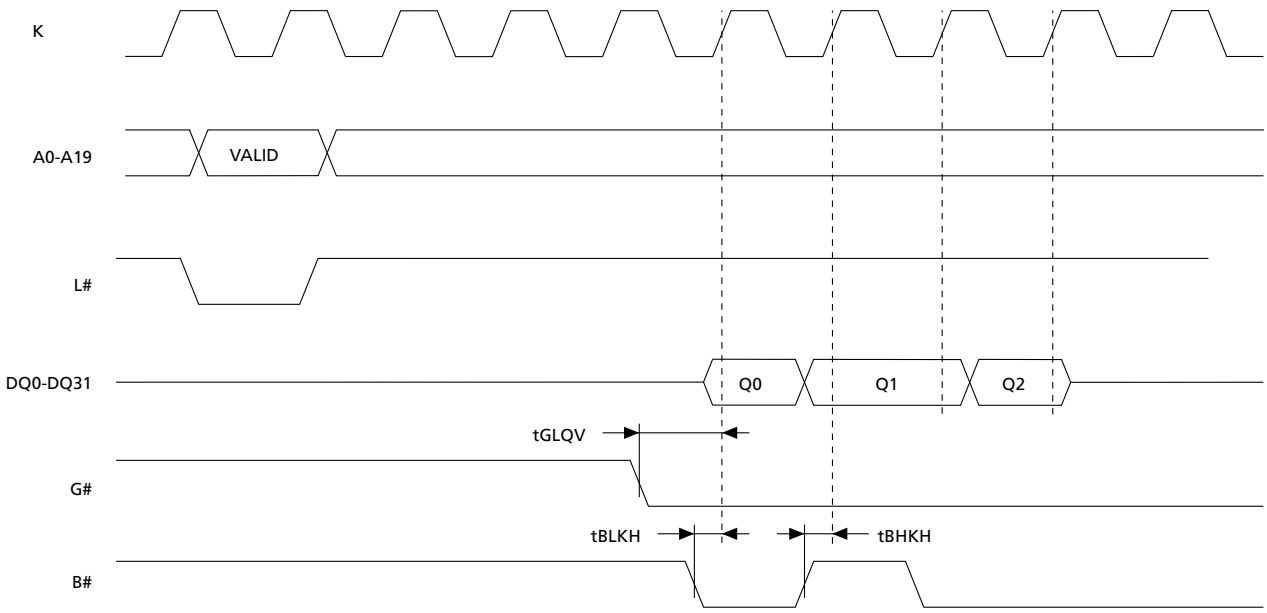


Figure 30: Clock Input AC waveform

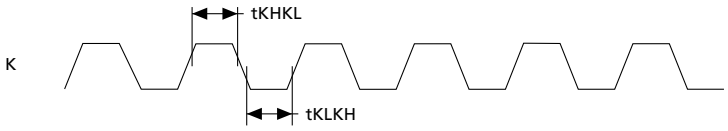


Table 32: Synchronous Burst Read AC Characteristics

Notes apply to the entire table.

Symbol	Parameter	Test condition		Max/Min	M58BWxxF		Unit
					45	55	
f	Clock frequency	X-Latency = 3		Max	40	33	MHz
		X-Latency = 4		Max	56	40	MHz
		X-Latency = 5 or 6		Max	75	56	MHz
t_{AVKH}	Address Valid to Valid Clock Edge	E# = V_{IL}, L# = V_{IL} X-Latency = 3		Min	12	13	ns
		E# = V_{IL}, L# = V_{IL} X-Latency = 4, 5 or 6		Min	6	7	ns
t_{KHKL}	Clock High time			Min	6	6	ns
t_{KLKH}	Clock Low time			Min	6	6	ns
t_{BHKH}	Burst Address Advance High to Valid Clock Edge	E# = V_{IL}, G# = V_{IL}, L# = V_{IH}		Min	8	8	ns
t_{BLKH}	Burst Address Advance Low to Valid Clock Edge	E# = V_{IL}, G# = V_{IL}, L# = V_{IH}		Min	8	8	ns
t_{ELKH}	Chip Enable Low to Valid Clock Edge	L# = V_{IL} X-Latency = 3		Min	12	13	ns
		L# = V_{IL} X-Latency = 4, 5 or 6		Min	6	7	ns
t_{GLQV}	Output Enable Low to Output Valid	E# = V_{IL}, L# = V_{IH}		Max	15	15	ns
t_{KHAX}	Valid Clock Edge to Address Transition	E# = V_{IL}		Min	5	5	ns
t_{KHEL}	Valid Clock Edge to Chip Enable Low	L# = V_{IL}		Min	0	0	ns
t_{KHLL}	Valid Clock Edge to Latch Enable Low	E# = V_{IL}		Min	0	0	ns
t_{KHLH}	Valid Clock Edge to Latch Enable High	E# = V_{IL}		Min	0	0	ns
t_{KHQX}	Valid Clock Edge to Output Transition	E# = V_{IL}, G# = V_{IL}, L# = V_{IH}		Min	2	2	ns
t_{LLKH}	Latch Enable Low to Valid Clock Edge	E# = V_{IL} X-Latency = 3		Min	12	13	ns
		E# = V_{IL} X-Latency = 4, 5 or 6	M58BW16F	Min	6	5	ns
			M58BW32F	Min	6	7	ns
t_{RLKH}	Valid Data Ready Low to Valid Clock Edge	E# = V_{IL}, G# = V_{IL}, L = V_{IH}		Min	6	6	ns
t_{KHQV}	Valid Clock Edge to Output Valid	E# = V_{IL}, G# = V_{IL}, L# = V_{IH}		Max	8	8	ns

Notes: 1. Data output should be read on the valid clock edge.
2. For other timings, see the Asynchronous Bus Read AC characteristics table.

AC and DC Power Characteristics

Figure 31: Power Supply Slope Specification

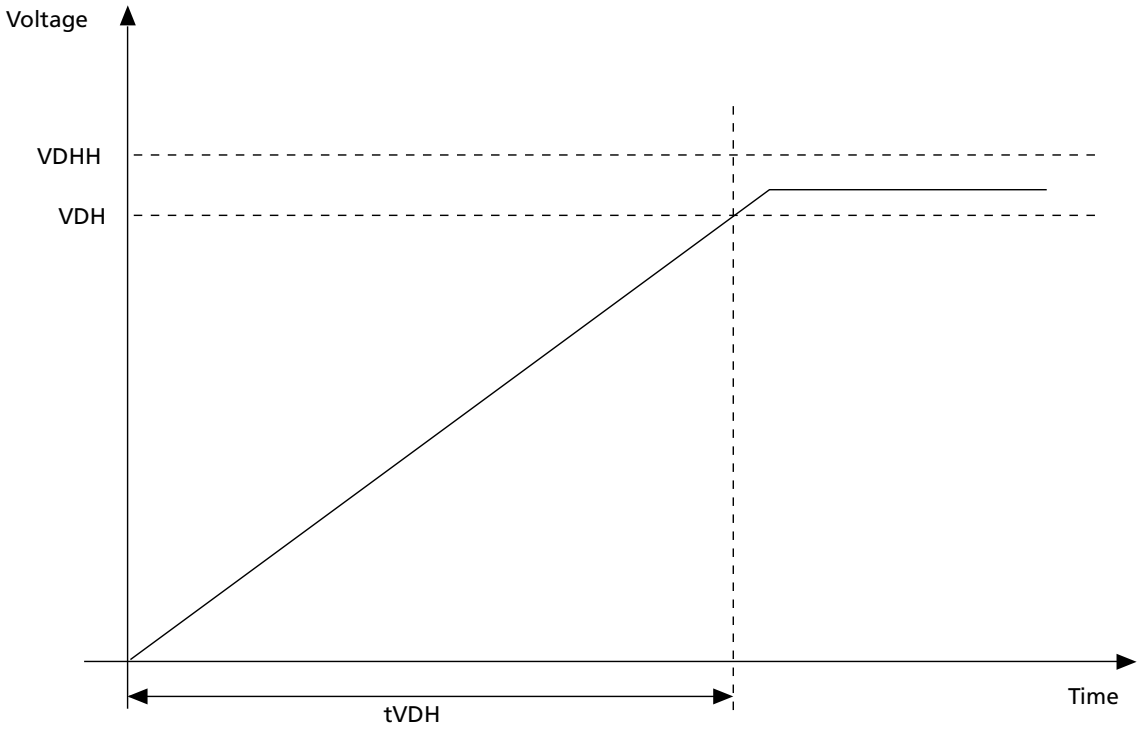


Table 33: Power Supply AC and DC Characteristics

Symbol	Description	Min	Max	Unit
V_{DH}	Minimum value of power supply (V_{DD})[1]	$0.9V_{DD}$		V
V_{DHH}	Maximum value of power supply (V_{DD})		3.6	V
t_{VDH}	Time required from power supply to reach the V_{DH} value	50	50000	µs

Note: 1. This threshold is 90% of the minimum value allowed to V_{DD}.

Figure 32: Reset, Power-down, and Power-up AC Waveforms - Control Pins Low

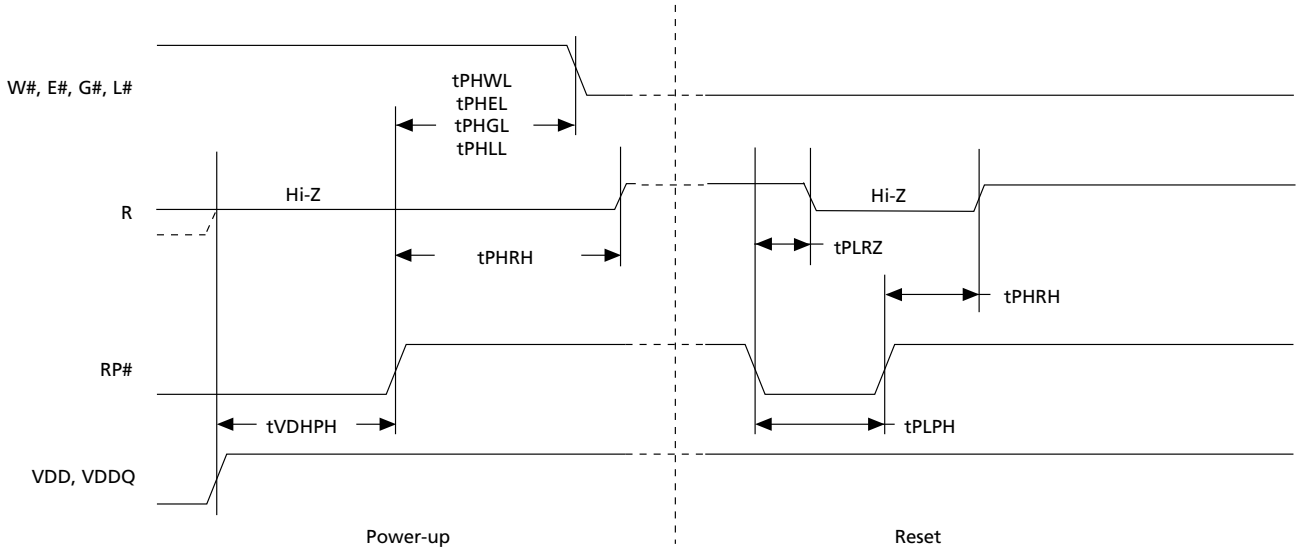


Figure 33: Reset, Power-down, and Power-up AC Waveforms - Control Pins Toggling

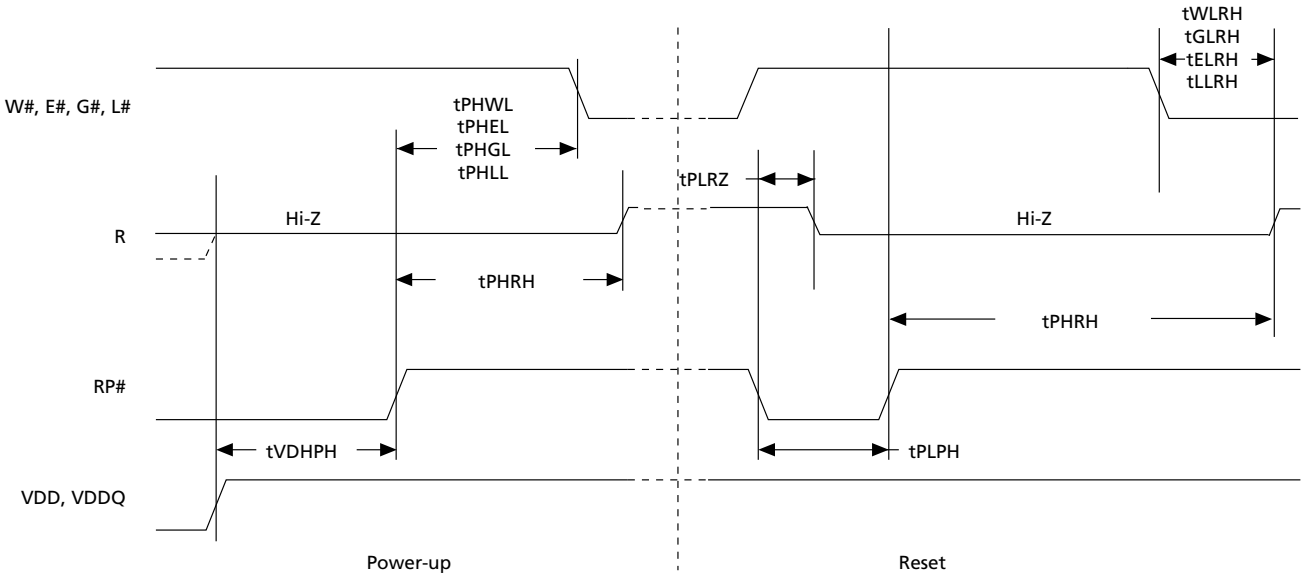


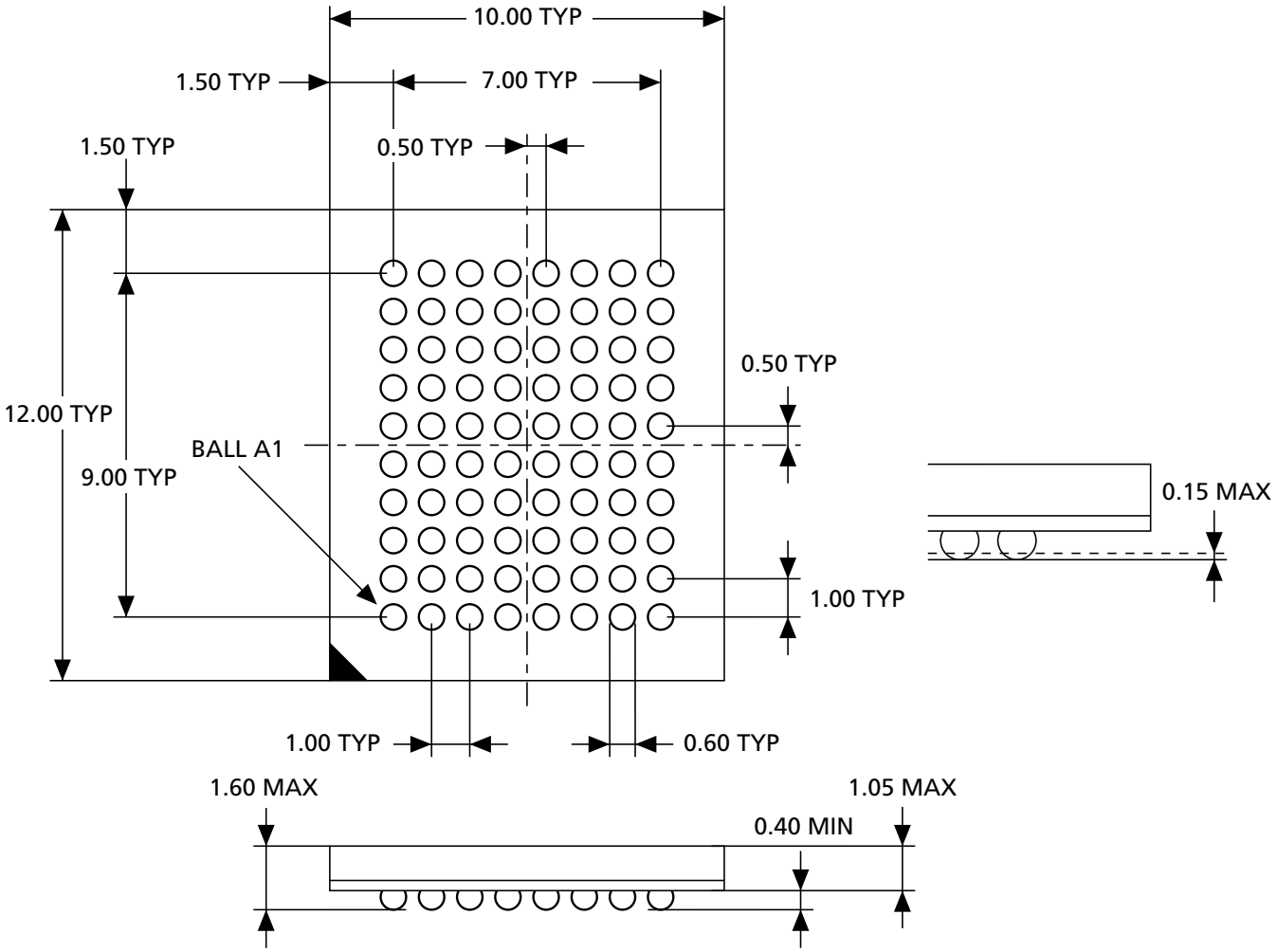
Table 34: Reset, Power-Down, and Power-Up AC Characteristics

Symbol	Parameter	Min	Max	Unit
t_{PHEL}	Reset/Power-down High to Chip Enable Low	50		ns
t_{PHLL}	Reset/Power-down High to Latch Enable Low	50		ns
t_{PHQV}[1]	Reset/Power-down High to Output Valid		95	ns
t_{PHWL}	Reset/Power-down High to Write Enable Low	50		ns
t_{PHGL}	Reset/Power-down High to Output Enable Low	50		ns
t_{PLPH}	Reset/Power-down Low to Reset/Power-down High	100		ns
t_{PHRH}[1]	Reset/Power-down High to Valid Data (Flash) Ready High		95	ns
t_{VDHPH}	Supply voltages High to Reset/Power-down High	50		µs
t_{PLRZ}	Reset/Power-down Low to Data Ready (Flash) High Impedance		80	ns
t_{WLRH}	Write Enable Low to Data Ready (Flash) High Impedance		80	ns
t_{GLRH}	Output Enable Low to Data Ready High Impedance		80	ns
t_{ELRH}	Chip Enable Low to Data Ready (Flash) High Impedance		80	ns
t_{LLRH}	Latch Enable Low to Data Ready (Flash) High Impedance		80	ns

Note: 1. This time is $t_{PHEL} + t_{AVQV}$ or $t_{PHEL} + t_{ELQV}$.

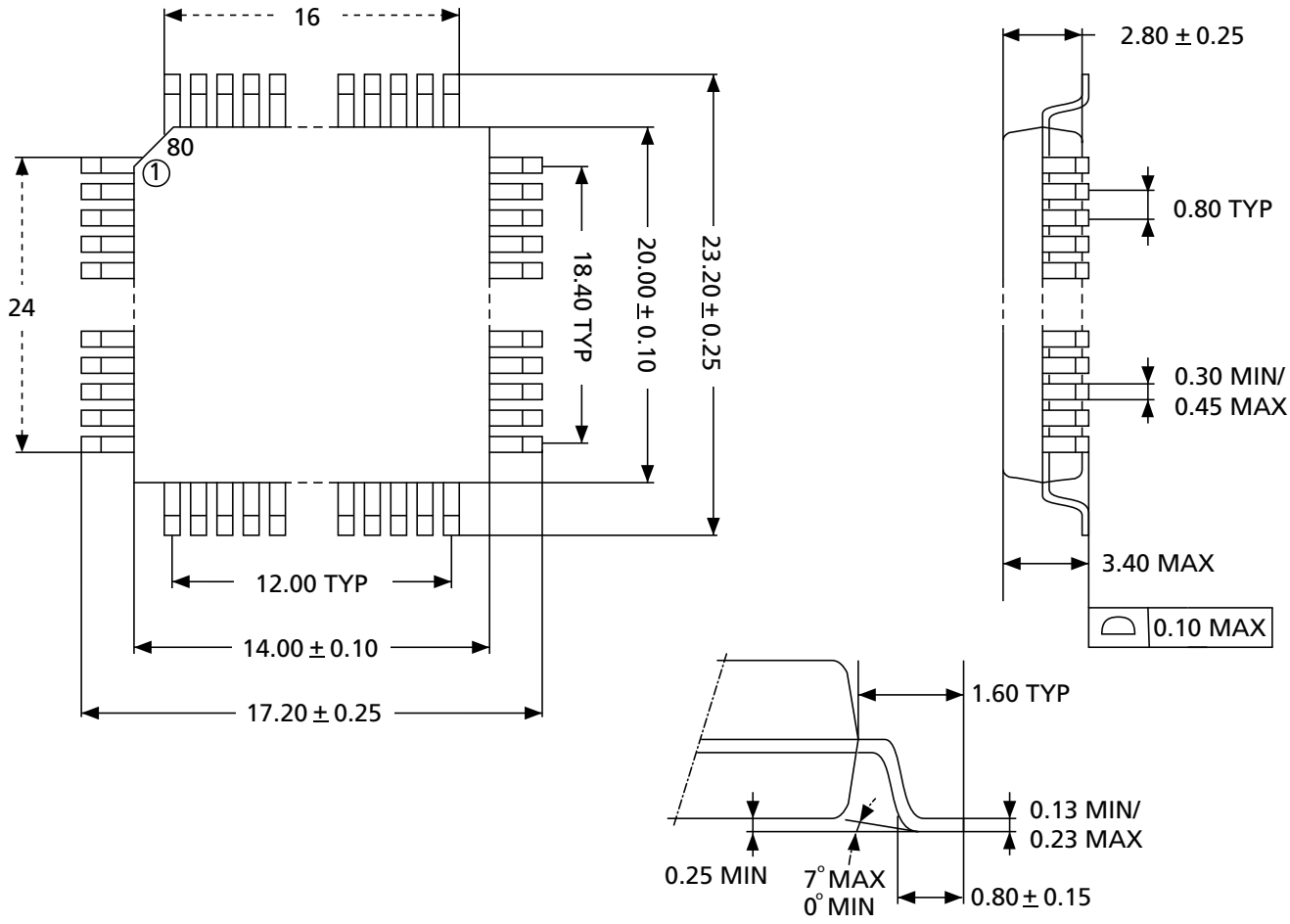
Package Dimensions

Figure 34: 80-Pin LBGA – 10mm x 12mm



Note: 1. All dimensions are in millimeters. Drawing is not to scale

Figure 35: 80-Lead PQFP



Note: 1. All dimensions are in millimeters. Drawing is not to scale.

Revision History

Rev. A – 1/13

- Micron rebrand initial release.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.