

KPS Series, High Voltage, X7R Dielectric, 500 VDC – 630 VDC (Commercial Grade)

Overview

KEMET Power Solutions (KPS) High Voltage stacked capacitors utilize a proprietary lead-frame technology to vertically stack one or two multilayer ceramic chip capacitors into a single compact surface mount package. The attached lead-frame mechanically isolates the capacitor(s) from the printed circuit board, thereby offering advanced mechanical and thermal stress performance. Isolation also addresses concerns for audible microphonic noise that may occur when a bias voltage is applied. A two-chip stack offers up to double the capacitance in the same or smaller design footprint when compared to traditional surface mount MLCC devices. Providing up to 10 mm of board flex capability, KPS Series High Voltage capacitors are environmentally friendly and in compliance with RoHS legislation.

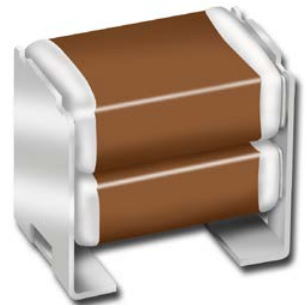
KEMET's KPS Series devices in X7R dielectric exhibit a

predictable change in capacitance with respect to time and voltage, and boast a minimal change in capacitance with reference to ambient temperature. Capacitance change is limited to $\pm 15\%$ from -55°C to $+125^{\circ}\text{C}$. These devices are capable of Pb-Free reflow profiles and provide lower ESR, ESL and higher ripple current capability when compared to other dielectric solutions.

Conventional uses include both snubbers and filters in applications such as switching power supplies and lighting ballasts. Their exceptional performance at high frequencies has made high voltage ceramic capacitors the preferred dielectric choice of design engineers worldwide. In addition to their use in power supplies, these capacitors are widely used in industries related to automotive (hybrid), telecommunications, medical, military, aerospace, semiconductors, and test/diagnostic equipment.

Benefits

- -55°C to $+125^{\circ}\text{C}$ operating temperature range
- Reliable and robust termination system
- EIA 2220 case size
- DC voltage ratings of 500 V and 630 V
- Capacitance offerings ranging from $0.047\ \mu\text{F}$ up to $1.0\ \mu\text{F}$
- Available capacitance tolerances of $\pm 10\%$ and $\pm 20\%$
- Higher capacitance in the same footprint
- Potential board space savings
- Advanced protection against thermal and mechanical stress
- Provides up to 10 mm of board flex capability
- Reduces audible microphonic noise
- Extremely low ESR and ESL
- Pb-Free and RoHS Compliant
- Capable of Pb-Free reflow profiles
- Non-polar device, minimizing installation concerns
- Film alternative



Ordering Information

C	2220	C	105	M	C	R	2	C	7186
Ceramic	Case Size (L"x W")	Specification/ Series	Capacitance Code (pF)	Capacitance Tolerance ¹	Rated Voltage (VDC)	Dielectric	Failure Rate/ Design	Leadframe Finish ²	Packaging/Grade (C-Spec) ³
	2220	C = Standard	2 significant digits + number of zeros.	K = $\pm 10\%$ M = $\pm 20\%$	C = 500 V B = 630 V	R = X7R	1 = KPS Single Chip Stack 2 = KPS Double Chip Stack	C = 100% Matte Sn	7186 = 7" Reel Unmarked 7289 = 13" Reel Unmarked

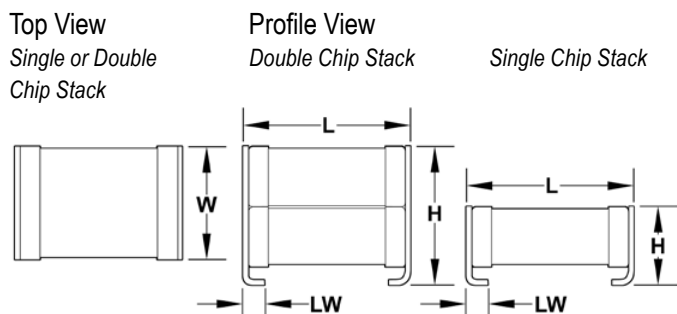
¹ Double chip stacks ("2" in the 13th character position of the ordering code) are only available in M ($\pm 20\%$) capacitance tolerance.

Single chip stacks ("1" in the 13th character position of the ordering code) are available in K ($\pm 10\%$) or M ($\pm 20\%$) tolerances.

² Additional leadframe finish options may be available. Contact KEMET for details.

³ Additional reeling or packaging options may be available. Contact KEMET for details.

Dimensions – Millimeters (Inches)



Number of Chips	EIA Size Code	Metric Size Code	L Length	W Width	H Height	LW Lead Width	Mounting Technique
Single	2220	5650	6.00 (0.236) ±0.50 (0.020)	5.00 (.197) ±0.50 (.020)	3.50 (.138) ±0.30 (.012)	1.60 (.063) ±0.30 (.012)	Solder Reflow Only
Double	2220	5650	6.00 (0.236) ±0.50 (0.020)	5.00 (.197) ±0.50 (.020)	5.00 (.197) ±0.50 (.020)	1.60 (.063) ±0.30 (.012)	

Applications

Typical applications include switch mode power supplies (input filters, resonators, tank circuits, snubber circuits, output filters), high voltage coupling and DC blocking, lighting ballasts, voltage multiplier circuits, DC/DC converters and coupling capacitors in Ćuk converters. Markets include power supply, LCD fluorescent backlight ballasts, HID lighting, telecom equipment, industrial and medical equipment/control, LAN/WAN interface, analog and digital modems, and automotive (electric and hybrid vehicles, charging stations and lighting applications).

Application Note

X7R dielectric is not recommended for AC line filtering or pulse applications.

Qualification/Certification

Commercial Grade products are subject to internal qualification. Details regarding test methods and conditions are referenced in Table 4 , Performance and Reliability.

Environmental Compliance

Pb-Free and RoHS Compliant.



RoHS Compliant

Electrical Parameters/Characteristics

Item	Parameters/Characteristics
Operating Temperature Range	-55°C to +125°C
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	±15%
Aging Rate (Maximum % Capacitance Loss/Decade Hour)	3.0%
Dielectric Withstanding Voltage (DWV)	150% of rated voltage for voltage rating of < 1,000 V 120% of rated voltage for voltage rating of ≥ 1,000 V (5 ±1 seconds and charge/discharge not exceeding 50 mA)
Dissipation Factor (DF) Maximum Limit @ 25°C	2.5%
Insulation Resistance (IR) Limit @ 25°C	See Insulation Resistance Limit Table (500 VDC applied for 120 ±5 seconds @ 25°C)

Regarding Aging Rate: Capacitance measurements (including tolerance) are indexed to a referee time of 1,000 hours.

To obtain IR limit, divide $M\Omega \cdot \mu F$ value by the capacitance and compare to $G\Omega$ limit. Select the lower of the two limits.

Capacitance and Dissipation Factor (DF) measured under the following conditions:

1 kHz ±50 Hz and 1.0 ±0.2 Vrms if capacitance ≤ 10 μF

120 Hz ±10 Hz and 0.5 ±0.1 Vrms if capacitance > 10 μF

Note: When measuring capacitance it is important to ensure the set voltage level is held constant. The HP4284 and Agilent E4980 have a feature known as Automatic Level Control (ALC). The ALC feature should be switched to "ON."

Post Environmental Limits

High Temperature Life, Biased Humidity, Moisture Resistance					
Dielectric	Rated DC Voltage	Capacitance Value	Dissipation Factor (Maximum %)	Capacitance Shift	Insulation Resistance
X7R	> 25	All	3.0	±20%	10% of Initial Limit
	16/25		5.0		
	< 16		7.5		

Insulation Resistance Limit Table

EIA Case Size	1,000 megohm microfarads or 100 GΩ	100 megohm microfarads or 10 GΩ
0805	< 0.0039 μF	≥ 0.0039 μF
1206	< 0.012 μF	≥ 0.012 μF
1210	< 0.033 μF	≥ 0.033 μF
1808	< 0.018 μF	≥ 0.018 μF
1812	< 0.027 μF	≥ 0.027 μF
≥ 1825	All	N/A

Table 1 – Capacitance Range/Selection Waterfall (2220 Case Sizes)

Capacitance	Capacitance Code	Series		C2220		
		Voltage Code		C	B	D
		Voltage DC		500	630	1000
		Capacitance Tolerance		Product Availability and Chip Thickness Codes – See Table 2 for Chip Thickness Dimensions		
Single Chip Stack						
0.047 μF	473	K	M	JP	JP	
0.10 μF	104	K	M	JP	JP	
0.15 μF	154	K	M	JP	JP	
0.22 μF	224	K	M	JP	JP	
0.33 μF	334	K	M	JP		
0.47 μF	474	K	M	JP		
1.0 μF	105	K	M			
Double Chip Stack						
0.10 μF	104		M	JR	JR	
0.22 μF	224		M	JR	JR	
0.33 μF	334		M	JR	JR	
0.47 μF	474		M	JR	JR	
0.68 μF	664		M	JR		
1.0 μF	105		M	JR		
2.2 μF	225		M			
Capacitance	Capacitance Code	Voltage DC		500	630	1000
		Voltage Code		C	B	D
		Series		C2220		

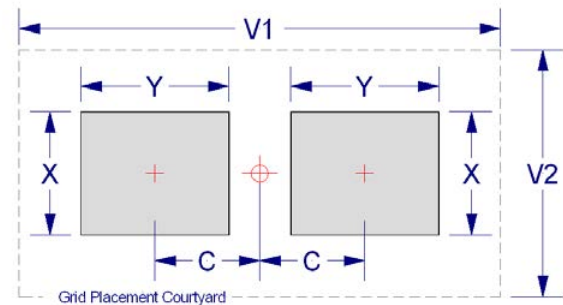
Table 2 – Chip Thickness/Packaging Quantities

Thickness Code	Case Size	Thickness ± Range (mm)	Paper Quantity		Plastic Quantity	
			7" Reel	13" Reel	7" Reel	13" Reel
JP	2220	3.50 ± 0.30	0	0	300	1,300
JR	2220	5.00 ± 0.50	0	0	200	800

Package quantity based on finished chip thickness specifications.

Table 3 – KPS Land Pattern Design Recommendations (mm)

EIA SIZE CODE	METRIC SIZE CODE	Median (Nominal) Land Protrusion				
		C	Y	X	V1	V2
1210	3225	1.50	1.14	1.75	5.05	3.40
1812	4532	2.20	1.35	2.87	6.70	4.50
2220	5650	2.69	2.08	4.78	7.70	6.00



Soldering Process

KEMET's KPS Series devices are compatible with IR reflow techniques. Preheating of these components is recommended to avoid extreme thermal stress. KEMET's recommended profile conditions for IR reflow reflect the profile conditions of the IPC/J-STD-020D standard for moisture sensitivity testing.

To prevent degradation of temperature cycling capability, care must be taken to prevent solder from flowing into the inner side of the lead frames (inner side of "J" lead in contact with the circuit board).

After soldering, the capacitors should be air cooled to room temperature before further processing. Forced air cooling is not recommended.

Hand soldering should be performed with care due to the difficulty in process control. If performed, care should be taken to avoid contact of the soldering iron to the capacitor body. The iron should be used to heat the solder pad, applying solder between the pad and the lead, until reflow occurs. Once reflow occurs, the iron should be removed immediately. (Preheating is required when hand soldering to avoid thermal shock.)

Profile Feature	SnPb Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Minimum (T_{smin})	100°C	150°C
Temperature Maximum (T_{smax})	150°C	200°C
Time (t_s) from T_{smin} to T_{smax}	60 – 120 seconds	60 – 120 seconds
Ramp-up Rate (T_L to T_p)	3°C/seconds maximum	3°C/seconds maximum
Liquidous Temperature (T_L)	183°C	217°C
Time Above Liquidous (t_L)	60 – 150 seconds	60 – 150 seconds
Peak Temperature (T_p)	235°C	250°C
Time within 5°C of Maximum Peak Temperature (t_p)	20 seconds maximum	10 seconds maximum
Ramp-down Rate (T_p to T_L)	6°C/seconds maximum	6°C/seconds maximum
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

Note: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow.

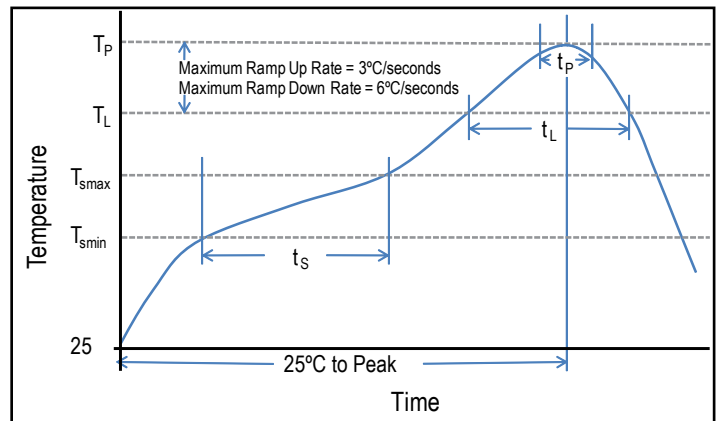


Table 4 – Performance & Reliability: Test Methods and Conditions

Stress	Reference	Test or Inspection Method
Terminal Strength	JIS-C-6429	Appendix 1, Note: Force of 1.8 kg for 60 seconds.
Board Flex	JIS-C-6429	Appendix 2, Note: 5.0 mm minimum
Solderability	J-STD-002	Magnification 50 X. Conditions:
		a) Method B, 4 hours @ 155°C, dry heat @ 235°C
		b) Method B @ 215°C category 3
		c) Method D, category 3 @ 250°C
Temperature Cycling	JESD22 Method JA-104	1,000 cycles (-55°C to +125°C). Measurement at 24 hours +/- 2 hours after test conclusion.
Biased Humidity	MIL-STD-202 Method 103	Load Humidity: 1,000 hours 85°C/85% RH and 200 VDC maximum. Add 100 K ohm resistor. Measurement at 24 hours +/- 2 hours after test conclusion.
		Low Volt Humidity: 1,000 hours 85°C/85% RH and 1.5 V. Add 100 K ohm resistor. Measurement at 24 hours +/- 2 hours after test conclusion.
Moisture Resistance	MIL-STD-202 Method 106	t = 24 hours/cycle. Steps 7a and 7b not required. Unpowered. Measurement at 24 hours +/- 2 hours after test conclusion.
Thermal Shock	MIL-STD-202 Method 107	-55°C/+125°C. Note: Number of cycles required – 300. Maximum transfer time – 20 seconds. Dwell time – 15 minutes. Air-Air.
High Temperature Life	MIL-STD-202 Method 108	1,000 hours at 125°C with rated voltage applied.
Storage Life	MIL-STD-202 Method 108	150°C, 0 VDC for 1,000 hours.
Vibration	MIL-STD-202 Method 204	5 g's for 20 minutes, 12 cycles each of 3 orientations. Note: Use 8" X 5" PCB 0.031" thick, 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10 – 2,000 Hz.
Mechanical Shock	MIL-STD-202 Method 213	Figure 1 of Method 213, Condition F.
Resistance to Solvents	MIL-STD-202 Method 215	Add aqueous wash chemical, OKEM Clean or equivalent.

Storage and Handling

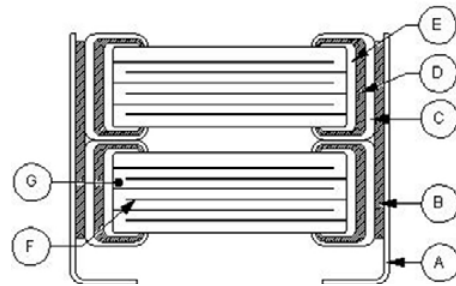
Ceramic chip capacitors should be stored in normal working environments. While the chips themselves are quite robust in other environments, solderability will be degraded by exposure to high temperatures, high humidity, corrosive atmospheres, and long term storage. In addition, packaging materials will be degraded by high temperature– reels may soften or warp and tape peel force may increase. KEMET recommends that maximum storage temperature not exceed 40°C and maximum storage humidity not exceed 70% relative humidity. Temperature fluctuations should be minimized to avoid condensation on the parts and atmospheres should be free of chlorine and sulfur bearing compounds. For optimized solderability chip stock should be used promptly, preferably within 1.5 years of receipt.

Construction

Reference	Item	Material
A	Leadframe	Phosphor Bronze – Alloy 510
B	Leadframe Attach	HMP Solder
C	Termination	Cu
D		Ni
E		Sn
F	Inner Electrode	Ni
G	Dielectric Material	BaTiO ₃

Note: Image is exaggerated in order to clearly identify all components of construction.

HMP = High Melting Point



Product Marking

Laser marking option is not available on:

- C0G, Ultra Stable X8R and Y5V dielectric devices
- EIA 0402 case size devices
- EIA 0603 case size devices with Flexible Termination option.
- KPS Commercial and Automotive grade stacked devices.

These capacitors are supplied unmarked only.

Tape & Reel Packaging Information

KEMET offers multilayer ceramic chip capacitors packaged in 8, 12 and 16 mm tape on 7" and 13" reels in accordance with EIA Standard 481. This packaging system is compatible with all tape-fed automatic pick and place systems. See Table 2 for details on reeling quantities for commercial chips.

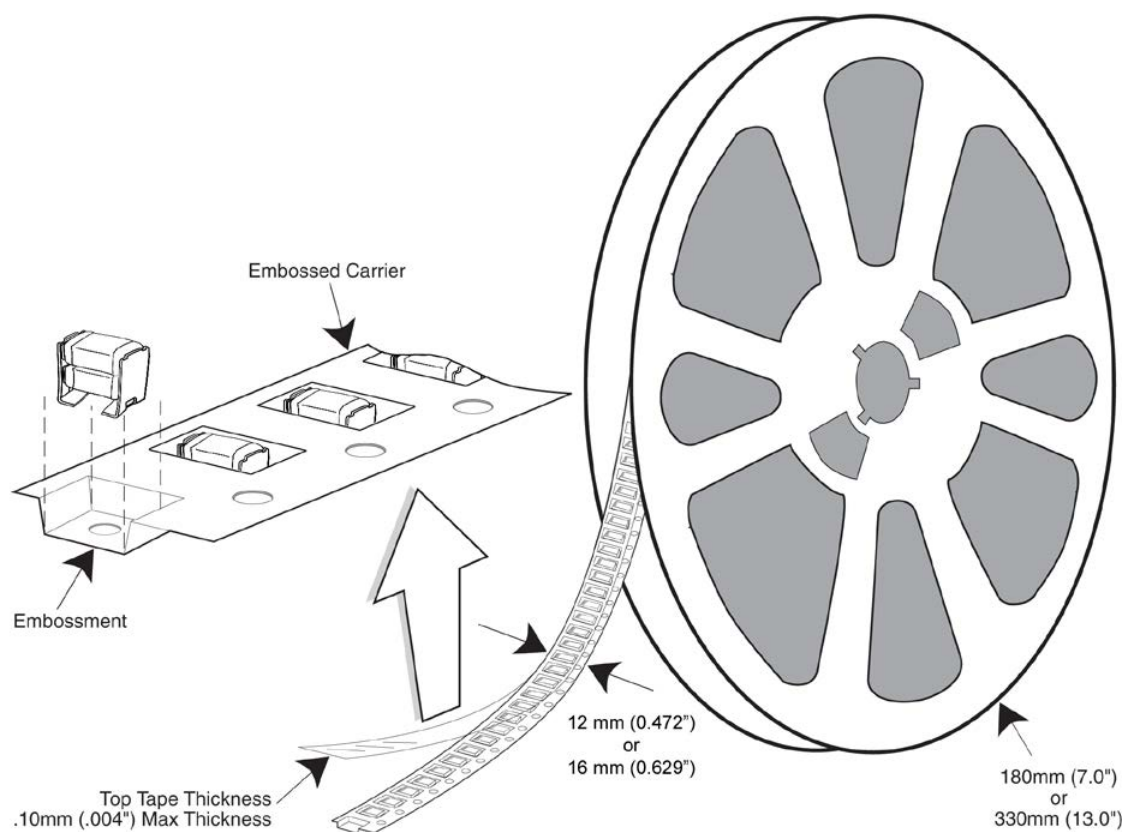


Table 5 – Carrier Tape Configuration – Embossed Plastic (mm)

EIA Case Size	Tape Size (W)*	Pitch (P ₁)*
01005 – 0402	8	2
0603 – 1210	8	4
1805 – 1808	12	4
≥ 1812	12	8
KPS 1210	12	8
KPS 1812 & 2220	16	12
Array 0508 & 0612	8	4

*Refer to Figure 1 for W and P₁ carrier tape reference locations.

*Refer to Table 5 for tolerance specifications.

Figure 1 – Embossed (Plastic) Carrier Tape Dimensions

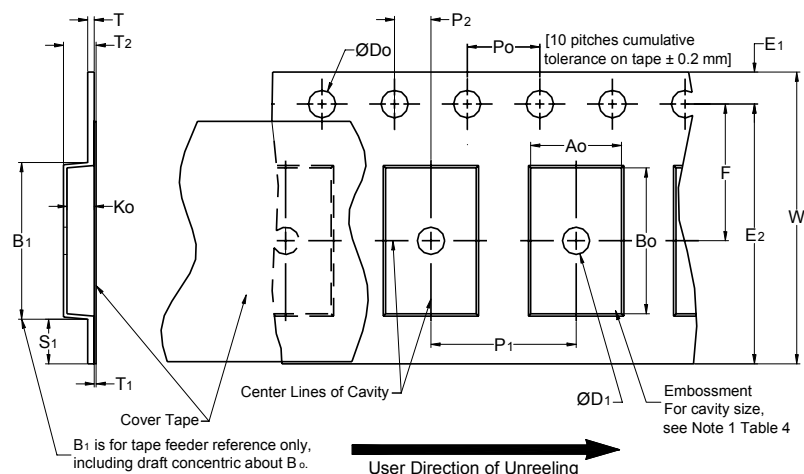


Table 6 – Embossed (Plastic) Carrier Tape Dimensions

Metric will govern

Constant Dimensions — Millimeters (Inches)									
Tape Size	D ₀	D ₁ Minimum Note 1	E ₁	P ₀	P ₂	R Reference Note 2	S ₁ Minimum Note 3	T Maximum	T ₁ Maximum
8 mm	1.5 +0.10/-0.0 (0.059 +0.004/-0.0)	1.0 (0.039)	1.75 ±0.10 (0.069 ±0.004)	4.0 ±0.10 (0.157 ±0.004)	2.0 ±0.05 (0.079 ±0.002)	25.0 (0.984)	0.600 (0.024)	0.600 (0.024)	0.100 (0.004)
12 mm		1.5 (0.059)				30 (1.181)			
16 mm									
Variable Dimensions — Millimeters (Inches)									
Tape Size	Pitch	B ₁ Maximum Note 4	E ₂ Minimum	F	P ₁	T ₂ Maximum	W Maximum	A ₀ , B ₀ & K ₀	
8 mm	Single (4 mm)	4.35 (0.171)	6.25 (0.246)	3.5 ±0.05 (0.138 ±0.002)	4.0 ±0.10 (0.157 ±0.004)	2.5 (0.098)	8.3 (0.327)	Note 5	
12 mm	Single (4 mm) & Double (8 mm)	8.2 (0.323)	10.25 (0.404)	5.5 ±0.05 (0.217 ±0.002)	8.0 ±0.10 (0.315 ±0.004)	4.6 (0.181)	12.3 (0.484)		
16 mm	Triple (12 mm)	12.1 (0.476)	14.25 (0.561)	7.5 ± 0.05 (0.138 ± 0.002)	12.0 ± 0.10 (0.157 ± 0.004)	4.6 (0.181)	16.3 (0.642)		

1. The embossment hole location shall be measured from the sprocket hole controlling the location of the embossment. Dimensions of embossment location and hole location shall be applied independent of each other.
2. The tape with or without components shall pass around R without damage (see Figure 5).
3. If S₁ < 1.0 mm, there may not be enough area for cover tape to be properly applied (see EIA Standard 481 paragraph 4.3 section b).
4. B₁ dimension is a reference dimension for tape feeder clearance only.
5. The cavity defined by A₀, B₀ and K₀ shall surround the component with sufficient clearance that:
 - (a) the component does not protrude above the top surface of the carrier tape.
 - (b) the component can be removed from the cavity in a vertical direction without mechanical restriction, after the top cover tape has been removed.
 - (c) rotation of the component is limited to 20° maximum for 8 and 12 mm tapes and 10° maximum for 16 mm tapes (see Figure 2).
 - (d) lateral movement of the component is restricted to 0.5 mm maximum for 8 and 12 mm wide tape and to 1.0 mm maximum for 16 mm tape (see Figure 3).
 - (e) for KPS Series product, A₀ and B₀ are measured on a plane 0.3 mm above the bottom of the pocket.
 - (f) see Addendum in EIA Standard 481 for standards relating to more precise taping requirements.

Packaging Information Performance Notes

- 1. Cover Tape Break Force:** 1.0 Kg minimum.
- 2. Cover Tape Peel Strength:** The total peel strength of the cover tape from the carrier tape shall be:

Tape Width	Peel Strength
8 mm	0.1 to 1.0 Newton (10 to 100 gf)
12 and 16 mm	0.1 to 1.3 Newton (10 to 130 gf)

The direction of the pull shall be opposite the direction of the carrier tape travel. The pull angle of the carrier tape shall be 165° to 180° from the plane of the carrier tape. During peeling, the carrier and/or cover tape shall be pulled at a velocity of 300 ±10 mm/minute.

- 3. Labeling:** Bar code labeling (standard or custom) shall be on the side of the reel opposite the sprocket holes. *Refer to EIA Standards 556 and 624.*

Figure 2 – Maximum Component Rotation

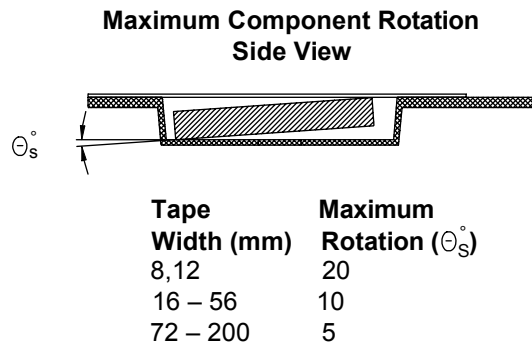
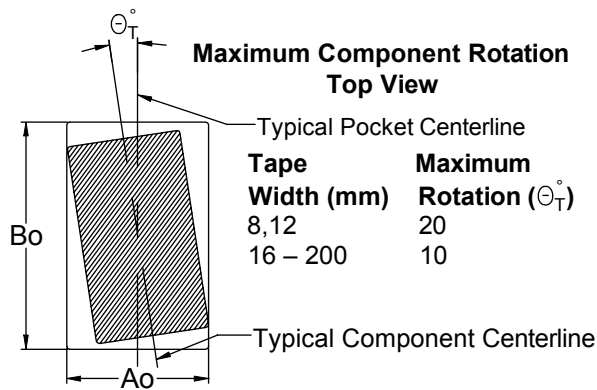


Figure 3 – Maximum Lateral Movement

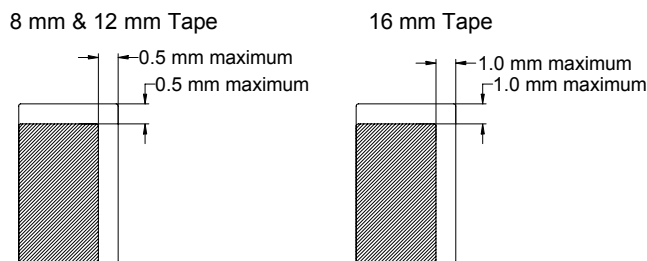


Figure 4 – Bending Radius

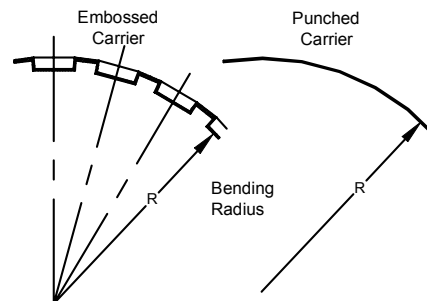
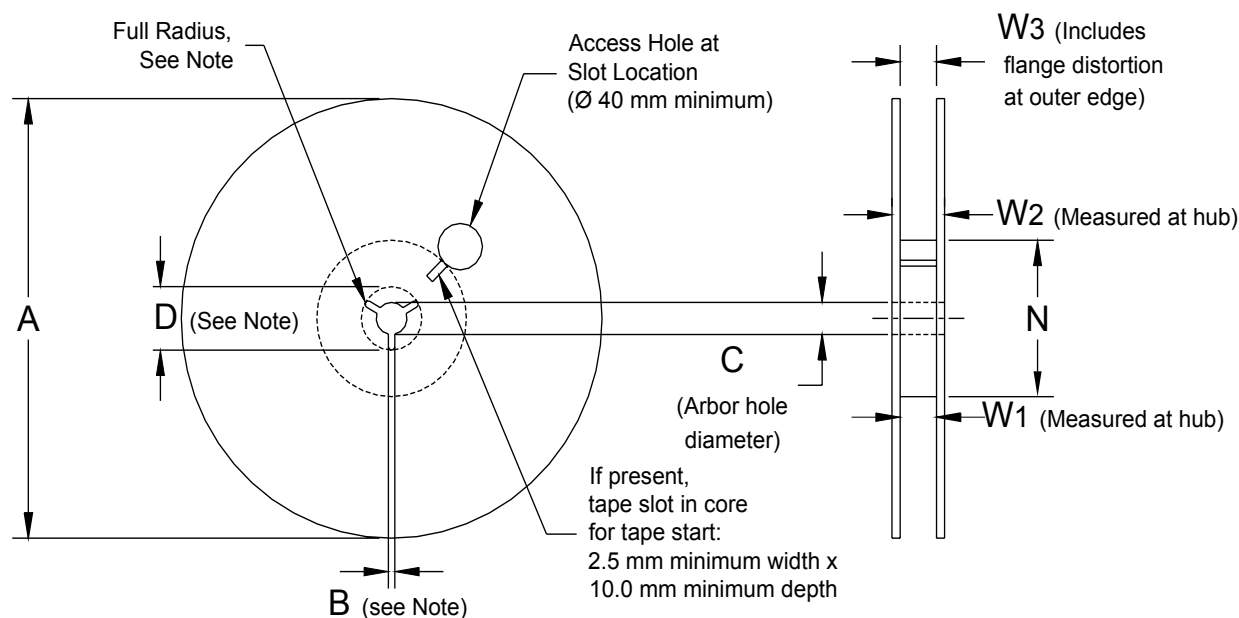


Figure 5 – Reel Dimensions



Note: Drive spokes optional; if used, dimensions B and D shall apply.

Table 7 – Reel Dimensions

Metric will govern

Constant Dimensions — Millimeters (Inches)				
Tape Size	A	B Minimum	C	D Minimum
8 mm	178 ±0.20 (7.008 ±0.008) or 330 ±0.20 (13.000 ±0.008)	1.5 (0.059)	13.0 +0.5/-0.2 (0.521 +0.02/-0.008)	20.2 (0.795)
12 mm				
16 mm				
Variable Dimensions — Millimeters (Inches)				
Tape Size	N Minimum	W ₁	W ₂ Maximum	W ₃
8 mm	50 (1.969)	8.4 +1.5/-0.0 (0.331 +0.059/-0.0)	14.4 (0.567)	Shall accommodate tape width without interference
12 mm		12.4 +2.0/-0.0 (0.488 +0.078/-0.0)	18.4 (0.724)	
16 mm		16.4 +2.0/-0.0 (0.646 +0.078/-0.0)	22.4 (0.882)	

Figure 6 – Tape Leader & Trailer Dimensions

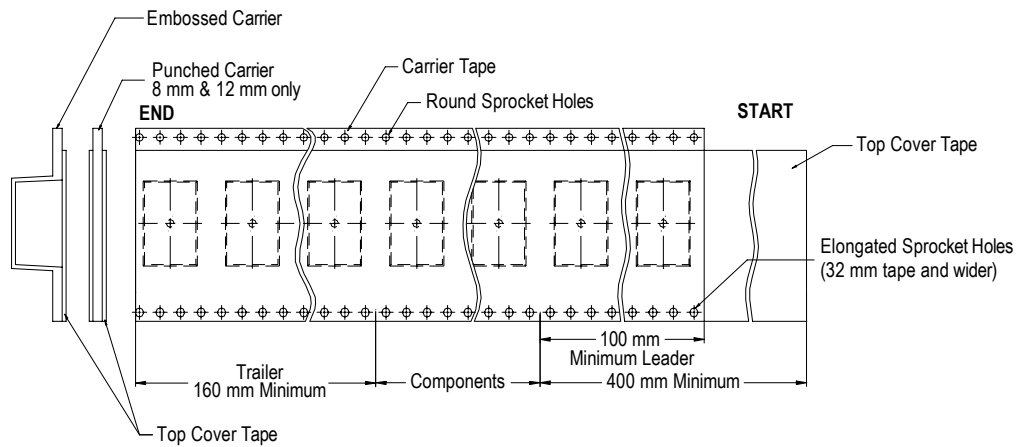
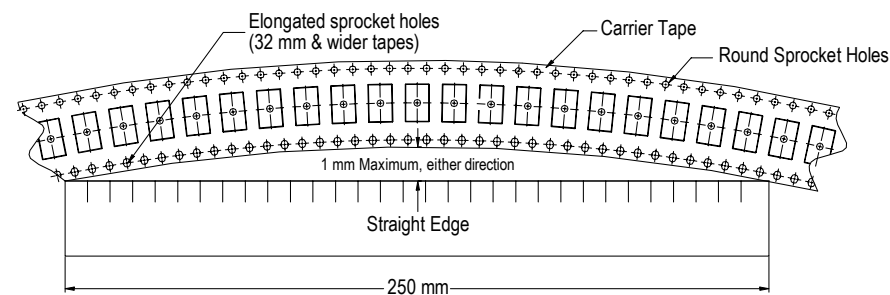


Figure 7 – Maximum Camber



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Mexico
Guadalajara, Jalisco
Tel: 52-33-3123-2141

Europe

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Sasso Marconi, Italy
Tel: 39-051-939111

Central Europe
Landsberg, Germany
Tel: 49-8191-3350800

Kamen, Germany
Tel: 49-2307-438110

Northern Europe
Bishop's Stortford, United Kingdom
Tel: 44-1279-460122

Espoo, Finland
Tel: 358-9-5406-5000

Asia

Northeast Asia
Hong Kong
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Shenzhen, China
Tel: 86-755-2518-1306

Beijing, China
Tel: 86-10-5829-1711

Shanghai, China
Tel: 86-21-6447-0707

Taipei, Taiwan
Tel: 886-2-27528585

Southeast Asia
Singapore
Tel: 65-6586-1900

Penang, Malaysia
Tel: 60-4-6430200

Bangalore, India
Tel: 91-806-53-76817

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Other KEMET Resources

Tools	
Resource	Location
Configure A Part: CapEdge	http://capacitoredge.kemet.com
SPICE & FIT Software	http://www.kemet.com/spice
Search Our FAQs: KnowledgeEdge	http://www.kemet.com/keask
Electrolytic LifeCalculator	http://www.kemet.com:8080/elc

Product Information	
Resource	Location
Products	http://www.kemet.com/products
Technical Resources (Including Soldering Techniques)	http://www.kemet.com/technicalpapers
RoHS Statement	http://www.kemet.com/rohs
Quality Documents	http://www.kemet.com/qualitydocuments

Product Request	
Resource	Location
Sample Request	http://www.kemet.com/sample
Engineering Kit Request	http://www.kemet.com/kits

Contact	
Resource	Location
Website	www.kemet.com
Contact Us	http://www.kemet.com/contact
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Call Us	1-877-MyKEMET
Twitter	http://twitter.com/kemetcapacitors

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Although KEMET designs and manufactures its products to the most stringent quality and safety standards, given the current state of the art, isolated component failures may still occur. Accordingly, customer applications which require a high degree of reliability or safety should employ suitable designs or other safeguards (such as installation of protective circuitry or redundancies) in order to ensure that the failure of an electrical component does not result in a risk of personal injury or property damage.

Although all product-related warnings, cautions and notes must be observed, the customer should not assume that all safety measures are indicated or that other measures may not be required.

