Fusion Embedded Development Kit

User's Guide

Actel
POWER MATTERS

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Trademarks

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Introduction

Fusion Embedded Development Kit Contents

The RoHS-compliant, environmentally friendly Fusion Embedded Development Kit is packaged in a recyclable cardboard box made from recycled materials. This low-cost Fusion development kit enables you to develop embedded processor and mixed-signal applications. The kit contains the items shown in Table 1.

Table 1 • **Fusion Embedded Development Kit Contents**

Quantity	Contents
1	Fusion Embedded Development Kit board (Figure 1) with M1-Enabled Fusion FPGA (M1AFS1500)
1	Low-Cost Programming Stick (LCPS) for programming the M1AFS1500 FPGA
1	External 5 V Power Supply
2	USB 2.0 high-speed cables
1	Packet of jumpers
1	Quick Start Guide
1	Actel Libero® Integrated Design Environment (IDE) software DVD

Figure 1 • **Fusion Embedded Development Kit Evaluation Board with LCPS Attached**

1 – Board Components and Settings

Board Description

The Fusion Embedded Development Kit board is intended to provide a low-cost embedded system management platform for evaluating the Fusion FPGA advanced features, such as mixed-signal and embedded processor development. The Fusion FPGA on this kit is M1-enabled for ARM® Cortex™-M1 embedded processor development. In addition, the Fusion Embedded Development Kit board consists of a variety of features for mixed-signal applications, such as voltage sequencing, voltage trimming, gaming, motor control, temperature monitor, and touch screen. The on-board mixed-signal header allows various daughter boards to be attached for extended mixed-signal applications.

When using the board in conjunction with Actel's power analysis tools, you should achieve a better understanding of power consumption at each stage in the design. In addition, Actel's Libero® Integrated Design Environment (IDE) tool suite includes power-driven layout (PDL), which can reduce the power consumption of designs.

The evaluation board, shown in Figure 1-1, has a small form factor, measuring about 2.5 × 3.5 inches, and supports a Cortex-M1–Enabled Fusion device in the FGG484 package. All major components used on the board are low-power. Also included on the evaluation board is an Ethernet and USB-to-UART interface for communication with the Fusion FPGA, which can be implemented for system management. To assist in embedded processor development, components such as I^2C, EEPROM, OLED, SRAM, and SPI flash are available on-board. Temperature diode, potentiometer, and PWM circuit are available on-board for mixed-signal applications. The board can be powered by USB and includes a programming stick header which allows the low-cost programming stick (LCPS) to be attached to the board for programming the Fusion M1AFS1500 device.

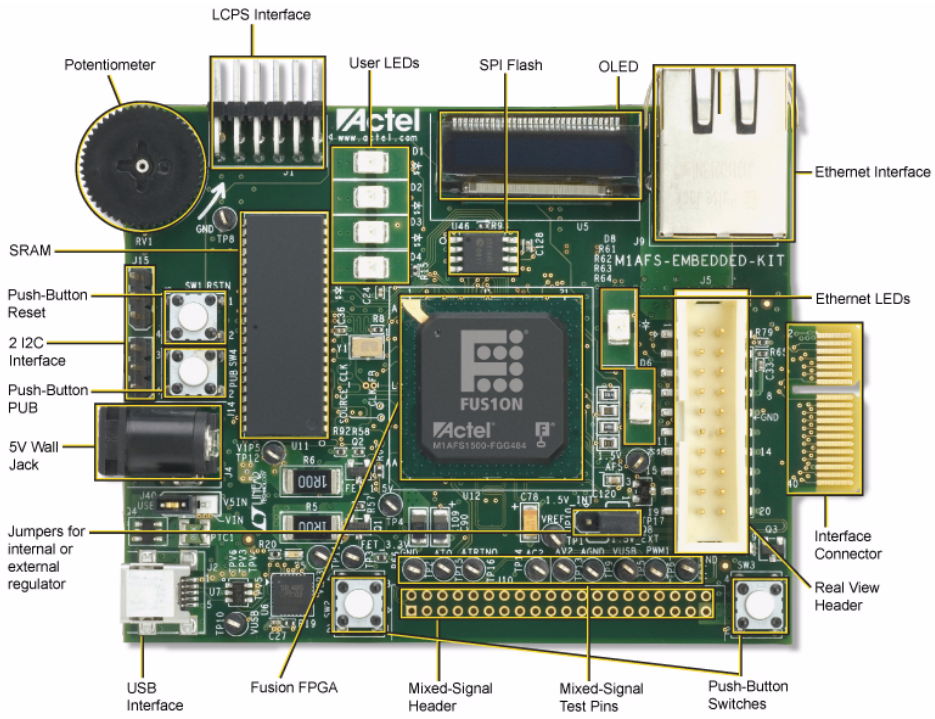

Figure 1-1 • Fusion Embedded Development Kit Evaluation Board

Fusion Embedded Development Kit Board Stackup

The Fusion Embedded Development Kit board is built on an 8-layer printed circuit board (PCB). The top and bottom silkscreens are provided in the following pages. Full PCB design layout is provided on the Fusion Embedded Development Kit board main website:

http://actel.com/products/hardware/devkits_boards/fusion_embedded.aspx

To view the PCB design layout files, you can use Allegro Free Physical Viewer, which can be downloaded from the Cadence Allegro Download page.

1. Top signal (Figure 1-2 on page 1-9)
2. GND1
3. Signal 1
4. PWR 1
5. PWR 2
6. Signal 2
7. GND 4
8. Bottom signal (Figure 1-3 on page 1-10)

L1 Top Silkscreen

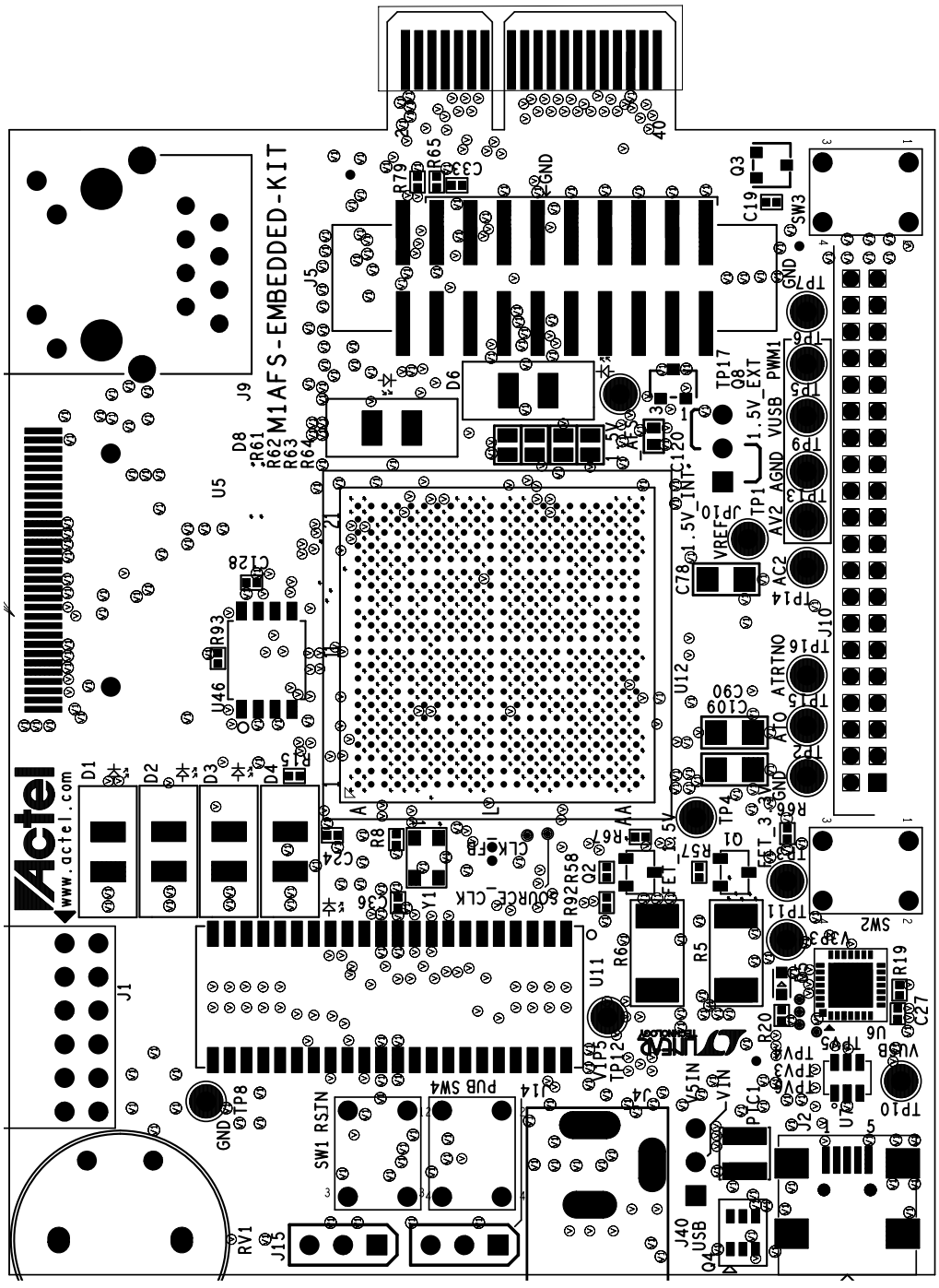

Figure 1-2 • **Top Silkscreen**

L8 Bottom Silkscreen

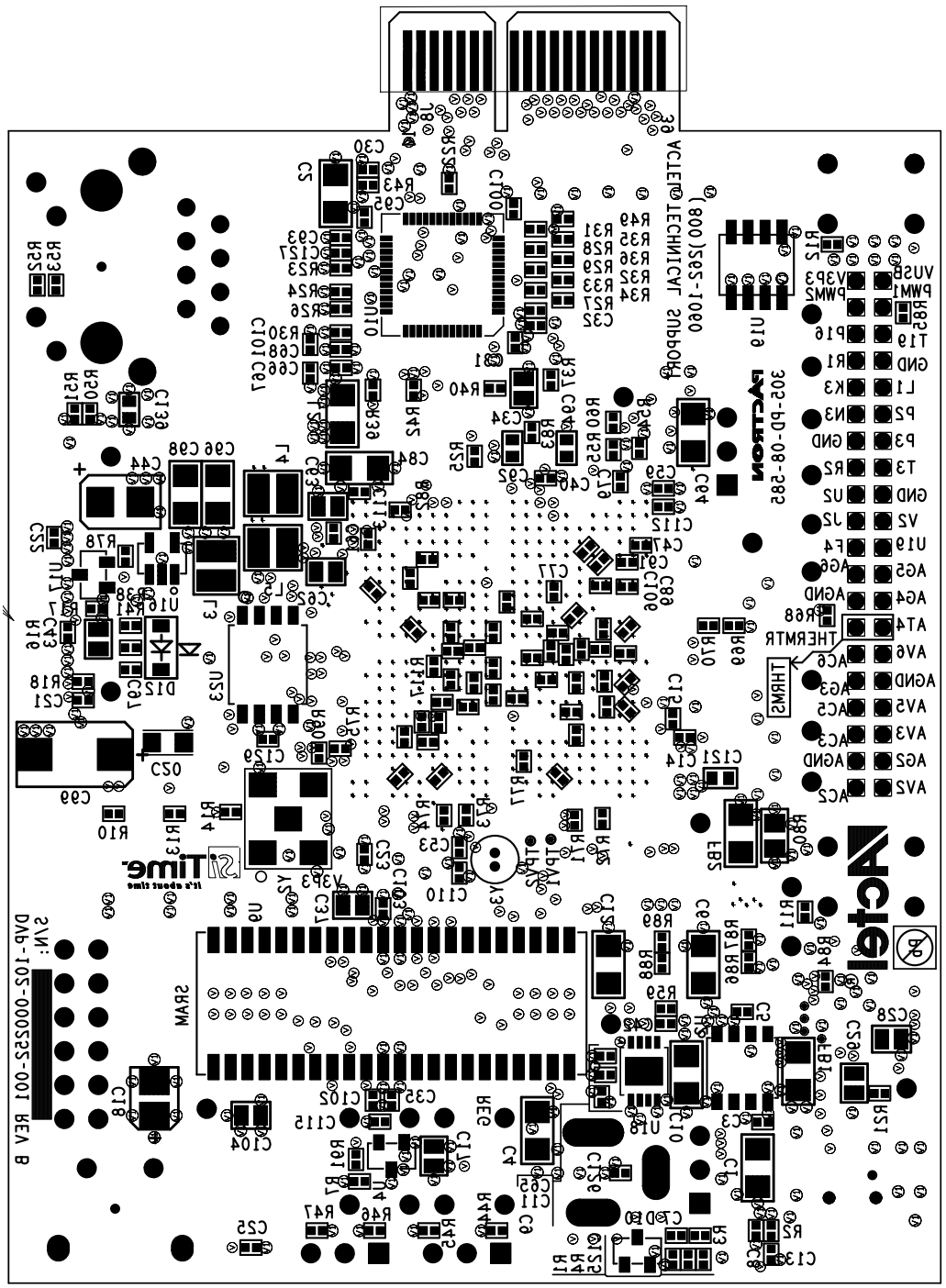

Figure 1-3 • **Bottom Silkscreen**

Jumper Settings

Recommended default jumper settings are defined in Table 1-1. Connect jumpers in the default settings to enable the pre-programmed demo design to function correctly.

Table 1-1 • **Jumper Settings**

Jumper	Default Setting	Comment
JP10	Pin 3–2	Jumper to select either 1.5 V external regulator or Fusion 1.5 V internal regulator. Pin 1–2 = 1.5 V Internal Pin 3–2 = 1.5 V External
J40	Pin 1–2	Jumper to select power source. Pin 3–2 = 5 V Power Brick Pin 1–2 = USB

Fusion M1AFS1500-FGG484

The Fusion Embedded Development Kit board is populated with a M1-Enabled Fusion M1AFS1500 FPGA. Here are some of its key features. Refer to the *Fusion Datasheet* for additional features.

Key Features

- High-performance reprogrammable flash technology
- Embedded flash memory
- Integrated A/D converter (ADC) and analog I/O
- On-chip clocking support
- Low power consumption
- In-system programming (ISP) and security
- Advanced digital I/Os
- SRAMs and FIFOs
- Soft ARM7™ core support in M1 Fusion devices

Table 1-2 • **Key Features of M1AFS1500**

System Gates	1,500,000
Tiles (D-flip-flop)	1,024
Secure (AES) ISP	Yes
PLLs	2
Globals	18
Flash Memory Blocks (2 Mbits)	4
Total Flash Memory Bits	8 M
FlashROM Bits	1 K
RAM Blocks (4,608 bits)	60
RAM Kbits	270
Analog Quads	10
Analog Input Channels	30
Gate Driver Outputs	10
I/O Banks (+JTAG)	5
Maximum Digital I/Os	252
Analog I/Os	40

Fusion Datasheet and FPGA Fabric User's Guide

For more information, refer to the *Fusion* datasheet at www.actel.com/documents/Fusion_DS.pdf and the *Fusion FPGA Fabric User's Guide* at www.actel.com/documents/Fusion_UG.pdf.

Digital Power Supply Pins for M1AFS1500-FGG484

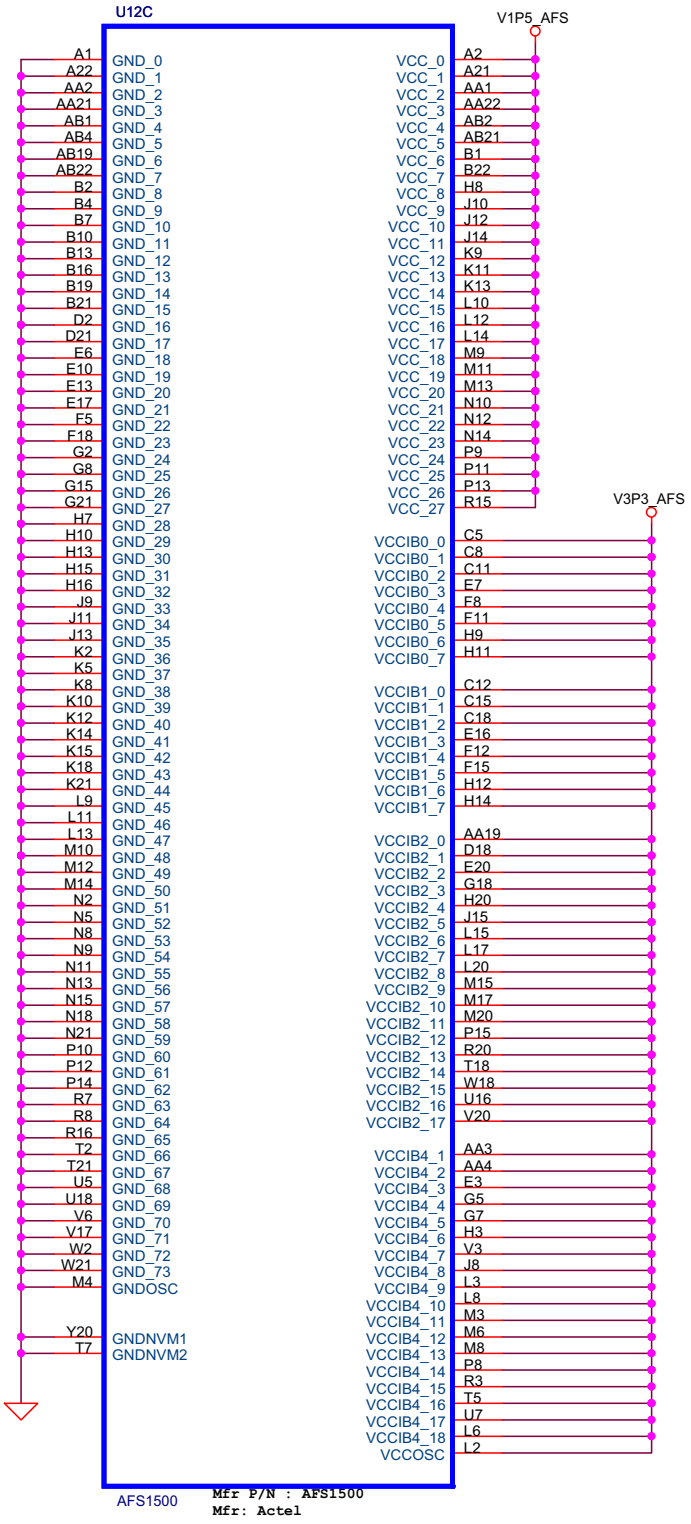

Figure 1-4 • **Digital Power Supply Pins Schematic**

Digital Signal Pins for M1AFS1500-FGG484

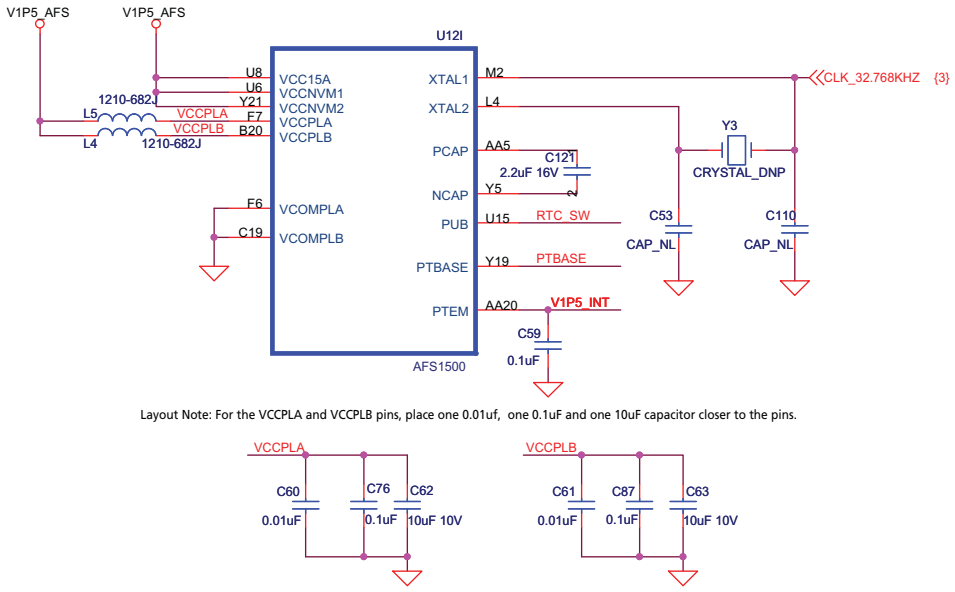

Figure 1-5 • **Digital Signal Pins Schematic**

Analog Power Supply Pins for M1AFS1500-FGG484

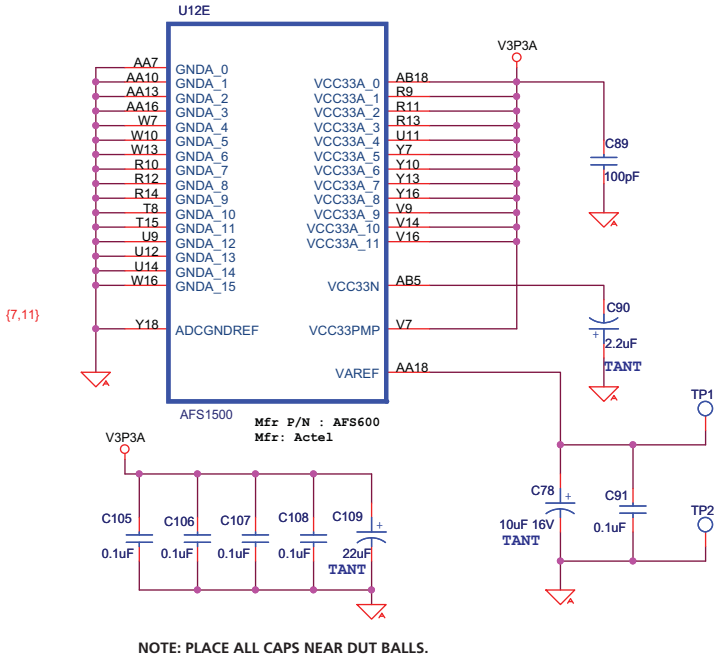

Figure 1-6 • **Analog Power Supply Pins Schematic**

Analog Signal Pins for M1AFS1500-FGG484

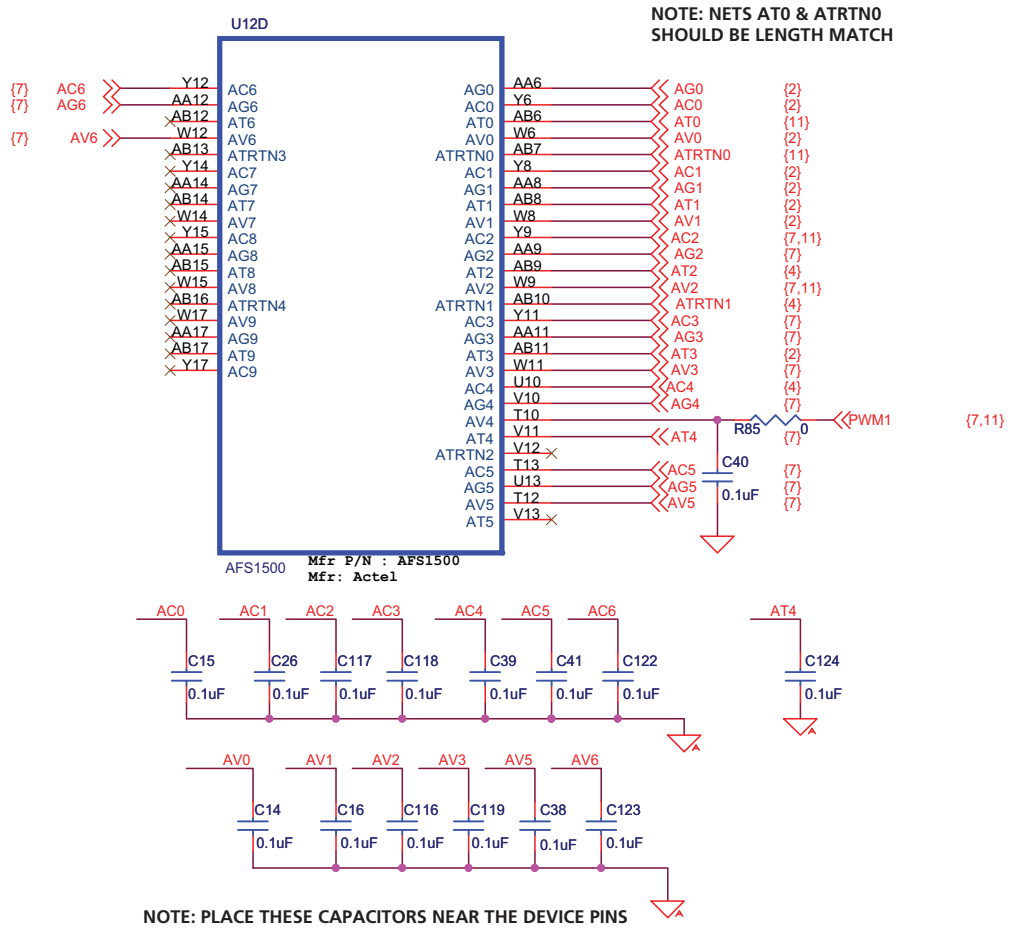

Figure 1-7 • Analog Supply Pins Schematic

I/O Pins for Bank 0 and Bank 1 on M1AFS1500-FGG484

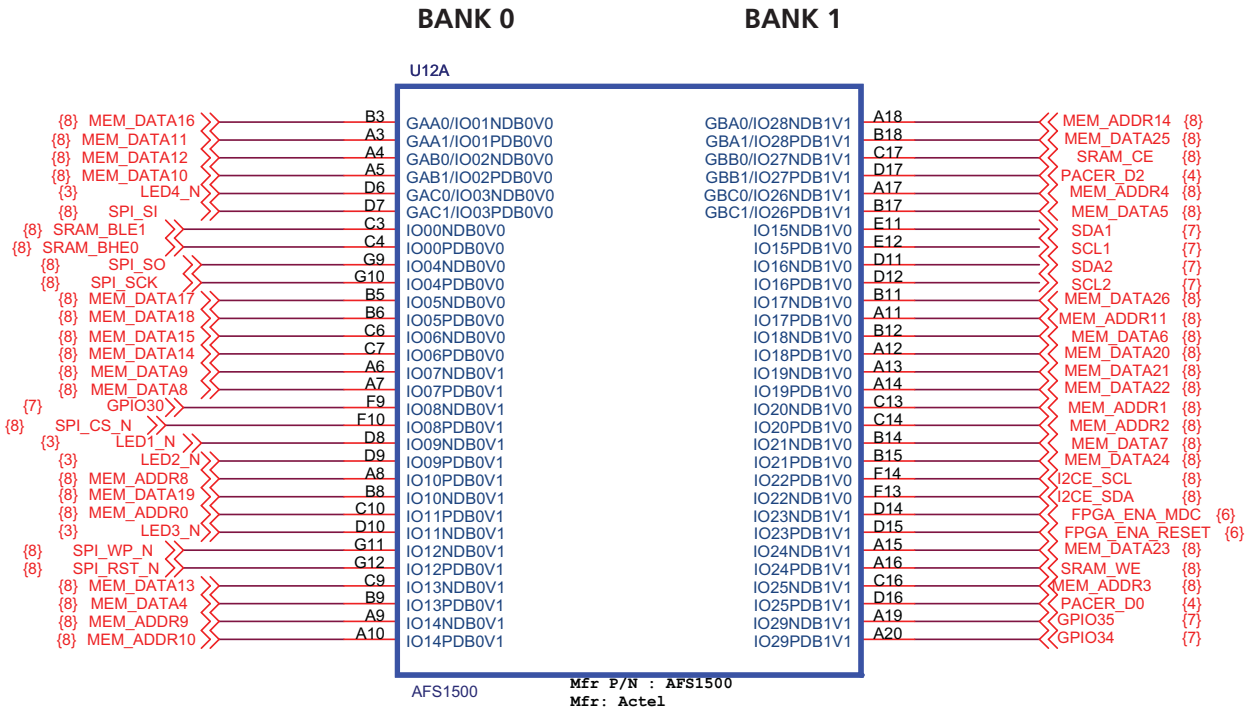

Figure 1-8 • **I/O Pins Schematic for Banks 0 and 1**

I/O Pins for Bank 2 on M1AFS1500-FGG484

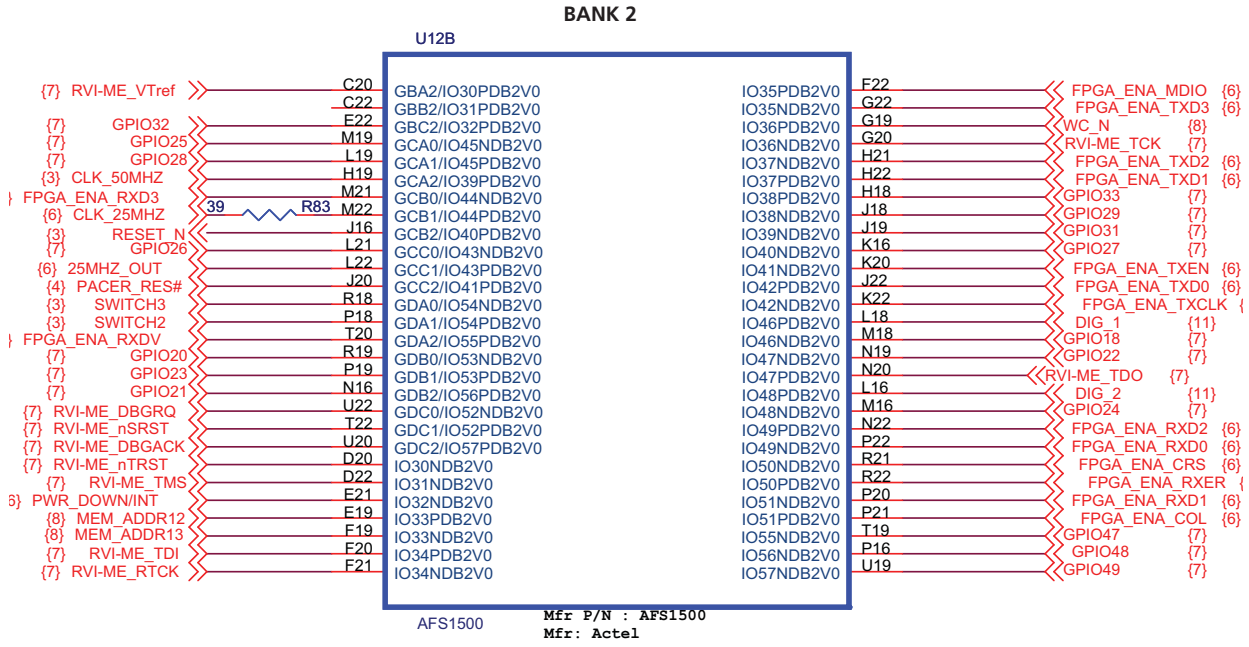

Figure 1-9 • **I/O Pins Schematic for Bank 2**

I/O Pins for Bank 4 on M1AFS1500-FGG484

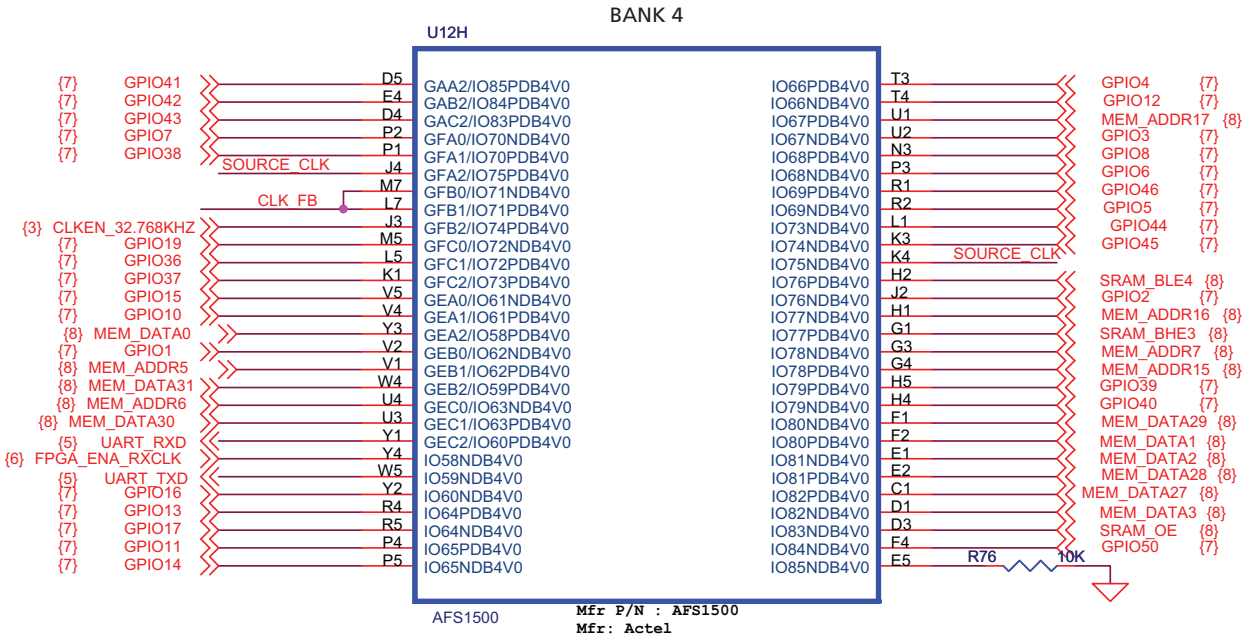

Figure 1-10 • **I/O Pins Schematic for Bank 4**

Fusion FPGA ADC Block

One main feature of Actel Fusion FPGA is its mixed-signal capabilities, which includes an integrated analog-to-digital (ADC) block. The Fusion ADC can support 8-, 10-, and 12-bit modes of operation. All results are MSB-justified in the ADC. The input to the ADC is a large 32:1 analog input multiplexer. A simplified block diagram of the Analog Quads, analog input multiplexer, and ADC is shown in Figure 1-11. The ADC offers multiple self-calibrating modes to ensure consistent high performance both at power-up and during runtime. The Fusion M1AFS1500 FPGA on this board has an ADC block with ten Analog Quads. In addition, an internal diode is available to monitor the FPGA's core temperature. Refer to the *Fusion FPGA Fabric User's Guide* for additional details on the ADC block.

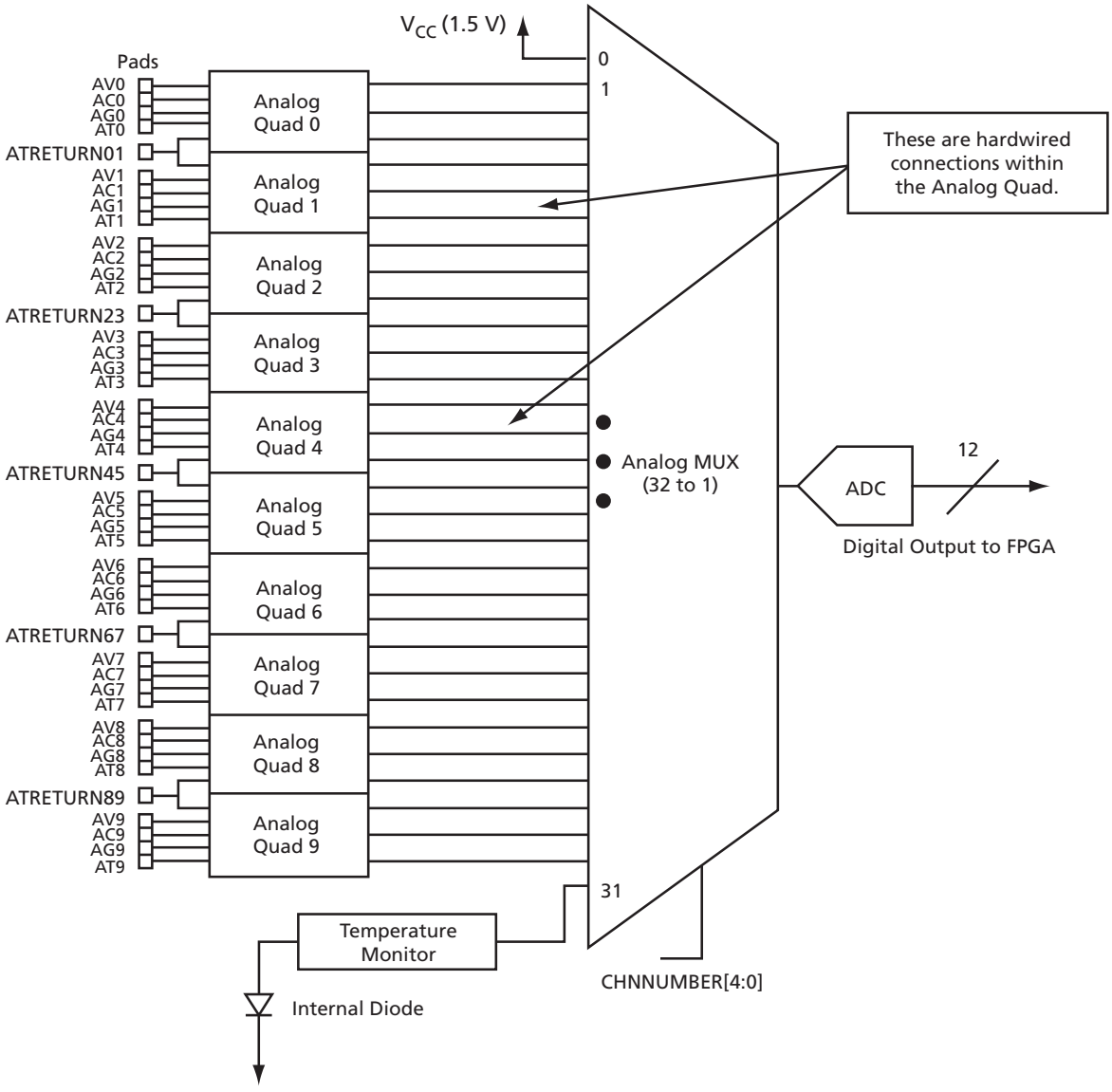

***Figure 1-11* • Analog Block ADC and MUX Architecture**

Fusion Analog Quad

Each Analog Quad in a Fusion FPGA consists of a Voltage Monitor, Current Monitor, Gate Driver, and Temperature Monitor block (Figure 1-12). The primary inputs to these Fusion Analog Quad are the AV, AC, AT, and AG pins. It is important to note that the Voltage, Current, and Temperature monitor blocks can all measure voltage, depending on the how the input pins are used. The Fusion Embedded Development Kit board provides on-board components, such as a PWM circuit, potentiometer, and temperature diode to demonstrate the mixed-signal features of the Analog Quad.

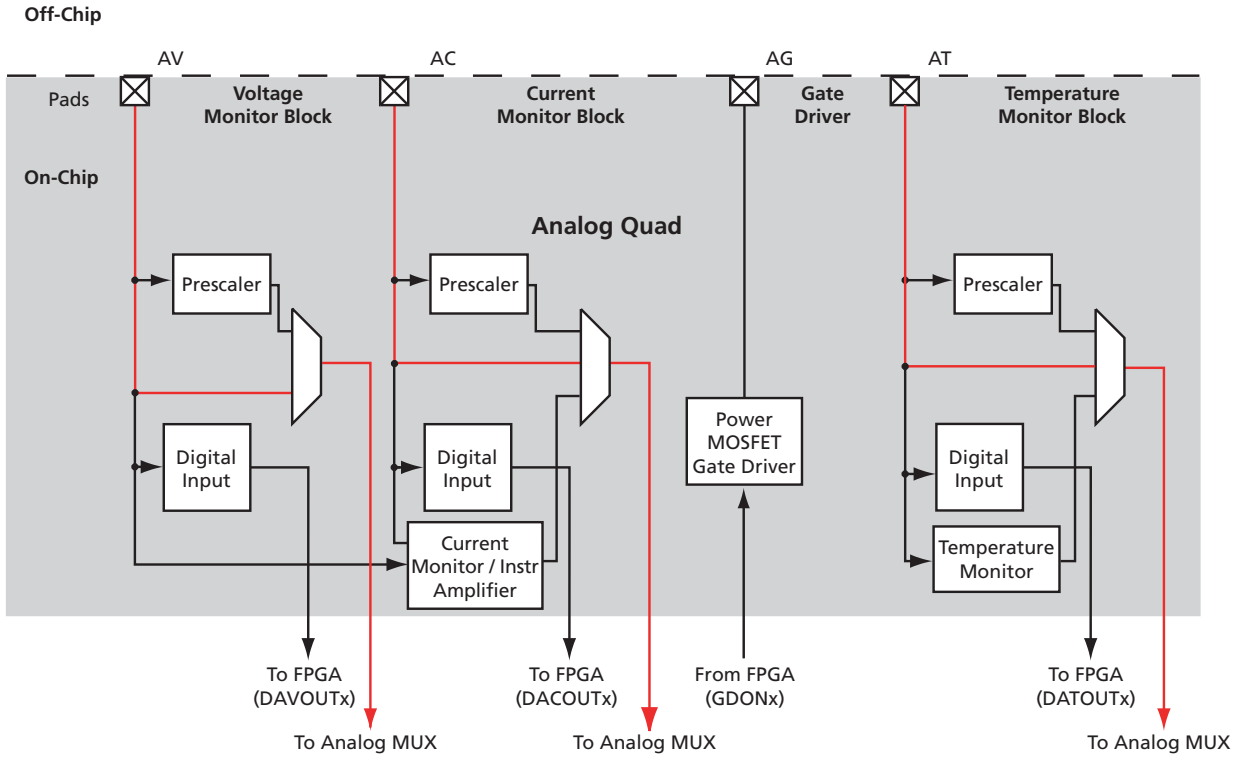

***Figure 1-12* • Block Diagram of the Fusion Analog Quad**

PWM Circuit

The PWM RC circuit shown in Figure 1-13 can be used with a CorePWM IP instantiated in the FPGA fabric to generate various voltages waveforms. These voltage waveforms can be displayed on the OLED or used via the mixed-signal header. In addition, one PWM RC circuit source is routed to the AV input pin of an Analog Quad. This AV pin can be used to monitor the generated voltage with high accuracy, depending on the ADC resolution configured in the FPGA.

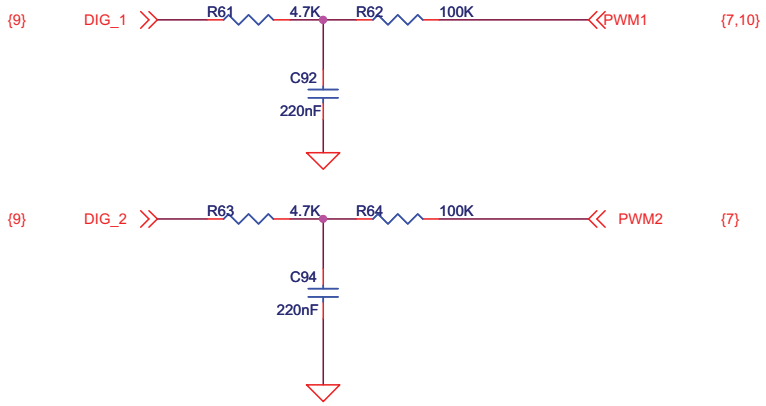

***Figure 1-13* • PWM Circuit Schematic**

Voltage Monitor Block

The AV pin is an input to the Voltage Monitor Block and one of the features of this block is to measure voltage. The Fusion Voltage Monitor block shown in Figure 1-14 contains a two-channel analog multiplexer that allows an incoming analog signal to be routed directly to the ADC or allows the signal to be routed to a prescaler circuit before being sent to the ADC. The prescaler circuit scales the voltage applied to the ADC input pad so that it is compatible with the ADC input voltage range. Additional prescaler and Voltage Monitor programmable functionality can be obtained as described in the *Fusion FPGA Fabric User's Guide*.

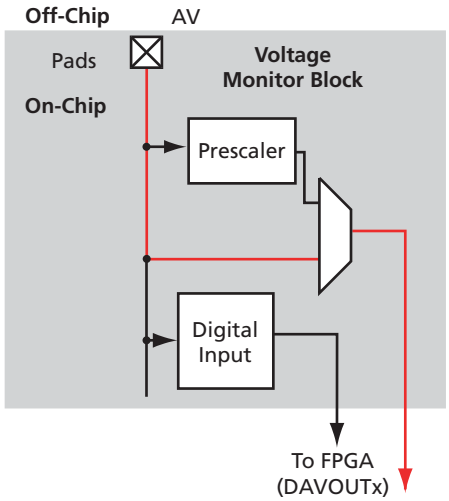

***Figure 1-14* • Voltage Monitor Block Diagram**

Potentiometer Circuit

A potentiometer circuit is provided on the Fusion Embedded Development Kit to sweep voltage and is connected to the AC input pin. This AC pin can be used to monitor voltage. One application is to adjust the potentiometer and measure the voltage on the AC pin.

Note: It is also possible to use an AC pin for current measurement.

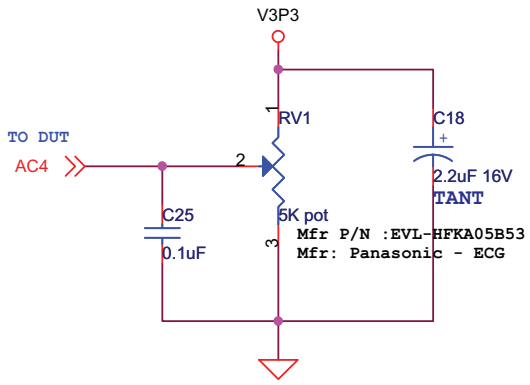

Figure 1-15 • **Potentiometer Circuit Schematic**

Current Sensing Circuit

For current monitor applications, two current sensing circuits are provided on the Fusion Embedded Development Kit board. One of the current sensing circuits is for the 3.3 V voltage rail and the other is for the 1.5 V voltage rail of the Fusion FPGA (Figure 1-16).

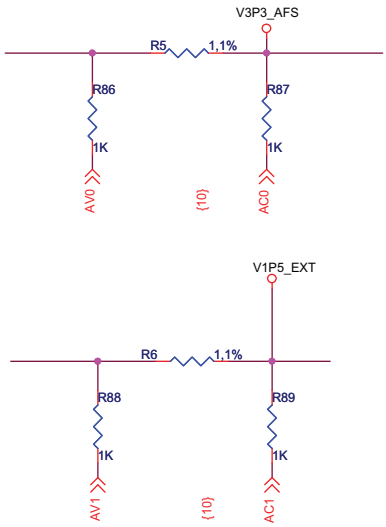

Figure 1-16 • **Current Sensing Schematic (3.3 V)**

Current Monitor Block

In addition to measuring voltage, the Current Monitor Block can be used to measure current (Figure 1-17). To measure current, a small external current sensing resistor (typically less than 1 ohm) is connected between the AV and AC pins in an Analog Quad and is in series with a power source. The Current Monitor Block contains a current monitor circuit that converts the current through the external resister to a voltage that can then be read using the Fusion ADC.

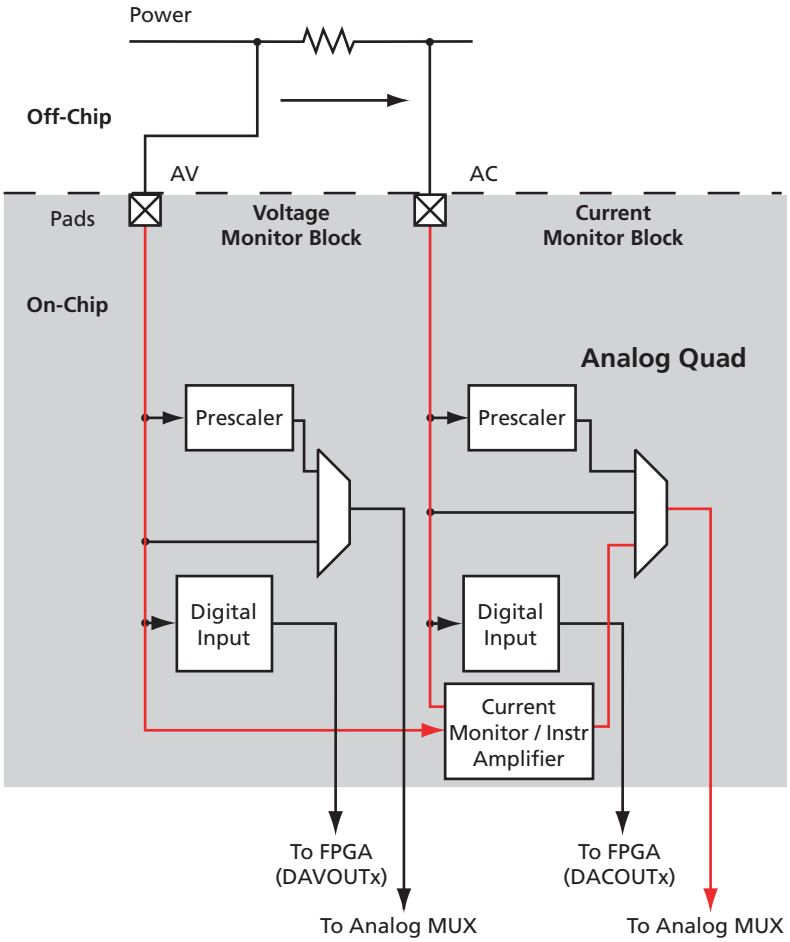

***Figure 1-17* • Analog Quad Block Diagram for Current Measurement**

Temperature Diodes

One external temperature diode on this Fusion Embedded Development Kit board is available for temperature measurement. This temperature diode is routed to the analog temperature (AT) and AT Return (ATRTN) input pins of the Temperature Monitor Block (Figure 1-18).

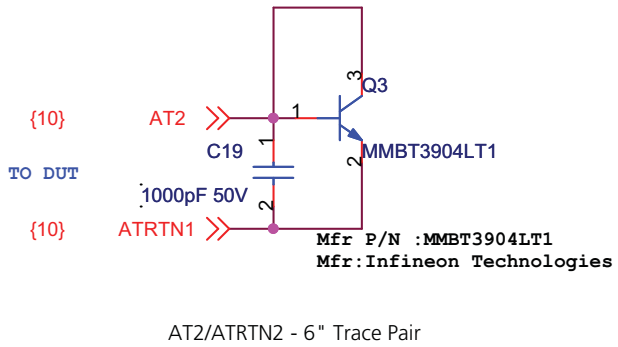

Figure 1-18 • **Temperature Diodes Schematic**

Temperature Monitor Block

The temperature Monitor Block can be used to monitor both voltage and temperature, depending on whether the ATRTN pin is used (Figure 1-19).

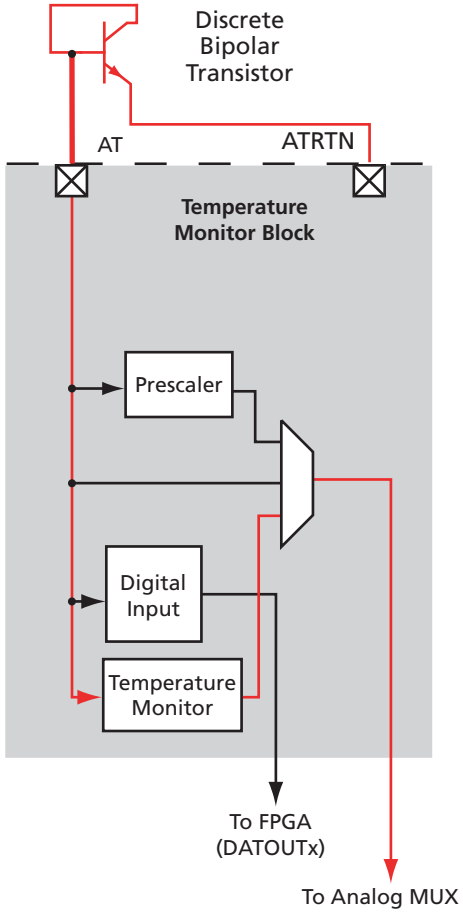

***Figure 1-19* • Temperature Monitor Block Diagram**

When both the AT and ATRTN pins are used, temperature can be monitored with high accuracy (±3°C), depending on the ADC resolution configured in the FPGA. Each Analog Quad in the Fusion FPGA device has one AT pin to monitor external temperature. In addition to external temperature monitoring, an internal temperature diode can be used to monitor the internal Fusion device temperature on Channel 31 of the ADCMUX.

MOSFET for the Gate Driver Block

Two external p-channel MOSFETs are populated on the board connected to the AG pins of the Fusion Analog Quad (Figure 1-20). One MOSFET is connected on the 3.3 V voltage rail and the other is on the 1.5 V voltage rail of the Fusion FPGA. The output of these MOSFETs goes to the AT pads, which can be set to monitor voltage. These MOSFETs can be used for a variety of voltage sequencing applications (see "Example 1: Voltage Sequencing with Gate Drivers Application" and "Example 2: Voltage Sequencing Application" on page 1-26).

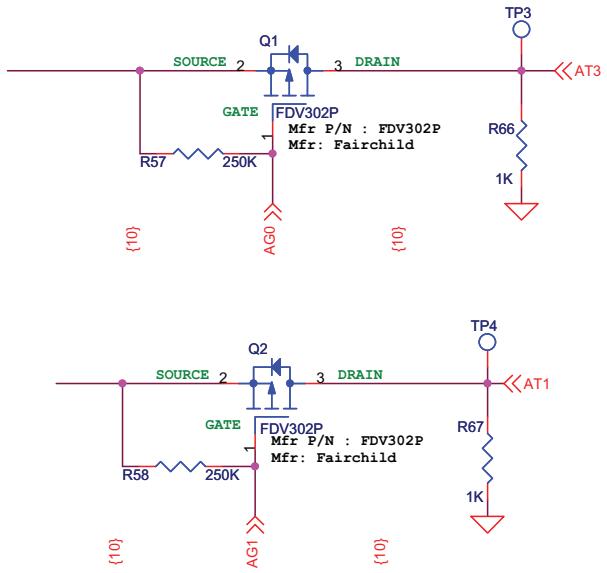

Figure 1-20 • **MOSFET Schematic (for 3.3 V, top; for 1.5 V, bottom)**

Example 1: Voltage Sequencing with Gate Drivers Application

The MOSFET and gate drivers can be used for voltage sequencing or wave shaping applications. A simple voltage sequencing application is enabled on the Fusion Embedded Development Kit board by connecting the source of the MOSFET to a 3.3 V and also a 1.5 V source (Figure 1-21). A PWM circuit can control the enable pin to the AG pad. Based on the gate drive, the MOSFET can be turned ON/OFF to create different waveforms. The result can be displayed on the on-board OLED or oscilloscope.

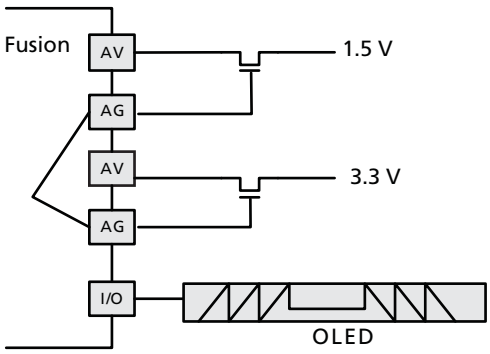

Figure 1-21 • **Voltage Sequencing with Gate Drivers**

Example 2: Voltage Sequencing Application

Another method for voltage sequencing is implementing a PWM to generate a voltage between 0 and 3.3 V or from 0 to 1.5 V. The generated voltage can be monitored via the AT channels to which it is connected, and can be displayed on the OLED or oscilloscope via test points (Figure 1-22).

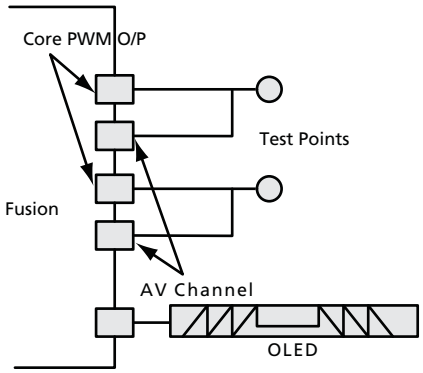

***Figure 1-22* • Voltage Sequencing Application**

Mixed-Signal Header

A range of Fusion mixed-signal pins, particularly the analog AV, AC, AG, and AT pins of the Analog Quad and GPIO I/O pins, are available on the Mixed-Signal Header on this board (Figure 1-23). This header can be used by various daughter boards to access the Fusion analog pins to demonstrate various applications, such as motor control, touch screen, and voltage trimming.

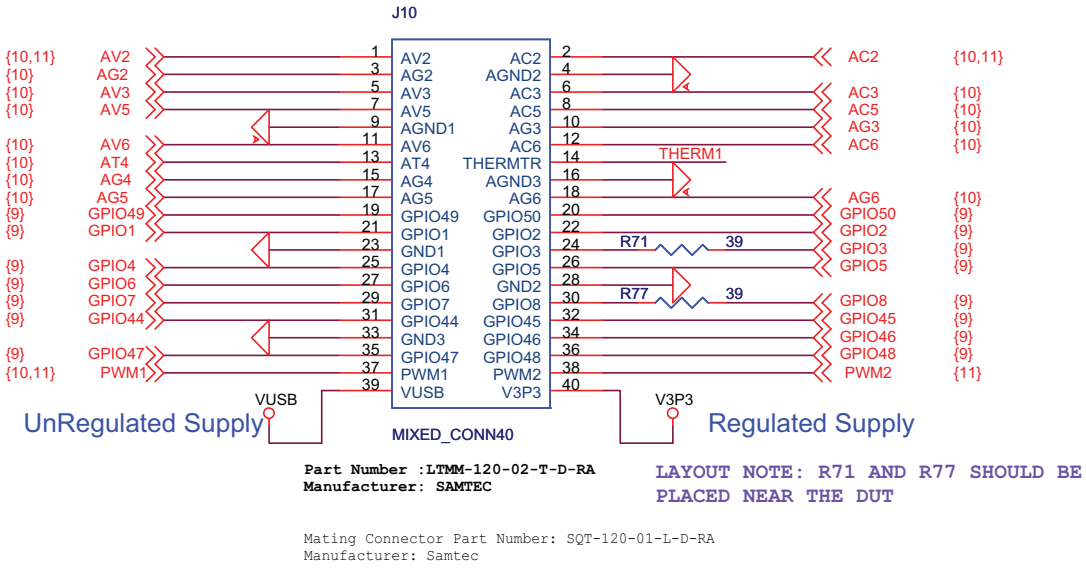

***Figure 1-23* • Mixed-Signal Header Schematic**

A thermistor circuit is available to use with the Mixed-Signal Header for temperature monitor applications (Figure 1-24).

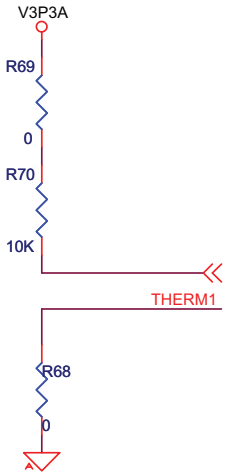

Figure 1-24 • **Thermistor Schematic**

Test Pins

Additional test pins are available on the Fusion Embedded Development Kit board for mixed-signal applications (Figure 1-25). The AT0 and ATRTN0 test pins can be used for additional temperature monitor applications. Power and ground test pins are also provided.

The Test Pins below have two specific applications:

1. Temperature monitoring of an external source
2. Voltage trimming on evaluation or daughter boards

Refer to the application note, *Using Fusion for Closed-Loop Power Supply Margining:*

www.actel.com/documents/Fusion_ClsdLoopPwr_AN.pdf

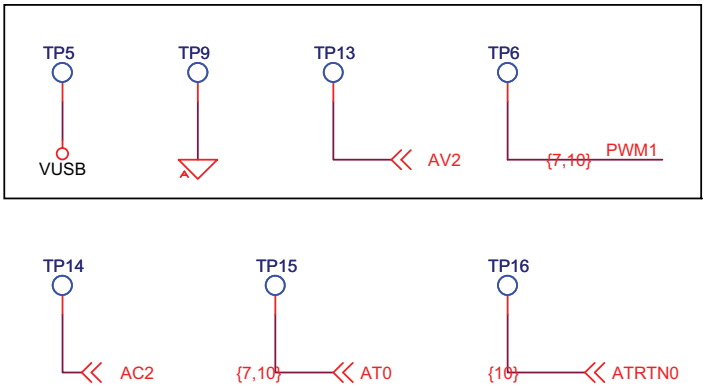

Figure 1-25 • **Test Pins Schematic**

Fusion FPGA Embedded Microprocessor

Actel offers several microprocessor and microcontroller solutions for developers, all of which are tightly integrated with Actel Libero IDE, optimized for Actel FPGA architecture, and supplied with a complete toolset for code compile and debug.

The Fusion Embedded Development Kit board contains a Fusion M1AFS1500 FPGA device, which is Cortex-M1–enabled. Cortex-M1 is the first ARM processor developed specifically for implementation in FPGAs. In addition to Cortex-M1, this Fusion FPGA can be programmed with Core8051(s) or CoreABC.

A few components are populated on the Embedded Development Kit board for basic Cortex-M1 development. These components include SRAM, SPI-based flash, Ethernet interface, USB-to-UART bridge, OLED, EEPROM, and I^2C interfaces. To integrate these components for a complete solution, Actel supplies a full range of subsystem IP cores: memory controllers, timers, mailbox, serial interface controllers, and others. These subsystem IP can connect to the embedded processor via the AMBA bus. Refer to Actel's IP catalog for additional information on available IPs for Fusion M1-Enabled embedded processors: http://www.actel.com/products/ip/default.aspx.

For the ARM-based embedded processors, Actel offers the Analog Interface IP (CoreAI) to communicate with the Analog System of the mixed-signal Fusion FPGA. CoreAI allows for simple control of the analog peripherals within Fusion. This control can be implemented with an embedded microprocessor within the FPGA fabric. The AMBA APB slave interface is used as the primary control mechanism within CoreAI. CoreAI instantiates the Analog Block (AB) macro, which includes the Analog Configuration MUX (ACM) interface, Analog Quads, and Real-Time Counter (RTC). The block diagram in Figure 1-26 is an example embedded processor system using CoreAI. Refer to the *Fusion FPGA Fabric User's Guide* for additional details on the Fusion FPGA embedded microprocessor.

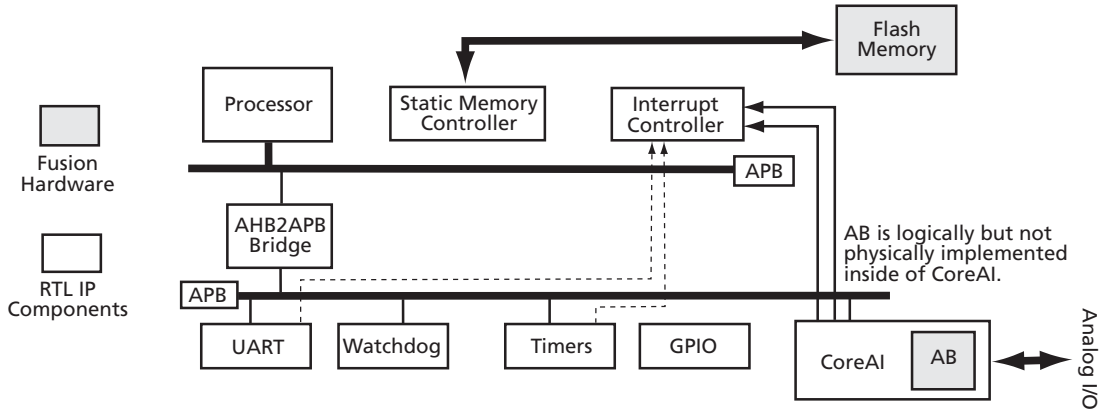

Figure 1-26 • **Embedded Processor System Using CoreAI**

2 – Power

The Fusion Embedded Development Kit board is powered through an external 5 V power supply (power brick) or through USB (Figure 2-1). The board does not switch seamlessly between the power brick and USB, so the 3-pin header must be set properly with jumpers to select the desired power source. With the USB option, the inrush current meets the USB specifications. The power brick option is provided in cases when 100% of total I/Os are utilized and USB power is insufficient.

Three voltage rails (10 V, 3.3 V, and 1.5 V) are provided on the board. Since both the FPGA core and programming functions at 1.5 V, the VJTAGENB signal on the programming connector is left floating. The 10 V regulator is used for the on-board OLED.

Table 2-1 • **Current Ratings**

Regulator	Current Rating
10 V	100 mA
3.3 V	1 A
1.5 V	500 mA

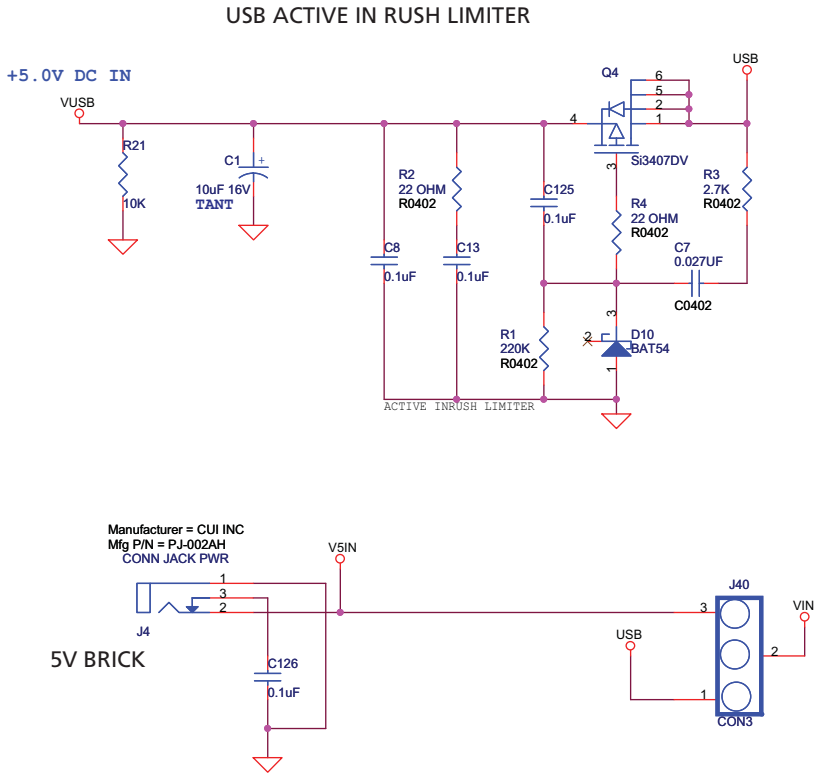

Figure 2-1 • **Power Sources**

3 – Operation of Board Components

Clock Oscillator

A 50 MHz clock oscillator with 50 ppm is available on the board (Figure 3-1). This clock oscillator is connected to the FPGA to provide a system or reference clock. An on-chip Fusion PLL can be configured and instantiated in the FPGA to generate a wide range of high precision clock frequencies.

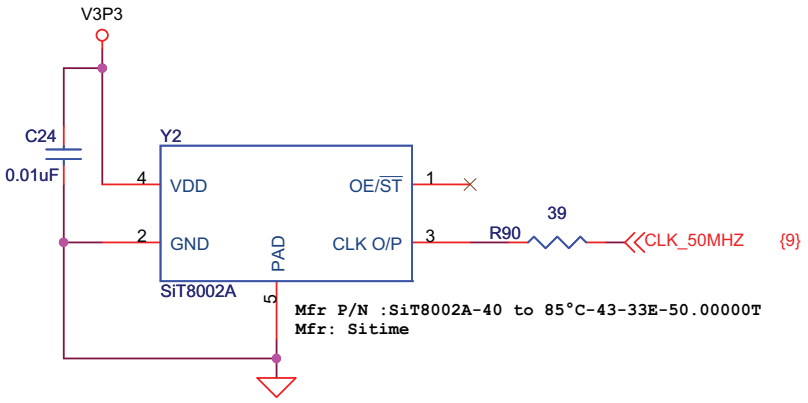

Figure 3-1 • **Clock Oscillator Schematic**

Crystal Oscillator

A 32.768 KHz off-chip crystal oscillator with 50 ppm is populated on the board. The off-chip crystal oscillator is connected to the digital XTAL1 and XTAL2 (on-chip crystal oscillator) inputs of the Fusion FPGA. The on-chip crystal oscillator circuit works with the low frequency off-chip crystal to generate a high-precision clock. It has an accuracy of 100 ppm (0.01%) and is capable of providing system clocks for Fusion peripherals and other system clock networks, both on-chip and off-chip. When combined with the Fusion on-chip CCC/PLL blocks, a wide range of clock frequencies can be created to support various design requirements. In addition, a Fusion programmable Real-Time Counter (RTC), which is clocked by the on-chip crystal oscillator, help provides power sequencing and voltage regulator control. Refer to the *Fusion FPGA Fabric User's Guide* for additional details on these clocking resources.

A sample clocking option utilizing the on- and off-chip crystal oscillator for a Fusion FPGA is shown in Figure 3-2.

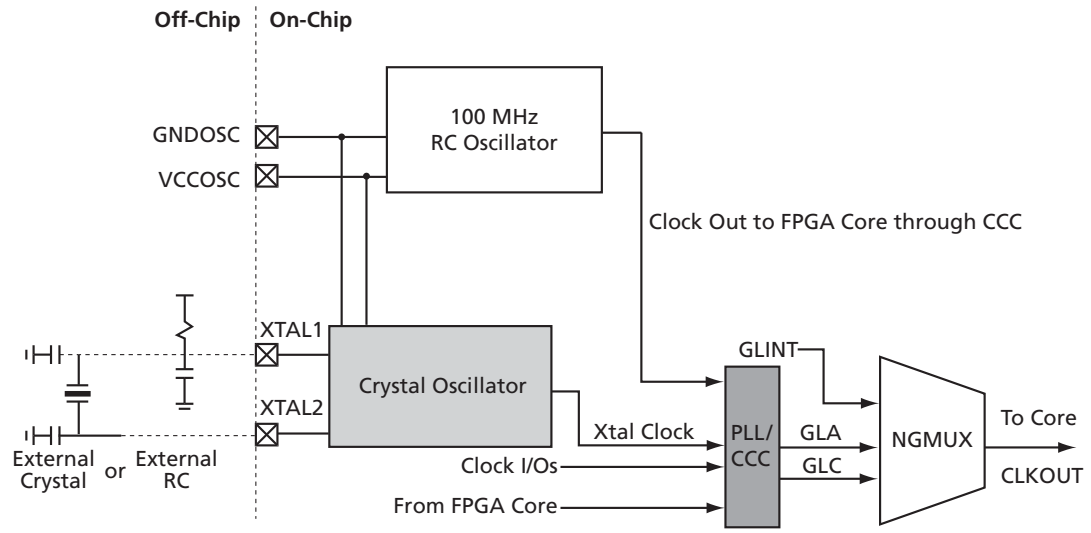

Figure 3-2 • **Fusion Clock Options**

Figure 3-3 shows the schematic for the off-chip crystal oscillator.

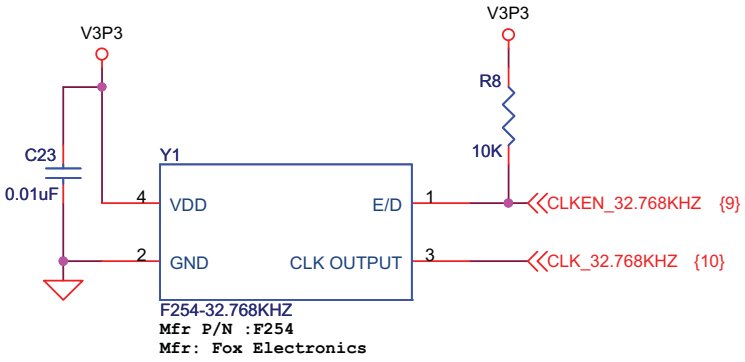

Figure 3-3 • **Off-Chip Crystal Oscillator Schematic**

Push-Button System Reset

A push-button system reset switch with Schmitt Trigger device is provided on the board (Figure 3-4). The Schmitt Trigger device helps reduce noise on the system reset push-button.

Additional information on this push-button device is available at the Fusion Embedded Development Kit main webpage:

http://www.actel.com/products/hardware/devkits_boards/fusion_embedded.aspx.

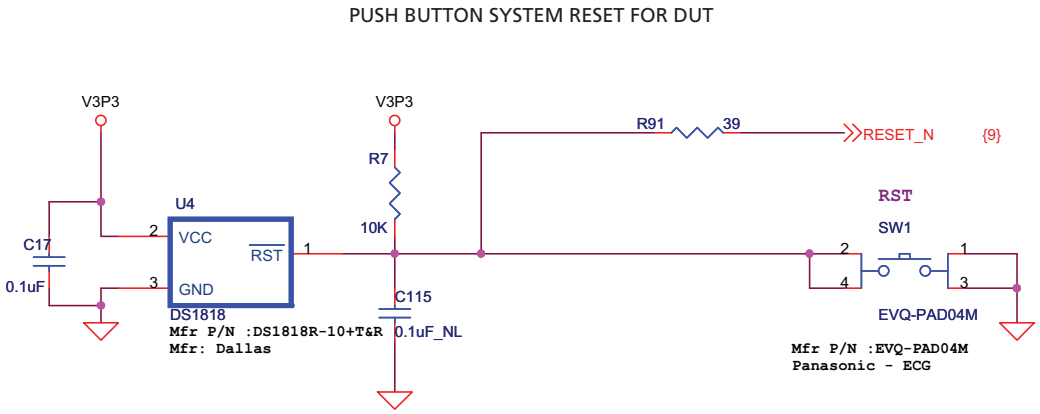

Figure 3-4 • **Push-Button System Reset Schematic**

Push-Button Switches and User LEDs

Two active low push-button switches for input control are available (Table 3-1 and Figure 3-5 on page 3-34). In addition, four active low LEDs for status and debug are available on the board. These push-button switches and user LEDs can also be used for debug and various applications such as gaming. The Fusion Embedded Development Kit is not populated with DIP switches; however, you can utilize any unused debug pins available.

Table 3-1 • **Push-Button Switches**

Push-Button Switch	Comment
SW1	Push-button reset switch (refer to Figure 3-4 on page 3-33)
SW2	Push-button test switch
SW3	Push-button test switch
SW4	Push-button switch for PUB. This negative active switch is connected to the PUB pin, which is a digital input to the Fusion FPGA. PUB is the connection for the external momentary switch used to turn on the 1.5 V voltage regulator (refer to Figure 3-6 on page 3-34).

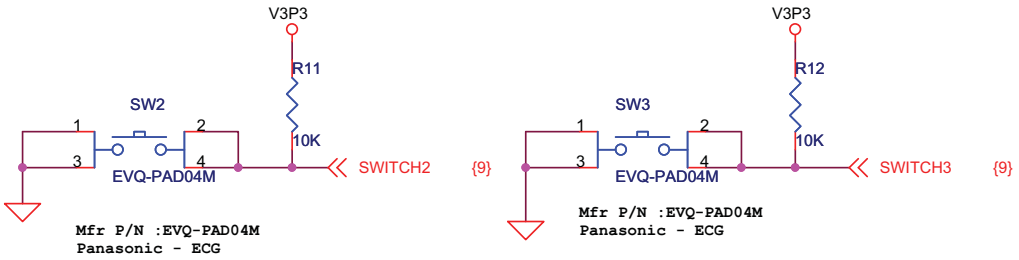

Figure 3-5 • **Push-Button Switches Schematic**

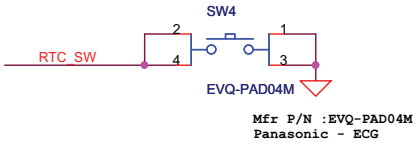

Figure 3-6 • **Push-Button Switch for PUB**

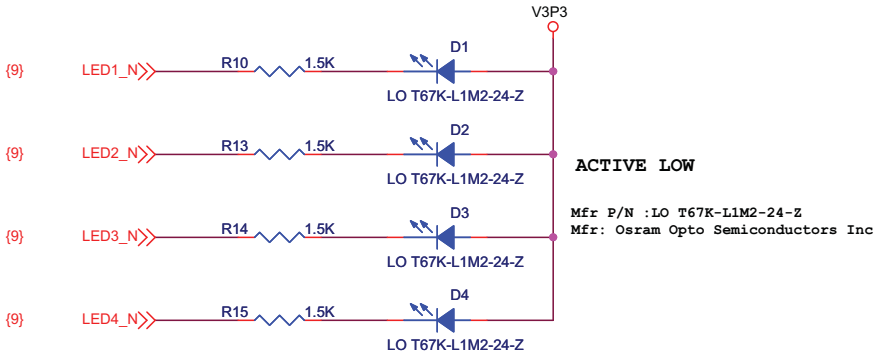

Figure 3-7 • **LEDs Schematic**

I2C Interface and EEPROM

Two Inter-Integrated Circuit (I2C) headers, J14 and J15, with pull-up resistors and an I2C EEPROM (U19) are provided on-board to showcase the I2C capabilities of this embedded development kit (Figure 3-8 and Figure 3-9). These standard I2C interface signals are directly connected to the Fusion FPGA and can extend the capabilities of this embedded system.

Any standard I2C controller can be implemented or instantiated in the Fusion FPGA to allow communication with the I2C interface. In addition, Actel IP catalog includes various programmable I2C controllers, specifically CoreI2C with an APB interface that can be instantiated in the FPGA design with a Cortex-M1 embedded processor. CoreI2C controller supports both Master and Slave modes with configurable parameters for various applications. To further evaluate the ability of the M1-enabled Fusion embedded system to communicate with an I2C device on this development kit, the board is populated with an EEPROM and OLED display with I2C interfaces.

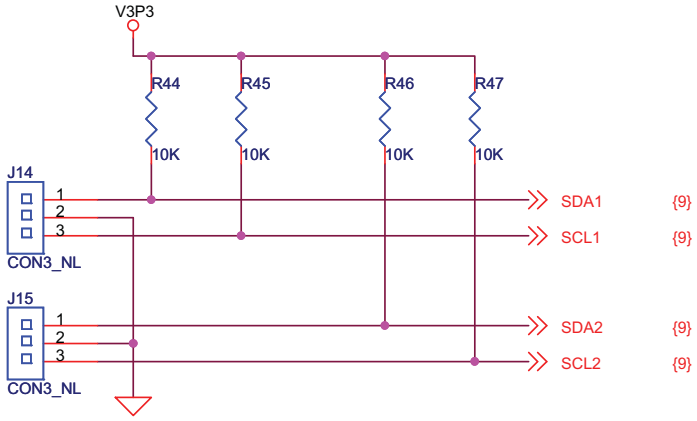

Figure 3-8 • **I2C Interface Schematic**

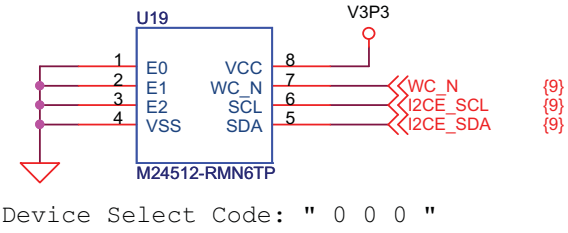

Figure 3-9 • **I2C EEPROM Schematic**

OLED Display

A 96×16-pixel low-power blue organic light emitting diode (OLED) is available on the board for display (Figure 3-10). The OLED features another I^2C interface in this embedded development kit. It is capable of displaying sharp gaming images or text. For example, the Fusion FPGA RTC current time or time between two events can be displayed on the OLED.

Additional information on this OLED component is available at the Fusion Embedded Development Kit main webpage:

http://www.actel.com/products/hardware/devkits_boards/fusion_embedded.aspx

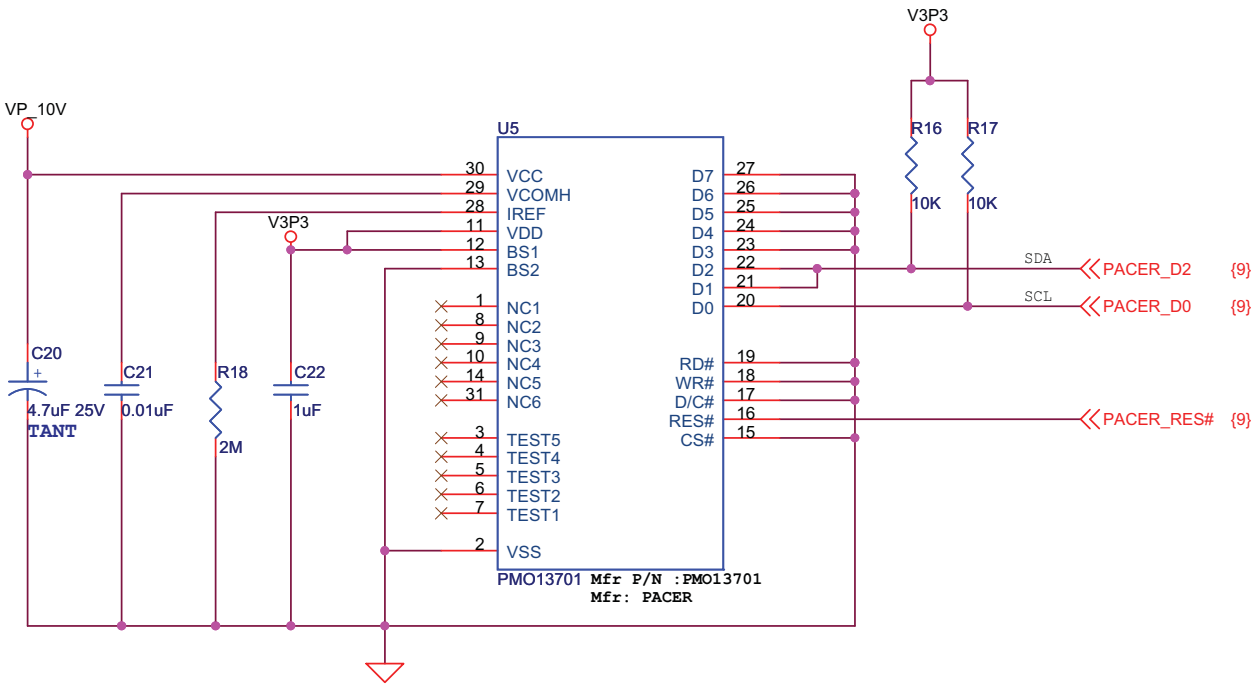

***Figure 3-10* • OLED Display Schematic**

Interface Connector

A standard interface connector on the board can be used extend this embedded development kit to connect with additional daughter cards, some of which are developed by partners and third party vendors (Figure 3-11). The interface possibilities are numerous, such as flash and SRAM memory interfaces, keyboard (HMI) interfaces, LCD interfaces, and motor control interfaces.

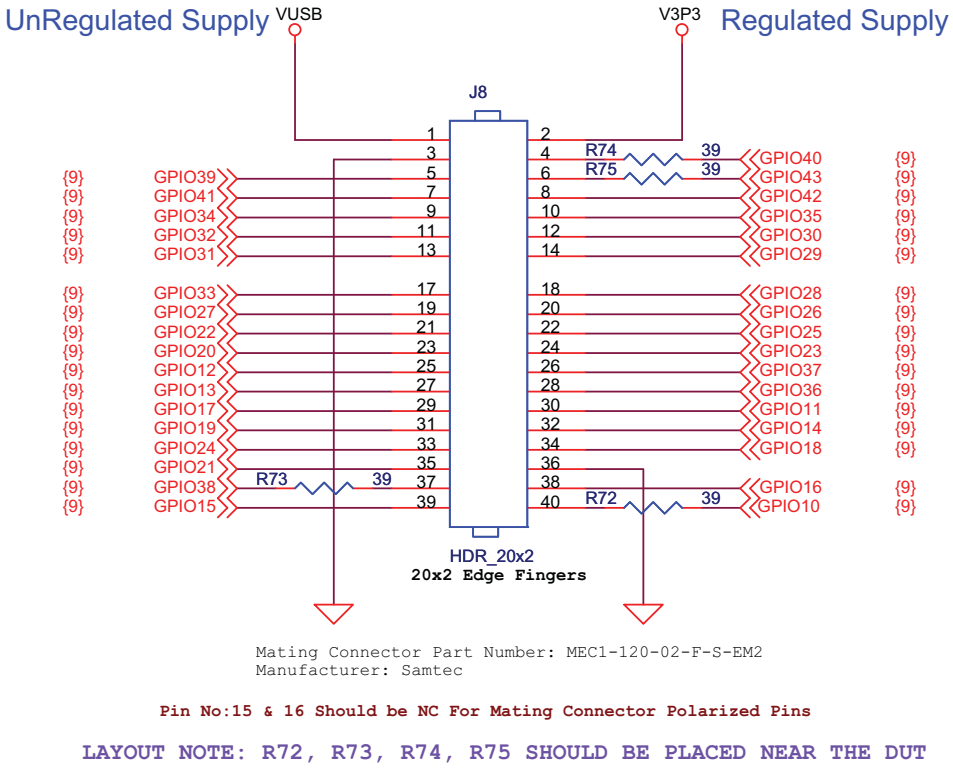

***Figure 3-11* • Interface Connector Schematic**

RealView Header

One 10×2 RealView Header is provided on the board for debugging (Figure 3-12). This header allows RealView software development tools to easily debug or configure the embedded Cortex-M1 processor during board bring-up.

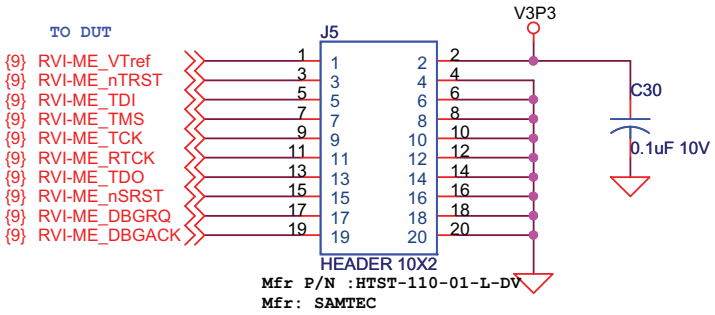

***Figure 3-12* • RealView Header Schematic**

Ethernet Interface

One Ethernet interface and a low-power 10/100 Mbps single-port Ethernet physical layer transceiver (U10) are provided on-board (Figure 3-14 on page 3-39). The Ethernet physical layer features integrated sub-layers to support both 10BASE-T and 100BASE-TX Ethernet protocols. These sub-layers ensure compatibility and interoperability with many other standard-based Ethernet solutions.

Two LEDs are populated on the Fusion Embedded Development Kit board for this ethernet interface. One is for speed and the other is for activity. Refer to the Ethernet physical layer datasheet on the Fusion Embedded Development Kit main webpage for additional information:

http://www.actel.com/products/hardware/devkits_boards/fusion_embedded.aspx

The Ethernet RJ45 interface and physical layer, along with an Ethernet Media Access Controller (MAC) that can be programmed onto the M1-enabled Fusion FPGA serves many purposes. For example, this interface can be utilized to access the Fusion FPGA to monitor the ADC data over a network (Figure 3-13). The embedded system memory and control registers can be accessed and processed remotely to support system management. The Actel IP catalog includes a Core10100 Ethernet MAC with Host Controller.

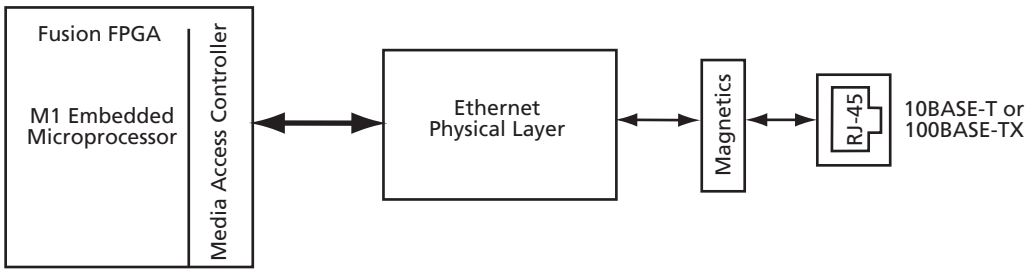

***Figure 3-13* • Typical Application**

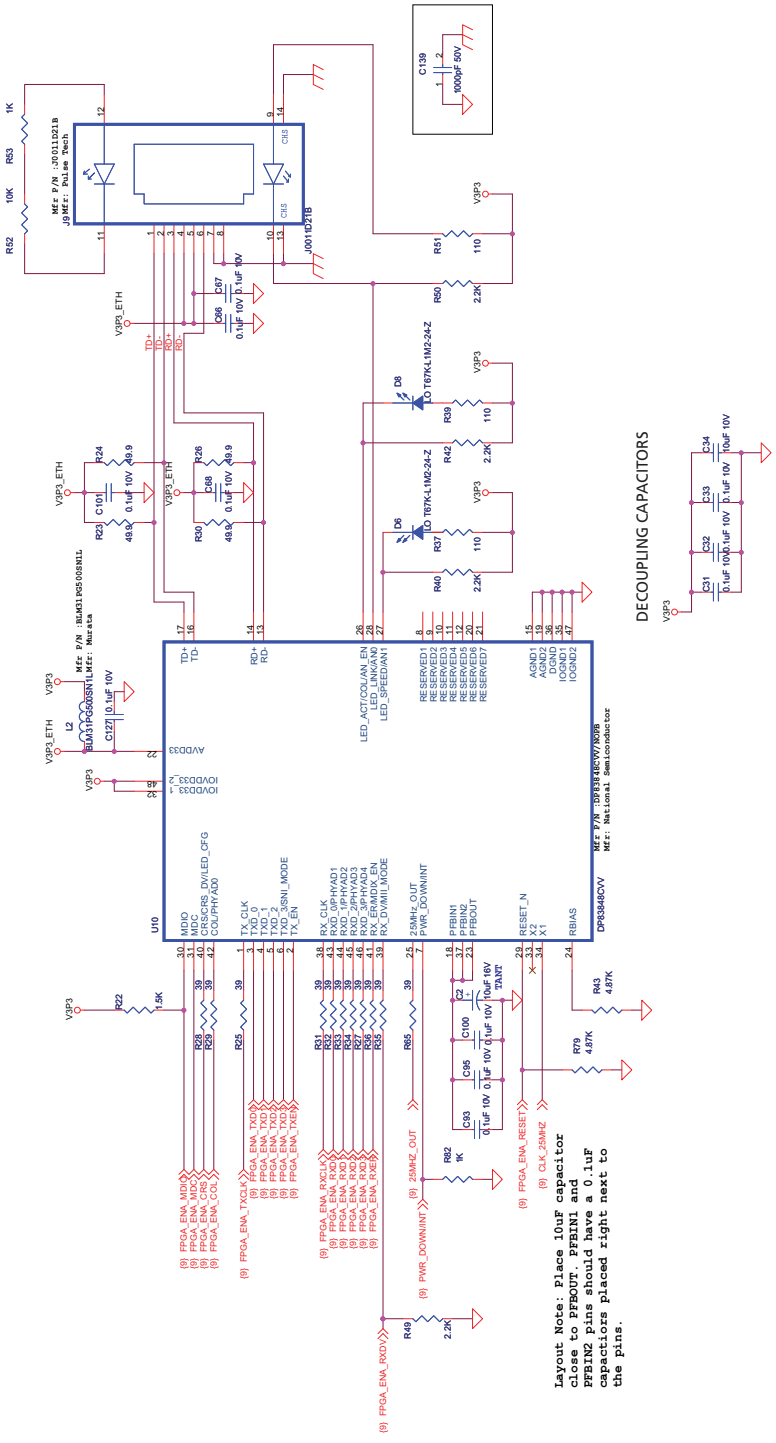

Figure 3-14 • **Ethernet Interface Schematic**

USB-to-UART Interface

Included on the evaluation board is a USB-to-UART interface with ESD protection (Figure 3-15 on page 3-41). This interface includes an integrated USB-to-UART bridge controller (U6) to provide a standard UART connection with the Fusion FPGA. Any standard UART controller can be implemented in the Fusion FPGA to allow access with this interface. In addition, the Actel IP catalog includes various UART controllers, specifically CoreUARTapb, with an AMBA APB interface that can be instantiated in the FPGA with a Cortex-M1 embedded processor. The programmable CoreUARTapb controller supports both asynchronous and synchronous modes with configurable parameters for various applications.

One application of the USB-to-UART interface is to allow HyperTerminal on a PC to communicate with the Fusion FPGA. HyperTerminal is a serial communications application program that can be installed in the Windows® operating system. A basic HyperTerminal program is usually distributed with Windows. With a USB driver properly installed, and the correct COM port and communication settings selected, you can use the HyperTerminal program to communicate with a design running on the Fusion FPGA device.

Information on the USB-to-UART bridge datasheet and device drivers are available at the Fusion Embedded Development Kit website:

http://www.actel.com/products/hardware/devkits_boards/fusion_embedded.aspx

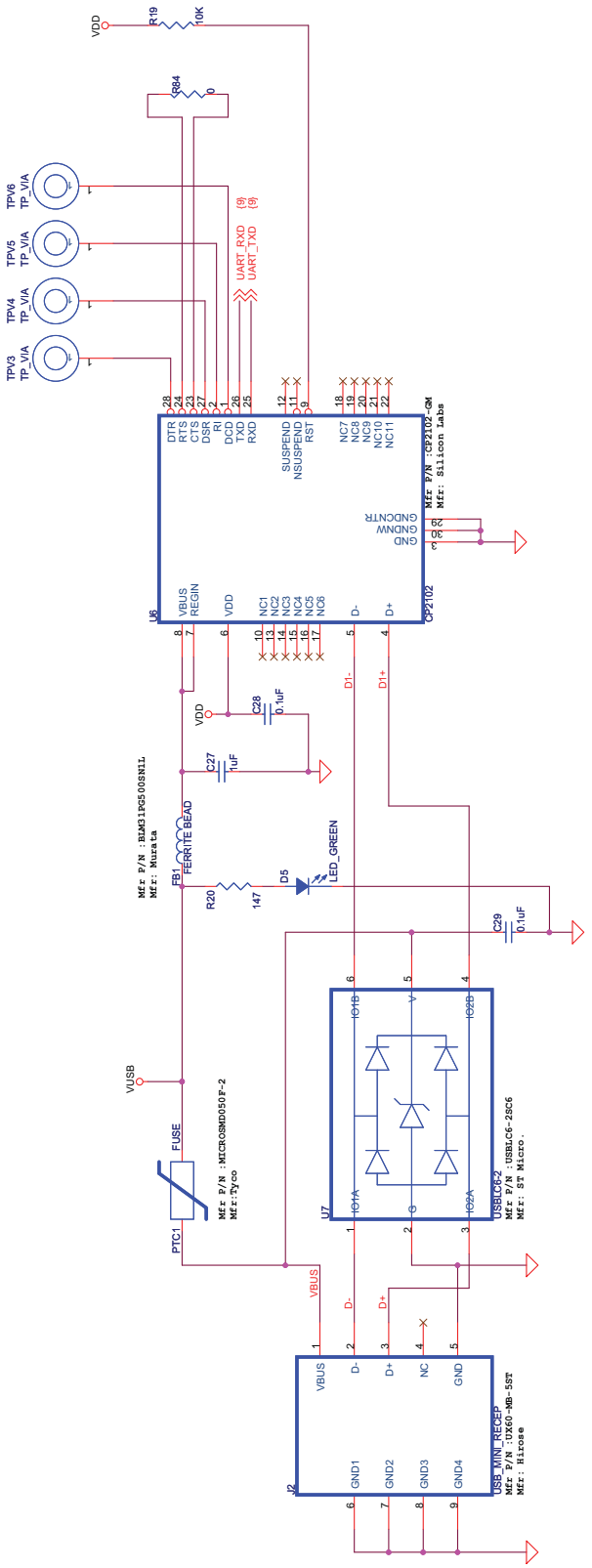

Figure 3-15 • **USB-to-UART Interface Schematic**

SRAM Components

Two SRAM components are provided on this M1-embedded Fusion Embedded Development Kit board, totaling 512 Kbytes of memory. Each SRAM has a 16-bit data bus interface to achieve a 32-bit data bus. In addition to the embedded flash memory in the Fusion FPGA, these on-board SRAMs extend the memory space of the system and can be easily accessed by an embedded processor, such as Cortex-M1 (Figure 3-16).

In a embedded processor system, these on-board SRAM can be accessed by a standard memory controller, such as CoreMemCtrl (available from Actel's IP catalog). For additional information on these SRAM components, visit the Fusion Embedded Development Kit main webpage:

http://www.actel.com/products/hardware/devkits_boards/fusion_embedded.aspx

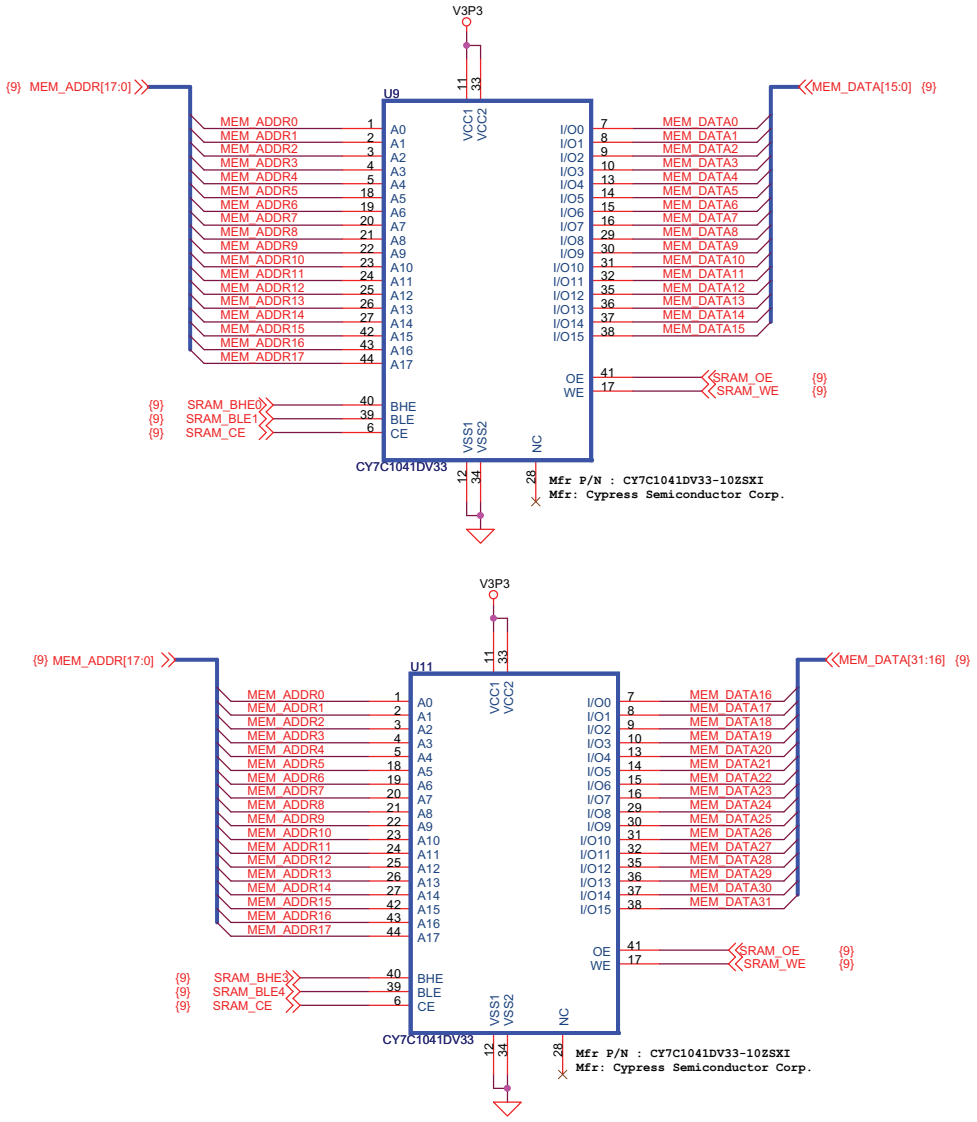

Figure 3-16 • **SRAM Components Schematic**

SPI Flash

One 2-MByte flash memory with SPI interface is available on the board and can be used by an embedded CoreABC or a Cortex-M1 embedded microprocessor to access additional memory off-chip. The flash interface, serial peripheral interface (SPI), is a synchronous serial data link standard. In an embedded microprocessor system, CoreSPI (available from Actel's IP catalog) can be instantiated to communicate with the SPI flash. Some advantages of the SPI interface are full duplex communication and higher throughput than I^2C. In the schematics shown in Figure 3-17, either the Winbond or Atmel SPI flash will be populated on this Fusion Embedded Development Kit board.

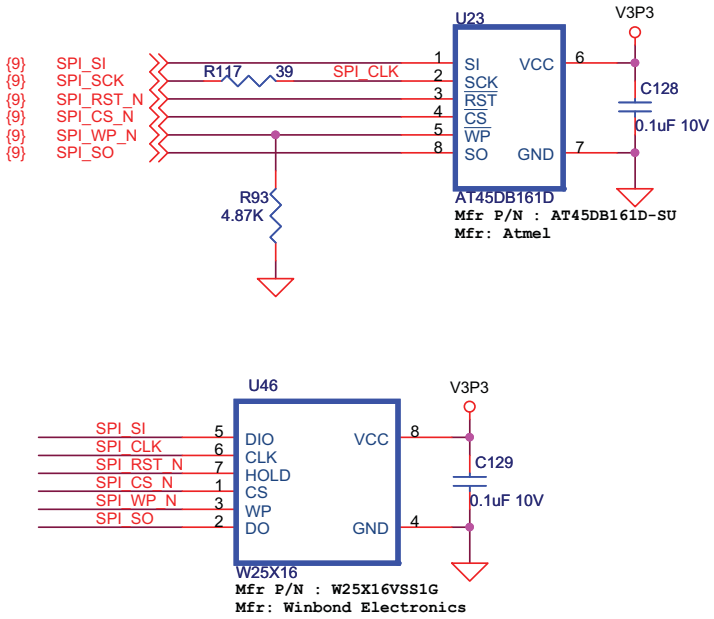

Figure 3-17 • **SPI Flash Schematic**

Note: Only one of the two SPI flash schematics shown here will be populated on the board.

Low-Cost Programming Stick (LCPS)

This Fusion Embedded Development Kit board can be programmed by the low-cost programming stick (LCPS, Figure 3-18). The LCPS is a special version of the FlashPro3 programming circuitry that is compatible with FlashPro3 and the generic FlashPro programming software.

The LCPS, like this Fusion Embedded Development Kit board, is RoHS-compliant and is completely lead (Pb) free. To use the LCPS with the FlashPro software, select the FlashPro3 from the list of programmer types. The LCPS behaves exactly as if it were a regular encased FlashPro3 programmer. The 12-pin female connector socket is designed to interface to the 12-pin right-angle male header on the Fusion Embedded Development Kit board. One of the pins is a special VJTAGENB signal that goes high when programming is taking place and returns to a low level when programming has completed. The Fusion Embedded Development Kit board uses this signal to effect a change in the value of V_{CC} from 1.2 V to 1.5 V, which is required for programming Fusion FPGA devices.

You do not need to have the LCPS connected to the Fusion Embedded Development Kit board to operate once the FPGA has been programmed. The Fusion Embedded Development Kit board requires the LCPS connected only during programming.

The LCPS programs the FPGA through the JTAG pins. Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). V_{CC} must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and V_{CC} to the Fusion part must be supplied to allow JTAG signals to transition the Fusion device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND. Refer to the schematic in Figure 3-19 on page 3-45.

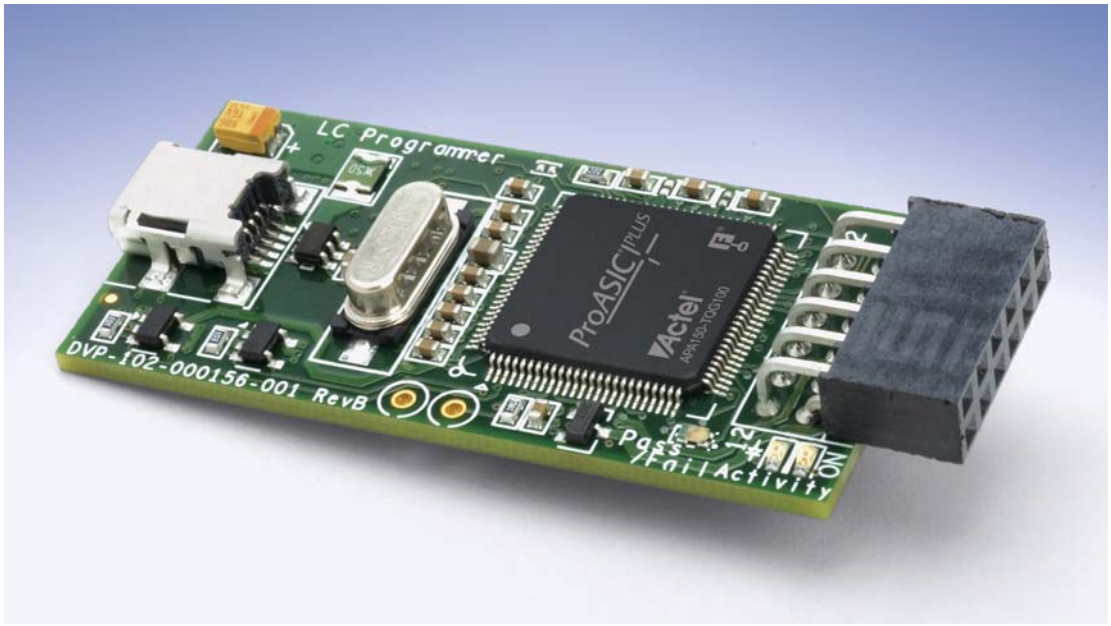

Figure 3-18 • **Low-Cost Programming Stick**

Note: The LCPS supplied with this kit is intended for use with the Fusion Embedded Development Kit. An LCPS supplied for other kits, although electrically and functionally equivalent, may not connect seamlessly with the Fusion Embedded Development Kit board.

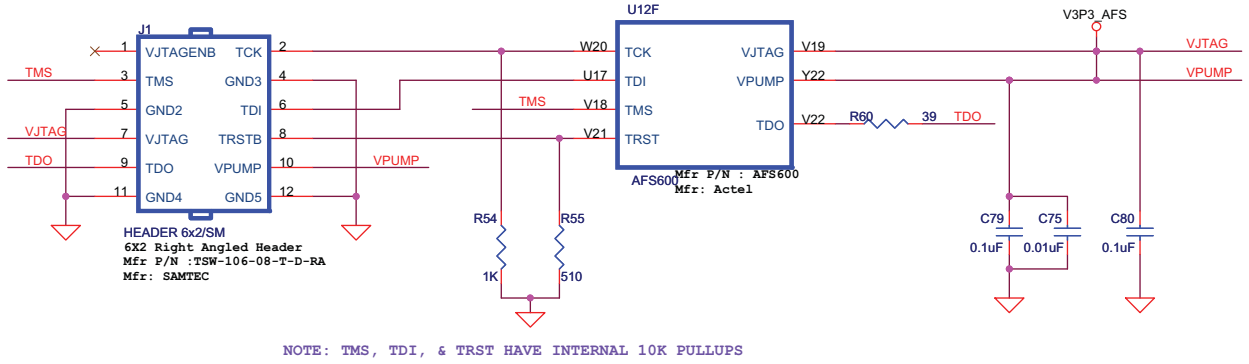

Figure 3-19 • **JTAG Header Schematic for LCPS Connection**

Low-Cost Programming Stick (LCPS): Stackup

The LCPS is built on a four-layer PCB with the layers arranged in the following stackup:

1. Top signal layer (Figure 3-19 on page 3-45)
2. Ground plane
3. Power plane
4. Bottom signal layer (Figure 3-20 on page 3-46)

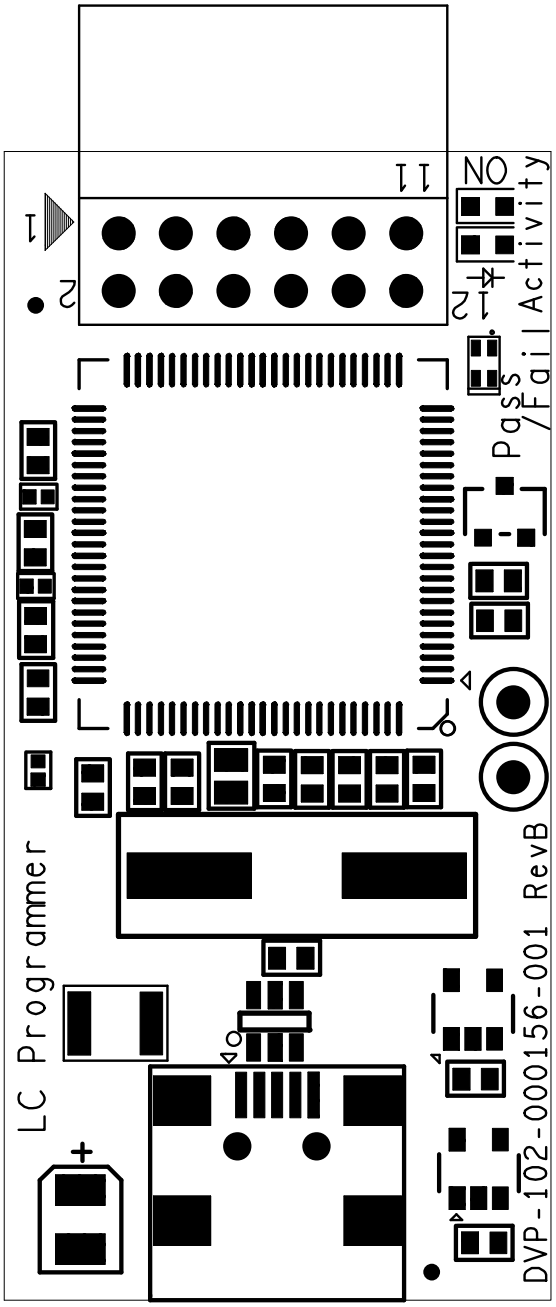

Figure 3-20 • **Low-Cost Programming Stick (LCPS) Stackup (Top Silkscreen)**

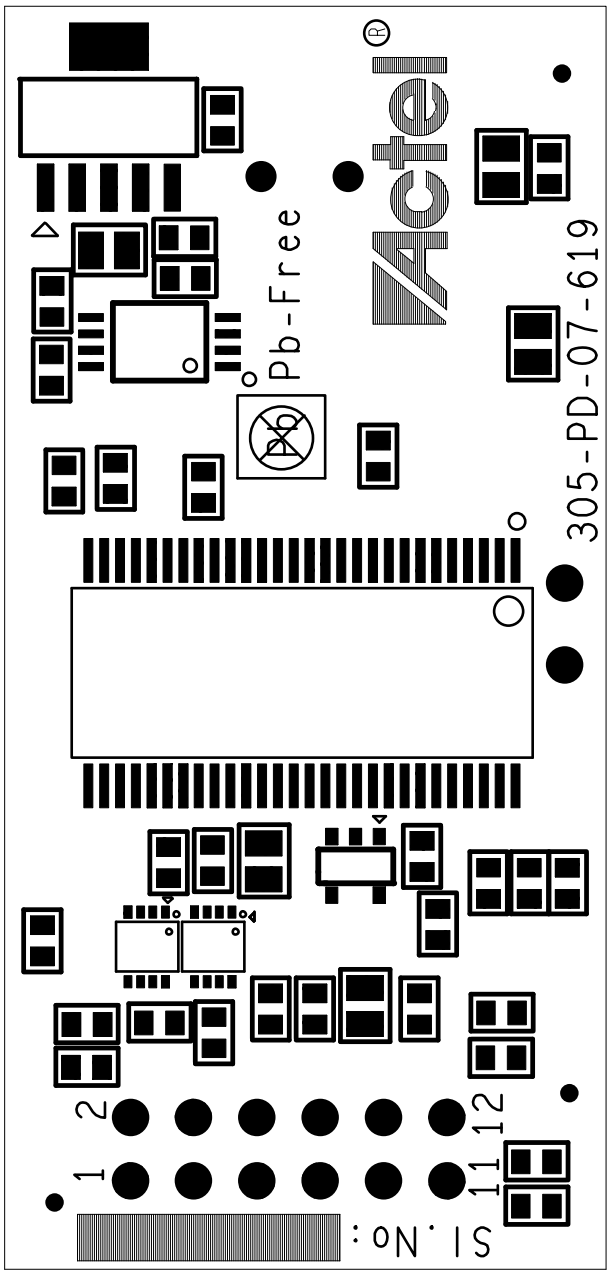

Figure 3-21 • **Low-Cost Programming Stick (LCPS) Stackup (Bottom Silkscreen)**

4 – Programming the Fusion FPGA

1. To program a design into the Fusion FPGA, attach the low-cost programming stick (LCPS) to the Fusion Embedded Development Kit board's 12-pin header.
2. Attach one end of the USB cable to the LCPS and the other end to the programming PC.
3. Set power source jumper (J40) to connect pins 1 and 2. Connecting pins 1 and 2 will select USB as the power source. Attach one end of the USB cable to the USB interface of the board and the other end to a PC (Figure 4-1).

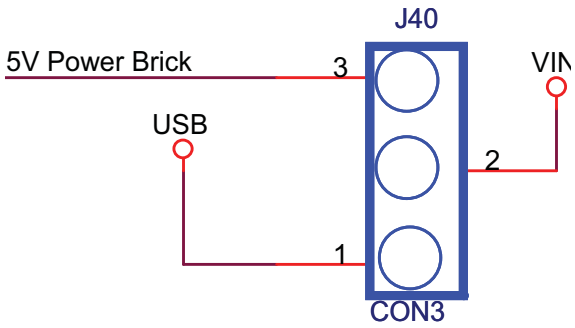

Figure 4-1 • **Power Source Jumper Schematic**

4. Once the USB cables are connected, launch the Actel FlashPro programming software. When using the FlashPro programming software, the programmer selects FlashPro3. The LCPS is functionally equivalent to a FlashPro programmer, but designed specifically for use with this Fusion Embedded Development Kit.
5. Click on the **New Project** button to create a new project. Set a user define project name and location.
6. Click on the **Configure Device** button.
7. In the Device Configuration window, **Browse** and select the programming database (PDB) file or STAPL (STP) file.
8. Once the programming database file is loaded, click on the **PROGRAM** button to start programming the Fusion FPGA. The activity LED on the LCPS should begin blinking.
9. When the programming successfully completes, remove the LCPS and then press the system reset button on the Fusion Embedded Development Kit board to reset the system.
10. Verify that your design is working.

5 – Demonstration Design

Fusion Embedded Development Kit Demo

The first production run of the Fusion Embedded Development Kit was programmed only with the manufacturing test design. Newer boards are programmed with the Webserver demo design. If, when you power up your board, you do not see the functions described below, program your board with the demo design file:

www.actel.com/download/rsc/?f=M1AFS_EMBEDDED_KIT_PF

Running the Pre-Programmed Design

The design can be run in two modes: PIO mode and Webserver mode. On device reset, a menu appears on the organic light-emitting diode (OLED). The options available in this menu are:

- PIO – SW2
- Webserver – SW3

PIO Mode

Pressing SW2 will display M1AFS EMBEDDED KIT. Push SW2 again to access the PIO main menu. The OLED displays the main menu options below. Press SW3 to step through individual readings in each mode.

- Multimeter mode (press SW2 once for Multimeter mode)
- Use the potentiometer (POT) to vary the input voltage.
- DAC mode (press SW2 two times for DAC mode)
- Use the POT to vary the input voltage.
- Auxiliary mode (press SW2 three times for Auxiliary mode)
- This mode allows external inputs to the board. Refer to the kit user's guide for more information.
- Self-Wakeup mode (press SW2 four times for Self-Wakeup mode)
- All LEDs except for the green one will turn off. The Fusion device will then restart from the beginning with the Options menu.

Webserver Mode

The Webserver demonstration can be run in two ways. If connected directly to the internet, it will use the local area network (LAN) with a dynamic host configuration protocol (DHCP) server; if connected only to a PC through a loopback cable, it will use the LAN without a DHCP server. Some features will not operate fully when using the loopback cable. Refer to the *Fusion Embedded Development Kit Webserver Demo User's Guide* for more information.

Press SW3 to enter Webserver mode. The OLED displays a static internet protocol (IP) address for the board. The value will vary, but one example is shown in Figure 5-1.

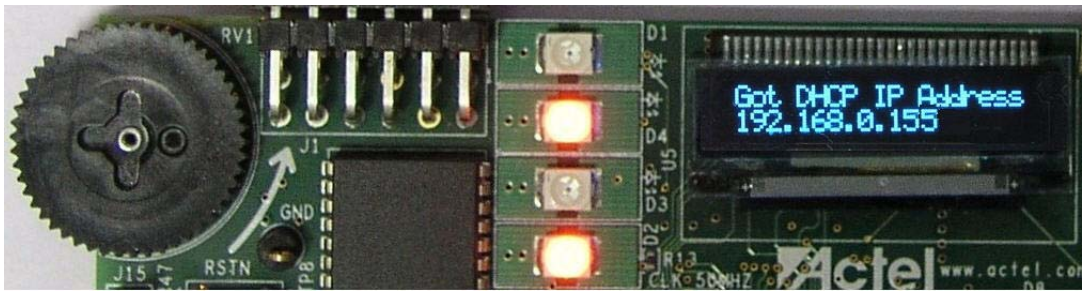

Figure 5-1 • **IP Address Example**

If the board is connected to the internet or connected through a loopback cable, you can open a web browser and enter the IP address shown on your OLED display. For the example above, enter:

http://192.168.0.155 (yours will be different)

This will open a web page and you can then step through various features (Figure 5-1):

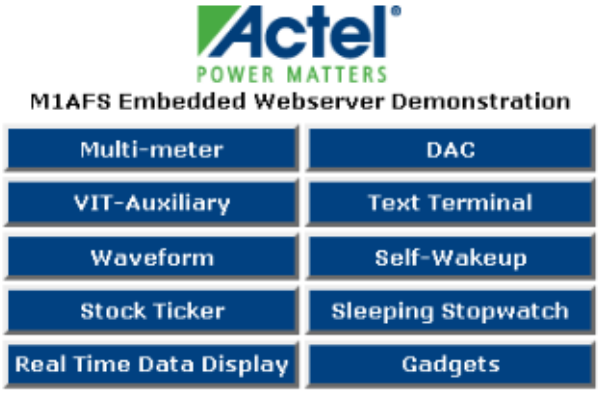

Figure 5-2 • **Webserver Demonstration Menu**

A – Resources

Fusion Embedded Development Kit
http://www.actel.com/products/hardware/devkits_boards/fusion_embedded.aspx

Fusion Overview
http://www.actel.com/products/fusion/default.aspx

Fusion Datasheet
http://www.actel.com/documents/Fusion_DS.pdf

Fusion FPGA Fabric User's Guide
http://www.actel.com/documents/Fusion_UG.pdf

Libero IDE Design Software
http://www.actel.com/products/software/libero/default.aspx

B – Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650.318.8044**

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support website (www.actel.com/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 a.m. to 6:00 p.m., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 a.m. to 6:00 p.m., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/company/contact/default.aspx.

Index

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