



# FSA831A — USB2.0 High-Speed (480Mbps) Charger Detection with Isolation Switch

## Features

USB Detection	USB Battery Charging Rev. 1.2 Supports Data Contact Detect (DCD) Dead Battery Provision (DBP) with 30-Minute Timer
Switch Type	Isolation Switch Closes for Charging Downstream Port (CDP) Standard Downstream Port (SDP)
V <sub>BUS</sub>	28 V Over-Voltage Tolerance -2 V Under-Voltage Tolerance
Package	10-Lead MicroPak™ 1.6 x 2.1 mm, 0.5 mm Pitch
Ordering Information	FSA831AL10X

## Description

The FSA831A is a charger-detection IC with an integrated isolation switch for use with a micro/mini USB port. The FSA831A detects battery chargers and is compliant with USB Battery Charging Specification, Rev 1.2 (BC1.2). The algorithm incorporates Data Contact Detection (DCD), which ensures that the shorter, inner pins of the USB connector are making contact prior to continuing with battery charger detection. The device determines if a Dedicated Charging Port (DCP), Charging Downstream Port (CDP), or a typical PC host, called a Standard Downstream Port (SDP), is connected. If a charger is detected, the FSA831A determines whether the charger is a DCP or CDP. For SDP and CDP detection, an internal isolation switch is closed to connect the D+/D- lines of the USB cable to the resident USB transceiver within the portable device. The FSA831A conforms to all the constraints for the Dead Battery Provision (DBP) within the BC1.2 specification, including a 30-minute timer that cannot exceed 45 minutes, per BC1.2.

## Applications

- MP3, Mobile Internet Device (MID), Cell Phone, PDA, Digital Camera, Notebook and Netbook

## Related Resources

- For samples and questions, please contact: [analogswitch@fairchildsemi.com](mailto:analogswitch@fairchildsemi.com).

## Typical Application

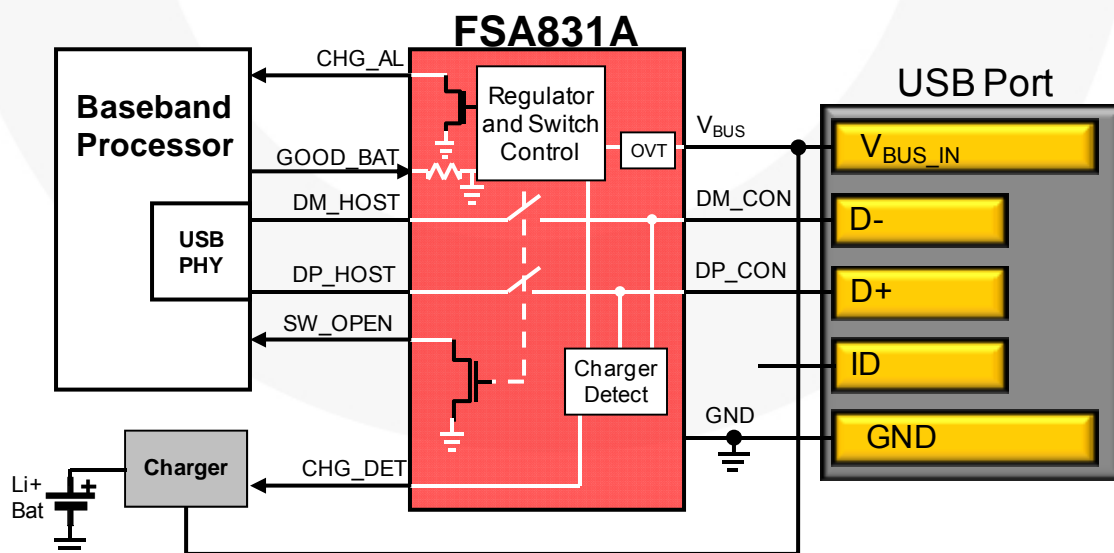


Figure 1. Mobile Phone Example

## Pin Configurations

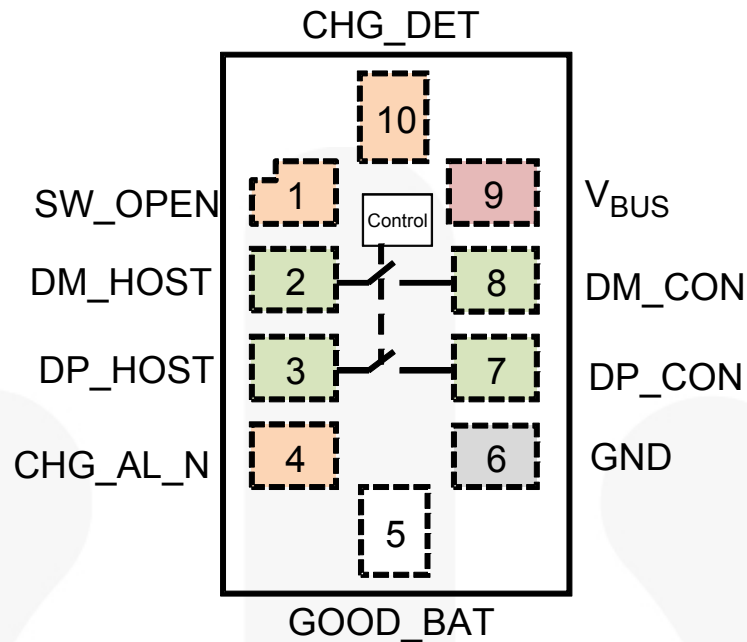


Figure 2. Pin Assignments (Top View)

## Pin Descriptions

Name	Pin #	Description
<b>USB Interface</b>		
DP_HOST	3	D+ signal connected to the resident USB transceiver on the phone
DM_HOST	2	D- signal connected to the resident USB transceiver on the phone
<b>Connector Interface</b>		
V <sub>BUS</sub>	9	Input voltage supply pin to be connected to the V <sub>BUS</sub> pin of the USB connector
GND	6	Ground
DP_CON	7	Connected to the USB connector D+ pin
DM_CON	8	Connected to the USB connector D- pin
<b>Status Outputs</b>		
CHG_DET	10	CMOS push/pull output connected to charger IC for indicating if a charger has been detected (LOW=charger not detected, HIGH=DCP or CDP charger has been detected).
SW_OPEN	1	Open-drain output pin; requires pull-up resistor to I/O voltage supply (LOW=switch closed, Hi-Z=switch open).
CHG_AL_N	4	CMOS open-drain output pin (LOW=V <sub>BUS</sub> is valid and charge is allowed to be drawn from V <sub>BUS</sub> , Hi-Z=V <sub>BUS</sub> is not at a valid voltage).
<b>Input Pin</b>		
GOOD_BAT	5	Input that indicates if the battery is a good battery or a dead battery (LOW=dead battery, HIGH=good battery).

Table 1. Functionality

Device Detected	GOOD_BAT	SW_OPEN	CHG_AL_N	CHG_DET	DP_HOST	DM_HOST	DP_CON	DM_CON
DCP	X	Hi-Z	LOW	HIGH	Hi-Z	Hi-Z	V <sub>DP_SRC</sub>	Hi-Z <sup>(1)</sup>
CDP	HIGH	LOW	LOW	HIGH	DP_CON	DM_CON	DP_HOST	DM_HOST
CDP	LOW	Hi-Z	LOW	HIGH	Hi-Z	Hi-Z	V <sub>DP_SRC</sub>	Hi-Z
SDP <sup>(2)</sup>	HIGH	LOW	LOW	LOW	DP_CON	DM_CON	DP_HOST	DM_HOST
SDP <sup>(2)</sup>	LOW	Hi-Z	LOW	LOW	Hi-Z	Hi-Z	V <sub>DP_SRC</sub>	Hi-Z
SDP, CDP, or DCP plugged in and after 30-minute timer expires	LOW	Hi-Z	Hi-Z	LOW	Hi-Z	Hi-Z	Hi-Z	Hi-Z
V <sub>BUS</sub> < V <sub>BUS</sub> valid to V <sub>BUS</sub> > V <sub>BUS</sub> valid operation prior to completing detection of SDP, CDP, or DCP. Upon detection, all outputs switch as in rows above.	X	Hi-Z	Hi-Z	Hi-Z to LOW	Hi-Z	Hi-Z	Hi-Z	Hi-Z

**Notes:**

1. Hi-Z is the internal state of DM\_CON. Since a DCP has been detected, DM\_CON is shorted to DP\_CON externally and DM\_CON is shorted to V<sub>DP\_SRC</sub>.
2. Proprietary chargers that leave DP\_CON and DM\_CON floating are detected as SDP. Proprietary chargers that force DP\_CON=2V and DM\_CON=2.7 V (or any other voltages) can be detected as CDP, DCP or SDP depending on the resistances of the resistor dividers on DP\_CON and DM\_CON used to create the voltages on those pins.

## Functional Description

### Data Contact Detect (DCD)

DCD relies on the D+ and D- lines being present. DCD waits until the internal timeout ( $t_{DCD\_TIMEOUT}$ ) has expired in the following cases:

- If a charger does not have a D+ pin on the USB connector
- If the D+ pin is not shorted to D- pin on the connector
- If D+ is pulled up to a supply
- If D+ does not have a sufficient path to ground to defeat a pull-up  $I_{DP\_SRC}$  (10  $\mu$ A typical) current source.

The FSA831A proceeds with charger detection even though it is unlikely a charger is present. If there is no charger, the algorithm reports an SDP and closes the switch. If a device is pulling D+ HIGH, this voltage presents itself to the USB transceiver or Physical Layer Interface (PHY) block within a System on Chip (SoC) after the switch is closed.

If the DCD timeout was insufficient and the PHY block is so equipped, DCD and the charging algorithm can be repeated in the PHY block. The stipulation is that the total time from  $V_{BUS}$  valid to USB transceiver connection with a 1.5 k $\Omega$  pull-up to 3.3 V must be one (1) second, per USB 2.0 standards (USB 2.0 connect timing), provided the portable device does not have a dead battery.

A typical PS/2 port (old PC mouse / keyboard port) has a resistive pull-up to  $V_{BUS}$ . This can cause the DCD to exceed the maximum wait time ( $t_{DCD\_TIMEOUT}$ ) and proceed to charger detection. The likely path through charger detection is classifying the PS/2 port as an SDP port. This results in closing the USB switches, which causes the voltage on the DP\_CON and DM\_CON pins to pass through the switch to DP\_HOST and DM\_HOST, respectively. Since voltages on the PS/2 port can go as high as the  $V_{BUS}$  voltage, the DP\_HOST and DM\_HOST pins can be pulled up to  $V_{BUS}$ . The USB PHY connected to DP\_HOST and DM\_HOST must be equipped to handle these higher voltages.

### CHG\_AL\_N Output and Output Timing

CHG\_AL\_N output indicates that charge is allowed to be drawn from  $V_{BUS}$  when CHG\_AL\_N is LOW. When FSA831A first powers up and prior to detection, the CHG\_AL\_N pin can follow  $V_{BUS}$  up to 28 V, which is the absolute maximum  $V_{BUS}$  voltage allowed. Whenever  $V_{BUS}$  is at GND, the FSA831A is completely off and the switches and all I/Os are in the Hi-Z state. When  $V_{BUS}$  climbs above the valid  $V_{BUS}$  threshold, detection occurs automatically and CHG\_DET, SW\_OPEN, and CHG\_AL\_N all simultaneously switch to the states indicated in Table 1 if GOOD\_BAT is HIGH (see *Dead Battery Provision description for GOOD\_BAT = LOW*).

### Dead Battery Provision (DBP)

BC1.2 and USB 2.0 allow a portable device (defined as a device with a battery) with a dead battery to take a maximum of 100 mA from the USB  $V_{BUS}$  line for a maximum of 45 minutes as long as the portable device forces the D+ line to  $V_{DP\_SRC}$  (0.6 V typical). FSA831A starts detection when  $V_{BUS}$  crosses the  $V_{BUSVLD}$  threshold and, if it detects a CDP or

SDP and GOOD\_BAT is HIGH, automatically closes the switch and does not force the DP\_CON pin to  $V_{DP\_SRC}$ .

Once the charger detection is completed, the FSA831A starts a 30-minute timer and forces the DP\_CON pin to  $V_{DP\_SRC}$  until the timer elapses. During the 30 minute period, if GOOD\_BAT is LOW,  $V_{DP\_SRC}$  is applied to DP\_CON and the D+/D- switches are opened. If GOOD\_BAT is HIGH,  $V_{DP\_SRC}$  is not applied to DP\_CON and the D+/D- switches are closed. If GOOD\_BAT is LOW when 30 minute timer expires; regardless of whether an SDP, CDP, or DCP was previously detected; the FSA831A removes  $V_{DP\_SRC}$  from DP\_CON and forces CHG\_DET LOW and CHG\_AL\_N to Hi-Z (SW\_OPEN remains Hi-Z). To exit this fault condition, remove  $V_{BUS}$ , wait for all the  $V_{BUS}$  Printed Circuit Board (PCB) capacitance to discharge, and re-apply  $V_{BUS}$ . Table 1 provides the functionality of the pins when the timer expires.

When GOOD\_BAT is HIGH and the battery is removed from the portable device while  $V_{BUS}$  is valid, bringing GOOD\_BAT LOW; the FSA831A opens the isolation switches on DP\_CON and DM\_CON and forces the DP\_CON pin to  $V_{DP\_SRC}$ . In this scenario, the timer generally expires because the SoC does not have a supply to bring GOOD\_BAT HIGH unless the battery that was removed is re-inserted within 30 minutes from when the USB plug is inserted.

If an SDP or CDP is inserted with GOOD\_BAT HIGH during the 30-minute timer, then GOOD\_BAT changes to LOW; SW\_OPEN changes to Hi-Z and the counter continues counting until the 30 minutes expires. If GOOD\_BAT then returns to HIGH, SW\_OPEN changes to LOW and finishes out the 30-minute time.

GOOD\_BAT has an internal pull-down resistor to ensure it is LOW when the SoC is powered down. This input is designed to have very low thresholds to interface with low-voltage SoCs driven with 1.2 V supplies.

### Proprietary Chargers

Only legitimate USB chargers that force  $V_{DM\_SRC}$  (0.6V typical) on DM\_CON when  $V_{DP\_SRC}$  is applied to DP\_CON are detected by the FSA831A and cause CHG\_DET signal to be asserted. Any charger that forces a HIGH on both DP\_CON and DM\_CON can be detected as CDP, DCP, or SDP (depending on the resistances of the resistor dividers on DP\_CON and DM\_CON) and used to create the HIGH voltages on those pins. Any charger that lets both DP\_CON and DM\_CON signals float is detected as an SDP and CHG\_DET stays de-asserted. In cases where the proprietary charger is detected as an SDP or CDP, since the switches are closed and access is made from the USB connector D+ and D- lines to the USB PHY block; the chargers can be detected within the PHY if so equipped

### Ground Drops

When a DCP is detected,  $V_{DP\_SRC}$  is forced on DP\_CON provided GOOD\_BAT is HIGH or if GOOD\_BAT is LOW and the DBP timer has not expired. For current up to 1.5 A flowing into the  $V_{BUS}$  and GND lines of the USB cable, this can translate to substantial ground drops that lift the ground of the portable device. This drop adds to the voltage at the

DP\_CON pin as seen from the DCP D+ pin. For the maximum ground drop of 375 mV specified in the BC1.2 specification and for the maximum  $V_{DP\_SRC}$  of 0.7 V, the voltage as seen by the DCP would be 1.075 V. Smart DCPs that rely on this voltage detection to determine attach and detach detection need to take this into account.

### $V_{BUS}$ Tolerance

When  $V_{BUS}$  rises, an internal Power On Reset (POR) detects this voltage and prepares the FSA831A for charger detection.

$V_{BUS}$  voltages up to 28 V can be tolerated by the  $V_{BUS}$  pin.  $V_{BUS}$  can tolerate voltages up to -2 V for cases where a charger is plugged in backwards.

### Detection Flow

The flow diagram in Figure 3 shows how the FSA831A achieves battery charger detection consistent with BC1.2.

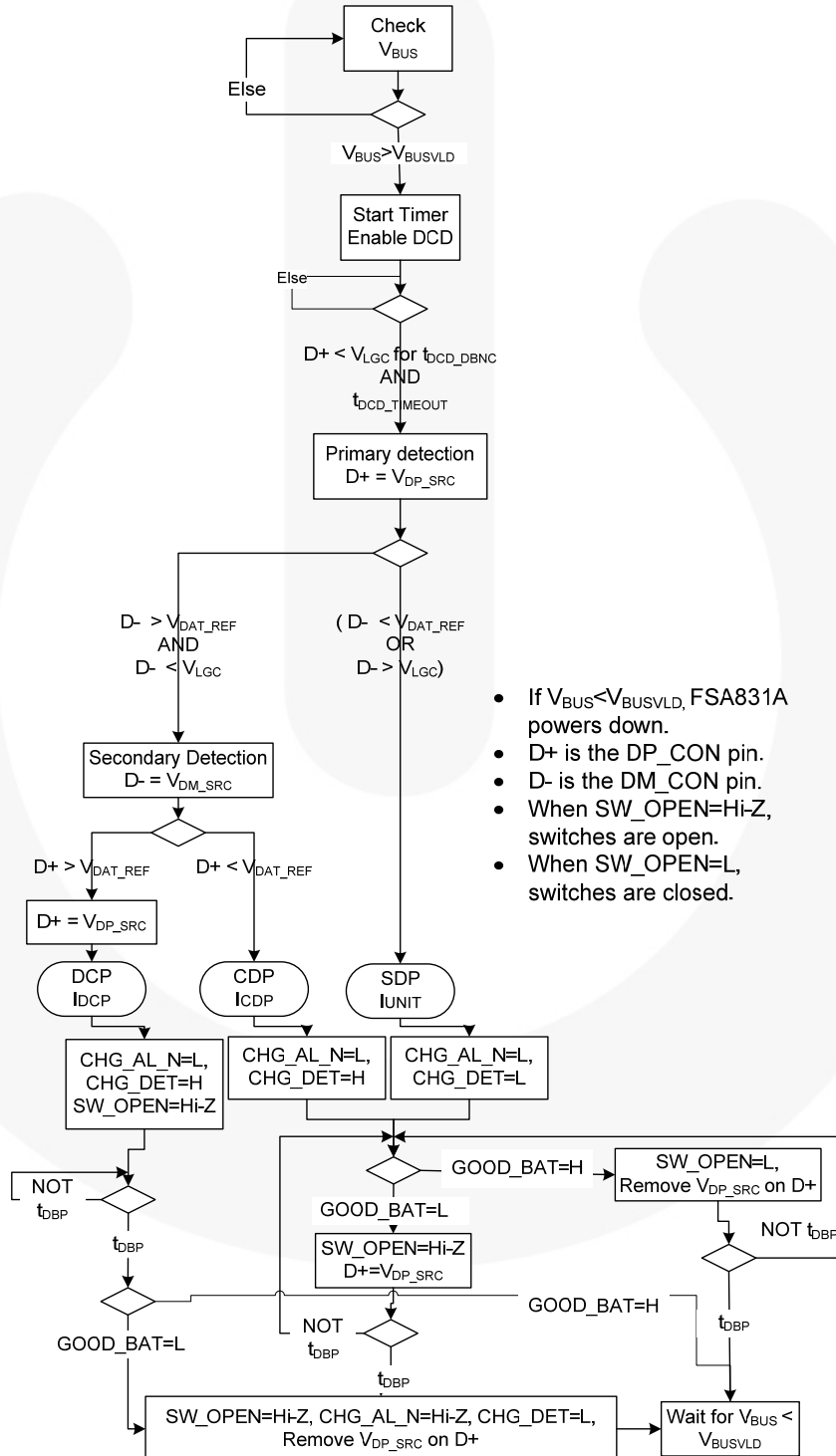


Figure 3. Battery Charger Detection

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V <sub>BUS</sub>	Voltage from USB Connector		-2	28	V
V <sub>SW</sub>	USB Switch I/O Voltage (DP_CON, DM_CON, DP_HOST, DM_HOST)		-0.5	6.0	V
I <sub>SW</sub>	USB Switch Current (DP_CON to DP_HOST, DM_CON to DM_HOST)		-30	+30	mA
V <sub>I/O</sub>	Voltage from GOOD_BAT, CHG_AL_N, CHG_DET and SW_OPEN I/Os		-0.5	6.0	V
V <sub>CA</sub>	Voltage from CHG_AL_N Output		-0.5	28.0	V
I <sub>I/O</sub>	CHG_AL_N, CHG_DET and SW_OPEN Outputs Sink/Source Current		-5	+5	mA
T <sub>STG</sub>	Storage Temperature Range		-65	+150	°C
T <sub>J</sub>	Maximum Junction Temperature			+150	°C
T <sub>L</sub>	Lead Temperature (Soldering, 10 Seconds)			+260	°C
ESD	IEC 61000-4-2 System	USB Pins (DP_CON, DM_CON, V <sub>BUS</sub> )	Air Gap	15	kV
			Contact	8	
	Human Body Model, JEDEC JESD22-A114		All Pins	6	
	Charged Device Model, JEDEC JESD22-C101		All Pins	1	

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V <sub>BUS</sub>	V <sub>BUS</sub> Input HIGH Voltage	4	6	V
V <sub>SW</sub>	Switch I/O Voltage for USB Path	0	3.6	V
T <sub>A</sub>	Operating Temperature	-40	+85	°C

## DC Electrical Characteristics

Unless otherwise indicated,  $V_{BUS}=4\text{ V to }6\text{ V}$  and  $T_A=-40\text{ to }+85^\circ\text{C}$ . Typical values are at  $T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Status Outputs</b>						
$V_{OHCD}$	Output HIGH Voltage (CHG_DET)	$I_{OH}=-2\text{ mA}$	2.0			V
$V_{OL}$	Output LOW Voltage (CHG_DET, CHG_AL_N, SW_OPEN)	$I_{OL}=2\text{ mA}$			0.4	V
$t_{DIFF}$	Skew Between Any Output (CHG_DET, CHG_AL_N, SW_OPEN) Switching Relative to the Other Outputs Switching	$I_{IO}=\pm 2\text{ mA}$ , CHG_AL_N=20 k $\Omega$ to 5 V, SW_OPEN=10 k $\Omega$ to 1.8 V			100	ns
<b>V<sub>BUS</sub> Pin</b>						
$V_{BUSVLD}$	$V_{BUS}$ Valid Detection Threshold <sup>(1)</sup>		0.8		4.0	V
$I_{BUSIN}$	$V_{BUS}$ Input Leakage	$V_{BUS}=0\text{ V to }0.8\text{ V}$			3	$\mu\text{A}$
$I_{VBUSACT}$	$V_{BUS}$ Active Mode Average Current	USB Path Active, USB Switch Closed After Charger Detection			250	$\mu\text{A}$
$t_{OUT}$	Time from $V_{BUS}$ Valid Asserted to CHG_DET, CHG_AL_N and SW_OPEN Outputs Valid	DP_CON pulled down to GND, 15k $\Omega$ , all voltages forced on $V_{BUS}$ , DP_CON, DM_CON and GND simultaneously			250	ms
<b>Switch Characteristics</b>						
$I_{OFF}$	Power Off Leakage Current	USB Path $V_{BUS}=0\text{ V}$ , $V_{SW}=0\text{ V}$ or 3.6 V, Figure 5			10	$\mu\text{A}$
$R_{ONUSB}$	High-Speed USB Range Switch On Resistance <sup>(1)</sup>	$V_{DP\_CON} / V_{DM\_CON}=0\text{ V}$ , 0.4 V; $I_{ON}=8\text{ mA}$ ; Figure 4; $V_{BUS}=4\text{ V to }6\text{ V}$		4.5	6.5	$\Omega$
<b>Control Input</b>						
$V_{IH}$	Input HIGH Voltage (GOOD_BAT)		1.1			V
$V_{IL}$	Input LOW Voltage (GOOD_BAT)				0.5	V
$R_{PD}$	Pull Down Resistance (GOOD_BAT)		1			M $\Omega$
$I_{IN}$	Input Leakage Current (GOOD_BAT)	$V_{BUS}=5\text{ V}$ , GOOD_BAT=0 V to 4.4 V			10	$\mu\text{A}$
$I_{IOFF}$	OFF State Leakage Current (GOOD_BAT)	$V_{BUS}=0\text{ V}$ , GOOD_BAT=0 V to 4.4 V			10	$\mu\text{A}$
$t_{DBP}$	Dead Battery Provision (DBP) Timer		15	30	45	min
$t_{GB}$	Time from GOOD_BAT Asserted to SW_OPEN De-Asserted, Switches Closed and Meet the $R_{ONUSB}$ Specification				30	ms
$t_{DB}$	Time from GOOD_BAT De-asserted to SW_OPEN Asserted, Switches Opened				65	ms
<b>Battery Charger Detection Parameters from BC1.2 Specification</b>						
$V_{DAT\_REF}$	Data Detect Voltage		0.25		0.40	V
$V_{DM\_SRC}$	D- Source Voltage <sup>(2)</sup>		0.5		0.7	V
$V_{DP\_SRC}$	D+ Source Voltage <sup>(2)</sup>		0.5		0.7	V
$V_{LGC}$	Logic Threshold		0.8		2.0	V
$I_{DM\_SINK}$	D- Sink Current		25		175	$\mu\text{A}$
$I_{DP\_SINK}$	D+ Sink Current		25		175	$\mu\text{A}$
$I_{DP\_SRC}$	Data Contact Detect Current Source		7		13	$\mu\text{A}$
$t_{DCD\_DBNC}$	Data Contact Detect Debounce		10			ms
$t_{DCD\_TOUT}$	Time for DCD to Timeout		300	450	900	ms
$t_{VDPSRC\_ON}$	D+ Voltage Source On Time		40			ms
$t_{VDMSRC\_ON}$	D- Voltage Source On Time		40			ms

### Notes:

- Guaranteed by characterization; not production tested.
- The voltage source,  $V_{DP\_SRC} / V_{DM\_SRC}$ , is able to source at least 250  $\mu\text{A}$  when the output voltage is in the specified range. This voltage source should not pull DP\_CON / DM\_CON below 2.2V when DP\_CON / DM\_CON is pulled to a voltage of 3.0 V minimum or 3.6 V maximum with a resistance of 900  $\Omega$  minimum or 1575  $\Omega$  maximum.

## AC Electrical Characteristics

Unless otherwise specified, values are at  $T_A = -40$  to  $+85^\circ\text{C}$ ; all typical values are for  $V_{CC} = 3.3\text{ V}$  at  $T_A = 25^\circ\text{C}$ .

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	Figure
Xtalk	Active Channel Crosstalk, DP_CON to DM_CON <sup>(3)</sup>	f=1 MHz, $R_T=50\ \Omega$ , $C_L=0\text{ pF}$		-78		dB	Figure 7
		f=240 MHz, $R_T=50\ \Omega$ , $C_L=0\text{ pF}$		-36			
$O_{IRR}$	Off Isolation Rejection Ratio, DM_HOST to DM_CON, DP_HOST to DP_CON <sup>(3)</sup>	f=1 MHz, $R_T=50\ \Omega$ , $C_L=0\text{ pF}$		-84		dB	Figure 6
		f=240 MHz, $R_T=50\ \Omega$ , $C_L=0\text{ pF}$		-34			
BW	Bandwidth of Switch	$R_T=50\ \Omega$		1.7		GHz	Figure 7

**Note:**

3. Guaranteed by characterization; not production tested.

## Capacitance

Unless otherwise specified, values are at  $T_A = -40$  to  $+85^\circ\text{C}$ .

Symbol	Parameter	Condition	Typical	Unit	Figure
$C_{OFF}$	DP_CON, DM_CON Off Capacitance <sup>(4)</sup>	$V_{BIAS}=0.2\text{ V}$ , f=1MHz	3.2	pF	Figure 8
$C_{ON}$	DP_CON, DM_CON On Capacitance <sup>(4)</sup>	$V_{BIAS}=0.2\text{ V}$ , f=1MHz	5.8	pF	Figure 9

**Note:**

4. Guaranteed by characterization; not production tested.



## Test Diagrams

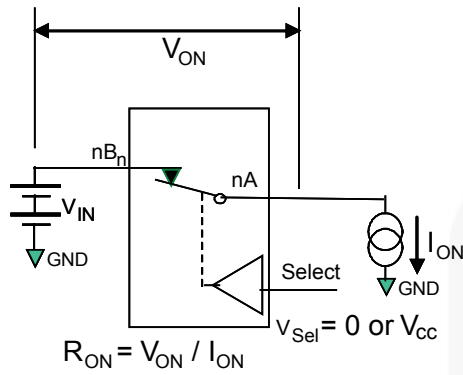
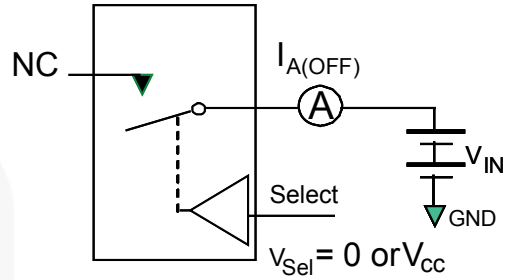


Figure 4. On Resistance



\*\*Each switch port is tested separately.

Figure 5. Off Leakage

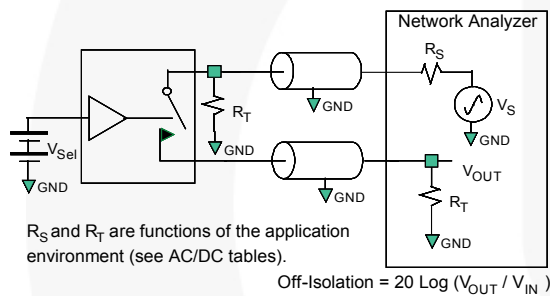


Figure 6. Channel Off Isolation

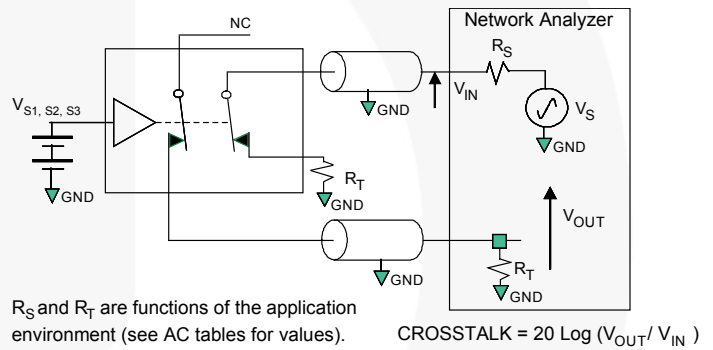


Figure 7. Active Channel Crosstalk

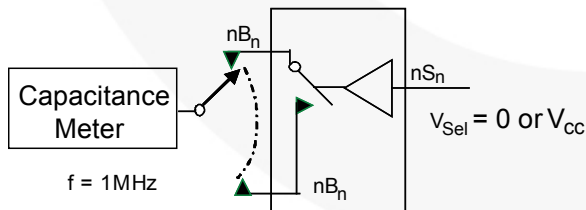


Figure 8. Channel Off Capacitance

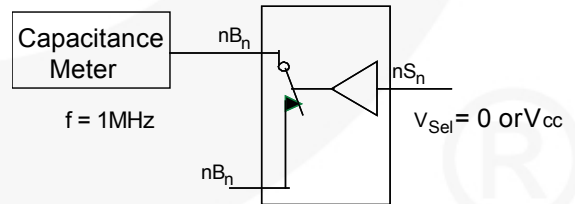


Figure 9. Channel On Capacitance

## Physical Dimensions

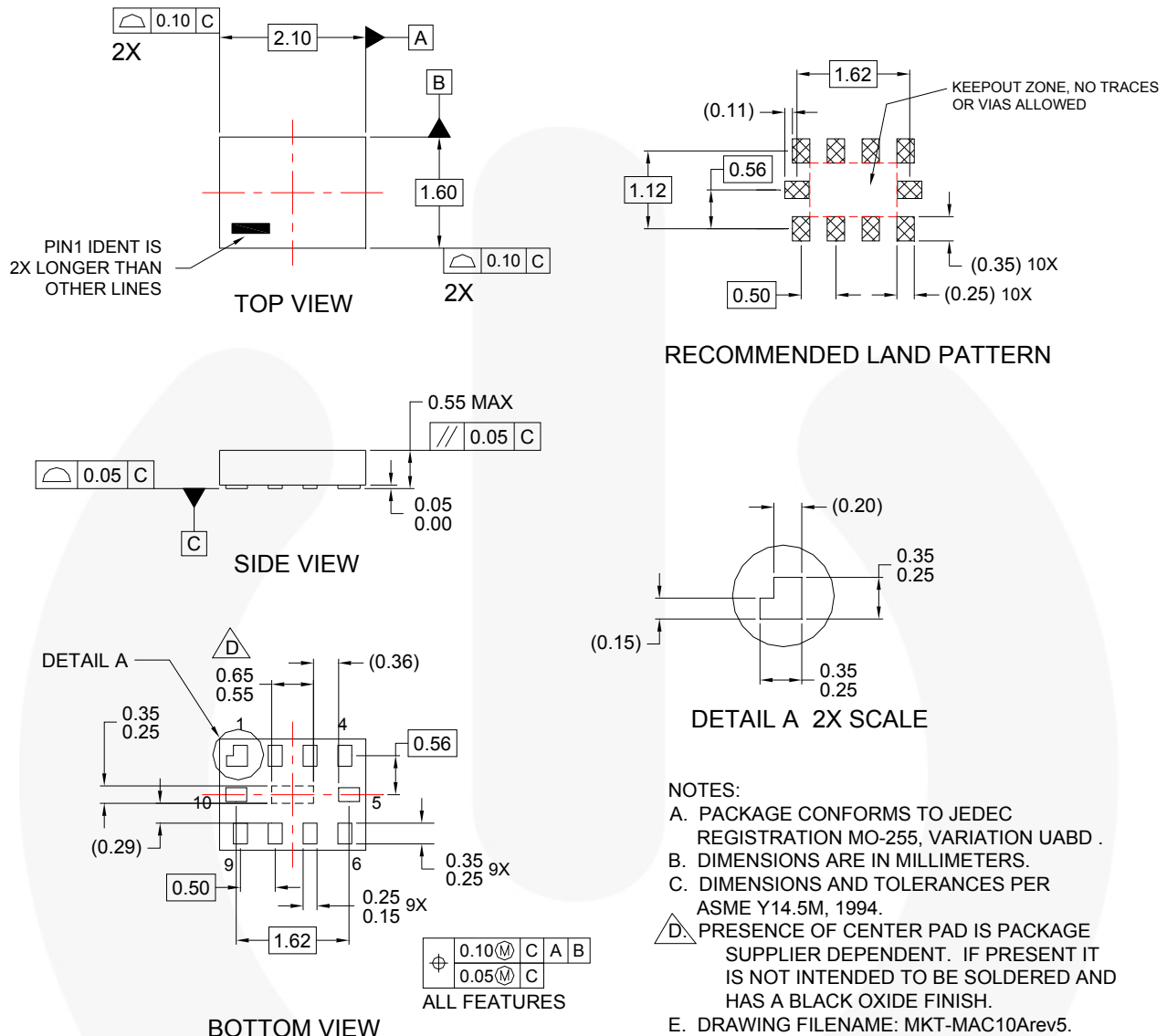


Figure 10. 10-Lead, MicroPak™

Part Number	Top Mark	Operating Temperature Range	Package Description	Packing Method
FSA831AL10X	NY	-40 to 85°C	10-Lead, MicroPak™ 1.6 x 2.1 mm, 0.5 mm Pitch	Tape & Reel

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
<http://www.fairchildsemi.com/packaging/>.



## TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

2Cool™	FPST™	PowerTrench®	Sync-Lock™
AccuPower™	F-PFST™	PowerXS™	SYSTEM GENERAL®
AX-CAP®	FRFET®	Programmable Active Droop™	TinyBoost™
BitSiC™	Global Power Resource™	QFET®	TinyBuck™
Build it Now™	GreenBridge™	QS™	TinyCalc™
CorePLUS™	Green FPS™	Quiet Series™	TinyLogic®
CorePOWER™	Green FPS™ e-Series™	RapidConfigure™	TINYOPTO™
CROSSVOL7™	Gmax™	Saving our world, 1mW/WkV at a time™	TinyPower™
CTL™	GTO™	SignalWise™	TinyPWM™
Current Transfer Logic™	IntelliMAX™	SmartMax™	TinyWire™
DEUXPEED®	ISOPLANAR™	SMART START™	TransiC™
Dual Cool™	Making Small Speakers Sound Louder and Better™	Solutions for Your Success™	TriFault Detect™
EcoSPARK®	MegaBuck™	SPM®	TRUECURRENT®
EfficientMax™	MICROCOUPLER™	STEALTH™	µSerDes™
ESBC™	MicroFET™	SuperFET®	UHC®
F <sup>®</sup>	MicroPak™	SuperSOT™-3	Ultra FRFET™
Fairchild®	MicroPak2™	SuperSOT™-8	UniFET™
Fairchild Semiconductor®	MillerDrive™	SupreMOS®	VCO™
FACT Quiet Series™	MotionMax™	SyncFET™	VisualMax™
FACT®	mWVaver™		VoltagePlus™
FAST®	OptoHiT™		XS™
FastvCore™	OPTOLOGIC®		
FETBench™	OPTOPLANAR®		

\* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN, NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I64