

October 2013

FJN4301R PNP Epitaxial Silicon Transistor

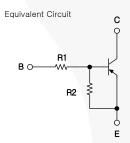
Features

- · Switching Circuit, Inverter, Interface Circuit, Driver Circuit
- Built-in Bias Resistor ($R_1 = 4.7 \text{ k}\Omega, R_2 = 4.7 \text{ k}\Omega$)
- Complement to FJN3301R

Application

• Switching Application (Integrated Bias Resistor)





Ordering Information

Part Number Top Mark		Package	Packing Method		
FJN4301RTA	R4301	TO-92 3L	Ammo		

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^{\circ}\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Units
V _{CBO}	Collector-Base Voltage	-50	V
V _{CEO}	Collector-Emitter Voltage	-50	V
V_{EBO}	Emitter-Base Voltage	-10	V
I _C	Collector Current	-100	mA
TJ	Junction Temperature	150	°C
T _{STG}	Storage Temperature	-55 to 150	°C

1

Thermal Characteristics(1)

Values are at $T_A = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Value	Unit
D	Power Dissipation	300	mW
P _D	Derate Above T _A = 25°C	2.4	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	416	°C/W

Note:

1. PCB Board Size: FR-4 76 x 114 x 0.6T mm³(3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

Electrical Characteristics

Values are at $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units
BV _{CBO}	Collector-Base Breakdown Voltage	$I_C = -10 \mu A, I_E = 0$	-50			V
BV _{CEO}	Collector-Emitter Breakdown Voltage	$I_C = -100 \mu\text{A}, I_B = 0$	-50			V
I _{CBO}	Collector Cut-Off Current	$V_{CB} = -40 \text{ V}, I_{E} = 0$			-0.1	μΑ
h _{FE}	DC Current Gain	$V_{CE} = -5 \text{ V}, I_{C} = -10 \text{ mA}$	20			
V _{CE(sat)}	Collector-Emitter Saturation Voltage	$I_C = -10 \text{ mA}, I_B = -0.5 \text{ mA}$			-0.3	V
f _T	Current Gain Bandwidth Product	$V_{CE} = -10 \text{ V}, I_{C} = -5 \text{ mA}$		200		MHz
C _{ob}	Output Capacitance	$V_{CB} = -10 \text{ V}, I_{E} = 0,$ f = 1.0 MHz		5.5		pF
V _{I(off)}	Input Off Voltage	$V_{CE} = -5 \text{ V}, I_{C} = -100 \mu\text{A}$			-0.5	V
V _{I(on)}	Input On Voltage	$V_{CE} = -0.3 \text{ V}, I_{C} = -20 \text{ mA}$	-3			V
R ₁	Input Resistor		3.2	4.7	6.2	kΩ
R ₁ /R ₂	Resistor Ratio		0.9	1.0	1.1	

Typical Performance Characteristics

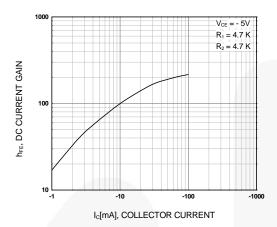


Figure 1. DC Current Gain

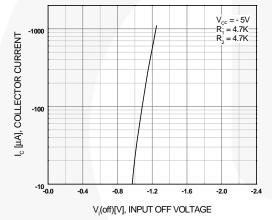


Figure 3. Input Off Voltage

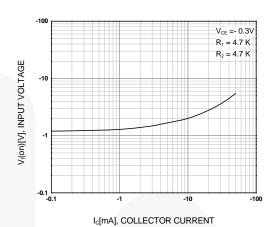


Figure 2. Input On Voltage

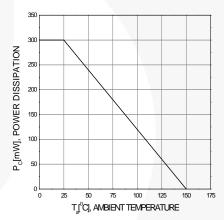
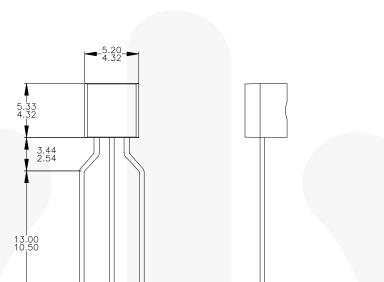
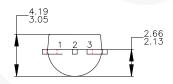


Figure 4. Power Derating

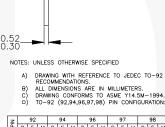
Physical Dimensions



TO-92



0.56





E) FOR PACKAGE 92, 94, 96, 97 AND 98:
PIN CONFIGURATION DRAIN "D" AND SOURCE "S"
ARE INTERCHANDEAGLE AT JETE "F" OPTION.
F) DRAWING FILENAME: MKT-ZAO3FREV2.

Figure 5. 3-LEAD, TO-92, MOLDED 0.200 IN LINE SPACING LD FORM (J61Z OPTION) (ACTIVE)

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Definition of Terms		
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