LAPIS SEMICONDUCTOR

FEUL610Q421-05

ML610Q421/ML610Q422
ML610421/ML610422
User's Manual

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Preface

This manual describes the operation of the hardware of the 8-bit microcontroller ML610Q421/ML610Q422/ML610421/ML610422.

The following manuals are also available. Read them as necessary.

- nX-U8/100 Core Instruction Manual
  Description on the basic architecture and the each instruction of the nX-U8/100 Core.

- MACU8 Assembler Package User's Manual
  Description on the method of operating the relocatable assembler, the linker, the librarian, and the object converter and also on the specifications of the assembler language.

- CCU8 User's Manual
  Description on the method of operating the compiler.

- CCU8 Programming Guide
  Description on the method of programming.

- CCU8 Language Reference
  Description on the language specifications.

- DTU8 Debugger User's Manual
  Description on the method of operating the debugger DTU8.

- IDEU8 User's Manual
  Description on the integrated development environment IDEU8.

- uEASE User's Manual
  Description on the on-chip debug tool uEASE.

- uEASE connection Manual for ML610Q421/ML610Q422
  Description about the connection between uEASE and ML610Q421/ML610Q422.

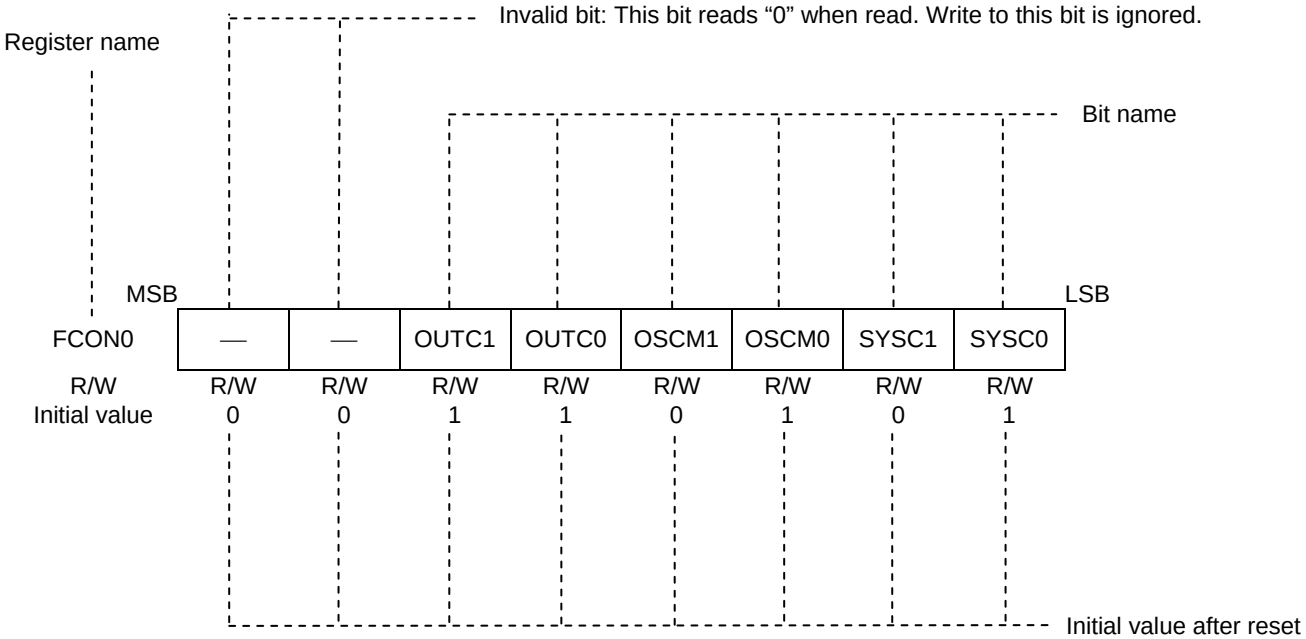
- FWuEASE Flash Writer Host Program User's Manual
  Description on the Flash Writer host program.

Notation

Classification	Notation	Description
♦ Numeric value	xxh, xxH	Indicates a hexadecimal number. x: Any value in the range of 0 to F
	xxb	Indicates a binary number; "b" may be omitted. x: A value 0 or 1
♦ Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 8 bits
	nibble, N	1 nibble = 4 bits
	maga-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, μ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
♦ Terminology	"H" level, "1" level	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level, "0" level	Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

♦ Register description

R/W: Indicates that Read/Write attribute. "R" indicates that data can be read and "W" indicates that data can be written. "R/W" indicates that data can be read or written.



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Chapter 1

Overview

1. Overview

1.1 Features

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, I^2C bus interface (master), melody driver, battery level detect circuit, RC oscillation type A/D converter, 12-bit successive approximation type A/D converter, and LCD driver, are incorporated around 8-bit CPU nX-U8/100.
The CPU nX-U8/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by 3-stage pipe line architecture parallel procesing.
The Flash ROM that is installed as program memory to ML610Q421/ML610Q422 achieves low-voltage low-power consumption operation (read operation) equivalent to mask ROM and is most suitable for battery-driven applications.
The on-chip debug function that is installed enables program debugging and programming.

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function (ML610Q421/ML610Q422 only)
  - Minimum instruction execution time
    30.5 μs (@32.768 kHz system clock)
    0.24 4μs (@4.096 MHz system clock)

- Internal memory
  - ML610Q421/ML610Q422:Internal 32KByte Flash ROM (16K×16 bits) (including unusable 1KByte TEST area)
  - ML610421/ML610422 :Internal 32KByte Mask ROM (16K×16 bits) (including unusable 1KByte TEST area)
  - Internal 1KByte Data RAM (1024×8 bits), 1KByte Display Allocation RAM (1024 x 8bit)
  - Internal 100-byte RAM for display

- Interrupt controller
  - 2 non-maskable interrupt sources (Internal source: 1, External source: 1)
  - 20 maskable interrupt sources (Internal sources: 16, External sources: 4)

- Time base counter
  - Low-speed time base counter ×1 channel
    Frequency compensation (Compensation range: Approx. –488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter ×1 channel

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)

- Timers
  - 8 bits × 4 channels (Timer0-3: 16-bit x 2 configuration available by using Timer0-1 or Timer2-3)
  - Clock frequency measurement mode (in one channel of 16-bit configuration using Timer2-3)

- 1 kHz timer
  - 10 Hz/1 Hz interrupt function

- Capture
  - Time base capture × 2 channels (4096 Hz to 32 Hz)

- PWM
  - Resolution 16 bits × 1 channel

- Synchronous serial port
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - Half-Duplex Communication
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- I^2C bus interface
  - Master function only
  - Fast mode (400 kbps@4MHz), standard mode (100 kbps@1MHz, 50kbps@500kHz)

- Melody driver
  - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  - Tone length: 63 types
  - Tempo: 15 types
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)

- RC oscillation type A/D converter
  - 24-bit counter
  - Time division × 2 channels

- Successive approximation type A/D converter
  - 12-bit A/D converter
  - Input × 2 channels

- General-purpose ports
  - Non-maskable interrupt input port × 1 channel
  - Input-only port × 6 channels (including secondary functions)
  - Output-only port × 3 channels (including secondary functions)
  - Input/output port
    ML610Q421/ML610421: 22 channels (including secondary functions)
    ML610Q422/ML610422: 14 channels (including secondary functions)

- LCD driver
  - Dot matrix can be supported.
    ML610Q421/ML610421: 400 dots max. (50 seg × 8 com), 1/1 to 1/8 duty
    ML610Q422/ML610422: 800 dots max. (50 seg × 16 com), 1/1 to 1/16 duty
  - 1/3 or 1/4 bias (built-in bias generation circuit)
  - Frame frequency selecable (approx. 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
  - Bias voltage multiplying clock selectable (8 types)
  - Contrast adjustment (1/3 bias: 32 steps, 1/4 bias: 20 steps)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
  - Programmable display allocation function (available only when 1/1~1/8 duty is selected)

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected
    (ML610Q421B/ML610Q422B/ML610421B/ML610422B does not have this function)
  - Reset by the watchdog timer (WDT) overflow

- Power supply voltage detect function
  - Judgment voltages: One of 16 levels
  - Judgment accuracy: ±2% (Typ.)

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation withoug low-speed clock)
    Crystal oscillation (32.768 kHz)
  - High-speed clock:
    Built-in RC oscillation (500 kHz)
    Built-in PLL oscillation (8.192 MHz ±2.5%), crystal/ceramic oscillation (4.096 MHz), external clock
  - Selection of high-speed clock mode by software:
    Built-in RC oscillation, built-in PLL oscillation, crystal/ceramic oscillation, external clock

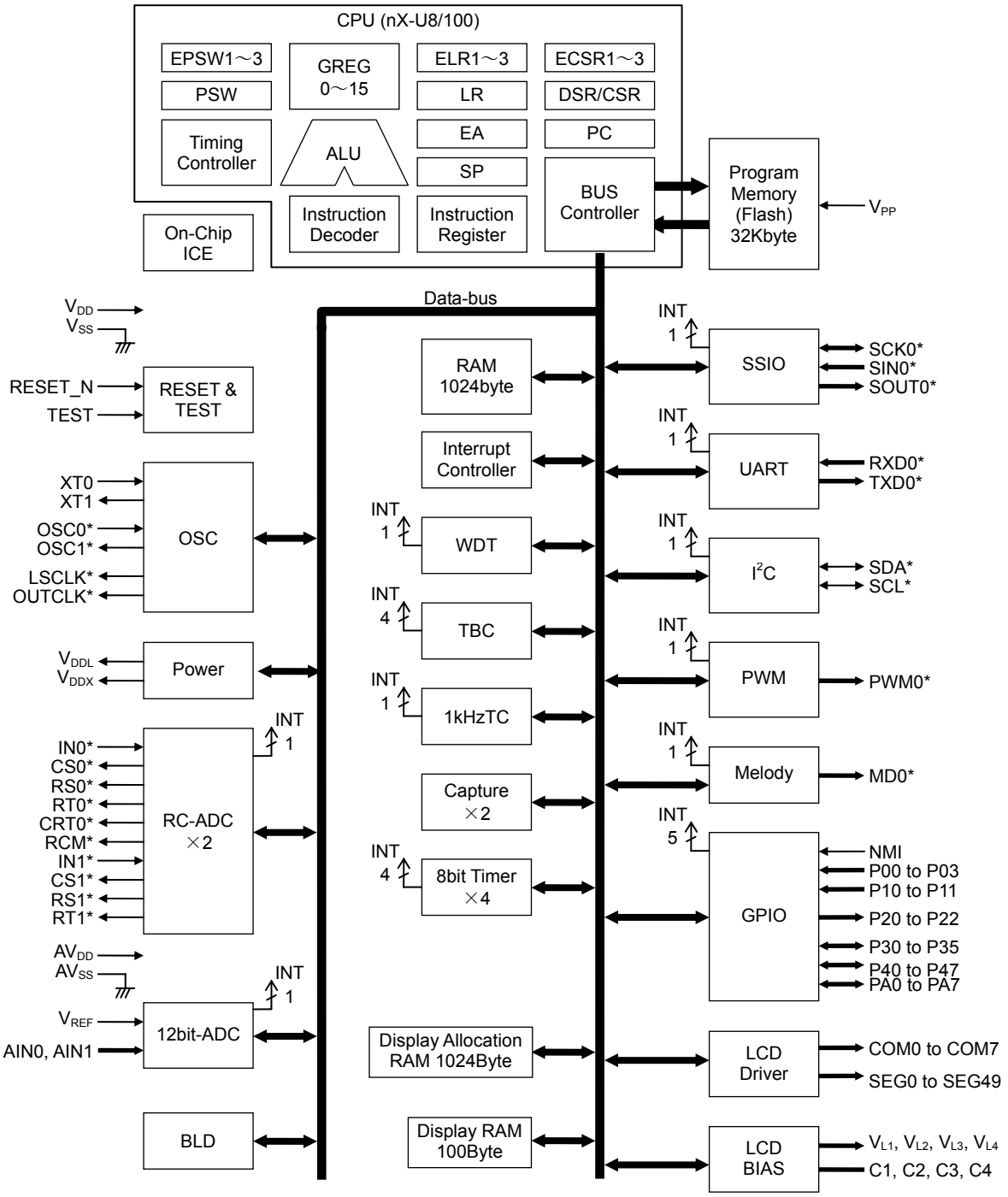
- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Shipment
  - Chip (Die)
    ML610Q421-xxxWA (Blank product: ML610Q421-NNNWA)
    ML610Q422-xxxWA (Blank product: ML610Q422-NNNWA)
    ML610Q421P-xxxWA (Blank product: ML610Q421P-NNNWA)
    ML610Q422P-xxxWA (Blank product: ML610Q422P-NNNWA)
    ML610Q421B-xxxWA (Blank product: ML610Q421B-NNNWA)
    ML610Q422B-xxxWA (Blank product: ML610Q422B-NNNWA)
    ML610421-xxxWA
    ML610422-xxxWA
    ML610421P-xxxWA
    ML610422P-xxxWA
    ML610421B-xxxWA
    ML610422B-xxxWA
  - 120-pin plastic TQFP
    ML610Q421-xxxTBZ03A (Blank product: ML610Q421-NNNTBZ03A)
    ML610Q422-xxxTBZ03A (Blank product: ML610Q422-NNNTBZ03A)
    ML610Q421P-xxxTBZ03A (Blank product: ML610Q421P-NNNTBZ03A)
    ML610Q422P-xxxTBZ03A (Blank product: ML610Q422P-NNNTBZ03A)
    ML610Q421B-xxxTBZ03A (Blank product: ML610Q421B-NNNTBZ03A)
    ML610Q422B-xxxTBZ03A (Blank product: ML610Q422B-NNNTBZ03A)
    ML610421-xxxTBZ03A
    ML610422-xxxTBZ03A
    ML610421P-xxxTBZ03A
    ML610422P-xxxTBZ03A
    ML610421B-xxxTBZ03A
    ML610422B-xxxTBZ03A
    xxx: ROM code number
    P: Wide range temperature version
    B: Low-speed clock oscillation stop detection reset un-carrying version

- Guaranteed operating range
  - Operating temperature: –20°C to 70°C (P version: –40°C to +85°C)
  - Operating voltage: V_{DD} = 1.1V to 3.6V, AV_{DD} = 2.2V to 3.6V

1.2 Configuration of Functional Blocks

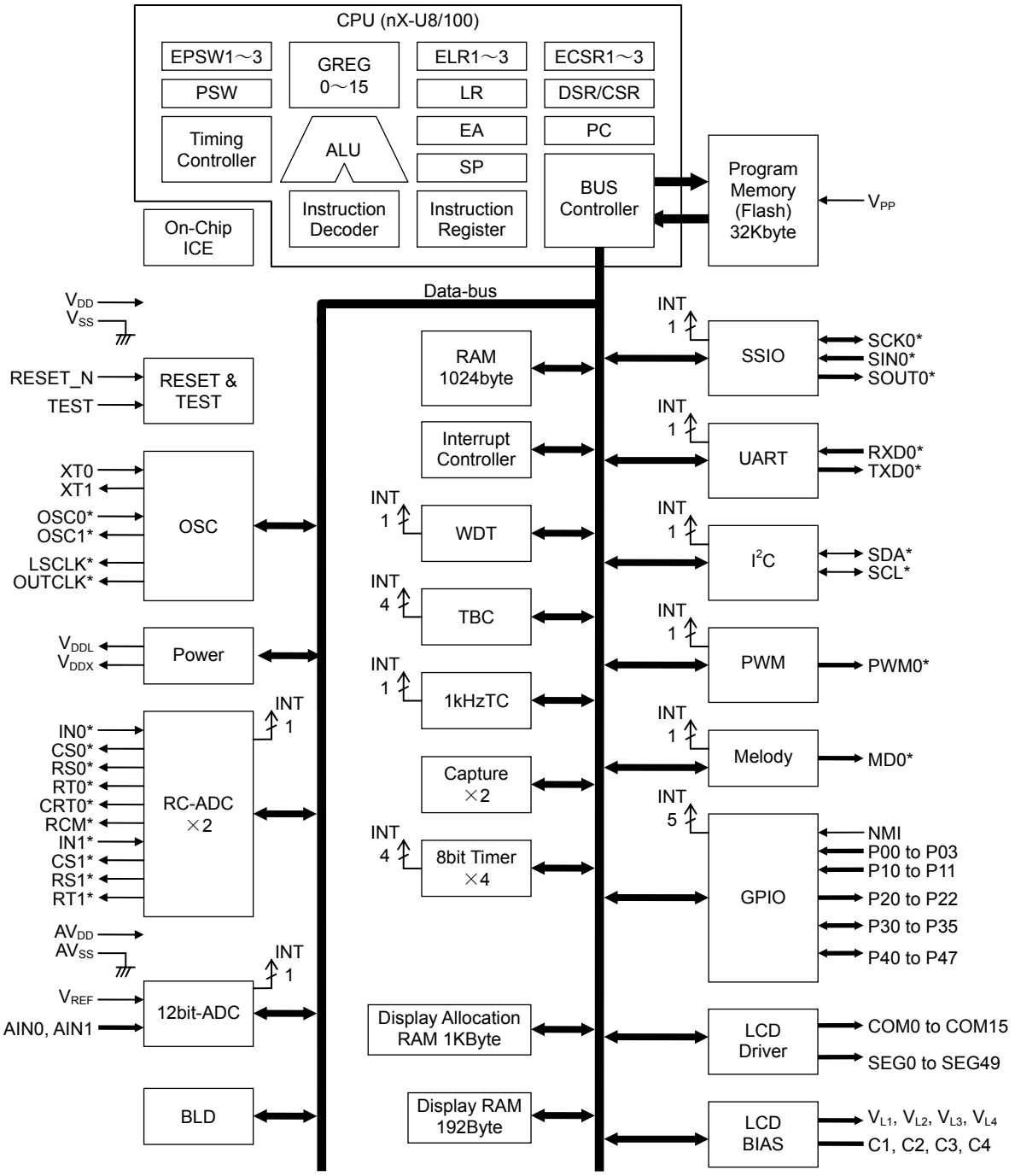
1.2.1 Block Diagram of ML610Q421



* Secondary function or Tertiary function

Figure 1-1 Block Diagram of ML610Q421

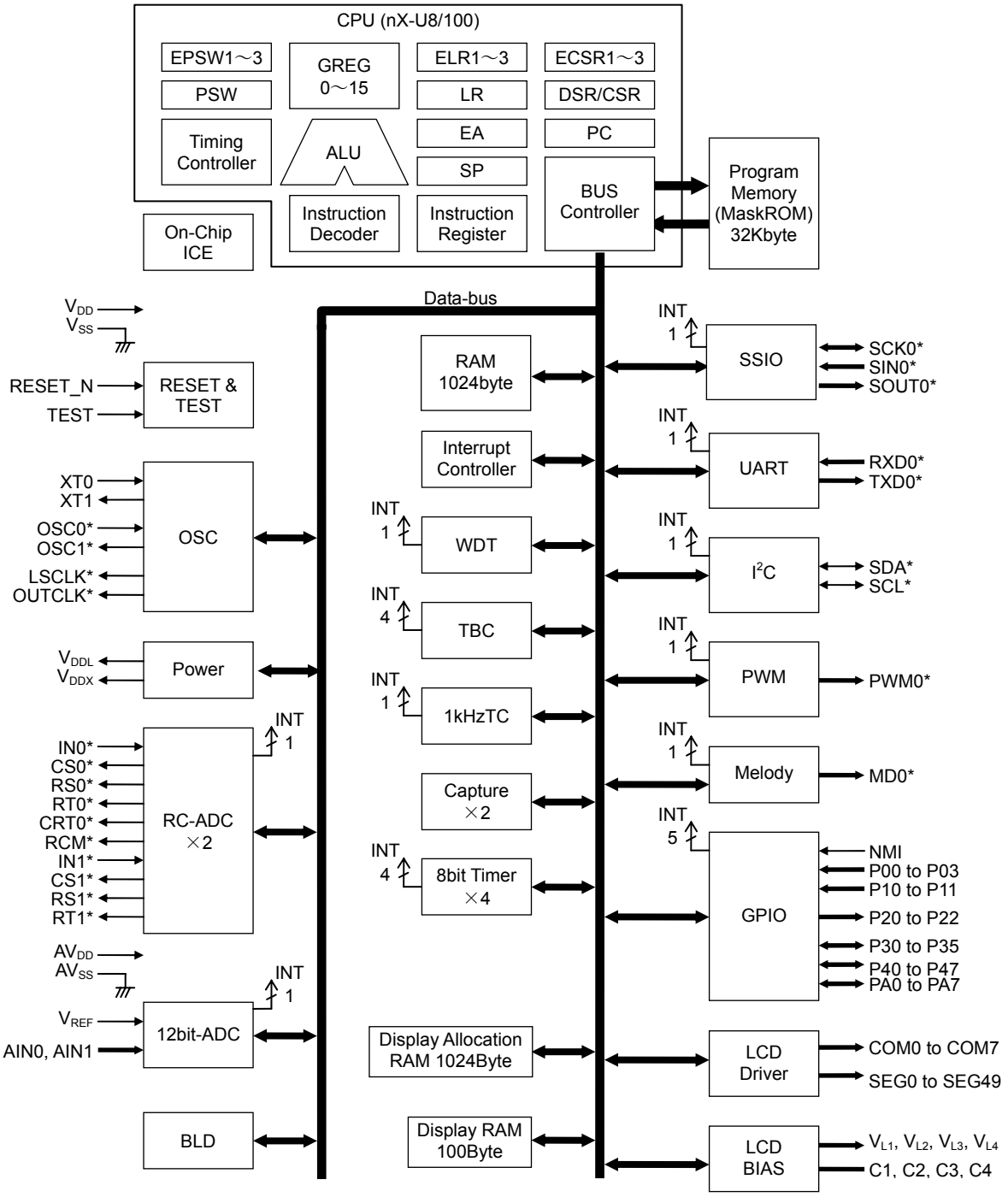
1.2.2 Block Diagram of ML610Q422



* Secondary function or Tertiary function

Figure 1-2 Block Diagram of ML610Q422

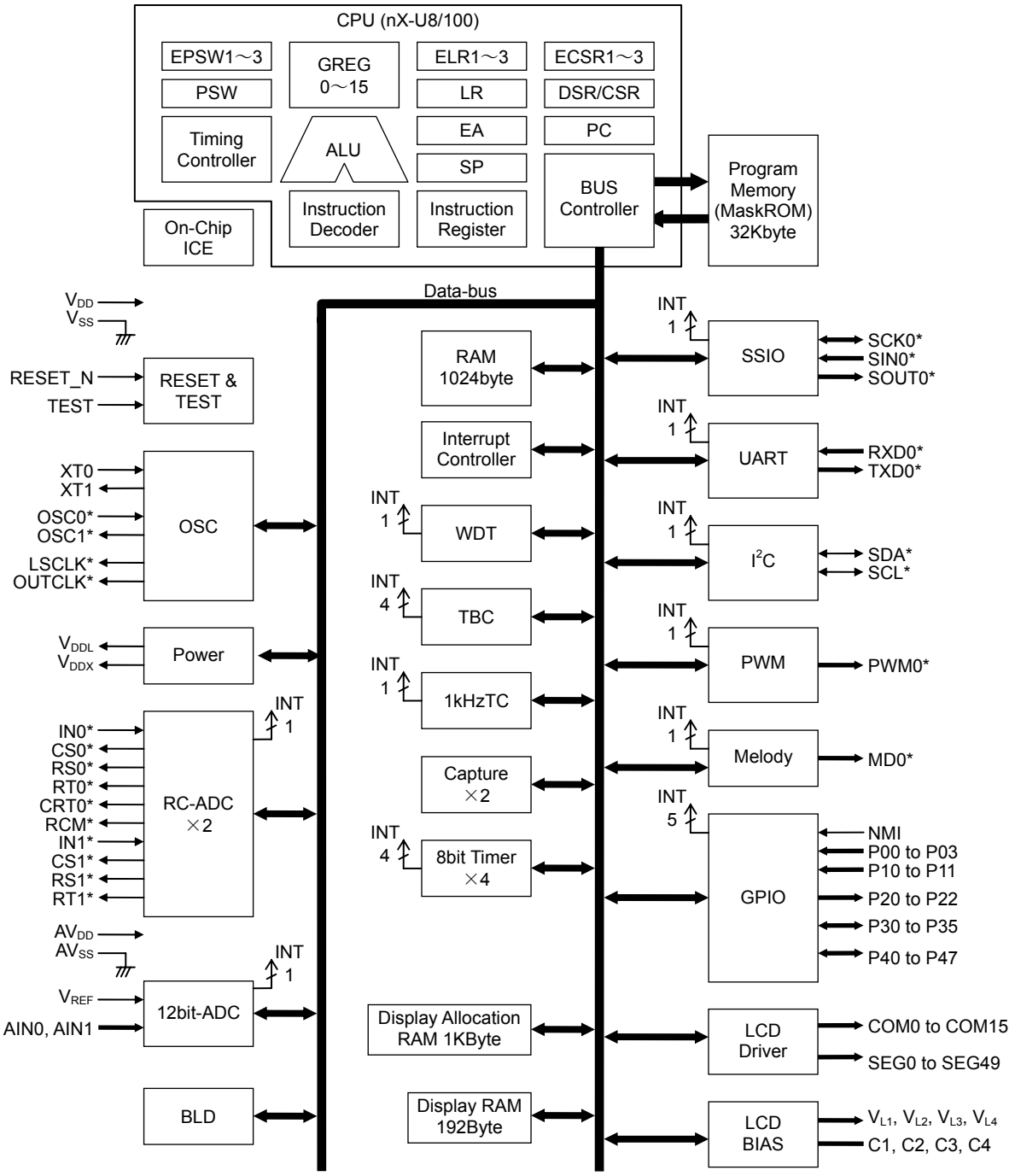
1.2.3 Block Diagram of ML610421



* Secondary function or Tertiary function

Figure 1-3 Block Diagram of ML610421

1.2.4 Block Diagram of ML610422



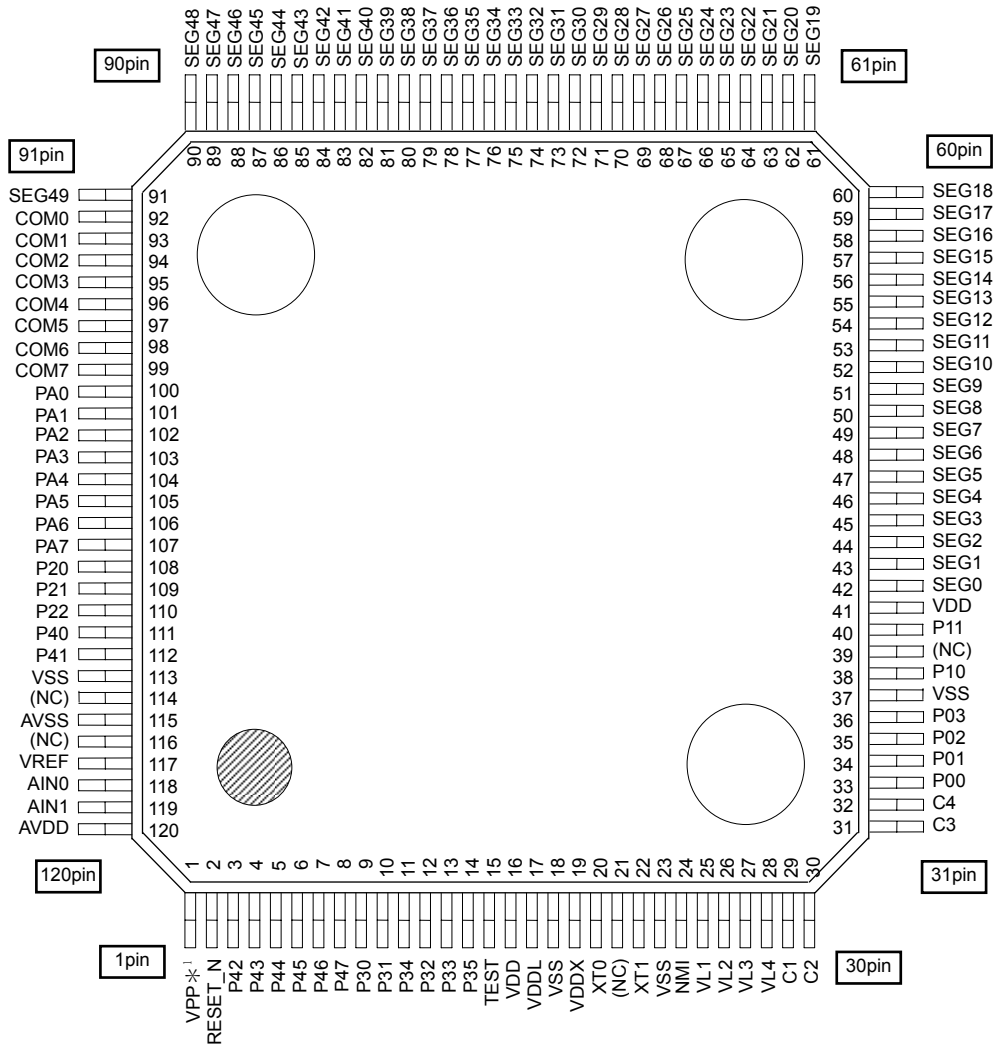
* Secondary function or Tertiary function

Figure 1-4 Block Diagram of ML610422

1.3 Pins

1.3.1 Pin Layout

1.3.1.1 Pin Layout of ML610Q421/ML610421 TQFP Package

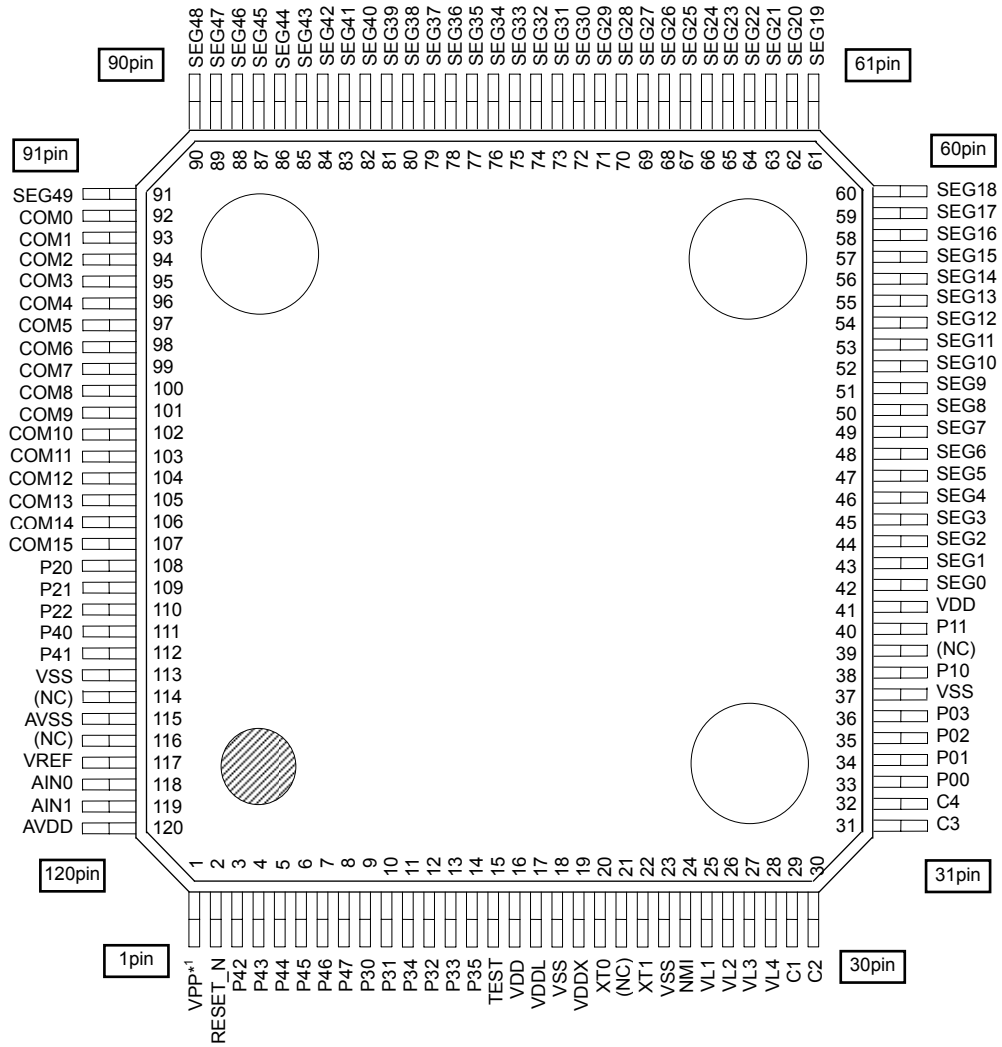


(NC): No Connection

Note:
The assignment of the pads P30 to P35 are not in order.
*1: A VPP terminal exists only ML610Q421. Please use (NC) in ML610421.

Figure 1-5 Pin Layout of ML610Q421/ML610421 Package

1.3.1.2 Pin Layout of ML610Q422/ML610422 TQFP Package



(NC): No Connection

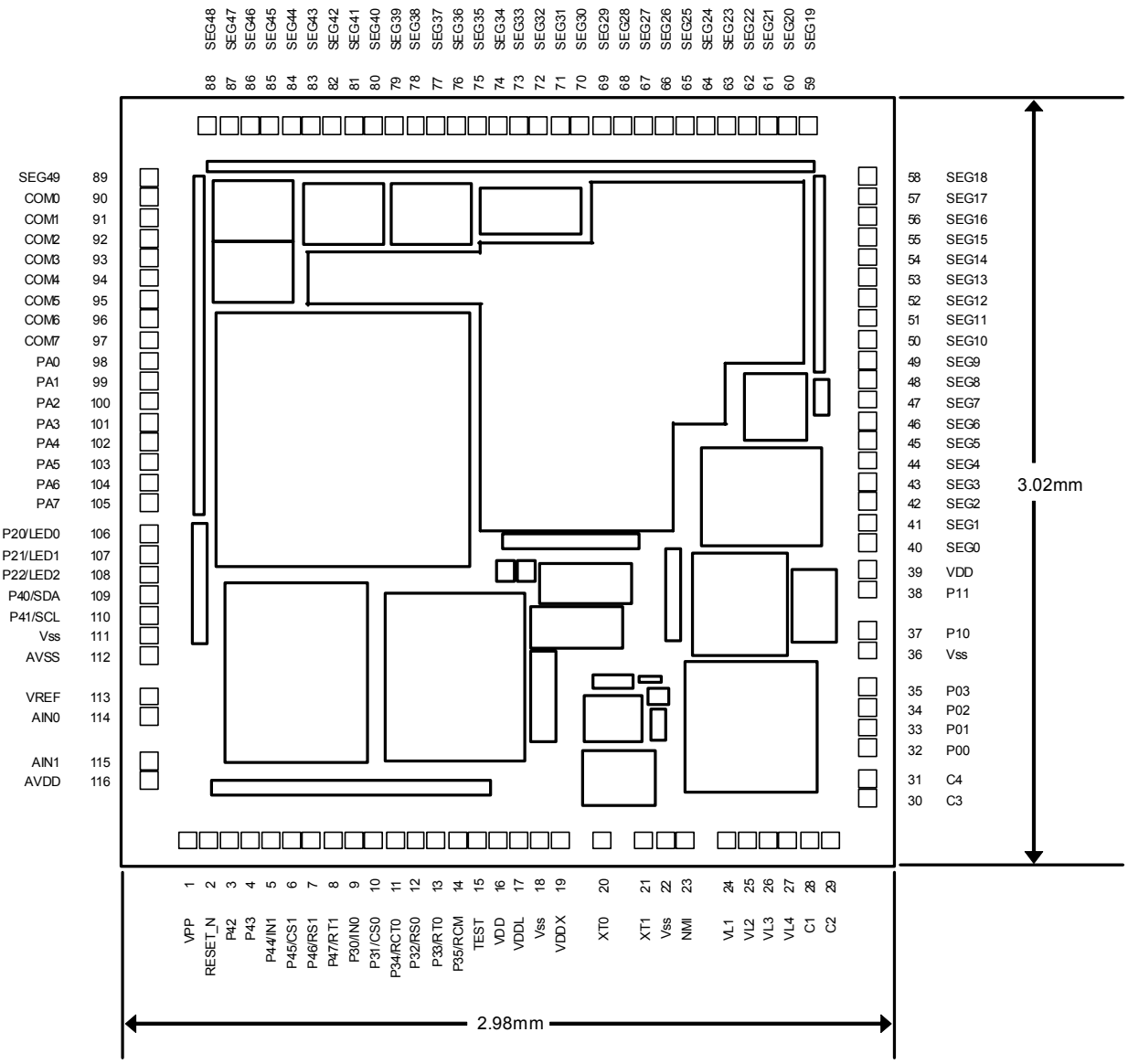
Note:

The assignment of the pads P30 to P35 are not in order.

*1: A VPP terminal exists only ML610Q422. Please use (NC) in ML610422.

Figure 1-6 Pin Layout of ML610Q422/ML610422 Package

1.3.1.3 Pin Layout of ML610Q421 Chip

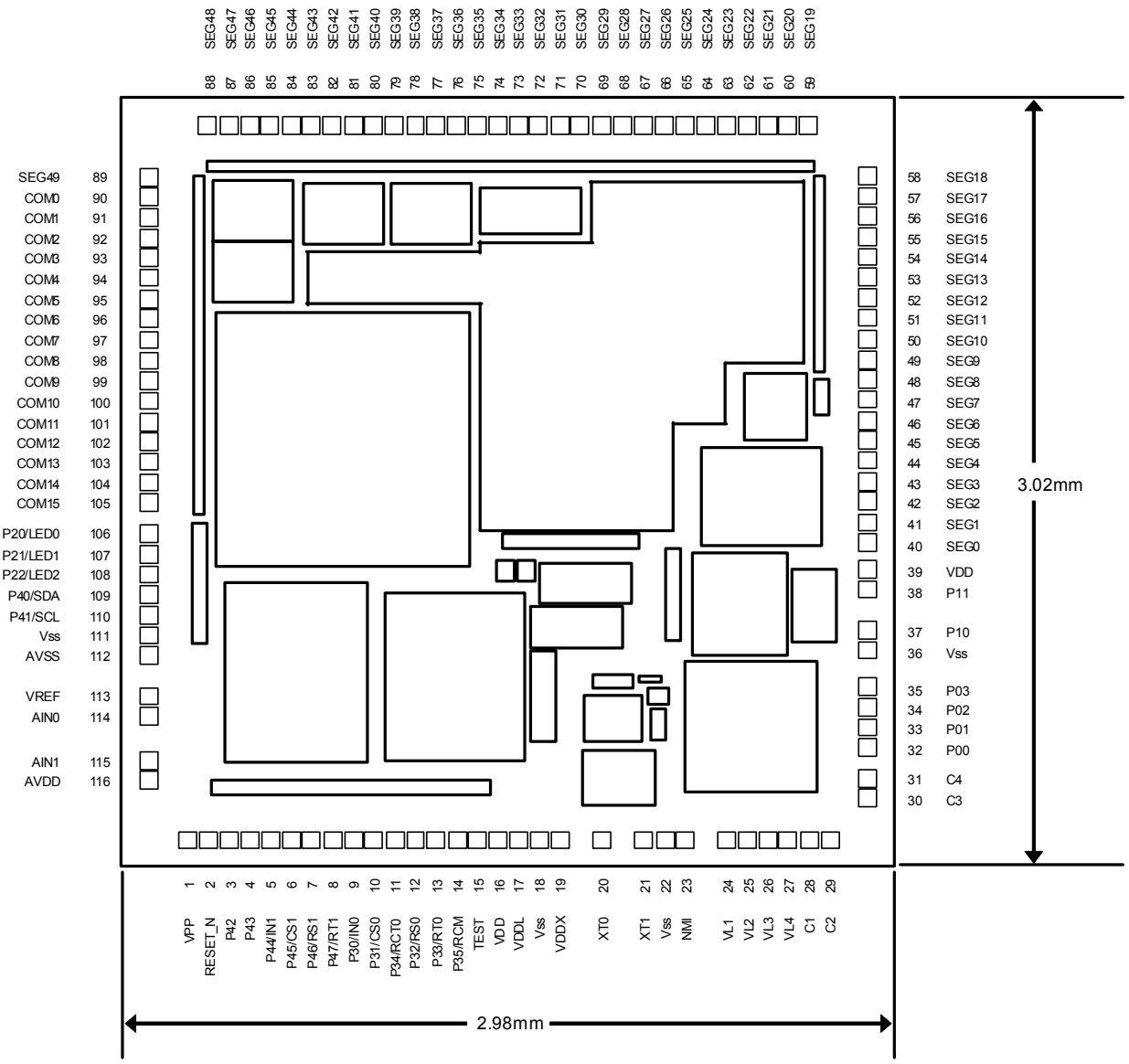


Note:
The assignment of the pads P30 to P35 are not in order.

Chip size:	2.98 mm × 3.02mm
PAD count:	116 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm ×70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 1-7 Dimensions of ML610Q421 Chip

1.3.1.4 Pin Layout of ML610Q422 Chip

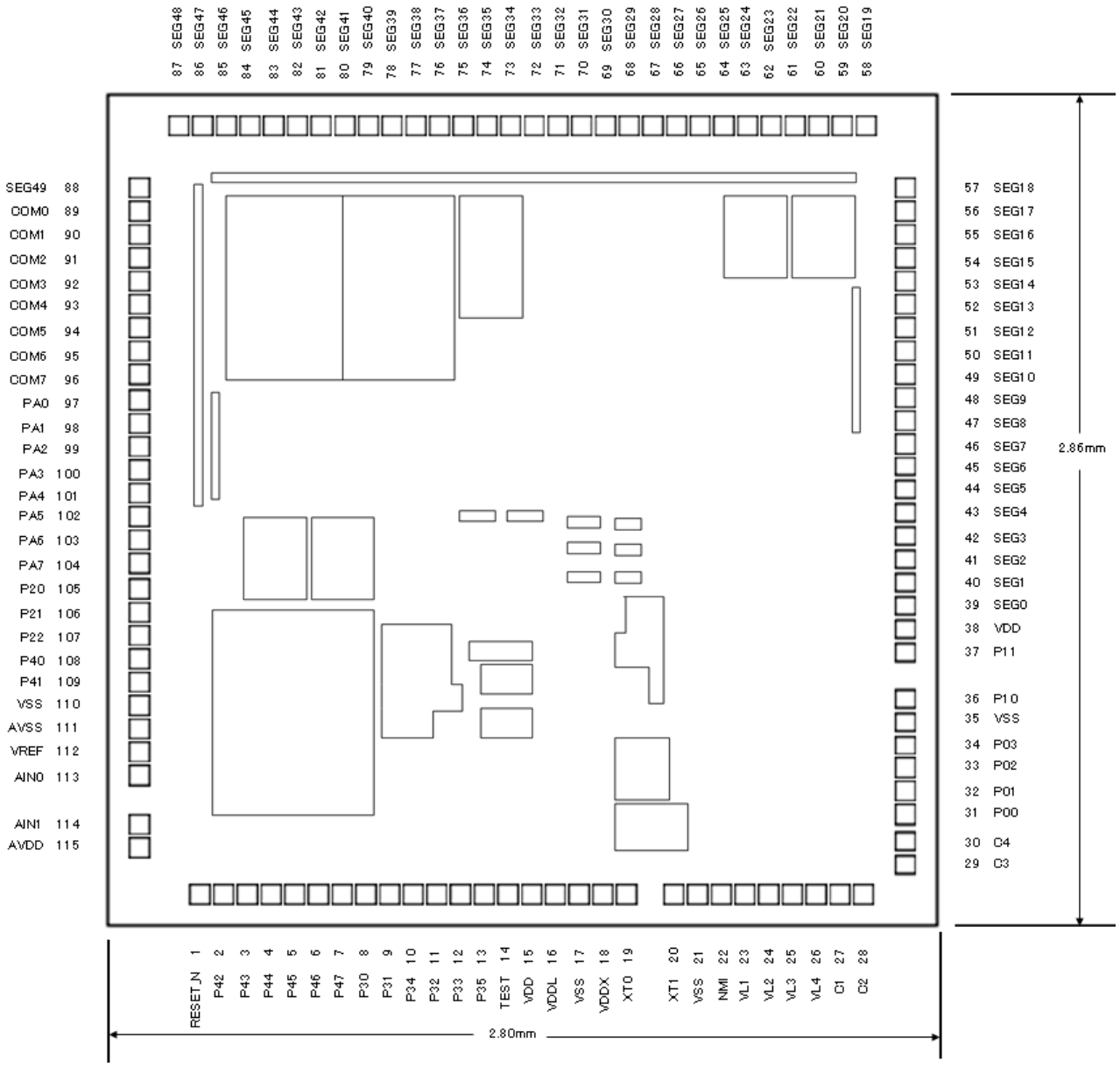


Note:
The assignment of the pads P30 to P35 are not in order.

Chip size:	2.98 mm × 3.02 mm
PAD count:	116 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 1-8 Dimensions of ML610Q422 Chip

1.3.1.5 Pin Layout of ML610421 Chip

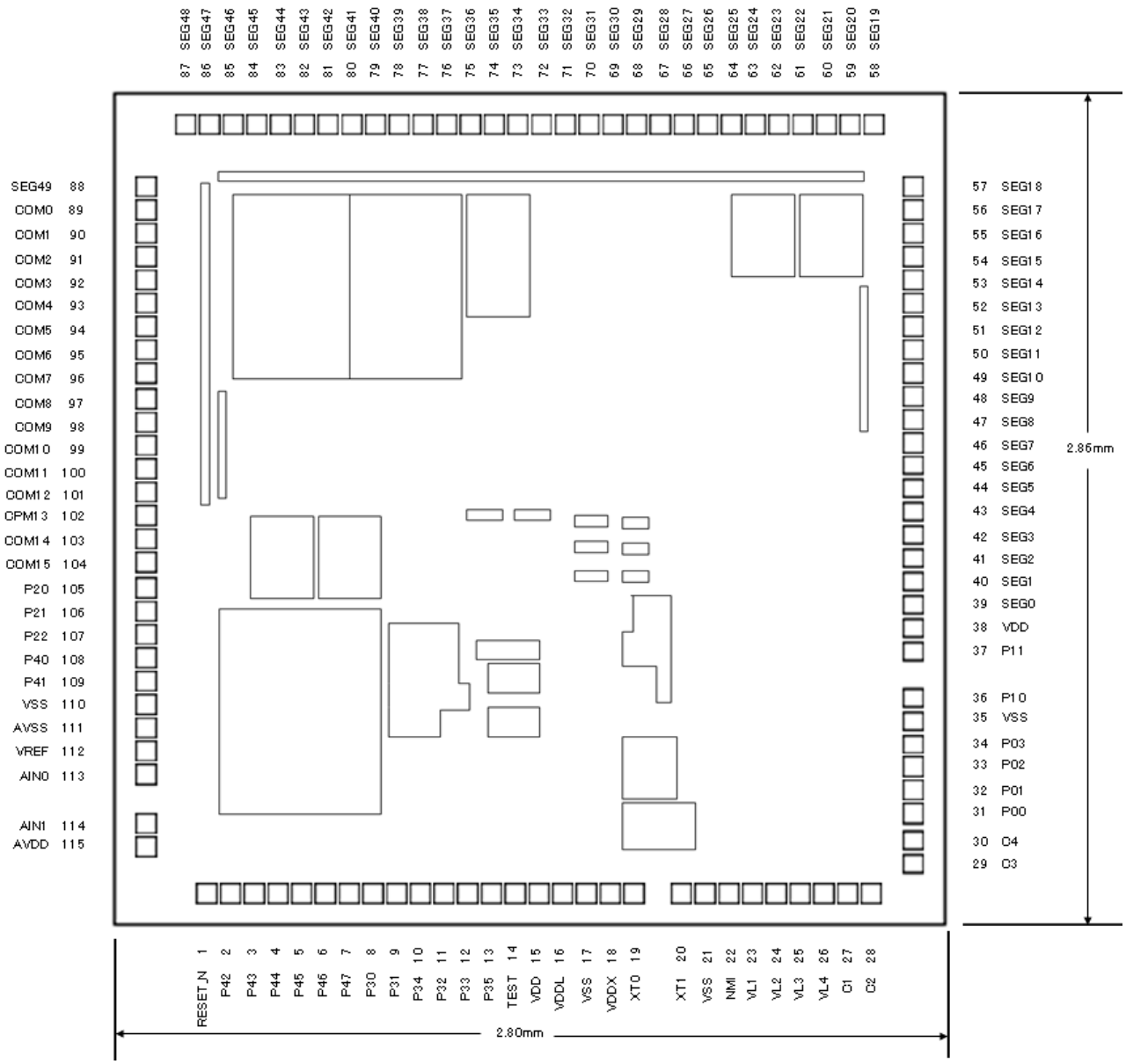


Note:
The assignment of the pads P30 to P35 are not in order.

Chip size:	2.80 mm × 2.86mm
PAD count:	115 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm ×70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 1-9 Dimensions of ML610421 Chip

1.3.1.6 Pin Layout of ML610422 Chip



Note:
The assignment of the pads P30 to P35 are not in order.

Chip size:	2.80 mm × 2.86 mm
PAD count:	115 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 1-10 Dimensions of ML610422 Chip

1.3.1.7 Pad Coordinates of ML610Q421 Chip

Table 1-1 Pad Coordinates of ML610Q421

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	VPP	-1240	-1404	51	SEG11	1384	640	101	PA3	-1384	240
2	RESET_N	-1160	-1404	52	SEG12	1384	720	102	PA4	-1384	160
3	P42	-1080	-1404	53	SEG13	1384	800	103	PA5	-1384	80
4	P43	-1000	-1404	54	SEG14	1384	880	104	PA6	-1384	0
5	P44	-920	-1404	55	SEG15	1384	960	105	PA7	-1384	-80
6	P45	-840	-1404	56	SEG16	1384	1040	106	P20	-1384	-200
7	P46	-760	-1404	57	SEG17	1384	1120	107	P21	-1384	-280
8	P47	-680	-1404	58	SEG18	1384	1200	108	P22	-1384	-360
9	P30	-600	-1404	59	SEG19	1160	1404	109	P40	-1384	-440
10	P31	-520	-1404	60	SEG20	1080	1404	110	P41	-1384	-520
11	P34	-440	-1404	61	SEG21	1000	1404	111	Vss	-1384	-600
12	P32	-360	-1404	62	SEG22	920	1404	112	AVss	-1384	-680
13	P33	-280	-1404	63	SEG23	840	1404	113	VREF	-1384	-840
14	P35	-200	-1404	64	SEG24	760	1404	114	AIN0	-1384	-920
15	TEST	-120	-1404	65	SEG25	680	1404	115	AIN1	-1384	-1092
16	VDD	-40	-1404	66	SEG26	600	1404	116	AVDD	-1384	-1172
17	VDDL	40	-1404	67	SEG27	520	1404				
18	Vss	120	-1404	68	SEG28	440	1404				
19	VDDX	200	-1404	69	SEG29	360	1404				
20	XT0	360	-1404	70	SEG30	280	1404				
21	XT1	520	-1404	71	SEG31	200	1404				
22	Vss	600	-1404	72	SEG32	120	1404				
23	NMI	680	-1404	73	SEG33	40	1404				
24	VL1	840	-1404	74	SEG34	-40	1404				
25	VL2	920	-1404	75	SEG35	-120	1404				
26	VL3	1000	-1404	76	SEG36	-200	1404				
27	VL4	1080	-1404	77	SEG37	-280	1404				
28	C1	1160	-1404	78	SEG38	-360	1404				
29	C2	1240	-1404	79	SEG39	-440	1404				
30	C3	1384	-1240	80	SEG40	-520	1404				
31	C4	1384	-1160	81	SEG41	-600	1404				
32	P00	1384	-1040	82	SEG42	-680	1404				
33	P01	1384	-960	83	SEG43	-760	1404				
34	P02	1384	-880	84	SEG44	-840	1404				
35	P03	1384	-800	85	SEG45	-920	1404				
36	Vss	1384	-660	86	SEG46	-1000	1404				
37	P10	1384	-580	87	SEG47	-1080	1404				
38	P11	1384	-420	88	SEG48	-1160	1404				
39	VDD	1384	-340	89	SEG49	-1384	1200				
40	SEG0	1384	-240	90	COM0	-1384	1120				
41	SEG1	1384	-160	91	COM1	-1384	1040				
42	SEG2	1384	-80	92	COM2	-1384	960				
43	SEG3	1384	0	93	COM3	-1384	880				
44	SEG4	1384	80	94	COM4	-1384	800				
45	SEG5	1384	160	95	COM5	-1384	720				
46	SEG6	1384	240	96	COM6	-1384	640				
47	SEG7	1384	320	97	COM7	-1384	560				
48	SEG8	1384	400	98	PA0	-1384	480				
49	SEG9	1384	480	99	PA1	-1384	400				
50	SEG10	1384	560	100	PA2	-1384	320				

1.3.1.8 Pad Coordinates of ML610Q422 Chip

Table 1-2 Pad Coordinates of ML610Q422

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	VPP	-1240	-1404	51	SEG11	1384	640	101	COM11	-1384	240
2	RESET_N	-1160	-1404	52	SEG12	1384	720	102	COM12	-1384	160
3	P42	-1080	-1404	53	SEG13	1384	800	103	COM13	-1384	80
4	P43	-1000	-1404	54	SEG14	1384	880	104	COM14	-1384	0
5	P44	-920	-1404	55	SEG15	1384	960	105	COM15	-1384	-80
6	P45	-840	-1404	56	SEG16	1384	1040	106	P20	-1384	-200
7	P46	-760	-1404	57	SEG17	1384	1120	107	P21	-1384	-280
8	P47	-680	-1404	58	SEG18	1384	1200	108	P22	-1384	-360
9	P30	-600	-1404	59	SEG19	1160	1404	109	P40	-1384	-440
10	P31	-520	-1404	60	SEG20	1080	1404	110	P41	-1384	-520
11	P34	-440	-1404	61	SEG21	1000	1404	111	Vss	-1384	-600
12	P32	-360	-1404	62	SEG22	920	1404	112	AVss	-1384	-680
13	P33	-280	-1404	63	SEG23	840	1404	113	VREF	-1384	-840
14	P35	-200	-1404	64	SEG24	760	1404	114	AIN0	-1384	-920
15	TEST	-120	-1404	65	SEG25	680	1404	115	AIN1	-1384	-1092
16	VDD	-40	-1404	66	SEG26	600	1404	116	AVDD	-1384	-1172
17	VDDL	40	-1404	67	SEG27	520	1404				
18	Vss	120	-1404	68	SEG28	440	1404				
19	VDDX	200	-1404	69	SEG29	360	1404				
20	XT0	360	-1404	70	SEG30	280	1404				
21	XT1	520	-1404	71	SEG31	200	1404				
22	Vss	600	-1404	72	SEG32	120	1404				
23	NMI	680	-1404	73	SEG33	40	1404				
24	VL1	840	-1404	74	SEG34	-40	1404				
25	VL2	920	-1404	75	SEG35	-120	1404				
26	VL3	1000	-1404	76	SEG36	-200	1404				
27	VL4	1080	-1404	77	SEG37	-280	1404				
28	C1	1160	-1404	78	SEG38	-360	1404				
29	C2	1240	-1404	79	SEG39	-440	1404				
30	C3	1384	-1240	80	SEG40	-520	1404				
31	C4	1384	-1160	81	SEG41	-600	1404				
32	P00	1384	-1040	82	SEG42	-680	1404				
33	P01	1384	-960	83	SEG43	-760	1404				
34	P02	1384	-880	84	SEG44	-840	1404				
35	P03	1384	-800	85	SEG45	-920	1404				
36	Vss	1384	-660	86	SEG46	-1000	1404				
37	P10	1384	-580	87	SEG47	-1080	1404				
38	P11	1384	-420	88	SEG48	-1160	1404				
39	VDD	1384	-340	89	SEG49	-1384	1200				
40	SEG0	1384	-240	90	COM0	-1384	1120				
41	SEG1	1384	-160	91	COM1	-1384	1040				
42	SEG2	1384	-80	92	COM2	-1384	960				
43	SEG3	1384	0	93	COM3	-1384	880				
44	SEG4	1384	80	94	COM4	-1384	800				
45	SEG5	1384	160	95	COM5	-1384	720				
46	SEG6	1384	240	96	COM6	-1384	640				
47	SEG7	1384	320	97	COM7	-1384	560				
48	SEG8	1384	400	98	COM8	-1384	480				
49	SEG9	1384	480	99	COM9	-1384	400				
50	SEG10	1384	560	100	COM10	-1384	320				

1.3.1.9 Pad Coordinates of ML610421 Chip

Table 1-3 Pad Coordinates of ML610421

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	RESET_N	-1090	-1324	51	SEG12	1294	630	101	PA4	-1294	60
2	P42	-1010	-1324	52	SEG13	1294	710	102	PA5	-1294	-20
3	P43	-930	-1324	53	SEG14	1294	790	103	PA6	-1294	-100
4	P44	-850	-1324	54	SEG15	1294	870	104	PA7	-1294	-180
5	P45	-770	-1324	55	SEG16	1294	950	105	P20	-1294	-270
6	P46	-690	-1324	56	SEG17	1294	1030	106	P21	-1294	-350
7	P47	-610	-1324	57	SEG18	1294	1110	107	P22	-1294	-430
8	P30	-530	-1324	58	SEG19	1160	1324	108	P40	-1294	-510
9	P31	-450	-1324	59	SEG20	1080	1324	109	P41	-1294	-590
10	P34	-370	-1324	60	SEG21	1000	1324	110	Vss	-1294	-670
11	P32	-290	-1324	61	SEG22	920	1324	111	AVss	-1294	-750
12	P33	-210	-1324	62	SEG23	840	1324	112	VREF	-1294	-830
13	P35	-130	-1324	63	SEG24	760	1324	113	AIN0	-1294	-910
14	TEST	-50	-1324	64	SEG25	680	1324	114	AIN1	-1294	-1082
15	VDD	30	-1324	65	SEG26	600	1324	115	AVDD	-1294	-1162
16	VDDL	110	-1324	66	SEG27	520	1324				
17	Vss	190	-1324	67	SEG28	440	1324				
18	VDDX	270	-1324	68	SEG29	360	1324				
19	XT0	350	-1324	69	SEG30	280	1324				
20	XT1	510	-1324	70	SEG31	200	1324				
21	Vss	590	-1324	71	SEG32	120	1324				
22	NMI	670	-1324	72	SEG33	40	1324				
23	VL1	750	-1324	73	SEG34	-40	1324				
24	VL2	830	-1324	74	SEG35	-120	1324				
25	VL3	910	-1324	75	SEG36	-200	1324				
26	VL4	990	-1324	76	SEG37	-280	1324				
27	C1	1070	-1324	77	SEG38	-360	1324				
28	C2	1150	-1324	78	SEG39	-440	1324				
29	C3	1294	-1220	79	SEG40	-520	1324				
30	C4	1294	-1140	80	SEG41	-600	1324				
31	P00	1294	-1050	81	SEG42	-680	1324				
32	P01	1294	-970	82	SEG43	-760	1324				
33	P02	1294	-890	83	SEG44	-840	1324				
34	P03	1294	-810	84	SEG45	-920	1324				
35	Vss	1294	-730	85	SEG46	-1000	1324				
36	P10	1294	-650	86	SEG47	-1080	1324				
37	P11	1294	-490	87	SEG48	-1160	1324				
38	VDD	1294	-410	88	SEG49	-1294	1110				
39	SEG0	1294	-330	89	COM0	-1294	1030				
40	SEG1	1294	-250	90	COM1	-1294	950				
41	SEG2	1294	-170	91	COM2	-1294	870				
42	SEG3	1294	-90	92	COM3	-1294	790				
43	SEG4	1294	-10	93	COM4	-1294	710				
44	SEG5	1294	70	94	COM5	-1294	630				
45	SEG6	1294	150	95	COM6	-1294	550				
46	SEG7	1294	230	96	COM7	-1294	470				
47	SEG8	1294	310	97	PA0	-1294	380				
48	SEG9	1294	390	98	PA1	-1294	300				
49	SEG10	1294	470	99	PA2	-1294	220				
50	SEG11	1294	550	100	PA3	-1294	140				

1.3.1.10 Pad Coordinates of ML610422 Chip

Table 1-4 Pad Coordinates of ML610422

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	RESET_N	-1090	-1324	51	SEG12	1294	630	101	COM12	-1294	60
2	P42	-1010	-1324	52	SEG13	1294	710	102	COM13	-1294	-20
3	P43	-930	-1324	53	SEG14	1294	790	103	COM14	-1294	-100
4	P44	-850	-1324	54	SEG15	1294	870	104	COM15	-1294	-180
5	P45	-770	-1324	55	SEG16	1294	950	105	P20	-1294	-270
6	P46	-690	-1324	56	SEG17	1294	1030	106	P21	-1294	-350
7	P47	-610	-1324	57	SEG18	1294	1110	107	P22	-1294	-430
8	P30	-530	-1324	58	SEG19	1160	1324	108	P40	-1294	-510
9	P31	-450	-1324	59	SEG20	1080	1324	109	P41	-1294	-590
10	P34	-370	-1324	60	SEG21	1000	1324	110	Vss	-1294	-670
11	P32	-290	-1324	61	SEG22	920	1324	111	AVss	-1294	-750
12	P33	-210	-1324	62	SEG23	840	1324	112	VREF	-1294	-830
13	P35	-130	-1324	63	SEG24	760	1324	113	AIN0	-1294	-910
14	TEST	-50	-1324	64	SEG25	680	1324	114	AIN1	-1294	-1082
15	VDD	30	-1324	65	SEG26	600	1324	115	AVDD	-1294	-1162
16	VDDL	110	-1324	66	SEG27	520	1324				
17	Vss	190	-1324	67	SEG28	440	1324				
18	VDDX	270	-1324	68	SEG29	360	1324				
19	XT0	350	-1324	69	SEG30	280	1324				
20	XT1	510	-1324	70	SEG31	200	1324				
21	Vss	590	-1324	71	SEG32	120	1324				
22	NMI	670	-1324	72	SEG33	40	1324				
23	VL1	750	-1324	73	SEG34	-40	1324				
24	VL2	830	-1324	74	SEG35	-120	1324				
25	VL3	910	-1324	75	SEG36	-200	1324				
26	VL4	990	-1324	76	SEG37	-280	1324				
27	C1	1070	-1324	77	SEG38	-360	1324				
28	C2	1150	-1324	78	SEG39	-440	1324				
29	C3	1294	-1220	79	SEG40	-520	1324				
30	C4	1294	-1140	80	SEG41	-600	1324				
31	P00	1294	-1050	81	SEG42	-680	1324				
32	P01	1294	-970	82	SEG43	-760	1324				
33	P02	1294	-890	83	SEG44	-840	1324				
34	P03	1294	-810	84	SEG45	-920	1324				
35	Vss	1294	-730	85	SEG46	-1000	1324				
36	P10	1294	-650	86	SEG47	-1080	1324				
37	P11	1294	-490	87	SEG48	-1160	1324				
38	VDD	1294	-410	88	SEG49	-1294	1110				
39	SEG0	1294	-330	89	COM0	-1294	1030				
40	SEG1	1294	-250	90	COM1	-1294	950				
41	SEG2	1294	-170	91	COM2	-1294	870				
42	SEG3	1294	-90	92	COM3	-1294	790				
43	SEG4	1294	-10	93	COM4	-1294	710				
44	SEG5	1294	70	94	COM5	-1294	630				
45	SEG6	1294	150	95	COM6	-1294	550				
46	SEG7	1294	230	96	COM7	-1294	470				
47	SEG8	1294	310	97	COM8	-1294	380				
48	SEG9	1294	390	98	COM9	-1294	300				
49	SEG10	1294	470	99	COM10	-1294	220				
50	SEG11	1294	550	100	COM11	-1294	140				

1.3.2 List of Pins

1.3.2.1 List of ML610Q421/ML610Q422 Pins

PAD No.		Primary function			Secondary function			Tertiary function		
Q422	Q421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
18,22, 36,111	18,22, 36,111	Vss	—	Negative power supply pin	—	—	—	—	—	—
16,39	16,39	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—
17	17	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—	—	—
19	19	V_{DDX}	—	Power supply pin for low-speed oscillation (internally generated)	—	—	—	—	—	—
1	1	V_{PP}	—	Power supply pin for Flash ROM	—	—	—	—	—	—
112	112	AV_{SS}	—	Negative power supply pin for successive approximation type ADC	—	—	—	—	—	—
116	116	AV_{DD}	—	Positive power supply pin for successive approximation type ADC	—	—	—	—	—	—
24	24	V_{L1}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
25	25	V_{L2}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
26	26	V_{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
27	27	V_{L4}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
28	28	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
29	29	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
30	30	C3	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
31	31	C4	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
15	15	TEST	I/O	Input/output pin for testing	—	—	—	—	—	—
2	2	RESET_N	I	Reset input pin	—	—	—	—	—	—
20	20	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
21	21	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
113	113	V_{REF}	—	Reference power supply pin for successive approximation type ADC	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q422	Q421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
114	114	AIN0	I	Successive approximation type ADC input	—	—	—	—	—	—
115	115	AIN1	I	Successive approximation type ADC input	—	—	—	—	—	—
23	23	NMI	I	Non-maskable interrupt pin	—	—	—	—	—	—
32	32	P00/EXI 0/CAP0	I	Input port, External interrupt 0, Capture 0 input	—	—	—	—	—	—
33	33	P01/EXI 1/CAP1	I	Input port, External interrupt 1, Capture 1 input	—	—	—	—	—	—
34	34	P02/EXI 2/RXD0	I	Input port, External interrupt 2, UART0 receive	—	—	—	—	—	—
35	35	P03/EXI 3	I	Input port, External interrupt 3	—	—	—	—	—	—
37	37	P10	I	Input port	OSC0	I	High-speed oscillation	—	—	—
38	38	P11	I	Input port	OSC1	O	High-speed oscillation	—	—	—
106	106	P20/LED 0	O	Output port	LSCLK	O	Low-speed clock output	—	—	—
107	107	P21LED 1	O	Output port	OUTCLK	O	High-speed clock output	—	—	—
108	108	P22/LED 2	O	Output port	MD0	O	Melody output	—	—	—
9	9	P30	I/O	Input/output port	IN0	I	RC type ADC0 oscillation input pin	—	—	—
10	10	P31	I/O	Input/output port	CS0	O	RC type ADC0 reference capacitor connection pin	—	—	—
11	11	P34	I/O	Input/output port	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin	PWM0	O	PWM output
12	12	P32	I/O	Input/output port	RS0	O	RC type ADC0 reference resistor connection pin	—	—	—
13	13	P33	I/O	Input/output port	RT0	O	RC type ADC0 resistor sensor connection pin	—	—	—
14	14	P35	I/O	Input/output port	RCM	O	RC type ADC oscillation monitor	—	—	—
109	109	P40	I/O	Input/output port	SDA	I/O	I^2C data input/output	SIN0	I	SSIO data input
110	110	P41	I/O	Input/output port	SCL	I/O	I^2C clock input/output	SCK0	I/O	SSIO synchronous clock
3	3	P42	I/O	Input/output port	RXD0	I	UART data input	SOUT0	O	SSIO data output
4	4	P43	I/O	Input/output port	TXD0	O	UART data output	PWM0	O	PWM output
5	5	P44/T02 P0CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	IN1	I	RC type ADC1 oscillation input pin	SIN0	I	SSIO0 data input
6	6	P45/T13 P1CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	CS1	O	RC type ADC1 reference capacitor connection pin	SCK0	I/O	SSIO0 synchronous clock
7	7	P46	I/O	Input/output port	RS1	O	RC type ADC1 reference resistor connection pin	SOUT0	O	SSIO0 data output
8	8	P47	I/O	Input/output port	RT1	O	RC type ADC1 resistor sensor connection pin	—	—	—
—	98	PA0	I/O	Input/output port	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q422	Q421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
—	99	PA1	I/O	Input/output port	—	—	—	—	—	—
—	100	PA2	I/O	Input/output port	—	—	—	—	—	—
—	101	PA3	I/O	Input/output port	—	—	—	—	—	—
—	102	PA4	I/O	Input/output port	—	—	—	—	—	—
—	103	PA5	I/O	Input/output port	—	—	—	—	—	—
—	104	PA6	I/O	Input/output port	—	—	—	—	—	—
—	105	PA7	I/O	Input/output port	—	—	—	—	—	—
90	90	COM0	O	LCD common pin	—	—	—	—	—	—
91	91	COM1	O	LCD common pin	—	—	—	—	—	—
92	92	COM2	O	LCD common pin	—	—	—	—	—	—
93	93	COM3	O	LCD common pin	—	—	—	—	—	—
94	94	COM4	O	LCD common pin	—	—	—	—	—	—
95	95	COM5	O	LCD common pin	—	—	—	—	—	—
96	96	COM6	O	LCD common pin	—	—	—	—	—	—
97	97	COM7	O	LCD common pin	—	—	—	—	—	—
98	—	COM8	O	LCD common pin	—	—	—	—	—	—
99	—	COM9	O	LCD common pin	—	—	—	—	—	—
100	—	COM10	O	LCD common pin	—	—	—	—	—	—
101	—	COM11	O	LCD common pin	—	—	—	—	—	—
102	—	COM12	O	LCD common pin	—	—	—	—	—	—
103	—	COM13	O	LCD common pin	—	—	—	—	—	—
104	—	COM14	O	LCD common pin	—	—	—	—	—	—
105	—	COM15	O	LCD common pin	—	—	—	—	—	—
40	40	SEG0	O	LCD segment pin	—	—	—	—	—	—
41	41	SEG1	O	LCD segment pin	—	—	—	—	—	—
42	42	SEG2	O	LCD segment pin	—	—	—	—	—	—
43	43	SEG3	O	LCD segment pin	—	—	—	—	—	—
44	44	SEG4	O	LCD segment pin	—	—	—	—	—	—
45	45	SEG5	O	LCD segment pin	—	—	—	—	—	—
46	46	SEG6	O	LCD segment pin	—	—	—	—	—	—
47	47	SEG7	O	LCD segment pin	—	—	—	—	—	—
48	48	SEG8	O	LCD segment pin	—	—	—	—	—	—
49	49	SEG9	O	LCD segment pin	—	—	—	—	—	—
50	50	SEG10	O	LCD segment pin	—	—	—	—	—	—
51	51	SEG11	O	LCD segment pin	—	—	—	—	—	—
52	52	SEG12	O	LCD segment pin	—	—	—	—	—	—
53	53	SEG13	O	LCD segment pin	—	—	—	—	—	—
54	54	SEG14	O	LCD segment pin	—	—	—	—	—	—
55	55	SEG15	O	LCD segment pin	—	—	—	—	—	—
56	56	SEG16	O	LCD segment pin	—	—	—	—	—	—
57	57	SEG17	O	LCD segment pin	—	—	—	—	—	—
58	58	SEG18	O	LCD segment pin	—	—	—	—	—	—
59	59	SEG19	O	LCD segment pin	—	—	—	—	—	—
60	60	SEG20	O	LCD segment pin	—	—	—	—	—	—
61	61	SEG21	O	LCD segment pin	—	—	—	—	—	—
62	62	SEG22	O	LCD segment pin	—	—	—	—	—	—
63	63	SEG23	O	LCD segment pin	—	—	—	—	—	—
64	64	SEG24	O	LCD segment pin	—	—	—	—	—	—
65	65	SEG25	O	LCD segment pin	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q422	Q421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
66	66	SEG26	O	LCD segment pin	—	—	—	—	—	—
67	67	SEG27	O	LCD segment pin	—	—	—	—	—	—
68	68	SEG28	O	LCD segment pin	—	—	—	—	—	—
69	69	SEG29	O	LCD segment pin	—	—	—	—	—	—
70	70	SEG30	O	LCD segment pin	—	—	—	—	—	—
71	71	SEG31	O	LCD segment pin	—	—	—	—	—	—
72	72	SEG32	O	LCD segment pin	—	—	—	—	—	—
73	73	SEG33	O	LCD segment pin	—	—	—	—	—	—
74	74	SEG34	O	LCD segment pin	—	—	—	—	—	—
75	75	SEG35	O	LCD segment pin	—	—	—	—	—	—
76	76	SEG36	O	LCD segment pin	—	—	—	—	—	—
77	77	SEG37	O	LCD segment pin	—	—	—	—	—	—
78	78	SEG38	O	LCD segment pin	—	—	—	—	—	—
79	79	SEG39	O	LCD segment pin	—	—	—	—	—	—
80	80	SEG40	O	LCD segment pin	—	—	—	—	—	—
81	81	SEG41	O	LCD segment pin	—	—	—	—	—	—
82	82	SEG42	O	LCD segment pin	—	—	—	—	—	—
83	83	SEG43	O	LCD segment pin	—	—	—	—	—	—
84	84	SEG44	O	LCD segment pin	—	—	—	—	—	—
85	85	SEG45	O	LCD segment pin	—	—	—	—	—	—
86	86	SEG46	O	LCD segment pin	—	—	—	—	—	—
87	87	SEG47	O	LCD segment pin	—	—	—	—	—	—
88	88	SEG48	O	LCD segment pin	—	—	—	—	—	—
89	89	SEG49	O	LCD segment pin	—	—	—	—	—	—

1.3.2.2 List of ML610421/ML610422 Pins

PAD No.		Primary function			Secondary function			Tertiary function		
422	421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
17,21, 35,110	17,21, 35,110	Vss	—	Negative power supply pin	—	—	—	—	—	—
15,38	15,38	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—
16	16	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—	—	—
18	18	V_{DDX}	—	Power supply pin for low-speed oscillation (internally generated)	—	—	—	—	—	—
111	111	AV_{SS}	—	Negative power supply pin for successive approximation type ADC	—	—	—	—	—	—
115	115	AV_{DD}	—	Positive power supply pin for successive approximation type ADC	—	—	—	—	—	—
23	23	V_{L1}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
24	24	V_{L2}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
25	25	V_{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
26	26	V_{L4}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
27	27	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
28	28	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
29	29	C3	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
30	30	C4	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
14	14	TEST	I	Input pin for testing	—	—	—	—	—	—
1	1	RESET_N	I	Reset input pin	—	—	—	—	—	—
19	19	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
20	20	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
112	112	V_{REF}	—	Reference power supply pin for successive approximation type ADC	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
422	421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
113	113	AIN0	I	Successive approximation type ADC input	—	—	—	—	—	—
114	114	AIN1	I	Successive approximation type ADC input	—	—	—	—	—	—
22	22	NMI	I	Non-maskable interrupt pin	—	—	—	—	—	—
31	31	P00/EXI 0/CAP0	I	Input port, External interrupt 0, Capture 0 input	—	—	—	—	—	—
32	32	P01/EXI 1/CAP1	I	Input port, External interrupt 1, Capture 1 input	—	—	—	—	—	—
33	33	P02/EXI 2/RXD0	I	Input port, External interrupt 2, UART0 receive	—	—	—	—	—	—
34	34	P03/EXI 3	I	Input port, External interrupt 3	—	—	—	—	—	—
36	36	P10	I	Input port	OSC0	I	High-speed oscillation	—	—	—
37	37	P11	I	Input port	OSC1	O	High-speed oscillation	—	—	—
105	105	P20/LED 0	O	Output port	LSCLK	O	Low-speed clock output	—	—	—
106	106	P21LED 1	O	Output port	OUTCLK	O	High-speed clock output	—	—	—
107	107	P22/LED 2	O	Output port	MD0	O	Melody output	—	—	—
8	8	P30	I/O	Input/output port	IN0	I	RC type ADC0 oscillation input pin	—	—	—
9	9	P31	I/O	Input/output port	CS0	O	RC type ADC0 reference capacitor connection pin	—	—	—
10	10	P34	I/O	Input/output port	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin	PWM0	O	PWM output
11	11	P32	I/O	Input/output port	RS0	O	RC type ADC0 reference resistor connection pin	—	—	—
12	12	P33	I/O	Input/output port	RT0	O	RC type ADC0 resistor sensor connection pin	—	—	—
13	13	P35	I/O	Input/output port	RCM	O	RC type ADC oscillation monitor	—	—	—
108	108	P40	I/O	Input/output port	SDA	I/O	I^2C data input/output	SIN0	I	SSIO data input
109	109	P41	I/O	Input/output port	SCL	I/O	I^2C clock input/output	SCK0	I/O	SSIO synchronous clock
2	2	P42	I/O	Input/output port	RXD0	I	UART data input	SOUT0	O	SSIO data output
3	3	P43	I/O	Input/output port	TXD0	O	UART data output	PWM0	O	PWM output
4	4	P44/T02 P0CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	IN1	I	RC type ADC1 oscillation input pin	SIN0	I	SSIO0 data input
5	5	P45/T13 P1CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	CS1	O	RC type ADC1 reference capacitor connection pin	SCK0	I/O	SSIO0 synchronous clock
6	6	P46	I/O	Input/output port	RS1	O	RC type ADC1 reference resistor connection pin	SOUT0	O	SSIO0 data output
7	7	P47	I/O	Input/output port	RT1	O	RC type ADC1 resistor sensor connection pin	—	—	—
—	97	PA0	I/O	Input/output port	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
422	421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
—	98	PA1	I/O	Input/output port	—	—	—	—	—	—
—	99	PA2	I/O	Input/output port	—	—	—	—	—	—
—	100	PA3	I/O	Input/output port	—	—	—	—	—	—
—	101	PA4	I/O	Input/output port	—	—	—	—	—	—
—	102	PA5	I/O	Input/output port	—	—	—	—	—	—
—	103	PA6	I/O	Input/output port	—	—	—	—	—	—
—	104	PA7	I/O	Input/output port	—	—	—	—	—	—
89	89	COM0	O	LCD common pin	—	—	—	—	—	—
90	90	COM1	O	LCD common pin	—	—	—	—	—	—
91	91	COM2	O	LCD common pin	—	—	—	—	—	—
92	92	COM3	O	LCD common pin	—	—	—	—	—	—
93	93	COM4	O	LCD common pin	—	—	—	—	—	—
94	94	COM5	O	LCD common pin	—	—	—	—	—	—
95	95	COM6	O	LCD common pin	—	—	—	—	—	—
96	96	COM7	O	LCD common pin	—	—	—	—	—	—
97	—	COM8	O	LCD common pin	—	—	—	—	—	—
98	—	COM9	O	LCD common pin	—	—	—	—	—	—
99	—	COM10	O	LCD common pin	—	—	—	—	—	—
100	—	COM11	O	LCD common pin	—	—	—	—	—	—
101	—	COM12	O	LCD common pin	—	—	—	—	—	—
102	—	COM13	O	LCD common pin	—	—	—	—	—	—
103	—	COM14	O	LCD common pin	—	—	—	—	—	—
104	—	COM15	O	LCD common pin	—	—	—	—	—	—
39	39	SEG0	O	LCD segment pin	—	—	—	—	—	—
40	40	SEG1	O	LCD segment pin	—	—	—	—	—	—
41	41	SEG2	O	LCD segment pin	—	—	—	—	—	—
42	42	SEG3	O	LCD segment pin	—	—	—	—	—	—
43	43	SEG4	O	LCD segment pin	—	—	—	—	—	—
44	44	SEG5	O	LCD segment pin	—	—	—	—	—	—
45	45	SEG6	O	LCD segment pin	—	—	—	—	—	—
46	46	SEG7	O	LCD segment pin	—	—	—	—	—	—
47	47	SEG8	O	LCD segment pin	—	—	—	—	—	—
48	48	SEG9	O	LCD segment pin	—	—	—	—	—	—
49	49	SEG10	O	LCD segment pin	—	—	—	—	—	—
50	50	SEG11	O	LCD segment pin	—	—	—	—	—	—
51	51	SEG12	O	LCD segment pin	—	—	—	—	—	—
52	52	SEG13	O	LCD segment pin	—	—	—	—	—	—
53	53	SEG14	O	LCD segment pin	—	—	—	—	—	—
54	54	SEG15	O	LCD segment pin	—	—	—	—	—	—
55	55	SEG16	O	LCD segment pin	—	—	—	—	—	—
56	56	SEG17	O	LCD segment pin	—	—	—	—	—	—
57	57	SEG18	O	LCD segment pin	—	—	—	—	—	—
58	58	SEG19	O	LCD segment pin	—	—	—	—	—	—
59	59	SEG20	O	LCD segment pin	—	—	—	—	—	—
60	60	SEG21	O	LCD segment pin	—	—	—	—	—	—
61	61	SEG22	O	LCD segment pin	—	—	—	—	—	—
62	62	SEG23	O	LCD segment pin	—	—	—	—	—	—
63	63	SEG24	O	LCD segment pin	—	—	—	—	—	—
64	64	SEG25	O	LCD segment pin	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
422	421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
65	65	SEG26	O	LCD segment pin	—	—	—	—	—	—
66	66	SEG27	O	LCD segment pin	—	—	—	—	—	—
67	67	SEG28	O	LCD segment pin	—	—	—	—	—	—
68	68	SEG29	O	LCD segment pin	—	—	—	—	—	—
69	69	SEG30	O	LCD segment pin	—	—	—	—	—	—
70	70	SEG31	O	LCD segment pin	—	—	—	—	—	—
71	71	SEG32	O	LCD segment pin	—	—	—	—	—	—
72	72	SEG33	O	LCD segment pin	—	—	—	—	—	—
73	73	SEG34	O	LCD segment pin	—	—	—	—	—	—
74	74	SEG35	O	LCD segment pin	—	—	—	—	—	—
75	75	SEG36	O	LCD segment pin	—	—	—	—	—	—
76	76	SEG37	O	LCD segment pin	—	—	—	—	—	—
77	77	SEG38	O	LCD segment pin	—	—	—	—	—	—
78	78	SEG39	O	LCD segment pin	—	—	—	—	—	—
79	79	SEG40	O	LCD segment pin	—	—	—	—	—	—
80	80	SEG41	O	LCD segment pin	—	—	—	—	—	—
81	81	SEG42	O	LCD segment pin	—	—	—	—	—	—
82	82	SEG43	O	LCD segment pin	—	—	—	—	—	—
83	83	SEG44	O	LCD segment pin	—	—	—	—	—	—
84	84	SEG45	O	LCD segment pin	—	—	—	—	—	—
85	85	SEG46	O	LCD segment pin	—	—	—	—	—	—
86	86	SEG47	O	LCD segment pin	—	—	—	—	—	—
87	87	SEG48	O	LCD segment pin	—	—	—	—	—	—
88	88	SEG49	O	LCD segment pin	—	—	—	—	—	—

1.3.3 Description of Pins

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V_{SS} as required.	—	—
OSC0	I	Crystal/ceramic connection pin for high-speed clock.	Secondary	—
OSC1	O	A crystal or ceramic is connected to this pin (4.1 MHz max.). Capacitors CDH and CGH (see measuring circuit 1) are connected across this pin and V_{SS}. This pin is used as the secondary function of the P10 pin(OSC0) and P11 pin(OSC1).	Secondary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P03	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P10-P11	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20-P22	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
PA0-PA7	I/O	General-purpose input/output port. These pins are for the ML610Q421/ML610421, but are not provided in the ML610Q422/ML610422.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/Secondary	Positive
I^2C bus interface				
SDA	I/O	I^2C data input/output pin. This pin is used as the secondary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
SCL	I/O	I^2C clock input/output pin. This pin is used as the secondary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P43 or P34 pin.	Tertiary	Positive
T02P0CK	O	PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
External interrupt				
NMI	I	External non-maskable interrupt input pin. An interrupt is generated on both edges.	Primary	Positive/ negative
EXI0-3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P03 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
CAP1	I		Primary	Positive/ negative
Timer				
T02P0CK	I	External clock input pin used for both Timer 0 and Timer 2. The clocks for these timers are selected by software. This pin is used as the primary function of the P44 pin.	Primary	—
T13P1CK	I	External clock input pin used for both Timer 1 and Timer 3. The clocks for these timers are selected by software. This pin is used as the primary function of the P45 pin.	Primary	—
Melody				
MD0	O	Melody/buzzer signal output pin. This pin is used as the secondary function of the P22 pin.	Secondary	Positive/ negative
LED drive				
LED0-2	O	Nch open drain output pins to drive LED.	Primary	Positive/ negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
Successive approximation type A/D converter				
AV_{SS}	—	Negative power supply pin for successive approximation type A/D converter.	—	—
AV_{DD}	—	Positive power supply pin for successive approximation type A/D converter.	—	—
V_{REF}	—	Reference power supply pin for successive approximation type A/D converter.	—	—
AIN0	I	Channel 0 analog input for successive approximation type A/D converter.	—	—
AIN1	I	Channel 1 analog input for successive approximation type A/D converter.	—	—
LCD drive signal				
COM0-7	O	Common output pins.	—	—
COM8-15	O	Common output pins. These pins are for the ML610Q422/ML610422, but are not provided in the ML610Q421/ML610421.	—	—
SEG0-49	O	Segment output pin.	—	—
LCD driver power supply				
V_{L1}	—	Power supply pins for LCD bias (internally generated). Capacitors Ca, Cb, Cc, and Cd (see measuring circuit 1) are connected between V_{SS} and V_{L1}, V_{L2}, V_{L3}, and V_{L4}, respectively.	—	—
V_{L2}	—		—	—
V_{L3}	—		—	—
V_{L4}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitors C12 and C34 (see measuring circuit 1) are connected between C1 and C2 and between C3 and C4, respectively.	—	—
C2	—		—	—
C3	—		—	—
C4	—		—	—
For testing				
TEST	I/O	ML610Q421/ML610Q422:Input/output pin for testing. ML610421/ML610422:Input pin for testing. ML610Q421/ML610Q422/ML610421/ML610422:A pull-down resistor is internally connected	—	—
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin.	—	—

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors CL0 and CL1 (see measuring circuit 1) are connected between this pin and V_{SS}.	—	—
V_{DDX}	—	Plus-side power supply pin (internally generated) for low-speed oscillation. Capacitor Cx (see measuring circuit 1) is connected between this pin and V_{SS}.	—	—
V_{PP}	—	Power supply pin for programming Flash ROM. A pull-up resistor is internally connected. These pins are for the ML610Q421/ML610Q422, but are not provided in the ML610421/ML610422.	—	—

1.3.4 Termination of Unused Pins

Table 1-5 shows methods of terminating the unused pins.

Table 1-5 Termination of Unused Pins

Pin	Recommended pin termination
V_{PP} *1	Open
AV_{DD}	V_{SS}
AV_{SS}	V_{SS}
V_{REF}	V_{SS}
AIN0, AIN1	Open
V_{L1}, V_{L2}, V_{L3}, V_{L4}	Open
C1, C2, C3, C4	Open
RESET_N	Open
TEST	Open
NMI	Open
P00 to P03	V_{DD} or V_{SS}
P10 to P11	V_{DD}
P20 to P22	Open
P30 to P35	Open
P40 to P47	Open
PA0 to PA7 *2	Open
COM0 to 7	Open
COM8 to 15 *3	Open
SEG0 to 49	Open

*1: ML610Q421/ML610Q422 only
*2: ML610Q421/ML610421 only
*3: ML610Q422/ML610422 only

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

Chapter 2

CPU and Memory Space

2. CPU and Memory Space

2.1 Overview

This LSI includes 8-bit CPU nX-U8/100 and the memory model is "SMALL model" .
For details of the CPU nX-U8/100, see "nX-U8/100 Core Instruction Manual".

2.2 Program Memory Space

The program memory space is used to store program codes, table data (ROM window), or vector tables.
The program codes have a length of 16 bits and are specified by a 16-bit program counter (PC).
The ROM window area data has a length of 8 bits and can be used as table data.
The vector table, which has 16-bit long data, can be used as reset vectors, hardware interrupt vectors, and software interrupt vectors.
The program memory space consists of 1 segments and has 32-Kbyte (16-Kword) capacity.
Figure 2-1 shows the configuration of the program memory space.

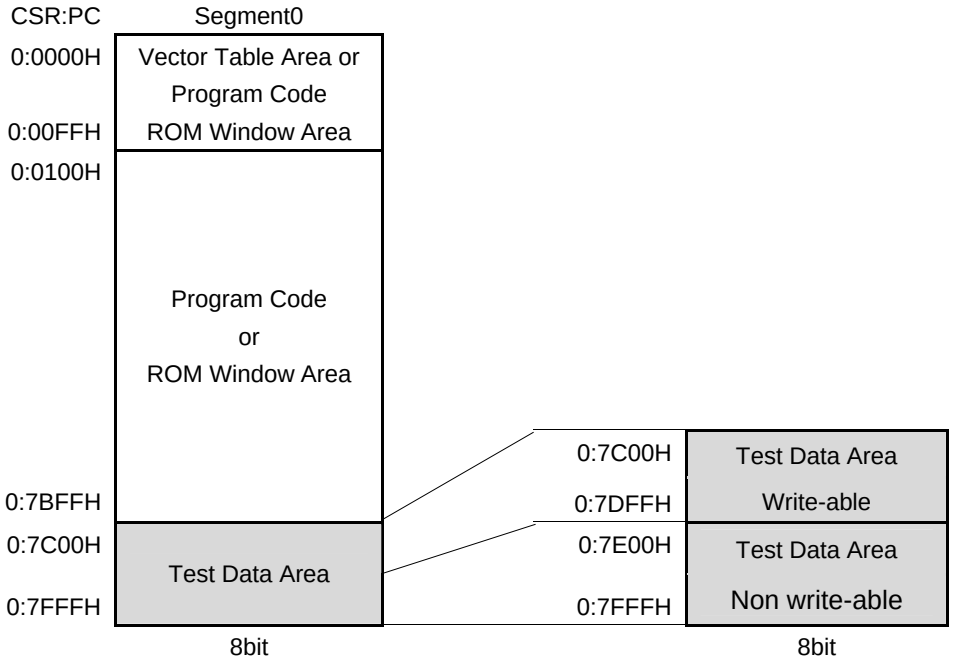


Figure 2-1 Configuration of Program Memory Space

Notes:
- Since test program data is stored in the 1024Byte (512Word) test data area (0:7C00H to 0:7FFFH) of Segment 0, this area cannot be used as a program code area.
- ML610Q421/ML610Q422
  The address "0: 7C00H to 0: 7DFFH" in the test area is write-able and erase-able. Fill the area with "0FFH".
  If data in the area is uncertain or other data (i.e. not 0FFH), operating with the code can not be guaranteed.
- Set "0FFH" data (BRK instruction) in the unused area of the program memory space.

2.3 Data Memory Space

The data memory space of this LSI consists of the ROM window area, 1KByte RAM area and SFR area of Segment 0 and the ROM reference areas of the Segment 1 and Segment 8.
The data memory stores 8-bit data and is specified by 20 bits consisting of higher 4 bits as DSR and lower 16 bits as addressing specified by each instruction.
Figure 2-2 shows the configuration of the data memory space.

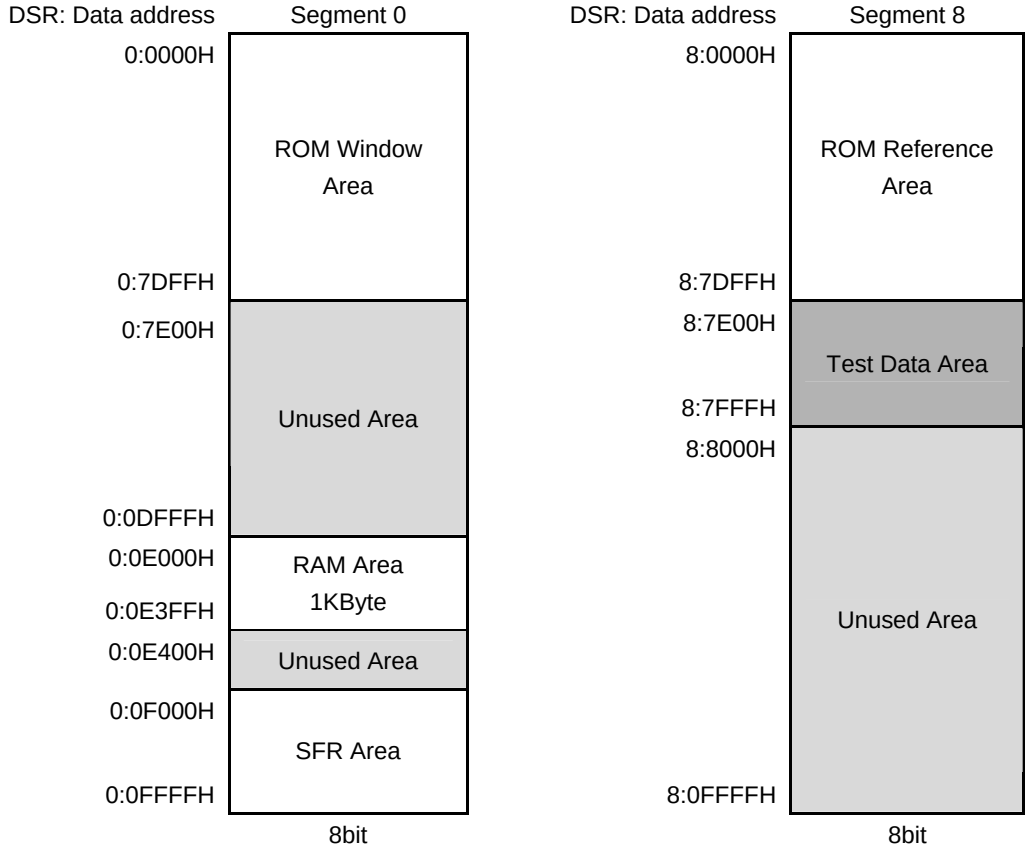


Figure 2-2 Configuration of Data Memory Space

Notes:
– The contents of the 1-Kbyte RAM area are undefined at system reset. Initialize this area by software.
– The contents of Segment 0 of the program memory space is read from the ROM reference area of Segment 8.

2.4 Instruction Length

The length of a instruction is 16 bits.

2.5 Data Type

The data types supported include byte (8 bits) and word (16 bits).

2.6 Description of Registers

2.6.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F000H	Data segment register	DSR	—	R/W	8	00H

2.6.2 Data Segment Register (DSR)

Address: 0F000H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
DSR	—	—	—	—	DSR3	DSR2	DSR1	DSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSR is a special function register (SFR) to retain a data segment. For details of DSR, see "nX-U8/100 Core Instruction Manual".

[Description of Bits]

- **DSR3-DSR0** (bits 3-0)

DSR3	DSR2	DSR1	DSR0	Description
0	0	0	0	Data segment 0 (initial value)
0	0	0	1	Prohibited
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	Data segment 8
1	0	0	1	Prohibited
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Chapter 3

Reset Function

3. Reset Function

3.1 Overview

This LSI has the five reset functions shown below. If any of the five reset conditions is satisfied, this LSI enters system reset mode.

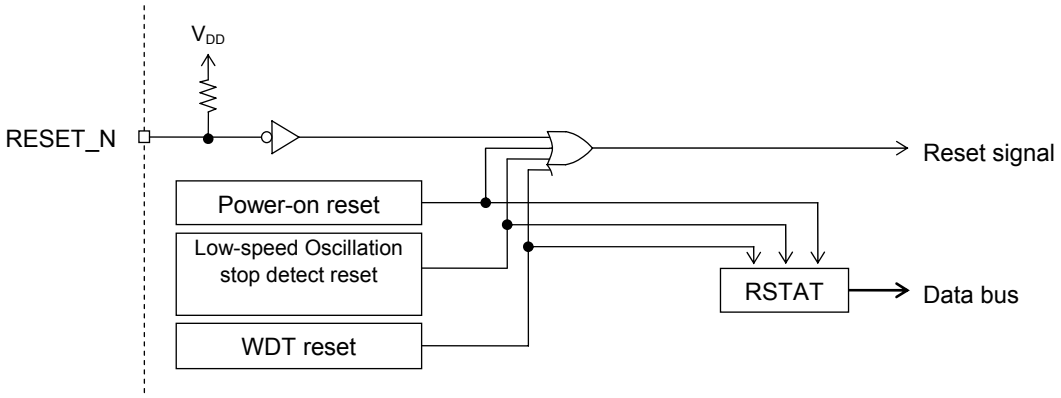
- Reset by the RESET_N pin
- Reset by power-on detection
- Reset by the low-speed oscillation stop detection
- Reset by the 2nd watchdog timer (WDT) overflow
- Software reset by execution of the BRK instruction

3.1.1 Features

- The RESER_N pin has an internal pull-up resistor
- The low-speeed oscillation stop deteciton time is 3 ms (typ.)
- 250 ms, 1 sec, 4 sec, or 16 sec can be selected as the 2nd watchdog timer (WDT) overflow period
- Built-in reset status register (RSTAT) indicating the reset generation causes
- Only the CPU is reset by the BRK instruction (neither the RAM area nor the SFR area are reset).

3.1.2 Configuration

Figure 3-1 shows the configuration of the reset generation circuit.



RSTAT:Reset status register

Figure 3-1 Configuration of Reset Generation Circuit

3.1.3 List of Pin

Pin name	I/O	Description
RESET_N	I	Reset input pin

3.2 Description of Registers

3.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F001H	Reset status register	RSTAT	—	R/W	8	—

3.2.2 Reset Status Register (RSTAT)

Address: 0F001H
Access: R/W
Access size: 8 bits
Initial value: Undefined

	7	6	5	4	3	2	1	0
RSTAT	—	—	—	—	—	WDTR	XSTR	POR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	x	1

RSTAT is a special function register (SFR) that indicates the causes by which the reset is generated.
At the occurrence of reset, the contents of RSTAT are not initialized, while the bit indicating the cause of the reset is set to "1". When checking the reset cause using this function, perform write operation to RSTAT in advance and initialize the contents of RSTAT to "00H".

[Description of Bits]

- **POR** (bit 0)
  The POR bit is a flag that indicates that the power-on reset is generated. This bit is set to "1" when powered on.

POR	Description
0	Power-on reset not generated
1	Power-on reset generated

- **XSTR** (bit 1)
  The XSTR bit is a flag that indicates the generation of low-speed oscillation stop detect reset. When low-speed oscillation stops for the period specified by the low-speed oscillation stop detection time (TSTOP) or more, this bit is set to "1".

XSTR	Description
0	Low-speed oscillation stop detect reset not occurred
1	Low-speed oscillation stop detect reset occurred

- **WDTR** (bit 2)
  The WSDTR is a flag that indicates that the watchdog timer reset is generated. This bit is set to "1" when the reset by overflow of the watchdog timer is generated.

WDTR	Description
0	Watchdog timer reset not occurred
1	Watchdog timer reset occurred

Note:
No flag is provided that indicates the occurrence of reset by the RESET_N pin.

3.3 Description of Operation

3.3.1 Operation of System Reset Mode

System reset has the highest priority among all the processings and any other processing being executed up to then is cancelled.
The system reset mode is set by any of the following causes.

- Reset by the RESET_N pin
- Reset by power-on detection
- Reset by low-speed oscillation stop detection
- Reset by 2nd watchdog timer (WDT) overflow
- Software reset by the BRK instruction (only the CPU is reset)

In system reset mode, the following processing is performed.

(1) The power circuit is initialized, but not initialized by the reset by the BRK instruction execution. For the details of the power circuit, refer to Chapter 28, "Power Circuit".
(2) All the special function registers (SFRs) whose initial value is not undefined are initialized. However, the initialization is not performed by software reset due to execution of the BRK instruction. See Appendix A "Registers" for the initial values of the SFRs.
(3) CPU is initialized.
   - All the registers in CPU are initialized.
   - The contents of addresses 0000H and 0001H in the program memory are set to the stack pointer (SP).
   - The contents of addresses 0002H and 0003H in the program memory are set to the program counter (PC). However, when the interrupt level (ELEEVL) of the program status word (PSW) at reset by the BRK instruction is 1 or lower, the contents of addresses 0004H and 0005H of the program memory are set in the program counter (PC). For the BRK instruction, see "nX-U8/100 Core Instruction Manual".

Note:
In system reset mode, the contents of data memory and those of any SFR whose initial value is undefined are not initialized and are undefined. Initialize them by software.
In system reset mode by the BRK instruction, no special function register (SFR) that has a fixed initial value is initialized either. Therefore initialize such an SFR by software.

Chapter 4

MCU Control Function

4. MCU Control Function

4.1 Overview

The operating states of this LSI are classified into the following 4 modes including system reset mode:

System reset mode
Program run mode
HALT mode
STOP mode

For system reset mode, see Chapter 3, "Reset Function".

This LSI has a block control function, which power downs the circuits of unused peripherals (reset registers and stop clock supplies) to make even more reducing the current consumption.

4.1.1 Features

- HALT mode, where the CPU stops operating and only the peripheral circuit is operating
- STOP mode, where both low-speed oscillation and high-speed oscillation stop
- Stop code acceptor function, which controls transition to STOP mode
- Block control function, which power downs the circuits of unused peripherals (reset registers and stop clock supplies).

4.1.2 Configuration

Figure 4-1 shows an operating state transition diagram.

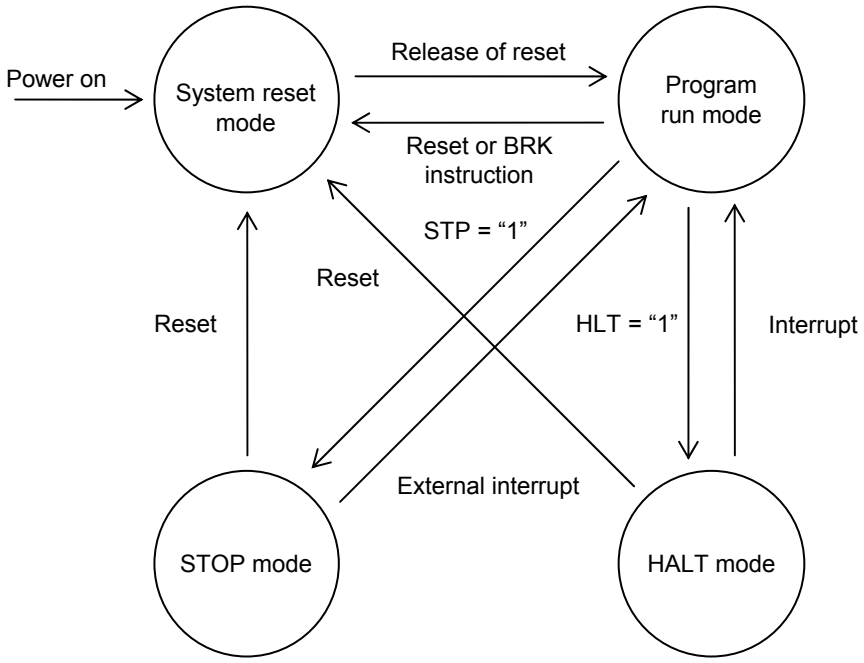


Figure 4-1 Operating State Transition Diagram

4.2 Description of Registers

4.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F008H	Stop code acceptor	STPACP	—	W	8	—
0F009H	Standby control register	SBYCON	—	W	8	00H
0F028H	Block control register 0	BLKCON0	—	R/W	8	00H
0F029H	Block control register 1	BLKCON1	—	R/W	8	00H
0F02AH	Block control register 2	BLKCON2	—	R/W	8	00H
0F02BH	Block control register 3	BLKCON3	—	R/W	8	00H
0F02CH	Block control register 4	BLKCON4	—	R/W	8	00H

4.2.2 Stop Code Acceptor (STPACP)

Address: 0F008H
Access: W
Access size: 8 bits
Initial value: — (Undefined)

	7	6	5	4	3	2	1	0
STPACP	—	—	—	—	—	—	—	—
W	W	W	W	W	W	W	W	W
Initial value	—	—	—	—	—	—	—	—

STPACP is a write-only special function register (SFR) that is used for setting a STOP mode.
When STPACP is read, "00H" is read.
When data is written to STPACP in the order of "5nH"(n: an arbitrary value) and "0AnH"(n: an arbitrary value), the stop code acceptor is enabled. When the STP bit of the standby control register (SBYCON) is set to "1" in this state, the mode is changed to the STOP mode. When the STOP mode is set, the STOP code acceptor is disabled.
When another instruction is executed between the instruction that writes "5nH" to STPACP and the instruction that writes "0AnH", the stop code acceptor is enabled after "0AnH" is written. However, if data other than "0AnH" is written to STPACP after "5nH" is written, the "5nH" write processing becomes invalid so that data must be written again starting from "5nH".
During a system reset, the stop code acceptor is disabled.

Note:
The STOP code acceptor can not be enabled on the condition of that both any interrupt enable flag and the corresponding interrupt request flag are "1"(An interrupt request occurrence with resetting MIE flag will have the condition).

4.2.3 Standby Control Register (SBYCON)

Address: 0F009H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SBYCON	—	—	—	—	—	—	STP	HLT
W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

SBYCON is a special function register (SFR) to control operating mode of MCU.

[Description of Bits]

- **STP** (bit 1)
  The STP bit is used for setting the STOP mode. When the STP bit is set to "1" with the stop code adapter enabled by using STPACP, the mode is changed to the STOP mode. When the NMI interrupt request or the P00–P03 interrupt request enabled by the interrupt enable register 1 (IE1) is issued, the STP bit is set to "0" and the LSI returns to the program run mode.

- **HLT** (bit 0)
  The HALT bit is used for setting a HALT mode. When the HALT bit is set to "1", the mode is changed to the HALT mode. When the NMI interrupt request, WDT interrupt request, or enabled (the interrupt enable flag is "1") interrupt request is issued, the HALT bit is set to "1" and the mode is returned to program run mode.

STP	HLT	Description
0	0	Program run mode (initial value)
0	1	HALT mode
1	0	STOP mode
1	1	Prohibited

Note:
The mode can not be changed to HALT mode or STOP mode on the condition of that both any interrupt enable flag and the corresponding interrupt request flag are "1"(An interrupt request occurrence with resetting MIE flag will have the condition).
When a maskable interrupt source (interrupt with enable bit) occurs while the MIE flag of the program status word (PSW) in the nX-U8/100 core is "0", the STOP mode and the HALT mode are simply released and interrupt processing is not performed. Refer to the "nX-U8/100 Core Instruction Manual" for details of PSW.

4.2.4 Block Control Register 0(BLKCON0)

Address: 0F028H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON0	—	—	—	—	DTM3	DTM2	DTM1	DTM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON0 is a special function register (SFR) to make even more reducing current consumption by turning unused peripherals off.

[Description of Bits]

- **DTM3** (bit 3)
  The DTM3 bit is used to control Timer3 operation. When the DTM3 bit is set to "1", the circuits related to Timer 3 are reset and turned off.

DTM3	Description
0	Enable operating Timer 3 (initial value)
1	Disable operating Timer 3

- **DTM2** (bit 2)
  The DTM2 bit is used to control Timer2 operation. When the DTM2 bit is set to "1", the circuits related to Timer 2 are reset and turned off.

DTM2	Description
0	Enable operating Timer 2 (initial value)
1	Disable operating Timer 2

- **DTM1** (bit 1)
  The DTM1 bit is used to control Timer1 operation. When the DTM1 bit is set to "1", the circuits related to Timer 1 are reset and turned off.

DTM1	Description
0	Enable operating Timer 1 (initial value)
1	Disable operating Timer 1

- **DTM0** (bit 0)
  The DTM0 bit is used to control Timer3 operation. When the DTM0 bit is set to "1", the circuits related to Timer 3 are reset and turned off.

DTM0	Description
0	Enable operating Timer 3 (initial value)
1	Disable operating Timer 3

Note:
When certain bits of block control registers are set to "1", corresponding peripherals are reset (all registers are reset) and operating clocks for the peripherals stop. Writing to every SFR (special function register) in the corresponding peripherals is not valid while the bits of block control registers are set to "1" and returns the initial value for read. Ensure the bits are reset to "0" before using the peripherals to enable the operation.

See Chapter 10, "Timers" for detail about operation of Timer 0, Timer 1, Timer 2 and Timer 3.

4.2.5 Block Control Register 1(BLKCON1)

Address: 0F029H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON1	—	DCAPR	—	DT1K	—	—	—	DPW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON1 is a special function register (SFR) to make even more reducing current consumption by turning unused peripherals off.

[Description of Bits]

- **DCAPR** (bit 6)
  The DCAPR bit is used to control Capture operation. When the DCAPR bit is set to "1", the circuits related to Capture are reset and turned off.

DCAPR	Description
0	Enable operating Capture (initial value)
1	Disable operating Capture

- **DT1K** (bit 4)
  The DT1K bit is used to control 1kHz Timer operation. When the DT1K bit is set to "1", the circuits related to 1kHz Timer are reset and turned off.

DT1K	Description
0	Enable operating 1kHz Timer (initial value)
1	Disable operating 1kHz Timer

- **DPW0** (bit 0)
  The DPW0 bit is used to control PWM0 operation. When the DPW0 bit is set to "1", the circuits related to PWM0 are reset and turned off.

DPW0	Description
0	Enable operating PWM0 (initial value)
1	Disable operating PWM0

Note:
When certain bits of block control registers are set to "1", corresponding peripherals are reset (all registers are reset) and operating clocks for the peripherals stop. Writing to every SFR (special function register) in the corresponding peripherals is not valid while the bits of block control registers are set to "1" and returns the initial value for read. Ensure the bits are reset to "0" before using the peripherals to enable the operation.

See Chapter 8, "Capture" for detail about operation of Capture.
See Chapter 9, "1kHz Timer" for detail about operation of 1kHz Timer.
See Chapter 11, "PWM" for detail about operation of PWM.

4.2.6 Block Control Register 2(BLKCON2)

Address: 0F02AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON2	DI2C0	—	—	—	—	DUA0	—	DSIO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON2 is a special function register (SFR) to make even more reducing current consumption by turning unused peripherals off.

[Description of Bits]

- **DI2C0** (bit 7)
  The DI2C0 bit is used to control I2C bus interface operation. When the DI2C0 bit is set to "1", the circuits related to I2C bus interface are reset and turned off.

DI2C0	Description
0	Enable operating I2C (initial value)
1	Disable operating I2C

- **DUA0** (bit 2)
  The DUA0 bit is used to control UART operation. When the DUA0 bit is set to "1", the circuits related to UART are reset and turned off.

DUA0	Description
0	Enable operating UART (initial value)
1	Disable operating UART

- **DSIO0** (bit 0)
  The DSIO0 bit is used to control SSIO operation. When the DSIO0 bit is set to "1", the circuits related to SSIO are reset and turned off.

DSIO0	Description
0	Enable operating SSIO (initial value)
1	Disable operating SSIO

Note:
When certain bits of block control registers are set to "1", corresponding peripherals are reset (all registers are reset) and operating clocks for the peripherals stop. Writing to every SFR (special function register) in the corresponding peripherals is not valid while the bits of block control registers are set to "1" and returns the initial value for read. Ensure the bits are reset to "0" before using the peripherals to enable the operation.

See Chapter 15, "I2C Bus Interface" for detail about operation of I2C Bus Interface.
See Chapter 14, "UART" for detail about operation of UART.
See Chapter 13, "Synchronous Serial Port" for detail about operation of SSIO.

4.2.7 Block Control Register 3(BLKCON3)

Address: 0F02BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON3	—	—	—	—	—	—	—	DMD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON3 is a special function register (SFR) to make even more reducing current consumption by turning unused peripherals off.

[Description of Bits]

- **DMD0** (bit 0)
  The DMD0 bit is used to control Melody/Buzzer operation. When the DMD0 bit is set to "1", the circuits related to Melody/Buzzer are reset and turned off.

DMD0	Description
0	Enable operating Melody/Buzzer (initial value)
1	Disable operating Melody/Buzzer

Note:
When certain bits of block control registers are set to "1", corresponding peripherals are reset (all registers are reset) and operating clocks for the peripherals stop. Writing to every SFR (special function register) in the corresponding peripherals is not valid while the bits of block control registers are set to "1" and returns the initial value for read. Ensure the bits are reset to "0" before using the peripherals to enable the operation.

See Chapter 23, "Melody Driver" for detail about operation of Melody/Buzzer.

4.2.8 Block Control Register 4(BLKCON4)

Address: 0F02CH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON4	—	DLCD	DBLD	DXTSP	—	—	DRAD	DSAD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON4 is a special function register (SFR) to make even more reducing current consumption by turning unused peripherals off.

[Description of Bits]

- **DLCD** (bit 6)
  The DLCD bit is used to control LCD driver operation. When the DLCD bit is set to "1", the circuits related to LCD driver are reset and turned off.

DLCD	Description
0	Enable operating LCD driver (initial value)
1	Disable operating LCD driver

- **DBLD** (bit 5)
  The DBLD bit is used to control BLD (Battery Level Detector) operation. When the DBLD bit is set to "1", the circuits related to BLD are reset and turned off.

DBLD	Description
0	Enable operating BLD (initial value)
1	Disable operating BLD driver

- **DXTSP** (bit 4)
  The DXTSP bit is used to control 32kHz oscillation stop detect operation. Only during HALT mode, When the DXTSP bit is set to "1", the circuits related to 32kHz oscillation stop detect are reset and turned off. When the operating mode is not in HALT, the 32kHz oscillation stop detect is always working regardless the condition of this bit.

DXTSP	Description
0	Enable operating 32kHz oscillation stop detect (initial value)
1	Disable operating 32kHz oscillation stop detect in HALT mode

- **DRAD** (bit 1)
  The DRAD bit is used to control RC type A/D converter operation. When the DRAD bit is set to "1", the circuits related to RC type A/D converter are reset and turned off.

DRAD	Description
0	Enable operating RC type A/D converter (initial value)
1	Disable operating RC type A/D converter

- **DSAD** (bit 0)
  The DSAD bit is used to control SA type A/D converter operation. When the DSAD bit is set to "1", the circuits related to SA type A/D converter are reset and turned off.

DSAD	Description
0	Enable operating SA type A/D converter (initial value)
1	Disable operating SA type A/D converter

Note:
When certain bits of block control registers are set to "1", corresponding peripherals are reset (all registers are reset) and operating clocks for the peripherals stop. Writing to every SFR (special function register) in the corresponding peripherals is not valid while the bits of block control registers are set to "1" and returns the initial value for read. Ensure the bits are reset to "0" before using the peripherals to enable the operation.

See Chapter 26, "LCD Driver" for detail about operation of LCD driver.
See Chapter 27, "Battery Level Detector" for detail about operation of BLD.
See Chapter 3, "Reset Function" for detail about operation of 32kHz oscillation stop detector.
See Chapter 24, "RC Oscillation Type A/D Converter" for detail about operation of RC oscillation type A/D converter.
See Chapter 25, "Successive Approximation" for detail about operation of SA type A/D converter.

4.3 Description of Operation

4.3.1 Program Run Mode

The program run mode is the state where the CPU executes instructions sequentially.
At power-on reset, RESET_N pin reset, low-speed oscillation stop detect reset, or WDT overflow reset, the CPU executes instructions from the addresses that are set in addresses 0002H and 0003H of program memory (ROM) after the system reset mode is released.
At reset by the BRK instruction, the CPU executes instructions from the addresses that are set in the addresses 0004H and 0005H of the program memory after the system reset mode is released. However, when the value of the interrupt level bit (ELEVEL) of the program status word (PSW) is 02H or higher at execution of the BRK instruction (after the occurrence of the WDT interrupt or NMI interrupt), the CPU executes instructions from the addresses that are set in the addresses 0002H and 0003H.
For details of the BRK instruction and PSW, see the "nX-U8/100 Core Instruction Manual" and for the reset function, see Chapter 3, "Reset Function".

4.3.2 HALT Mode

The HALT mode is the state where the CPU interrupts execution of instructions and only the peripheral circuits are running.
When the HLT bit of the standby control register (SBYCON) is set to "1", the HALT mode is set.
When a NMI interrupt request, a WDT interrupt request, or an interrupt request enabled by an interrupt enable register (IE1–IE7) is issued, the HLT bit is set to "0" on the falling edge of the next system clock (SYSCLK) and the HALT mode is returned to the program run mode released.
Figure 4-2 shows the operation waveforms in HALT mode.

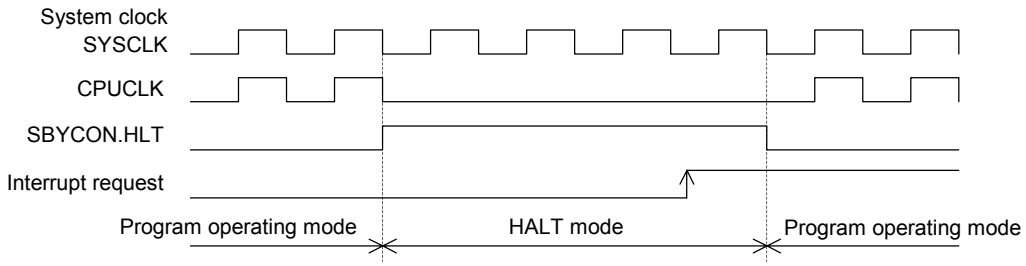


Figure 4-2 Operation Waveforms in HALT Mode

Note:
Since up to two instructions are executed during the period between HALT mode release and a transition to interrupt processing, place two NOP instructions next to the instruction that sets the HLT bit to "1".

4.3.3 STOP Mode

The STOP mode is the state where low-speed oscillation and high-speed oscillation stop and the CPU and peripheral circuits stop the operation.
When the stop code acceptor is enabled by writing "5nH"(n: an arbitrary value) and "0AnH"(n: an arbitrary value) to the stop code acceptor (STPACP) sequentially and the STP bit of the standby control register (SBYCON) is set to "1", the STOP mode is entered. When the STOP mode is set, the stop code acceptor is disabled.
When a NMI interrupt request or an interrupt-enabled (the interrupt enable flag is "1") P00 to P003 interrupt request is issued, the STP bit is set to "0", the STOP mode is released, and the mode is returned to the program run mode.

4.3.3.1 STOP Mode When CPU Operates with Low-Speed Clock

When the stop code acceptor is in the enabled state and the STP bit of SBYCON is set to "1", the STOP mode is entered, stopping low-speed oscillation and high-speed oscillation.
When the NMI interrupt request or the interrupt-enabled (the interrupt enable flag is "1") P00 to P03 interrupt request is issued, the STP bit is set to "0" and low-speed oscillation restarts. If the high-speed clock was oscillating before the STOP mode is entered, the high-speed oscillation restarts. When the high-speed clock was not oscillating before the STOP mode is entered, high-speed oscillation does not start.
When an interrupt request occurs, the STOP mode is released after the elapse of the low-speed oscillation start time (TXTL) and the low-speed clock (LSCLK) oscillation settling time (8192-pulse count), the mode is returned to the program mode, and the low-speed clock (LSCLK) restarts supply to the peripheral circuits. If the high-speed clock already started oscillation at this time, the high-speed clocks (OSCLK and HSCLK) also restart supply to the peripheral circuits.
For the low-speed oscillation start time (TXTL), see the "Electrical Characteristics" Section in Appendix C.
Figure 4-3 shows the operation waveforms in STOP mode when CPU operates with the low-speed clock.

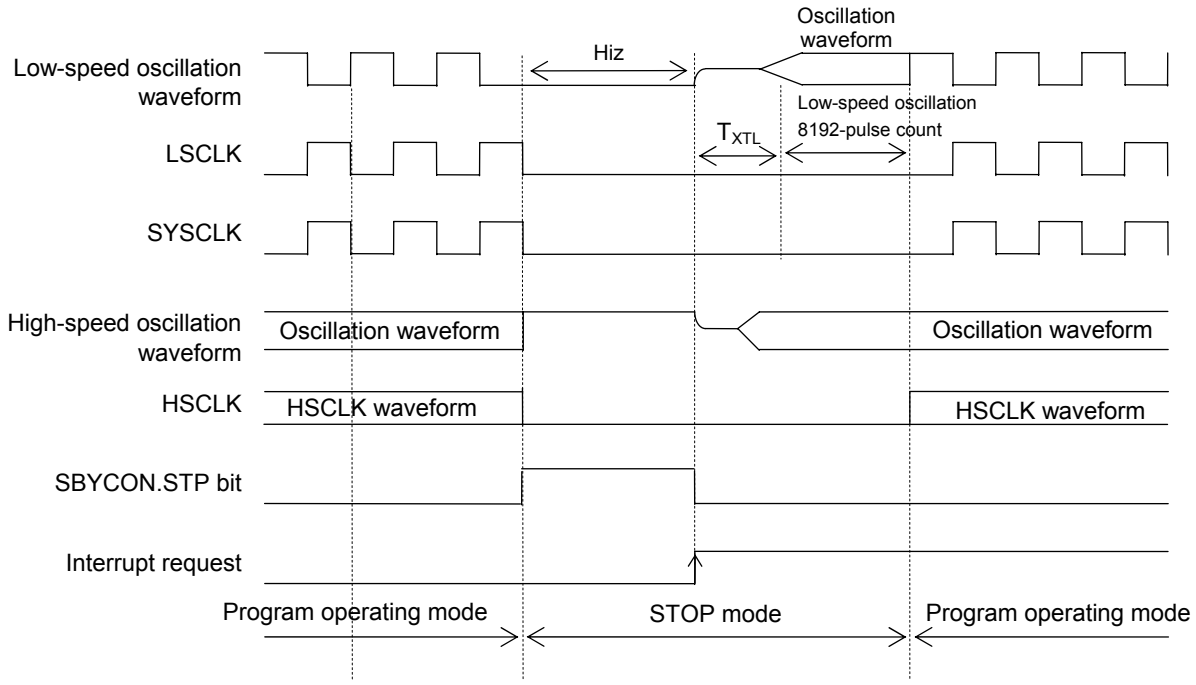


Figure 4-3 Operation Waveforms in STOP Mode When CPU Operates with Low-Speed Clock

4.3.3.2 STOP Mode When CPU Operates with High-Speed Clock

When the CPU is operating with a high-speed clock and the STP bit of SBYCON is set to "1" with the stop code acceptor enabled, the STOP mode is entered and high-speed oscillation and low-speed oscillation stop.
When the NMI interrupt request or the interrupt-enabled (the interrupt enable flag is "1") P00 to P03 interrupt request is issued, the STP bit is set to "0" and the low-speed and high-speed oscillation restart.
When an interrupt request is issued, the STOP mode is released after the elapse of the high-speed oscillation start time (TXTH/TRC) and the high-speed clock (OSCLK) oscillation stabilization time (8192-pulse count), the mode is returned to the program run mode, and the high-speed clocks (OSCLK and HSCLK) restart supply to the peripheral circuits.
The low-speed clock (LSCLK) restarts supply to the peripheral circuits after the elapse of the low-speed oscillation start time (TXTL) and low-speed clock (LSCLK) oscillation settling time (8192 count).
For the high-speed oscillation start time (TXTH) and low-speed oscillation start time (TXTL), see the "Electrical Characteristics" Section in Appendix C.
Figure 4-4 shows the operation waveforms in STOP mode when CPU operates with the high-speed clock.

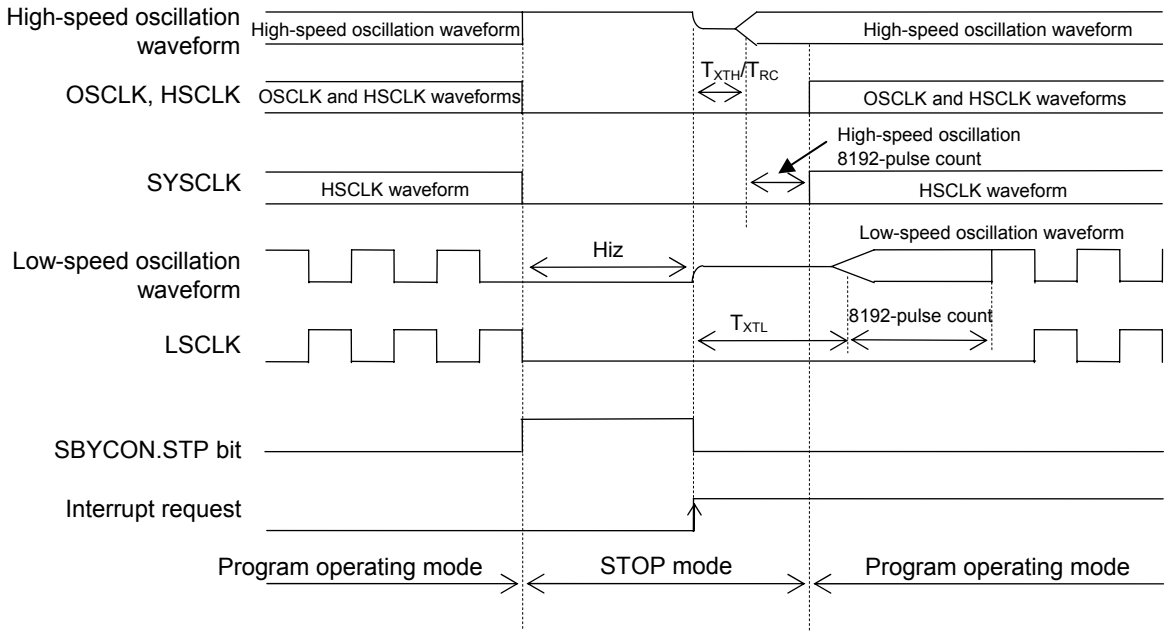


Figure 4-4 Operation Waveforms in STOP Mode When CPU Operates with High-Speed Clock

Note:
The STOP mode is entered two cycles after the instruction that sets the STP bit to "1" and up to two instructions are executed during the period between STOP mode release and a transition to interrupt processing. Therefore, place two NOP instructions next to the instruction that set the STP bit to "1".

4.3.3.3 Note on Return Operation from STOP/HALT Mode

The operation of returning from the STOP mode and HALT mode varies according to the interrupt level (ELEVEL) of the program status word (PSW), master interrupt enable flag (MIE), the contents of the interrupt enable register (IE0 to IE3), and whether the interrupt is a non-maskable interrupt or a maskable interrupt.
For details of PSW and the IE and IRQ registers, see "nX-U8/100 Core Instruction Manual" and Chapter 5, "Interrupt", respectively.

Table 4-1 and Table 4-2 show the return operations from STOP/HALT mode.

Table 4-1 Return Operation from STOP/HALT Mode (Non-Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT mode
*	*	–	0	Not returned from STOP/HALT mode.
3	*	–	1	After the mode is returned from STOP/HALT mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1". The program operation does not go to the interrupt routine.
0, 1, 2	*	–	1	After the mode is returned from the STOP/HALT mode, program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1", then goes to the interrupt routine.

Table 4-2 Return Operation from STOP/HALT Mode (Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT mode
*	*	*	0	Not returned from STOP/HALT mode.
*	*	0	1	
*	0	1	1	After the mode is returned from STOP/HALT mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1". The program operation does not go to the interrupt routine.
2,3	1	1	1	
0, 1	1	1	1	After the mode is returned from the STOP/HALT mode, program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1", then goes to the interrupt routine.

Notes:
- If the ELEVEL bit is 0H, it indicates that the CPU is performing neither nonmaskable interrupt processing nor maskable interrupt processing nor software interrupt processing.
- If the ELEVEL bit is 1H, it indicates that the CPU is performing maskable interrupt processing or software interrupt processing. (ELEVEL is set during interrupt transition cycle.)
- If the ELEVEL bit is 2H, it indicates that the CPU is performing non-maskable interrupt processing. (ELEVEL is set during interrupt transition cycle.)
- If the ELEVEL bit is 3H, it indicates that the CPU is performing interrupt processing specific to the emulator. This setting is not allowed in normal applications.

4.3.4 Block Control Function

This LSI has a block control function, which resets and completely turns operating circuits of unused peripherals off to make even more reducing current consumption.

When certain bits of block control registers are set to "1", corresponding peripherals are reset (all registers are reset) and operating clocks for the peripherals stop. Writing to every SFR (special function register) in the corresponding peripherals is not valid while the bits of block control registers are set to "1" and returns the initial value for read. Ensure the bits are reset to "0" before using the peripherals to enable the operation.

BLKCON0 register controls(disables/enables) operation of Timer 0, Timer 1, Timer 2 and Timer 3.
BLKCON1 register controls(disables/enables) operation of Capture, 1kHz Timer and PWM.
BLKCON2 register controls(disables/enables) operation of I2C, UART and SSIO.
BLKCON3 register controls(disables/enables) operation of Melody/Buzzer.
BLKCON4 register controls(disables/enables) operation of LCD driver, Battery Level Detector, 32kHz oscillation stop detector, RC type A/D converter and SAR type A/D converter.

Note:
DXTSP bit (bit 4) of BLKCON4 register disables the operation of 32kHz oscillation stop detector in HALT mode only.
See the each chapter for detail about the opeation of each peripheral and relevant notes.

Chapter 5

Interrupts (INTs)

5. Interrupts (INTs)

5.1 Overview

This LSI has 22 interrupt sources (External interrupts: 5 sources, Internal interrupts: 17 sources) and a software interrupt (SWI).
For details of each interrupt, see the following chapters:

Chapter 7, "Time Base Counter"
Chapter 9, "1 kHz Timer"
Chapter 10, "Timer"
Chapter 11, "PWM"
Chapter 12, "Watchdog Timer"
Chapter 13, "Synchronous Serial Port"
Chapter 14, "UART"
Chapter 15, "I^2C Bus Interface"
Chapter 16, "NMI"
Chapter 17, "Port0"
Chapter 18, "Port1"
Chapter 19, "Port2"
Chapter 20, "Port3"
Chapter 23, "Melody Driver"
Chapter 24, "RC Oscillation Type A/D Converter"
Chapter 25, "Successive Approximation Type A/D Converter"

5.1.1 Features

- 2 non-maskable interrupt sources (Internal source: 1, External source: 1)
- 20 maskable interrupt sources (Internal sources: 16, External sources: 4)
- Software interrupt (SWI): 64 sources max.
- External interrupts allow edge selection and sampling selection.

5.2 Description of Registers

5.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F011H	Interrupt enable register 1	IE1	—	R/W	8	00H
0F012H	Interrupt enable register 2	IE2	—	R/W	8	00H
0F013H	Interrupt enable register 3	IE3	—	R/W	8	00H
0F014H	Interrupt enable register 4	IE4	—	R/W	8	00H
0F015H	Interrupt enable register 5	IE5	—	R/W	8	00H
0F016H	Interrupt enable register 6	IE6	—	R/W	8	00H
0F017H	Interrupt enable register 7	IE7	—	R/W	8	00H
0F018H	Interrupt request register 0	IRQ0	—	R/W	8	00H
0F019H	Interrupt request register 1	IRQ1	—	R/W	8	00H
0F01AH	Interrupt request register 2	IRQ2	—	R/W	8	00H
0F01BH	Interrupt request register 3	IRQ3	—	R/W	8	00H
0F01CH	Interrupt request register 4	IRQ4	—	R/W	8	00H
0F01DH	Interrupt request register 5	IRQ5	—	R/W	8	00H
0F01EH	Interrupt request register 6	IRQ6	—	R/W	8	00H
0F01FH	Interrupt request register 7	IRQ7	—	R/W	8	00H

5.2.2 Interrupt Enable Register 1 (IE1)

Address: 0F011H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE1	—	—	—	—	EP03	EP02	EP01	EP00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE1 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE1 is not reset.

[Description of Bits]

- **EP00** (bit 0)
  EP00 is the enable flag for the input port P00 pin interrupt (P00INT).

EP00	Description
0	Disabled (initial value)
1	Enabled

- **EP01** (bit 1)
  EP01 is the enable flag for the input port P01 pin interrupt (P01INT).

EP01	Description
0	Disabled (initial value)
1	Enabled

- **EP02** (bit 2)
  EP02 is the enable flag for the input port P02 pin interrupt (P02INT).

EP02	Description
0	Disabled (initial value)
1	Enabled

- **EP03** (bit 3)
  EP03 is the enable flag for the input port P03 pin interrupt (P03INT).

EP03	Description
0	Disabled (initial value)
1	Enabled

5.2.3 Interrupt Enable Register 2 (IE2)

Address: 0F012H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE2	EI2C0	—	—	—	—	ESAD	—	ESIO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE2 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE2 is not reset.

[Description of Bits]

- **ESIO0** (bit 0)
  ESIO0 is the enable flag for the synchronous serial port 0 interrupt (SIO0INT).

ESIO0	Description
0	Disabled (initial value)
1	Enabled

- **ESAD** (bit 2)
  ESAD is the enable flag for the successive approximation type A/D converter interrupt (SADINT).

ESAD	Description
0	Disabled (initial value)
1	Enabled

- **EI2C0** (bit 7)
  EI2C0 is the enable flag for the I2C bus 0 interrupt (I2C0INT).

EI2C0	Description
0	Disabled (initial value)
1	Enabled

5.2.4 Interrupt Enable Register 3 (IE3)

Address: 0F013H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE3	—	—	—	—	—	—	ETM1	ETM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE3 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE3 is not reset.

[Description of Bits]

- **ETM0** (bit 0)
  ETM0 is the enable flag for the timer 0 interrupt (TM0INT).

ETM0	Description
0	Disabled (initial value)
1	Enabled

- **ETM1** (bit 1)
  ETM1 is the enable flag for the timer 1 interrupt (TM1INT).

ETM1	Description
0	Disabled (initial value)
1	Enabled

5.2.5 Interrupt Enable Register 4 (IE4)

Address: 0F014H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE4	—	—	ERAD	—	—	EMD0	—	EUA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE4 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE4 is not reset.

[Description of Bits]

- **EUA0** (bit 0)
  EUA0 is the enable flag for the UART0 interrupt (UA0INT).

EUA0	Description
0	Disabled (initial value)
1	Enabled

- **EMD0** (bit 2)
  EMD0 is the enable flag for the melody 0 interrupt (MD0INT).

EMD0	Description
0	Disabled (initial value)
1	Enabled

- **ERAD** (bit 5)
  ERAD is the enable flag for the RC oscillation type A/D converter interrupt (RADINT).

ERAD	Description
0	Disabled (initial value)
1	Enabled

5.2.6 Interrupt Enable Register 5 (IE5)

Address: 0F015H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE5	—	—	ETM3	ETM2	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE5 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE5 is not reset.

[Description of Bits]

- **ETM2** (bit 4)
  ETM2 the enable flag for the timer 2 interrupt (TM2INT).

ETM2	Description
0	Disabled (initial value)
1	Enabled

- **ETM3** (bit 5)
  ETM3 the enable flag for the timer 3 interrupt (TM3INT)

ETM3	Description
0	Disabled (initial value)
1	Enabled

5.2.7 Interrupt Enable Register 6 (IE6)

Address: 0F016H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE6	E32H	—	E128H	ET1K	—	—	—	EPW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE6 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE6 is not reset.

[Description of Bits]

- **EPW0** (bit 0)
  EPW0 is the enable flag for the PWM0 interrupt (PW0INT)

EPW0	Description
0	Disabled (initial value)
1	Enabled

- **ET1K** (bit 4)
  ET1K is the enable flag for the 1 kHz timer interrupt (T1KINT).

ET1K	Description
0	Disabled (initial value)
1	Enabled

- **E128H** (bit 5)
  E128H is the enable flag for the time base counter 128 Hz interrupt (T128HINT).

E128H	Description
0	Disabled (initial value)
1	Enabled

- **E32H** (bit 7)
  E32H is the enable flag for the time base counter 32 Hz interrupt (T32HINT).

E32H	Description
0	Disabled (initial value)
1	Enabled

5.2.8 Interrupt Enable Register 7 (IE7)

Address: 0F017H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE7	—	—	—	—	E2H	—	—	E16H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE7 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE7 is not reset.

[Description of Bits]

- **E16H** (bit 0)
  E16H is the enable flag for the time base counter 16 Hz interrupt (T16HINT).

E16H	Description
0	Disabled (initial value)
1	Enabled

- **E2H** (bit 3)
  E2H is the enable flag for the time base counter 2 Hz interrupt (T2HINT).

E2H	Description
0	Disabled (initial value)
1	Enabled

5.2.9 Interrupt Request Register 0 (IRQ0)

Address: 0F018H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ0	—	—	—	—	—	—	QNMI	QWDT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ0 is a special function register (SFR) to request an interrupt for each interrupt source.
The watchdog timer interrupt (WDTINT) and the NMI interrupt (NMINT) are non-maskable interrupts that do not depend on MIE. In this case, an interrupt is requested to the CPU regardless of the value of the Mask Interrupt Enable flag (MIE).
Each IRQ0 request flag is set to "1" regardless of the MIE value when an interrupt is generated. By setting the IRQ0 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ0 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QWDT** (bit 0)
  QWDT is the request flag for the watchdog timer interrupt (WDTINT).

QWDT	Description
0	No request (initial value)
1	Request

- **QNMI** (bit 1)
  QNMI is the request flag for the NMI interrupt (NMINT).

QNMI	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ0), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.10 Interrupt Request Register 1 (IRQ1)

Address: 0F019H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ1	—	—	—	—	QP03	QP02	QP01	QP00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ1 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ1 request flag is set to "1" regardless of the IE1 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE1) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ1 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ1 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QP00** (bit 0)
  QP00 is the request flag for the input port P00 pin interrupt (P00INT).

QP00	Description
0	No request (initial value)
1	Request

- **QP01** (bit 1)
  QP01 is the request flag for the input port P01 pin interrupt (P01INT).

QP01	Description
0	No request (initial value)
1	Request

- **QP02** (bit 2)
  QP02 is the request flag for the input port P02 pin interrupt (P02INT).

QP02	Description
0	No request (initial value)
1	Request

- **QP03** (bit 3)
  QP03 is the request flag for the input port P03 pin interrupt (P03INT).

QP03	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ1) or to the interrupt enable register (IE1), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.11 Interrupt Request Register 2 (IRQ2)

Address: 0F01AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ2	QI2C0	—	—	—	—	QSAD	—	QSIO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ2 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ2 request flag is set to "1" regardless of the IE2 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE2) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ2 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ2 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QSIO0** (bit 0)
  QSIO0 is the request flag for the synchronous serial port 0 interrupt (SIO0INT).

QSIO0	Description
0	No request (initial value)
1	Request

- **QSAD** (bit 2)
  QSAD is the request flag for the successive approximation type A/D converter interrupt (SADINT)

QSAD	Description
0	No request (initial value)
1	Request

- **QI2C0** (bit 7)
  QI2C0 is the request flag for the I2C bus 0 interrupt (I2C0INT).

QI2C0	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ2) or to the interrupt enable register (IE2), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.12 Interrupt Request Register 3 (IRQ3)

Address: 0F01BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ3	—	—	—	—	—	—	QTM1	QTM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ3 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ3 request flag is set to "1" regardless of the IE3 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE3) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ3 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ3 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QTM0** (bit 0)
  QTM0 is the request flag for the timer 0 interrupt (TM0INT).

QTM0	Description
0	No request (initial value)
1	Request

- **QTM1** (bit 1)
  QTM1 is the request flag for the timer 1 interrupt (TM1INT).

QTM1	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ3) or to the interrupt enable register (IE3), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.13 Interrupt Request Register 4 (IRQ4)

Address: 0F01CH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ4	—	—	QRAD	—	—	QMD0	—	QUA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ4 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ4 request flag is set to "1" regardless of the IE4 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE4) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ4 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ4 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QUA0** (bit 0)
  QUA0 is the request flag for the UART0 interrupt (UA0INT).

QUA0	Description
0	No request (initial value)
1	Request

- **QMD0** (bit 2)
  QMD0 is the request flag for the melody 0 interrupt (MD0INT).

QMD0	Description
0	No request (initial value)
1	Request

- **QRAD** (bit 5)
  QRAD is the request flag for the RC oscillation type A/D converter interrupt (RADINT).

QRAD	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ4) or to the interrupt enable register (IE4), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.14 Interrupt Request Register 5 (IRQ5)

Address: 0F01DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ5	—	QTM3	QTM2	—	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ5 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ5 request flag is set to "1" regardless of the IE5 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE5) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ5 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ5 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QTM2** (bit 5)
  QTM2 is the request flag for the timer 2 interrupt (TM2INT).

QTM2	Description
0	No request (initial value)
1	Request

- **QTM3** (bit 6)
  QTM3 is the request flag for the timer 3 interrupt (TM3INT).

QTM3	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ5) or to the interrupt enable register (IE5), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.15 Interrupt Request Register 6 (IRQ6)

Address: 0F01EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ6	Q32H	—	Q128H	QT1K	—	—	—	QPW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ6 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ6 request flag is set to "1" regardless of the IE6 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE6) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ6 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ6 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QPW0** (bit 0)
  QPW0 is the request flag for the PWM0 interrupt (PW0INT).

QPW0	Description
0	No request (initial value)
1	Request

- **QT1K** (bit 4)
  QT1K is the request flag for the 1 kHz timer interrupt (T1KINT).

QT1K	Description
0	No request (initial value)
1	Request

- **Q128H** (bit 5)
  Q128H is the request flag for the time base counter 128 Hz interrupt (T128HINT).

Q128H	Description
0	No request (initial value)
1	Request

- **Q32H** (bit 7)
  Q32H is the request flag for the time base counter 32 Hz interrupt (T32HINT).

Q32H	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ6) or to the interrupt enable register (IE6), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.16 Interrupt Request Register 7 (IRQ7)

Address: 0F01FH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ7	—	—	—	—	Q2H	—	—	Q16H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ7 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ7 request flag is set to "1" regardless of the IE7 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE7) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ7 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ7 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **Q16H** (bit 0)
  Q16H is the request flag for the time base counter 8 Hz interrupt (T8HINT).

Q16H	Description
0	No request (initial value)
1	Request

- **Q2H** (bit 3)
  Q2H is the request flag for the time base counter 2 Hz interrupt (T2HINT).

Q2H	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the instruction to write to the interrupt request register (IRQ7) or to the interrupt enable register (IE7), the the interrupt shift cycle starts after the next 1 instruction is executed.

5.3 Description of Operation

With the exception of the watchdog timer interrupt (WDTINT) and the NMI interrupt (NMINT), interrupt enable/disable for 20 sources is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE1 to 7). WDTINT and NMIINT are non-maskable interrupts.
When the interrupt conditions are satisfied, the CPU calls a branching destination address from the vector table determined for each interrupt source and the interrupt shift cycle starts to branch to the interrupt processing routine.
Table 5-1 lists the interrupt sources.

Table 5-1 Interrupt Sources

Priority	Interrupt source	Symbol	Vector table address
1	Watchdog timer interrupt	WDTINT	0008H
2	NMI interrupt	NMINT	000AH
3	P00 interrupt	P00INT	0010H
4	P01 interrupt	P01INT	0012H
5	P02 interrupt	P02INT	0014H
6	P03 interrupt	P03INT	0016H
7	Synchronous serial port 0 interrupt	SIO0INT	0020H
8	Successive approximation type A/D converter interrupt	SADINT	0024H
9	I^2C bus 0 interrupt	I2C0INT	002EH
10	Timer 0 interrupt	TM0INT	0030H
11	Timer 1 interrupt	TM1INT	0032H
12	UART 0 interrupt	UA0INT	0040H
13	Melody 0 interrupt	MD0INT	0044H
14	RC oscillation type A/D converter interrupt	RADINT	004AH
15	Timer 2 interrupt	TM2INT	0058H
16	Timer 3 interrupt	TM3INT	005AH
17	PWM0 interrupt	PW0INT	0060H
18	1 kHz timer interrupt	T1KINT	0068H
19	TBC128Hz interrupt	T128HINT	006AH
20	TBC32Hz interrupt	T32HINT	006EH
21	TBC16Hz interrupt	T16HINT	0070H
22	TBC2Hz interrupt	T2HINT	0076H

Note:
- When multiple interrupts are generated concurrently, the interrupts are serviced according to this priority and processing of low-priority interrupts is pending.
- Please define vector tables for all unused interrupts for fail safe.

5.3.1 Maskable Interrupt Processing

When an interrupt is generated with the MIE flag set to "1", the following processing is executed by hardware and the processing of program shifts to the interrupt destination.

(1) Transfer the program counter (PC) to ELR1.
(2) Transfer CSR to ECSR1.
(3) Transfer PSW toEPSW1.
(4) Set the MIE flag to "0".
(5) Set the ELEVEL field to"1".
(6) Load the interrupt start address into PC.

5.3.2 Non-Maskable Interrupt Processing

When an interrupt is generated regardless of the state of MIE flag, the following processing is performed by hardware and the processing of program shifts to the interrupt destination.

(1) Transfer PC to ELR2.
(2) Transfer CSR to ECSR2.
(3) Transfer PSW to EPSW2.
(4) Set the ELEVEL field to "2".
(5) Load the interrupt start address into PC.

5.3.3 Software Interrupt Processing

A software interrupt is generated as required within an application program. When the SWI instruction is performed within the program, a software interrupt is generated, the following processing is performed by hardware, and the processing program shifts to the interrupt destination. The vector table is specified by the SWI instruction.

(1) Transfer PC to ELR1.
(2) Transfer CSR to ECSR1.
(3) Transfer PSW to EPSW1.
(4) Set the MIE flag to "0".
(5) Set the ELEVEL field to "1".
(6) Load the interrupt start address into PC.

Reference:
For the MIE flag, Program Counter (PC), CSR, PSW, and ELEVEL, see "nX-U8/100 Core Instruction Manual".

5.3.4 Notes on Interrupt Routine

Notes are different in programming depending on whether a subroutine is called or not by the program in executing an interrupt routine, whether multiple interrupts are enabled or disabled, and whether such interrupts are maskable or non-maskable.

State A: Maskable interrupt is being processed

A-1: When a subroutine is not called by the program in executing an interrupt routine

A-1-1: When multiple interrupts are disabled

- Processing immediately after the start of interrupt routine execution
  No specific notes.
- Processing at the end of interrupt routine execution
  Specify the RTI instruction to return the contents of the ELR register to the PC and those of the EPSW register to PSW.

A-1-2: When multiple interrupts are enabled

- Processing immediately after the start of interrupt routine execution
  Specify "PUSH ELR, EPSW" to save the interrupt return address and the PSW status in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP PC, PSW" instead of the RTI instruction to return the contents of the stack to PC and PSW.

Example of description: State A-1-1

```
Intrpt_A-1-1:          ; A-1-1 state
   DI                  ; Disable interrupt
    :
    :
    :
   RTI                 ; Return PC from ELR
                       ; Return PSW form EPSW
                       ; End
```

Example of description: State A-1-2

```
Intrpt_A-1-2:          ; Start
   PUSH ELR, EPSW      ; Save ELR and EPSW at the
                         beginning
   EI                  ; Enable interrupt
    :
    :
    :
    :
    :
   POP PC, PSW         ; Return PC from the stack
                       ; Return PSW from the stack
                       ; End
```

A-2: When a subroutine is called by the program in executing an interrupt routine

A-2-1: When multiple interrupts are disabled

- Processing immediately after the start of interrupt routine execution
  Specify the "PUSH LR" instruction to save the subroutine return address in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP LR" immediately before the RTI instruction to return from the interrupt processing after returning the subroutine return address to LR.

A-2-2: When multiple interrupts are enabled

- Processing immediately after the start of interrupt routine execution
  Specify "PUSH LR, ELR, EPSW" to save the interrupt return address, the subroutine return address, and the EPSW status in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP PC, PSW, LR" instead of the RTI instruction to return the saved data of the interrupt return address to PC, the saved data of EPSW to PSW, and the saved data of LR to LR.

Example of description: A-2-2

```
Intrpt_A-2-2:           ; Start
   PUSH ELR, EPSW,      ; Save ELR, EPSW, LR at
   LR                     the beginning

   EI                   ; Enable interrupt
    :
    :
    :
   BL Sub_1             ; Call subroutine Sub_1
    :
   POP PC, PSW, LR      ; Return PC from the stack
                        ; Return PSW from the stack
                        ; Return LR from the stack
                        ; End

Sub_1:                  ;
DI                      ; Disable interrupt
                            :
                            :
                            :
RT                      ; Return PC from LR
                        ; End of subroutine
```

State B: Non-maskable interrupt is being processed

B-1: When no instruction is executed in an interrupt routine
- Processing immediately after the start of interrupt routine execution
  Specify the RTI instruction to return the contents of the ELR register to the PC and those of the EPSW register to PSW.

B-2: When one or more instructions are executed in an interrupt routine

B-2-1: When a subroutine is not called by the program in executing an interrupt routine
- Processing immediately after the start of interrupt routine execution
  Specify "PUSH ELR, EPSW" to save the interrupt return address and the PSW status in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP PC, PSW" instead of the RTI instruction to return the contents of the stack to PC and PSW.

B-2-2: When a subroutine is called by the program in executing an interrupt routine
- Processing immediately after the start of interrupt routine execution
  Specify "PUSH LR, ELR, EPSW" to save the interrupt return address, the subroutine return address, and the EPSW status in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP PC, PSW, LR" instead of the RTI instruction to return the saved data of the interrupt return address to PC, the saved data of EPSW to PSW, and the saved data of LR to LR.

Example of description: B-1

```
Intrpt_B-1:          ; B-1 state
  RTI                ; Return PC from ELR
                     ; Return PSW form EPSW
                     ; End
```

Example of description: B-2-1

```
Intrpt_B-2-1:        ; Start
  PUSH  ELR, EPSW    ; Save ELR, EPSW at the
                       beginning
  :
  :
  :
  POP   PC, PSW      ; Return PC from the stack
                     ; Return PSW from the stack
                     ; End
```

Example of description: B-2-2

```
Intrpt_B-2-2:        ; Start
  PUSH  ELR,EPSW,LR  ; Save ELR, EPSW, LR at the
                       beginning
  :
  :
  :
  BL Sub_1           ; Call subroutine Sub_1
  :
  POP   PC, PSW, LR  ; Return PC from the stack
                     ; Return PSW from the stack
                     ; Return LR from the stack
                     ; End
```

```
Sub_1:               ;
  :
  :
  :
  :
  RT                 ; Return PC from LR
                     ; End of subroutine
```

5.3.5 Interrupt Disable State

Even if the interrupt conditions are satisfied, an interrupt may not be accepted depending on the operating state. This is called an interrupt disabled state. See below for the interrupt disabled state and the handling of interrupts in this state.

Interrupt disabled state 1: Between the interrupt shift cycle and the instruction at the beginning of the interrupt routine

When the interrupt conditions are satisfied in this section, an interrupt is generated immediately following the execution of the instruction at the beginning of the interrupt routine corresponding to the interrupt that has already been enabled.

Interrupt disabled state 2: Between the DSR prefix instruction and the next instruction

When the interrupt conditions are satisfied in this section, an interrupt is generated immediately after execution of the instruction following the DSR prefix instruction.

Reference:
For the DSR prefix instruction, see "nX-U8/100 Core Instruction Manual".

Chapter 6

Clock Generation Circuit

6. Clock Generation Circuit

6.1 Overview

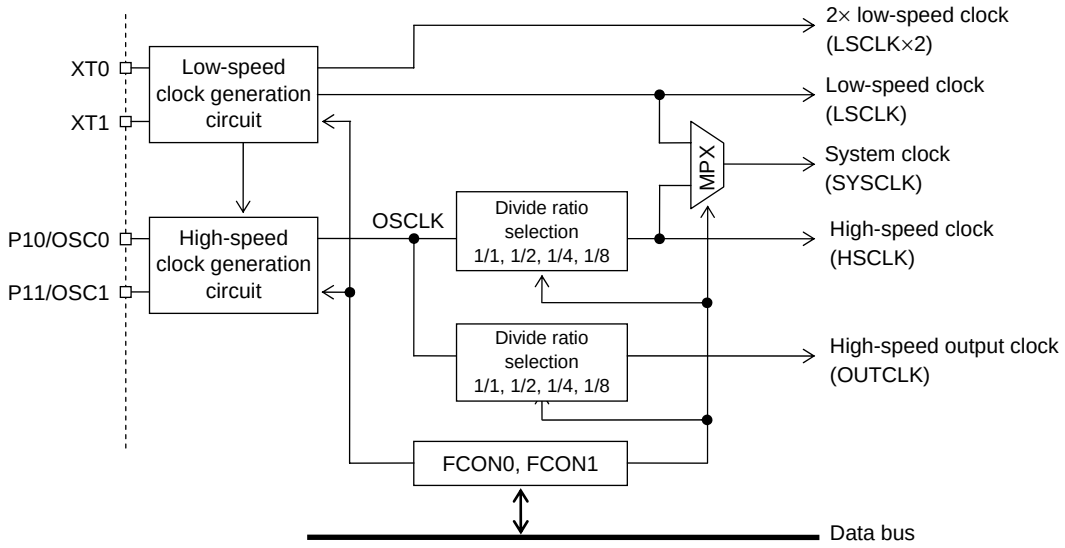
The clock generation circuit generates and provides a low-speed clock (LSCLK), 2× low-speed clock (LSCLK2), a high-speed clock (HSCLK), a system clock (SYSCLK), and a high-speed output clock (OUTCLK). LSCLK, LSCLK×2, and HSCLK are time base clocks for the peripheral circuits, SYSCLK is a basic operation clock of CPU, and OUTCLK is a clock that is output from a port.
For the OUTCLK output port, see Chapter 19, "Port 2".
Additionally, for the STOP mode described in this chapter, see Chapter 4, "MCU Control Function", and for BLD, see Chapter 27, "Battery Level Detection Circuit".

6.1.1 Features

- Low-speed clock: 32.768 kHz crystal oscillation mode
  – Capable of generating LSCLK × 2 (64 kHz) to be used for some peripherals.
- High-speed clock: Software selection
  – 500 kHz RC oscillation mode
  – Crytal/ceramic oscillation mode
  – Built-in PLL oscillation mode
  – External clock input mode

6.1.2 Configuration

Figure 6-1 shows the configuration of the clock generation circuit.



FCON0 : Frequency control register 0
FCON1 : Frequency control register 1

Figure 6-1 Configuration of Clock Generation Circuit

Note:
This LSI starts operation with a clock generated by dividing the 500 kHz RC oscillation frequency by 8 after power-on or a system reset. At initialization by software, set the FCON0 or FCON1 register to switch the clock to a required one. Operation of this LSI is not guaranteed under a condition where a low-speed clock is not supplied.

6.1.3 List of Pins

Pin name	I/O	Description
XT0	I	Pin for connecting a crystal for low-speed clock
XT1	O	Pin for connecting a crystal for low-speed clock
P10/OSC0	I	Pin for connecting a crystal/ceramic resonator for high-speed clock Used for the secondary function of the P10 pin
P11/OSC1	O	Pin for connecting a crystal/ceramic resonator for high-speed clock Used for the secondary function of the P11 pin

6.2 Description of Registers

6.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F002H	Frequency control register 0	FCON0	FCON	R/W	8/16	33H
0F003H	Frequency control register 1	FCON1		R/W	8	03H

6.2.2 Frequency Control Register 0 (FCON0)

Address: 0F002H
Access: R/W
Access size: 8/16 bits
Initial value: 33H

	7	6	5	4	3	2	1	0
FCON0	—	—	OUTC1	OUTC0	OSCM1	OSCM0	SYSC1	SYSC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	1	1	0	0	1	1

FCON0 is a special function register (SFR) to control the high-speed clock generation circuit and to select system clock.

[Description of Bits]

- **SYSC1, SYSC0** (bits 1, 0)

  The SYSC1 and SYSC0 bits are used to select the frequency of the high-speed clock (HSCLK) used for system clock and periphera1 circuits (including high-speed time base counter). OSCLK, 1/2OSCLK, 1/4OSCLK, or 1/8OSCLK can be selected. The maximum operating frequency guaranteed for the system clock (SYSCLK) of this LSI is 4.2 MHz.

  At system reset, 1/8OSCLK is selected.

SYSC1	SYSC0	Description
0	0	OSCLK (1/2OSCLK in built-in PLL oscillation mode)
0	1	1/2OSCLK
1	0	1/4OSCLK
1	1	1/8OSCLK (initial value)

- **OSCM1, OSCM0** (bits 3, 2)

  The OSCM1 and OSCM0 bits are used to select the mode of the high-speed clock generation circuit. RC oscillation mode, crystal/ceramic oscillation mode, PLL oscillation mode, or external clock input mode can be selected.

  The setting of OSCM1 and OSCM0 can be changed only when high-speed oscillation is being stopped (ENOSC bit of FCON1 is "0"). At system reset, RC oscillation mode is selected.

– When switching the high-speed oscillation mode, please first switch back to low speed clock before switching to other high-speed clock (set the ENOSC bit and SYSCLK bit of FCON1 to "0").

OSCM1	OSCM0	Description
0	0	RC oscillation mode (initial value)
0	1	Crystal/ceramic oscillation mode
1	0	Built-in PLL oscillation mode
1	1	External clock input mode

- **OUTC1, OUTC0** (bits 5, 4)

  The OUTC1 and OUTC0 bits are used to select the frequency of the high-speed output clock which is output when the secondary function of the port is used.

  OSCLK, 1/2OSCLK, 1/4OSCLK, or 1/8OSCLK can be selected.

  At system reset, 1/8OSCLK is selected.

OUTC1	OUTC0	Description
0	0	OSCLK
0	1	1/2OSCLK
1	0	1/4OSCLK
1	1	1/8OSCLK (initial value)

Note:

- To switch the mode of the high-speed clock generation circuit using the OSCM1 and OSCM0 bits, stop the high-speed oscillation and set the system clock to the low-speed clock (set the ENOSC bit and SYSCLK of FCON1 to "0").
- The oscillators that are connected to the P10/OSC0 and P11/OSC1 pins must not exceed 4.2 MHz. In external clock mode, input a clock that does not exceed 4.2 MHz. When a built-in PLL oscillation mode is selected (OSCM1 = "1", OSCM0 = "0"), 1/2OSCLK (about 4.096 MHz) is output as HSCLK even if OSCLK (SYSC0 = "0", SYSC1 = "1") is selected.
- When built-in PLL (about 8.192 MHz) oscillation mode is selected (OSCM1 = "1", OSCM0 = "0"), 1/2OSCLK (about 4.096 MHz) is output as HSCLK even if OSCLK (SYSC0 = "0", SYSC1 = "1") is selected.

6.2.3 Frequency Control Register 1 (FCON1)

Address: 0F003H
Access: R/W
Access size: 8 bits
Initial value: 03H

	7	6	5	4	3	2	1	0
FCON1	LPLL	—	—	—	—	ENMLT	ENOSC	SYSCLK
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	1	1

FCON1 is a special function register (SFR) to control the high-speed clock generation circuit and to select system clock.

[Description of Bits]

- **SYSCLK** (bit 0)
  The SYSCLK bit is used to select system clock. It allows selection of the low-speed clock (LSCLK) or HSCLK (1/nOSCLK: n = 1, 2, 4, 8) selected by using the high-speed clock frequency select bit (SYSC1, 0) of FCON0.
  When the oscillation of high-speed clock is stopped (ENOSC bit = "0"), the SYSCLK bit is fixed to "0" and the low-speed clock (LSCLK) is selected for system clock.

SYSCLK	Description
0	LSCLK
1	HSCLK (initial value)

- **ENOSC** (bit 1)
  The ENOSC bit is used to select enable/disable of the oscillation of the high-speed clock oscillator.

ENOSC	Description
0	Disables high-speed oscillation
1	Enables high-speed oscillation (initial value)

- **ENMLT** (bit 2)
  The ENMLT bit is used to select enable/disable of the operation of the 2× low-speed clock (LSCLK×2).

ENMLT	Description
0	Disables 2× low-speed clock operation (initial value)
1	Enables 2× low-speed clock operation

- **LPLL** (bit 7)
  The LPLL bit is used as a flag to indicate the oscillation state of PLL oscillation.
  When the LPLL bit is set to "1", this indicates that the PLL oscillation frequency is locked within 8.192 MHz±2.5%.
  When the LPLL bit is set to "0", this indicates that the PLL oscillation is inactive or the PLL oscillation frequency is not within 8.192 MHz±2.5%.
  LPLL is a read-only bit.

LPLL	Description
0	Disables the use of PLL oscillation (initial value)
1	Enables the use of PLL oscillation

6.3 Description of Operation

6.3.1 Low-Speed Clock

6.3.1.1 Low-Speed Clock Generation Circuit

Figure 6-2 shows the configuration of the low-speed clock generation circuit.
A low-speed clock generation circuit is provided with an external 32.768 kHz crystal. To match the oscillation frequency by using a trimmer capacitor, connect external capacitors (C_{GL} and C_{DL}) as required.
In STOP mode, V_{DDX} is powered off to stop low-speed oscillation, and the XT0 and XT1 pins become Hiz (Hi Impedance state).
When the ENMLT bit of FCON1 is set to "1", the 2× low-speed clock circuit starts to generate the LSCLK×2(64kHz)

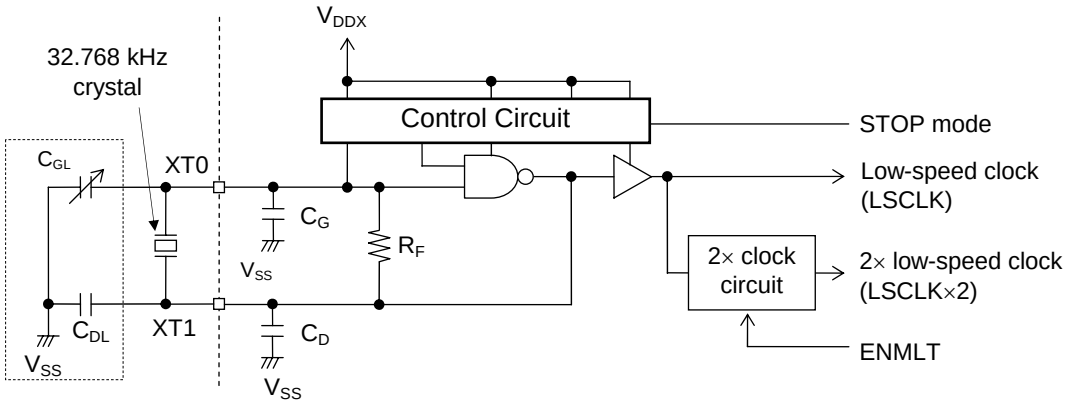


Figure 6-2 Circuit Configuration of 32.768 kHz Crystal Oscillation Mode

Notes:
- Install a crystal as close to the LSI as possible and make sure that signals causing noise and power supply wiring are not near the crystal and its wiring.
- Note that oscillation may stop due to condensation.

6.3.1.2 Operation of Low-Speed Clock Generation Circuit

The low-speed clock generation circuit is activated by the occurrence of power ON reset.
A low-speed clock (LSCLK) is supplied to the peripheral circuits after the elapse of the low-speed oscillation start period (T_{XTL}) and oscillation stabilization period (8192 counts) after powered on.
The low-speed clock generation circuit stops the oscillation in STOP mode. When oscillation is resumed by releasing of the STOP mode by external interrupt, LSCLK is supplied to the peripheral circuits after the elapse of the low-speed oscillation start period (T_{XTL}) and low-speed clock (LSCLK) oscillation stabilization period. For STOP mode, see Chapter 4, "MCU Control Function".
Figure 6-3 shows the waveforms of the low-speed clock generation circuit. For the low-speed oscillation start time (T_{XTL}), see Appendix C, "Electrical Characteristics".

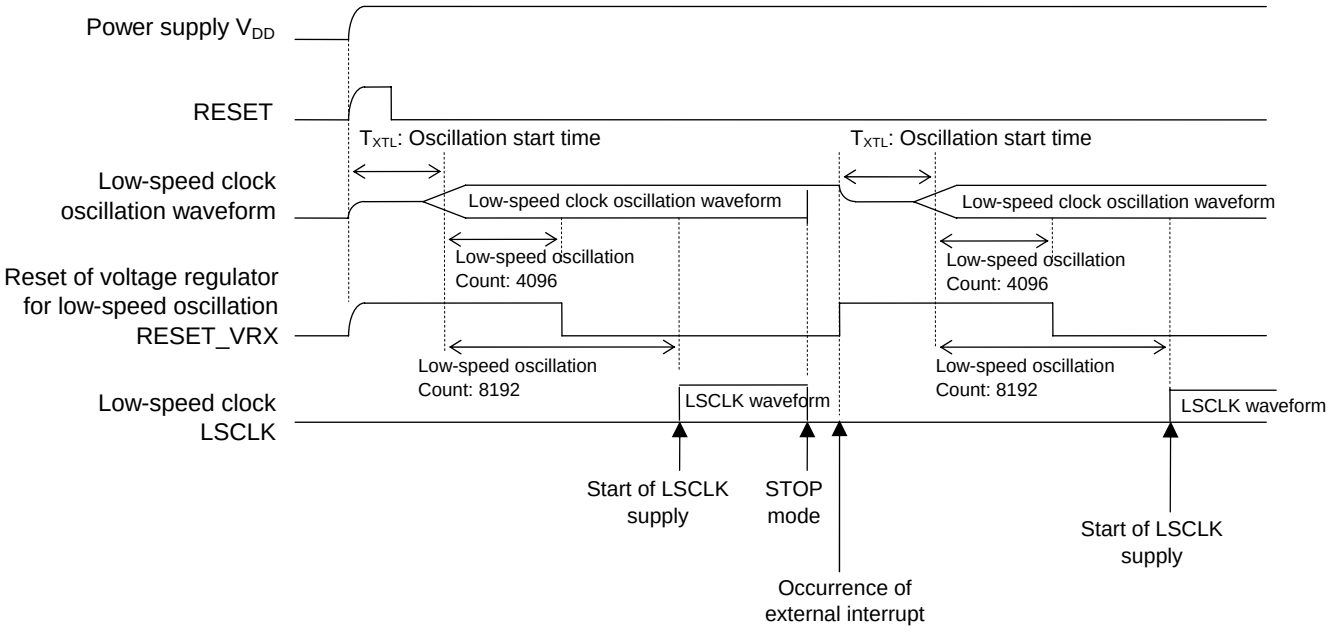


Figure 6-3 Operation of Low-Speed Clock Generation Circuit

Note:
After the power supply is turned on, CPU starts operation with a high-speed clock (500 kHz RC oscillation). It is recommended to switch to the low-speed clock after confirming that the low-speed clock is oscillating by checking that the 128 Hz interrupt request bit (Q128H) of the low-speed time base counter is "1". If the clock is switched before the low-speed clock oscillates, the CPU stops operation until oscillation of the low-speed clock starts.

6.3.2 High-Speed Clock

Setting of the OSCM1 and OSCM0 bits of the frequency control register 0 (FCON0) allows selection of the 500 kHz RC oscillation mode, crysta/ceramic oscillation mode, built-in PLL (Phase Locked Loop) oscillation mode, or external clock input mode for the high-speed clock generation circuit.

6.3.2.1 500 kHz RC Oscillation

In RC oscillation mode (OSCM0 = "0", OSCM1 = "0"), supply of OSCLK (high-speed oscillation clock) is started when RC oscillation clock pulse count reaches 128 after oscillation is enabled (ENOSC is set to "1").
In 500 kHz RC oscillation mode, both the P10/OSC0 pin and the P11/OSC1 pin can be used as general-purpose input ports.
Figure 6-4 shows the circuit configuration in RC oscillation mode.

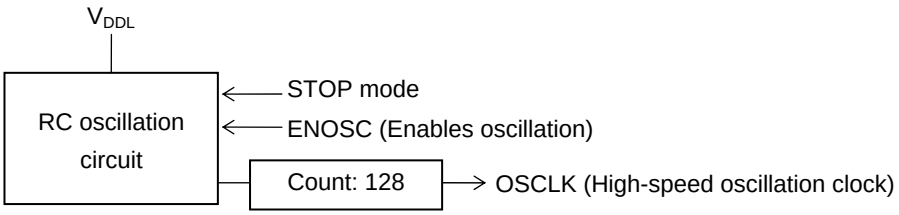


Figure 6-4 Circuit Configuration in RC Oscillation Mode

Notes:
- The RC oscillation mode is allowed within the range of V_{DD} = 1.3 V to 3.6 V.
- After system reset mode is released, supply of OSCLK starts after the RC oscillation clock pulse count reaches 8192. After release of a STOP mode, supply of OSCLK starts.

6.3.2.2 Crystal/Ceramic Oscillation Mode

In crystal/ceramic oscillation mode, both the P10/OSC0 pin and the P11/OSC1 pin are used for crystal ceramic oscillation.
In crystal/ceramic oscillation mode, a crystal or a ceramic resonator is externally connected to the P10/OSC0 and P11/OSC1 pins. If the high-speed oscillation clock pulse count reaches 4096 after oscillation enable, the clock is output to OSCLK (high-speed oscillation clock).
Figure 6-5 shows the circuit configuration in crystal/ceramic oscillation mode.

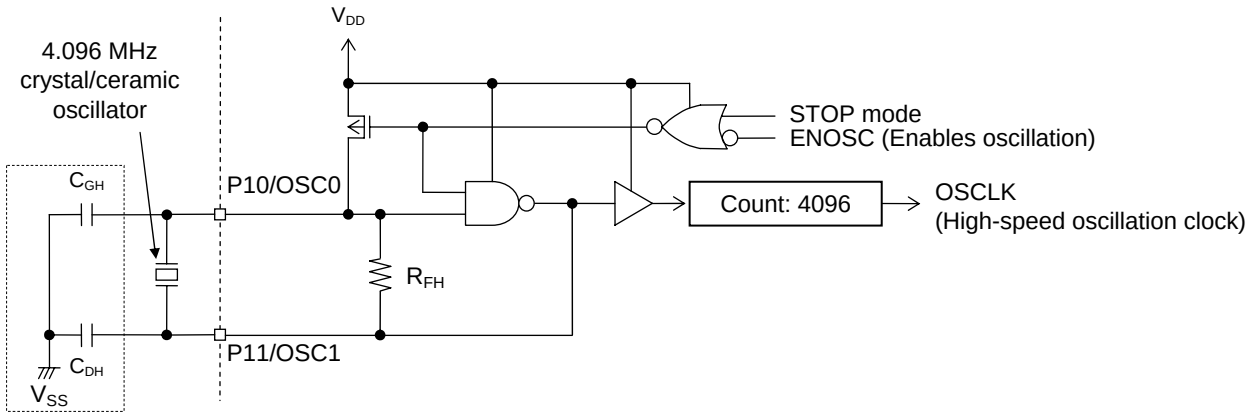


Figure 6-5 Circuit Configuration in Crystal/Ceramic Oscillation Mode

Notes:
- The crystal/ceramic oscillation mode can be used within a V_{DD} range of 1.8 V to 3.6 V. Select a frequency according to the operating voltage range by using the power supply voltage detection circuit (BLD). See Chapter 27, "Battery Level Detection Circuit" for details of BLD.
- Install a crystal or a ceramic resonator as close to the LSI as possible and make sure that signals causing noise and power supply wiring are not near the crystal or the ceramic resonator and their wiring.
- Note that oscillation may stop due to condensation.
- The crystal or the ceramic resonator connected to the P10/OSC0 and P11/OSC1 pins should not exceed the guaranteed maximum operation frequency of 4.2 MHz of the system clock (SYSCLK) of this LSI.

6.3.2.3 Built-in PLL Oscillation Mode

The PLL oscillation circuit generates a clock of 8.192 MHz (= 32.768 kHz × 250) ±2.5%. When the PLL oscillation clock (OSCLK) reaches within 8.192 MHz±2.5%, the LPLL flag of FCON1 is set.
In built-in PLL oscillation mode (OSCM0 = "0", OSCM1 = "1"), supply of OSCLK (high-speed oscillation clock) is started when PLL oscillation clock pulse count reaches 4096 after oscillation is enabled (ENOSC is set to "1").
In PLL oscillation mode, both the P10/OSC0 pin and the P11/OSC1 pin can be used as general-purpose input ports.
Figure 6-6 shows the circuit configuration in PLL oscillation mode.

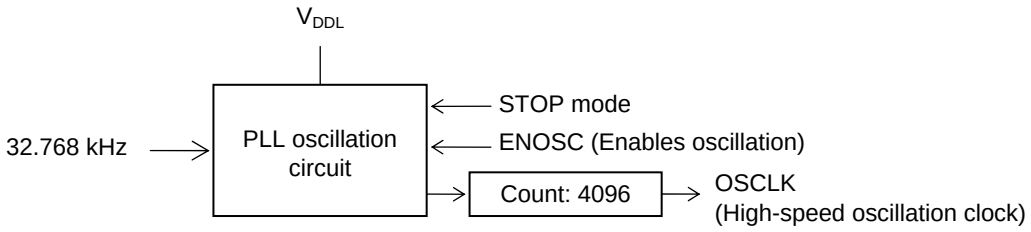


Figure 6-6 Circuit Configuration in PLL Oscillation Mode

Note:
The PLL oscillation mode can be used within a V_{DD} range of 1.8 V to 3.6 V. Select a frequency according to the operating voltage range by using the power supply voltage detection circuit (BLD).
When OSCLK is selected through SYSC1 or SYSC0 of FCON0 in PLL oscillation mode, about 4.096MHz, which is the same as 1/2OSCLK, is selected.
To use a PLL oscillation mode, a frequency of low-speed crystal oscillation 32.768kHz is necessary. The frequency of 32.768kHz is not adjusted by the frequency adjustment circuit of the time base counter.

6.3.2.4 External Clock Input Mode

In external clock input mode, external clock is input from the P10/OSC0 pin. The P11/OSC1 pin can be used as a general-purpose input port.
Figure 6-7 shows the circuit configuration in external clock input mode.

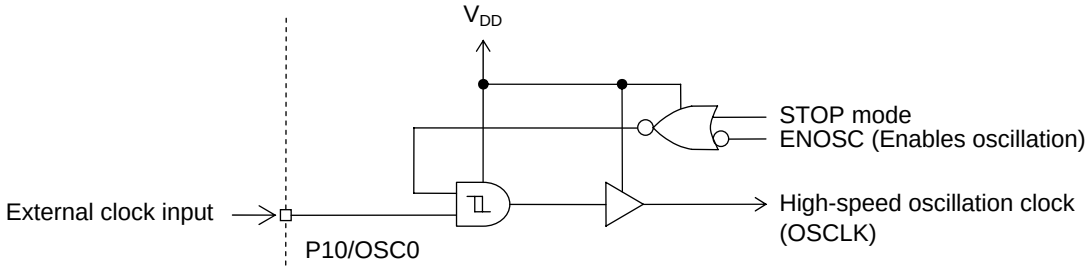


Figure 6-7 Circuit Configuration in External Clock Input Mode

Notes:
- The external clock input mode can be used within a V_{DD} range of 1.8 V to 3.6 V. Select a frequency according to the operation voltage range by using the power supply voltage detection circuit (BLD).
- Since the diodes are included between the P10/OSC0 pin and V_{DD} and between the P10/OSC0 pin and V_{SS}, do not apply voltages higher than V_{DD} and lower than V_{SS} to the P10/OSC0 pin.
- If the P10/OSC0 pin is left open in external clock input mode, excessive current can flow. Therefore, make sure that the "H" level (V_{DD}) or the "L" level (V_{SS}) is input.
- The clock that is input should not exceed the guaranteed maximum operating frequency 4.2 MHz of the system clock (SYSCLK) of this LSI.

6.3.2.5 Operation of High-Speed Clock Generation Circuit

The high-speed clock generation circuit is activated in 500Hz RC oscillation mode by power-on reset generation.
As a result of the occurrence of power-on reset, the circuit goes into system reset mode and then shifts to program operating mode after the elapse of the high-speed RC oscillation start time (T_{RC}) and the oscillation stabilization time (Count: 8192) of the high-speed oscillation clock (OSCLK) and at the same time, a high-speed clock (HSCLK) is supplied to the peripheral circuits.
Figure 6-8 shows the waveforms of the high-speed clock generation circuit at power on. For the high-speed RC oscillation start time (T_{RC}), see Appendix C, "Electrical Characteristics".

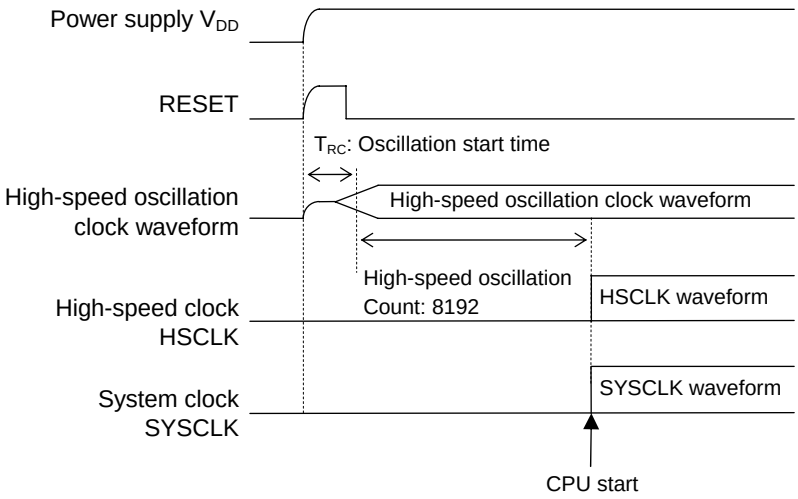


Figure 6-8 Operation of High-Speed Clock Generation Circuit at Power-On

The high-speed clock generation circuit allows selection of an oscillation mode and start/stop of oscillation by using the frequency control registers 0 and 1 (FCON0 and FCON1).
Oscillation can be started by setting the ENOSC bit to "1" after selecting a high-speed oscillation mode in FCON0 and a high-speed oscillation frequency. After the start of oscillation, HSCLK starts supply of a clock to the peripheral circuits following the elapse of the high-speed oscillation start period ($T_{RC}/T_{XTH}/T_{PLL}$) in each mode and the oscillation stabilization period of the high-speed oscillation clock (OSCLK).
The high-speed clock generation circuit stops oscillation when it shifts to a STOP mode by the software. When the STOP mode is released by external interrupt, HSCLK supplies clocks to peripheral circuits following the elapse of the high-speed oscillation start period ($T_{RC}/T_{XTH}/T_{PLL}$) in each mode and the oscillation stabilization period of the high-speed clock (OSCLK). The oscillation stabilization period is the duration of 128 clock pulses in 500 kHz RC oscillation mode and external clock input mode and the duration of 4096 clock pulses in the crystal/ceramic oscillation mode and PLL oscillation mode.

Figure 6-9 shows the waveforms of the high-speed clock generation circuit in crystal/ceramic oscillation mode.

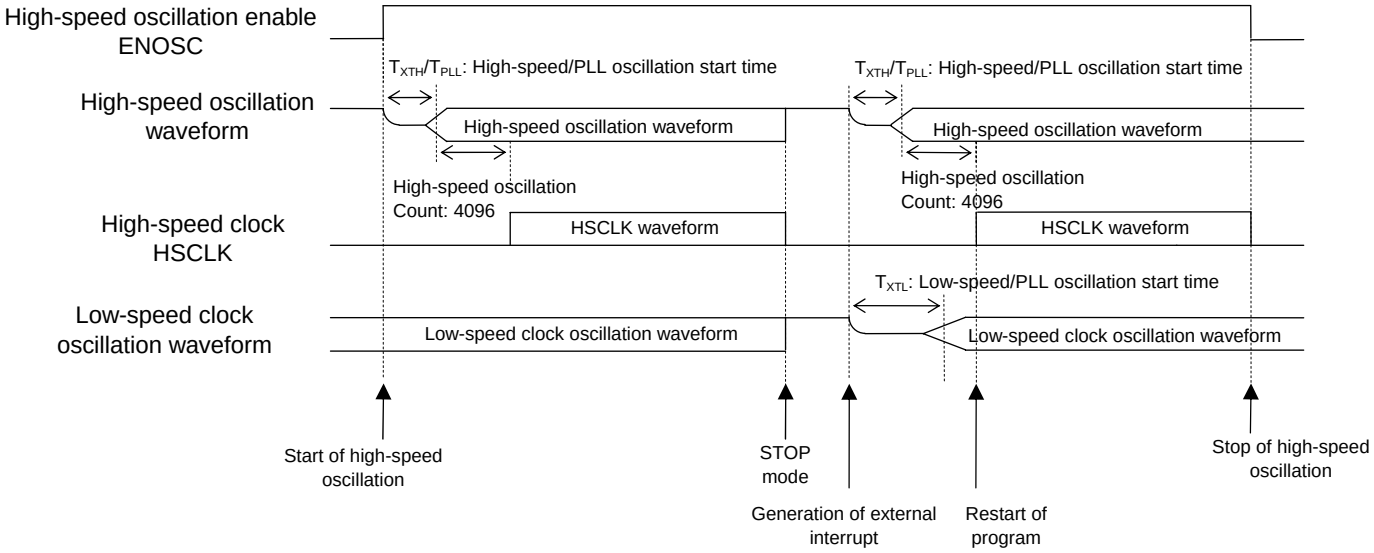


Figure 6-9 Operation of High-Speed Clock Generation Circuit in Crystal/Ceramic Oscillation Mode

6.3.3 Switching of System Clock

The system clock can be switched between high-speed clock (HSCLK) and low-speed clock (LSCLK) by using the frequency control registers (FCON0, FCON1).
Figure 6-10 shows a flow of system clock switching processing (HSCLK→LSCLK) and Figure 6-11 shows a flow of system clock switching processing (LSCLK→HSCLK).

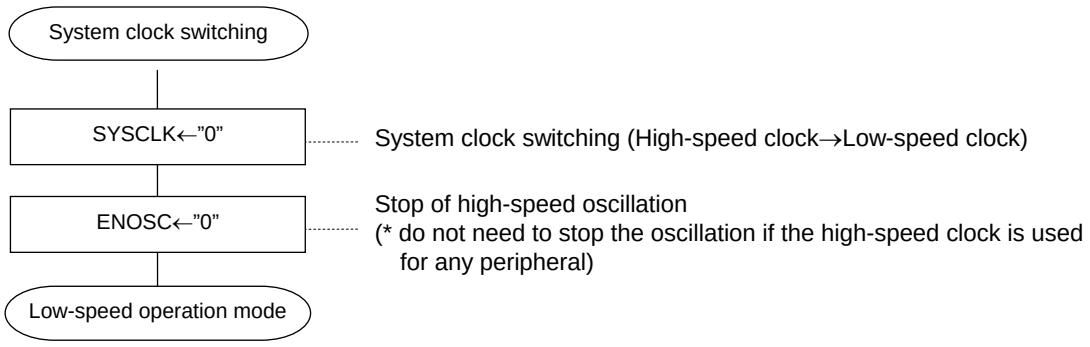


Figure 6-10 Flow of System Clock Switching Processing (HSCLK→LSCLK)

Note:
After the power is turned on or if the system clock is switched from HSCLK to LSCLK immediately following return from the STOP mode, the CPU becomes inactive until LSCLK starts clock supply to the peripheral circuits. Therefore, It is recommended to switch to LSCLK after confirming that the LSCLK is oscillating by checking that the time base counter interrupt request bit (Q128H) is "1".

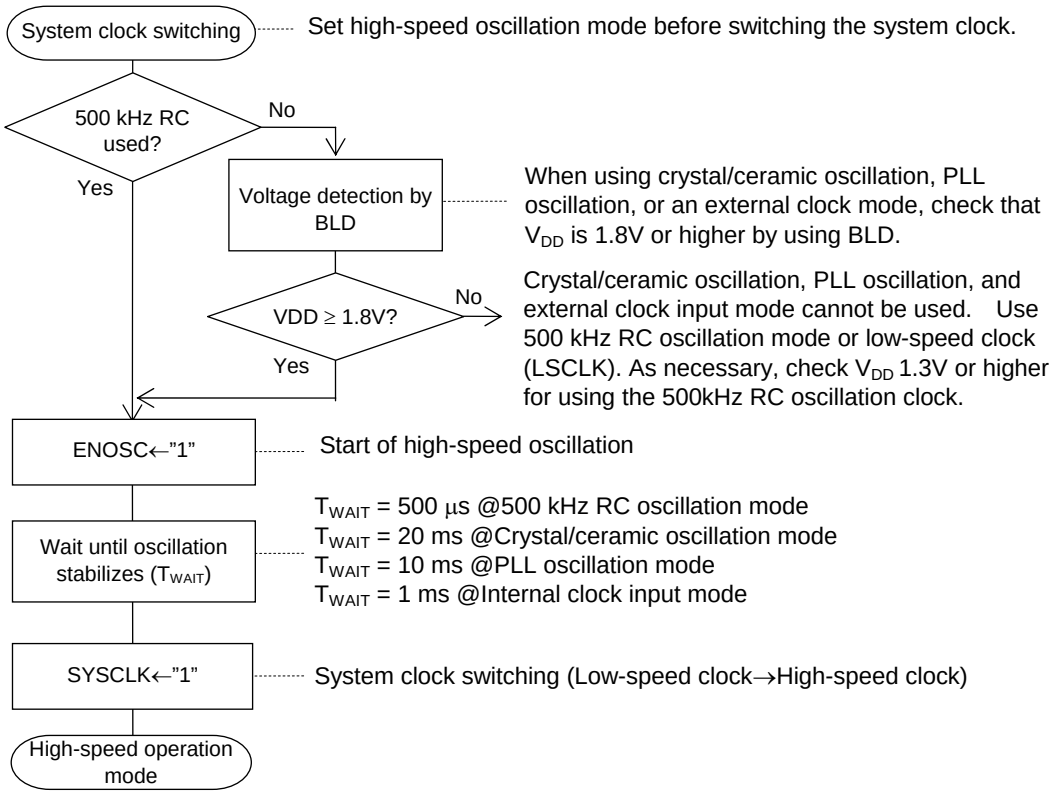


Figure 6-11 Flow of System Clock Switching Processing (LSCLK→HSCLK)

Note:
If the system clock is switched from a low-speed clock to a high-speed clock before the high-speed clock (HSCLK) starts oscillation, the CPU becomes inactive until HSCLK starts clock supply to the peripheral circuits.

6.4 Specifying port registers

When you want to make sure clock output functions are working, please check related port registers are specified. See Chapter 19, "Port2" for detail about the port registers.

6.4.1 Functioning P21 (OUTCLK) as the high speed clock output

Set P21MD bit (bit1 of P2MOD register) to "1" for specifying the high speed clock output as the secondary function of P21.

Reg. name	P2MOD register (Address: 0F214H)							
Bit	7	6	5	4	3	2	**1**	0
Bit name	-	-	-	-	-	P22MD	**P21MD**	P20MD
Data	-	-	-	-	-	*	**1**	*

Set P21C1 bit (bit1 of P2CON1 register) to "1" and set P21C0 bit(bit1 of P2CON0 register) to "1", for specifying the P21 as CMOS output.

Reg. name	P2CON1 register (Address: 0F213H)							
Bit	7	6	5	4	3	2	**1**	0
Bit name	-	-	-	-	-	P22C1	**P21C1**	P20C1
Data	-	-	-	-	-	*	**1**	*

Reg. name	P2CON0 register (Address: 0F212H)							
Bit	7	6	5	4	3	2	**1**	0
Bit name	-	-	-	-	-	P22C0	**P21C0**	P20C0
Data	-	-	-	-	-	*	**1**	*

Data of P21D bit (bit1 of P2D register) does not affect to the high speed clock output function, so don't care the data for the function.

Reg. name	P2D register (Address: 0F210H)							
Bit	7	6	5	4	3	2	**1**	0
Bit name	-	-	-	-	-	P22D	**P21D**	P20D
Data	-	-	-	-	-	*	******	*

- : Bit does not exist.
* : Bit not related to the high speed clock function
** : Don't care the data.

Note:
P21(Port2) is an output-only port, does not have an register to select the data direction(input or output).

6.4.2 Functioning P20 (LSCLK) as the low speed clock output

Set P20MD bit (bit0 of P2MOD register) to "1" for specifying the low speed clock output as the secondary function of P20.

Reg. name	P2MOD register (Address: 0F214H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	-	P22MD	P21MD	**P20MD**
Data	-	-	-	-	-	*	*	**1**

Set P20C1 bit (bit0 of P2CON1 register) to "1" and P20C0 bit (bit0 of P2CON0 register), for specifying P20 as CMOS output.

Reg. name	P2CON1 register (Address: 0F213H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	-	P22C1	P21C1	**P20C1**
Data	-	-	-	-	-	*	*	**1**

Reg. name	P2CON0 register (Address: 0F212H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	-	P22C0	P21C0	**P20C0**
Data	-	-	-	-	-	*	*	**1**

Data of P20D bit (bit0 of P2D register) does not affect to the low speed clock output function, so don't care the data for the function.

Reg. name	P2D register (Address: 0F210H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	-	P22D	P21D	**P20D**
Data	-	-	-	-	-	*	*	******

- : Bit does not exist.
* : Bit not related to the low speed clock function
** : Don't care the data.

Note:
P20(Port2) is an output-only port, does not have an register to select the data direction(i.e. input or output).

Chapter 7

Time Base Counter

7. Time Base Counter

7.1 Overview

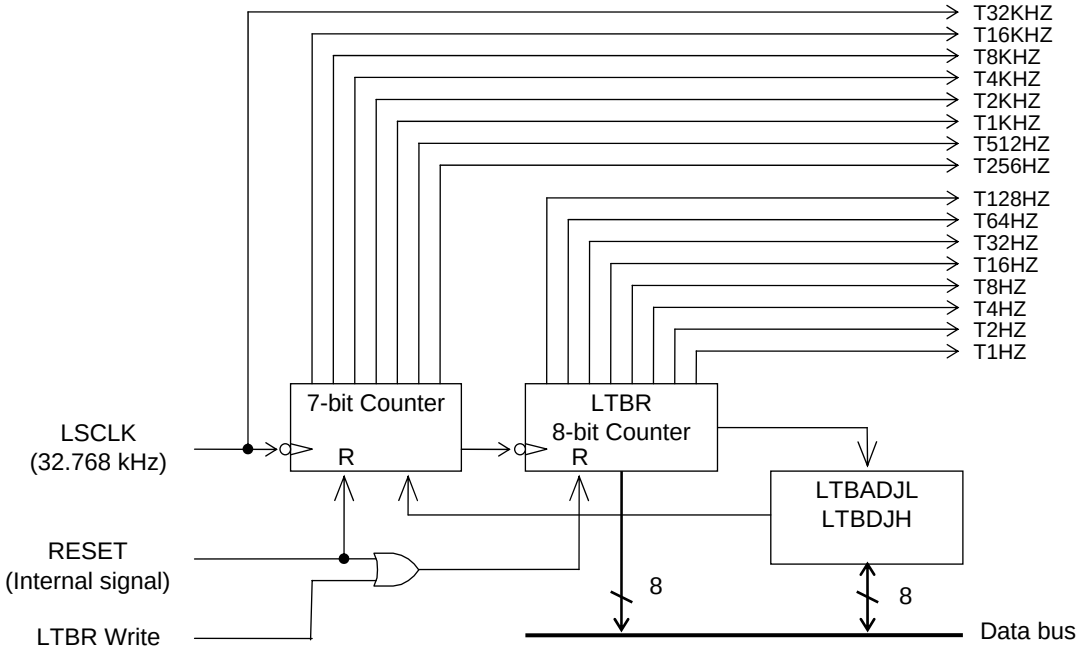
This LSI includes a low-speed time base counter (LTBC) and a high-speed time base counter (HTBC) that generate base clocks for peripheral circuits. By using the time base counter, it is possible to generate events periodically.
For input clocks, see Chapter 6, "Clock Generation Circuit". For interrupt permission, interrupt request flags, etc., described in this chapter, see Chapter 5, "Interrupts".

7.1.1 Features

- LTBC generates T32KHZ to T1HZ signals by dividing the low-speed clock (LSCLK) frequency.
- LTBC allows frequency adjustment (Adjustment range: Approx. –488ppm to +488ppm. Adjustment accuracy: Approx. 0.48ppm) by using the low-speed time base counter frequency adjustment registers (LTBADJH and LTBADJL).
- HTBC generates HTB1 to HTB32 signals by dividing the high-speed clock (HSCLK) frequency.
- Capable of generating 128Hz , 32Hz , 16Hz , and 2Hz interrupts.

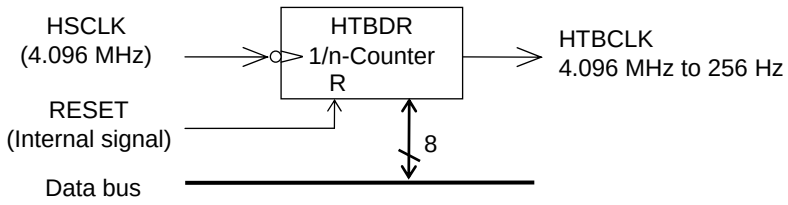
7.1.2 Configuration

Figure 7-1 and Figure 7-2 show the configuration of a low-speed time base counter and a high-speed time base counter, respectively.



LTBR : Low-speed time base counter register
LTBADJL : Low-speed time base counter frequency adjust register
LTBADJH : Low-speed time base counter frequency adjust register

Figure 7-1 Configuration of Low-Speed Time Base Counter (LTBC)



HTBDR: High-speed time base counter frequency divide register

Figure 7-2 Configuration of High-Speed Time Base Counter

Note:
The frequency of HSCLK changes according to specified data in SYSC1 bit and SYSC0 bit of Frequency control register 0 (FON0)

7.2 Description of Registers

7.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F00AH	Low-speed time base counter register	LTBR	—	R/W	8	00H
0F00BH	High-speed time base counter frequency divide register	HTBDR	—	R/W	8	00H
0F00CH	Low-speed time base counter frequency adjustment register L	LTBADJL	LTBADJ	R/W	8/16	00H
0F00DH	Low-speed time base counter frequency adjustment register H	LTBADJH		R/W	8	00H

7.2.2 Low-Speed Time Base Counter (LTBR)

Address: 0F00AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LTBR	T1HZ	T2HZ	T4HZ	T8HZ	T16HZ	T32HZ	T64HZ	T128HZ
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LTBR is a special function register (SFR) to read the T128HZ-T1HZ outputs of the low-speed time base counter. The T128HZ-T1HZ outputs are set to "0" when write operation is performed for LTBR.

Note:
A TBC interrupt (128Hz interrupt, 32Hz interrupt, 16Hz interrupt, or 2Hz interrupt) may occur depending on the LTBR write timing (see Figure 7-4, "Interrupt Timing and Reset Timing by Writing to LTBR"). Therefore, take care in software programming.

7.2.3 High-Speed Time Base Counter Divide Register (HTBDR)

Address: 0F00BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
HTBDR	—	—	—	—	HTD3	HTD2	HTD1	HTD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

HTBDR is a special function register (SFR) to set the divide ratio of the 4-bit, 1/n counter.

[Description of Bits]

- **HTD3-HTD0** (bits 3-0)
  The HTD3-HTD0 bits are used to set the frequency divide ratio of the 4-bit, 1/n counter. The frequency divide ratios selectable include 1/1 to 1/16.

HTD3	HTD2	HTD1	HTD0	Description	
				Divide ratio	Frequency of HTBCLK (*1)
0	0	0	0	× 1/16 (initial value)	256 kHz
0	0	0	1	× 1/15	273 kHz
0	0	1	0	× 1/14	293 kHz
0	0	1	1	× 1/13	315 kHz
0	1	0	0	× 1/12	341 kHz
0	1	0	1	× 1/11	372 kHz
0	1	1	0	× 1/10	410 kHz
0	1	1	1	× 1/9	455 kHz
1	0	0	0	× 1/8	512 kHz
1	0	0	1	× 1/7	585 kHz
1	0	1	0	× 1/6	683 kHz
1	0	1	1	× 1/5	819 kHz
1	1	0	0	× 1/4	1024 kHz
1	1	0	1	× 1/3	1365 kHz
1	1	1	0	× 1/2	2048 kHz
1	1	1	1	× 1/1	4096 kHz

*1: Indicates the frequency when the high-speed oscillation clock, HSCLK, is 4096 kHz.

7.2.4 Low-Speed Time Base Counter Frequency Adjustment Registers L and H (LTBADJL, LTBADJH)

Address: 0F00CH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LTBADJL	LADJ7	LADJ6	LADJ5	LADJ4	LADJ3	LADJ2	LADJ1	LADJ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F00DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LTBADJH	—	—	—	—	—	LADJS	LADJ9	LADJ8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LTBADJL and LTBADJH are special function registers (SFRs) to set the frequency adjustment values of the low-speed time base clock.

[Description of Bits]

- **LADJS, LADJ9-LADJ8** (bits 2-0) **LADJ7-LADJ0** (bits 7-0)
  The LADJS and LADJ9 to LADJ0 bits are used to adjust frequency.
  Adjustment range: Approx. –488ppm to +488ppm.
  Adjustment accuracy: Approx. 0.48ppm
  See Section 7.3.3, "Low-Speed Time Base Counter Frequency Adjustment Function" for the correspondence between the frequency adjustment values (LTBADJH, LTBADJL) and adjustment ratio.

7.3 Description of Operation

7.3.1 Low-Speed Time Base Counter

The low-speed time base counter (LTBC) starts counting from 0000H on the LSCLK falling edge after system reset.
The T128HZ, T32HZ, T16HZ, and T2HZ outputs of LTBC are used as time base interrupts and an interrupt is requested on the falling edge of each output. Each of LTBC outputs is also used as an operation clock for peripheral circuits.
The output data of T128HZ to T1HZ of LTBC can be read from the low-speed time base counter register (LTBR). When reading the data, read LTBR twice and check that the two values coincide to prevent reading of undefined data during counting.
Figure 7-3 shows an example of program to read LTBR.

```
        LEA     offset LTBR     ; EA←LTBR address
MARK:
        L       R0,     [EA]    ; 1st read
        L       R1,     [EA]    ; 2nd read
;
        CMP     R0,     R1      ; Comparison for LTBR
        BNE     MARK            ; To MARK when the values do not coincide
;
            :
```

Figure 7-3 Programming Example for Reading LTBR

LTBR is reset when write operation is performed and the T128HZ to T1HZ outputs are set to "0". Write data is invalid. Since an interrupt occurs if a falling edge occurs in the T128Hz to T1Hz outputs during writing to LTBR, take care in software programming.
Figure 7-4 shows interrupt generation timing and reset timing of the time base counter output by writing to LTBR.

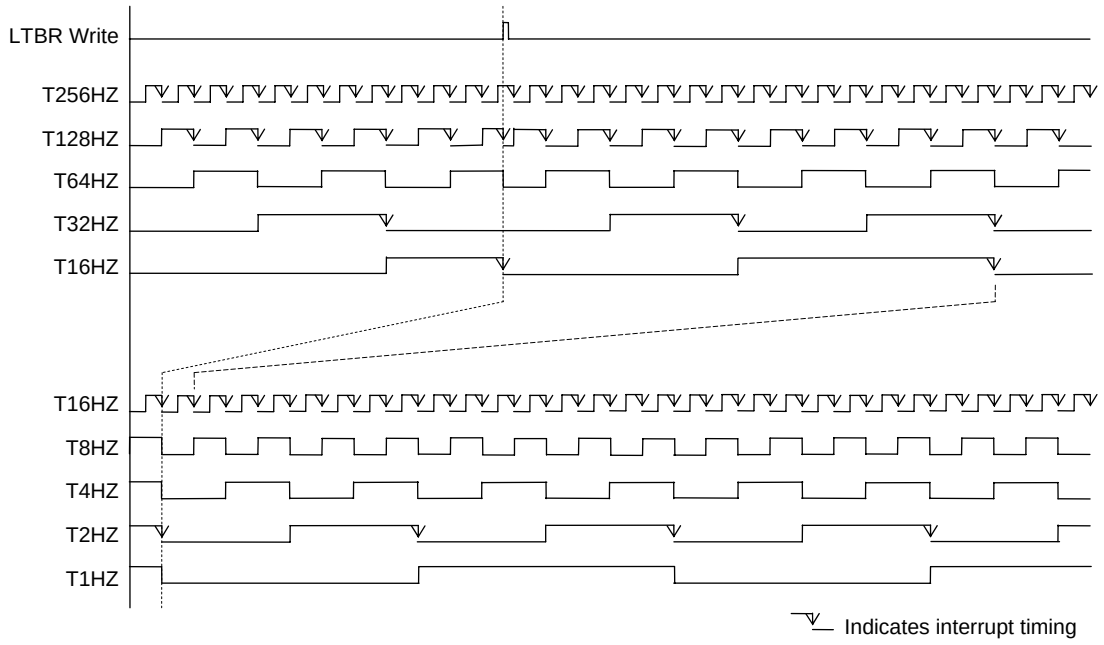


Figure 7-4 Interrupt Timing and Reset Timing by Writing to LTBR

7.3.2 High-Speed Time Base Counter

The high-speed time base counter is configured as a 4-bit 1/n counter (n = 1 to 16).
In the 4-bit 1/n counter, the divided clock (1/16×HSCLK to 1/1×HSCLK) selected by the high-speed time base counter divide register (HTBDR) is generated as HTBCLK. HTBCLK is used as a timer and also as an operation clock of PWM.
Figure 7-5 shows the output waveform of HTBCLK.

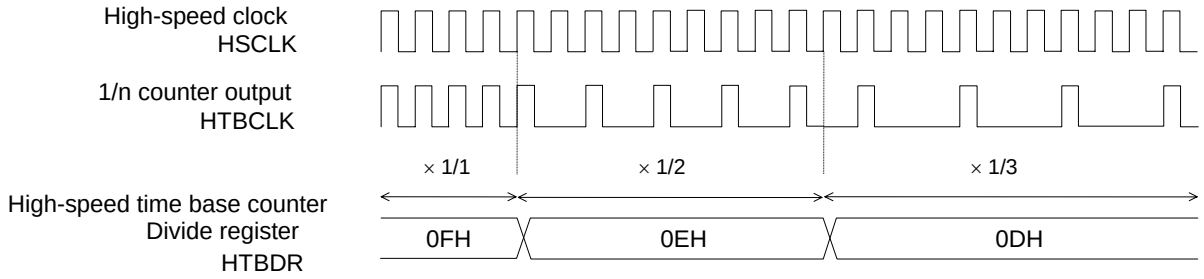


Figure 7-5 Output Waveform of HTBCLK

7.3.3 Low-Speed Time Base Counter Frequency Adjustment Function

Frequency adjustment (Adjustment range: Approx. –488ppm to +488ppm. Adjustment accuracy: Approx. 0.48ppm) is possible for outputs of T8KHZ to T1HZ of LTBC by using the low-speed time base counter frequency adjust registers (LTBADJH and LTBADJL).
Table7-1 shows correspondence between the frequency adjustment values (LTBADJH, LTBADJL) and adjustment ratio.

Table 7-1 Correspondence between Frequency Adjustment Values (LTBADJH, LTBADJL) and Adjustment Ratio

LADJ10 to 0											Hexadecimal	Frequency adjustment ratio (ppm)
0	1	1	1	1	1	1	1	1	1	1	3FFH	+487.80
0	1	1	1	1	1	1	1	1	1	0	3FEH	+487.33
:	:	:	:	:	:	:	:	:	:	:	:	:
0	0	0	0	0	0	0	0	0	1	1	003H	+1.43
0	0	0	0	0	0	0	0	0	1	0	002H	+0.95
0	0	0	0	0	0	0	0	0	0	1	001H	+0.48
0	0	0	0	0	0	0	0	0	0	0	000H	0
1	1	1	1	1	1	1	1	1	1	1	7FFH	–0.48
1	1	1	1	1	1	1	1	1	1	0	7FEH	–0.95
:	:	:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0	0	1	401H	–487.80
1	0	0	0	0	0	0	0	0	0	0	400H	–488.28

The adjustment values (LADJ10 to LADJ0) to be set in LTBADJH and LTBADJL can be obtained by using the following equations:

Adjustment value = Frequency adjustment ratio × 2097152 (decimal)
= Frequency adjustment ratio × 200000h (hexadecimal)

Example 1: When adjusting +15.0ppm (gaining time)
Adjustment value = +15.0ppm × 2097152 (decimal)
= $+15.0 \times 10^{-6} \times 2097152$
= +31.45728 (decimal)
≅ 01Fh (hexadecimal)

Example 2: When adjusting –25.5ppm (losing time)
Adjustment value = –25.5ppm × 2097152 (decimal)
= $-25.5 \times 10^{-6} \times 2097152$
= –53.477376 (decimal)
≅ 7CCh (hexadecimal)

Note:
The low-speed clock (LSCLK) and the outputs of T32KHZ and T16KHZ of LTBC are not adjusted by the frequency adjust function.
The frequency adjustment accuracy does not guarantee the accuracy including the frequency variation of the crystal oscillation (32.768kHz) due to temperature variations.

7.3.4 A signal generation for 16bit timer 2-3 frequency measurement mode

A signal (437C) used for 16bit timer 2-3 frequency measurement mode is generated in the time base conter block. See Chapter 10, "Timer" for more detail about the frequency measurement function.

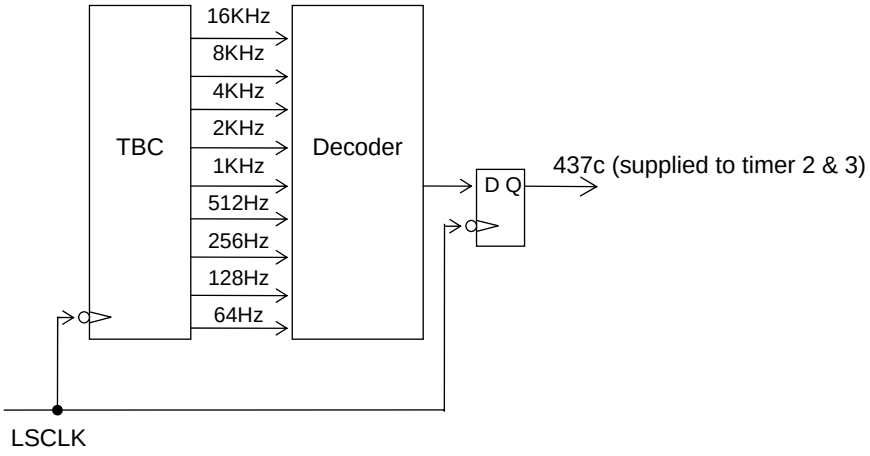


Figure 7-6 437c signal generation block diagram (used for frequency measurement mode)

Chapter 8

Capture

8. Capture

8.1 Overview

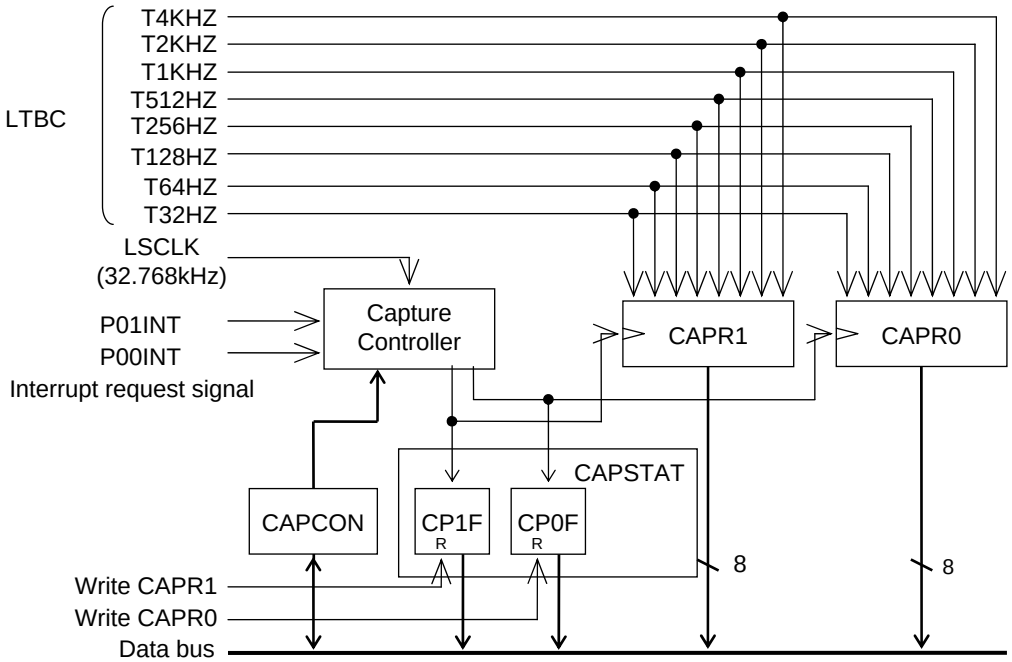
This LSI has two channels of capture circuits that capture the T4KHZ to T32HZ signals of the low-speed base counter (LTBC) to the capture register at the occurrence of P00 and P01 interrupts. The circuits capture timings at which each interrupt occurred, based on the time from the time base counter.
For the external interrupt (P00INT, P01INT) from the P00 or P01 pin, see Chapter 5, "Interrupt" and Chapter 18, "Port 0".

8.1.1 Features

- Time base capture×2ch (4096Hz to 32Hz)

8.1.2 Configuration

Figure 8-1 shows the configuration of the capture circuit.



CAPCON : Capture control register
CAPSTAT : Capture status register
CAPR0 : Capture data register 0
CAPR1 : Capture data register 1

Figure 8-1 Configuration of Capture Circuit

8.1.3 List of Pins

Pin name	I/O	Description
P00/CAP0	I	Capture 0 input pin Used as the secondary function of the P00 pin.
P01/CAP1	I	Capture 1 input pin Used as the secondary function of the P01 pin.

8.2 Description of Registers

8.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F090H	Capture control register	CAPCON	—	R/W	8	00H
0F091H	Capture status register	CAPSTAT	—	R/W	8	00H
0F092H	Capture data register 0	CAPR0	—	R/W	8	00H
0F093H	Capture data register 1	CAPR1	—	R/W	8	00H

8.2.2 Capture Control Register (CAPCON)

Address: 0F090H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CAPCON	—	—	—	—	—	—	ECAP1	ECAP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

CAPCON is a special function register (SFR) to control the capture circuit.

[Description of Bits]

- **ECAP0** (bit 0)
  The ECAP0 bit is used to start or stop the operation of capture 0.

ECAP0	Description
0	Stops the capture 0 operation. (initial value)
1	Starts the capture 0 operation.

- **ECAP1** (bit 1)
  The ECAP1 bit is used to start or stop the operation of capture 1.

ECAP1	Description
0	Stops the capture 1 operation. (initial value)
1	Starts the capture 1 operation.

8.2.3 Capture Status Register (CAPSTAT)

Address: 0F091H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CAPSTAT	—	—	—	—	—	—	CAPF1	CAPF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

CAPSTAT is a special function register (SFR) to indicate a state of the capture circuit.

[Description of Bits]

- **CAPF0** (bit 0)
  The CAPF0 bit is the flag to indicate whether data is captured in capture data register 0 (CARP0) or not.
  When the CAPF0 bit is set to "1", it indicates that data is captured in capture data register 0 (CAPR0).
  When the CAPF0 bit is set to "1", the next capture operation is stopped. So perform the write operation to capture data register 0 (CAPR0) to clear the CAPF0 bit to "0".

CAPF0	Description
0	No capture 0 latch (initial value)
1	Capture 0 latch

- **CAPF1** (bit 1)
  The CAPF1 bit is the flag to indicate whether data is captured in capture data register 0 (CARP1) or not.
  When the CAPF0 bit is set to "1", it indicates that data is captured in capture data register 0 (CAPR1).
  When the CAPF1 bit is set to "1", the next capture operation is stopped. So perform the write operation to capture data register 1 (CAPR1) to clear theCAPF0 bit to "0".

CAPF1	Description
0	No capture 1 latch (initial value)
1	Capture 1 latch

8.2.4 Capture Data Register 0 (CAPR0)

Address: 0F092H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CAPR0	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

CAPR0 is a register in which capture data is stored.
The T4KHZ to T32HZ signals of the low-speed time base counter (LTBC) are captured when the P00 interrupt request is generated with the CAPF0 flag (bit 0 of the CAPSTAT register) set to "0".
Writing to CAPR0 sets the CAPF0 flag of CAPSTAT to "0". The value of CAPR0 does not change even if data is written to it.

8.2.5 Capture Data Register 1 (CAPR1)

Address: 0F093H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CAPR1	CP17	CP16	CP15	CP14	CP13	CP12	CP11	CP10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

CAPR1 is a register in which capture data is stored.
The T4KHZ to T32HZ signals of the low-speed time base counter (LTBC) are captured when the P01 interrupt request is generated with the CAPF1 flag (bit 1 of the CAPSTAT register) set to "0".
Writing to CAPR1 sets the CAPF1 flag of CAPSTAT to "0". The value of CAPR1 does not change even if data is written to it.

8.3 Description of Operation

The capture circuit starts the capture operation by setting the ECAP0 or ECAP1 bit of the capture control register (CAPCON).
When the input trigger from the P00 or P01 pin selected by the external interrupt control register 0 or 1 (EXICON0 or EXICON1) is generated and the P00 or P01 interrupt request flag (QP00 or QP01) is set to "1", the T4KHZ to T32HZ signals of the low-speed time base counter (LTBC) are captured in the capture register 0 or 1 (CAPR0 or CAPR1) on the next low-speed clock (LSCLK) falling edge and the at the same time, the capture flag (CAPF0 or CAPF1) of the capture status register (CAPSTAT) is set to "1".
When the capture flag (CAPF0, CAPF1) is "1", the following capture operation stops.
After reading the value captured in the capture register 0 or 1 (CAPR0, CAPR1), perform write operation (write data is meaningless) for the capture register 0 or 1 (CAPR0, CAPR1), clear the capture flag (CAPF0, CAPF1) to "0", and wait for the next P00 or P01 interrupt.
Figure 8-2 shows the timing of the capture operation.

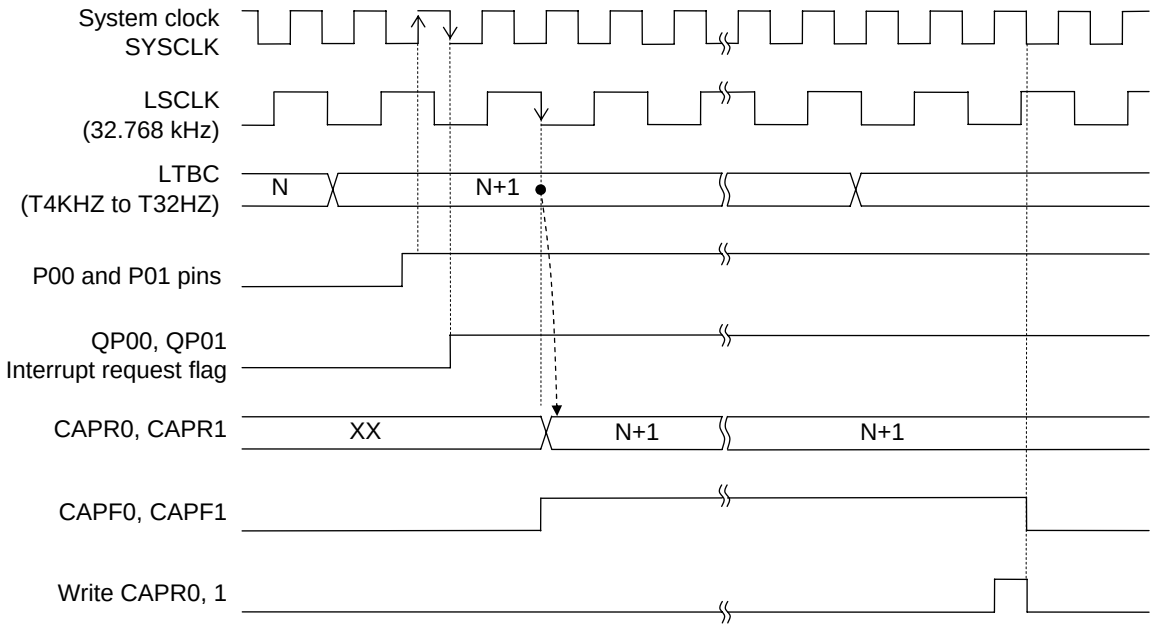


Figure 8-2 Timing Diagram of Capture Operation

Note:
When CPU is operating at the high speed (HSCLK), check that the capture flag (CAPF0, CAPF1) is set to "1" after the P00 or P01 interrupt request is generated and then read capture data register 0 or 1 (CAPR0, CAPR1).

Chapter 9

1 kHz Timer (1kHzTM)

9. 1 kHz Timer (1kHzTM)

9.1 Overview

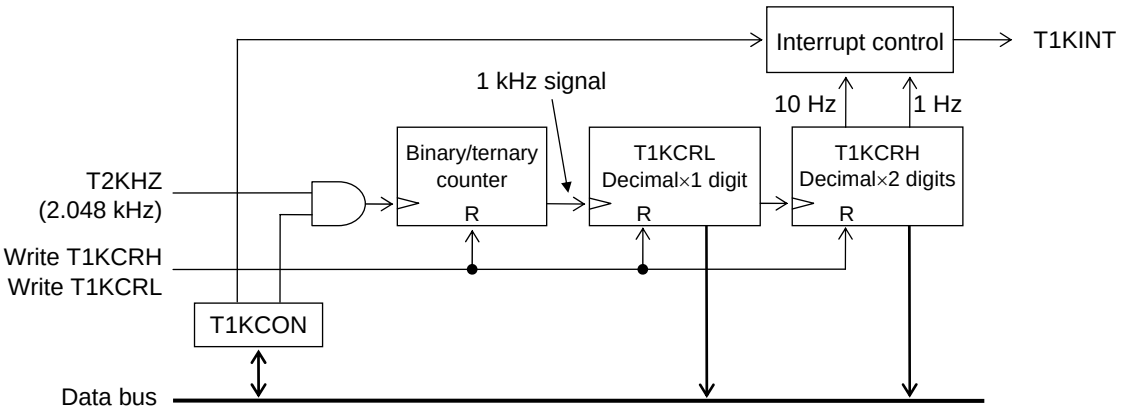
This LSI includes a 1 kHz timer to measure 1/1000 seconds.
The 1 kHz timer counts the 1 kHz signal created by dividing the T2KHZ output frequency (2.048 kHz) of the low-speed time base counter (LTBC) and generates a 10 Hz or 1 Hz interrupt (1 kHz timer interrupt).
With the 1 kHz timer, 1/1000 second, which is difficult to generate on a time-base-counter basis, represented by a decimal number can be obtained easily. The timer can be applied to period measurement for stopwatches.
For the timer base counter, see Chapter 7, "Time Base Counter".

9.1.1 Features

- 10 Hz/1 Hz interrupt select function

9.1.2 Configuration

Figure 9-1 shows the configuration of the 1 kHz timer.



T1KCON : 1 kHz timer control register
T1KCRL : 1 kHz timer count register L
T1KCRH : 1 kHz timer count register H

Figure 9-1 Configuration of 1 kHz Timer

9.2 Description of Registers

9.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F080H	1 kHz timer count register L	T1KCRL	T1KCR	R/W	8/16	00H
0F081H	1 kHz timer count register H	T1KCRH		R/W	8	00H
0F082H	1 kHz timer control register	T1KCON	—	R/W	8	00H

9.2.2 1 kHz Timer Count Registers (T1KCRL, T1KCRH)

Address: 0F080H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
T1KCRL	T1KC3	T1K02	T1KC1	T1KC0	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F081H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
T1KCRH	T1KC11	T1K010	T1KC9	T1KC8	T1KC7	T1K06	T1KC5	T1KC4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

T1KCRL and T1KCRH are special function registers (SFRs) to read the decimal count values of the 1 kHz timer. When the write operation to T1KCRL or T1KCRH, the valid bit of T1KCRL or T1KCRH is "0" respectively.

[Description of Bits]

- **T1KC11 to T1KC0** (T1KCRH: bits 7 to 0, T1KCRL: bits 7 to 4)
  T1KC11 to T1KC0 indicate the count values of the 1 kHz timer.

9.2.3 1 kHz Timer Control Register (T1KCON)

Address: 0F082H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
T1KCON	—	—	—	—	—	—	T1KSEL	T1KRUN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

T1KCON is a special function register (SFR) to control the 1 kHz timer.

[Description of Bits]

- **T1KRUN** (bit 0)
  The T1KRUN bit is used to control start/stop of the count operation of the 1 kHz timer counter.

T1KRUN	Description
0	Stops 1 kHz timer operation (initial value).
1	Starts 1 kHz operation.

- **T1KSEL** (bit 1)
  The T1LSEL bit is used to select the interrupt period of the 1 kHz timer. The 10 Hz or 1 Hz interrupt can be selected.

T1KSEL	Description
0	10 Hz interrupt (initial value)
1	1 Hz interrupt

9.3 Description of Operation

By setting the T1KRUN bit of the 1kHz timer control register (T1KCON) to "1", the 1kHz timer starts counting of the 1kHz timer counter registers L or H (T1KCRL, T1KCRH).
By dividing the T2KHz signal frequency (2.048kHz) of the low-speed timer base counter (LTBC) by the binary/ternary counter, the timer generates a 1kHz signal. Based on the 1kHz signal, a 1kHz timer interrupt request signal (T1KINT) is generated by the decimal counters of T1KCRL and T1KCRH. The period of the 1kHz timer interrupt can be selected between the 10Hz interrupt or 1Hz interrupt using the T1KSEL bit of T1KCON.
When write operation is performed for T1KCRL or T1KCRH, the value of the binary/ternary counter and the value of T1KCRL or T1KCRH is cleared to "0".
Data can be read from T1KCRL and T1KCRH. When reading data from T1KCRL or T1KCRH in the 1kHz timer operation start state, read T1KCRL or T1KCRH twice and check that the values match to prevent the reading of undefined data during counting.
Figure 9-2 shows an example of the program for reading T1KCL and T1LCRH.

```
        LEA   offset T1KCRL   ; EA←T1KCRL address
MARK:
        L   ER0,  [EA]          ; First read
        L   ER2,  [EA]          ; Second read
;
        CMP   ER0, ER1          ; Comparison of T1KCRL and T1CKRH
        BNE   MARK              ; To MARK when not matched.
;
          :
```

Figure 9-2 Example of Program for Reading T1KCRL and T1KCRH

Chapter 10

Timers

10. Timers

10.1 Overview

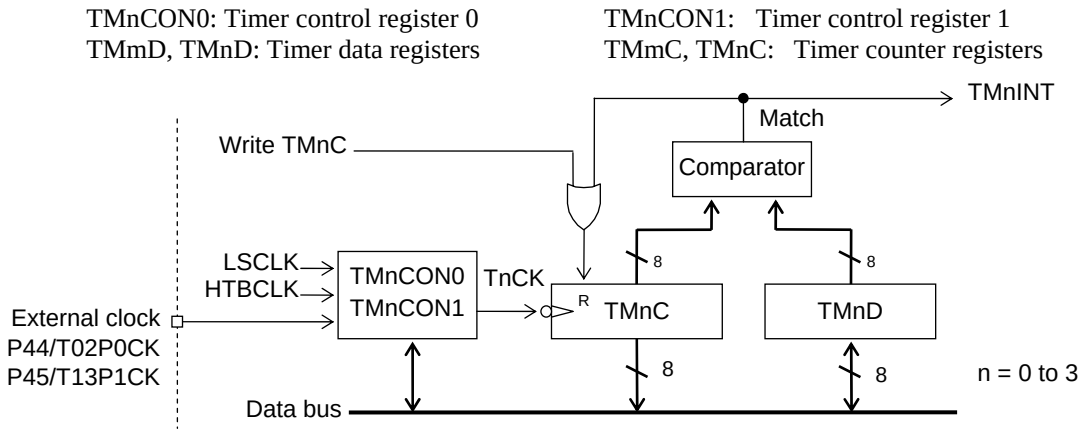
This LSI includes 4 channels of 8-bit timers.
For the input clock, see Chapter 6, "Clock Generation Circuit".

10.1.1 Features

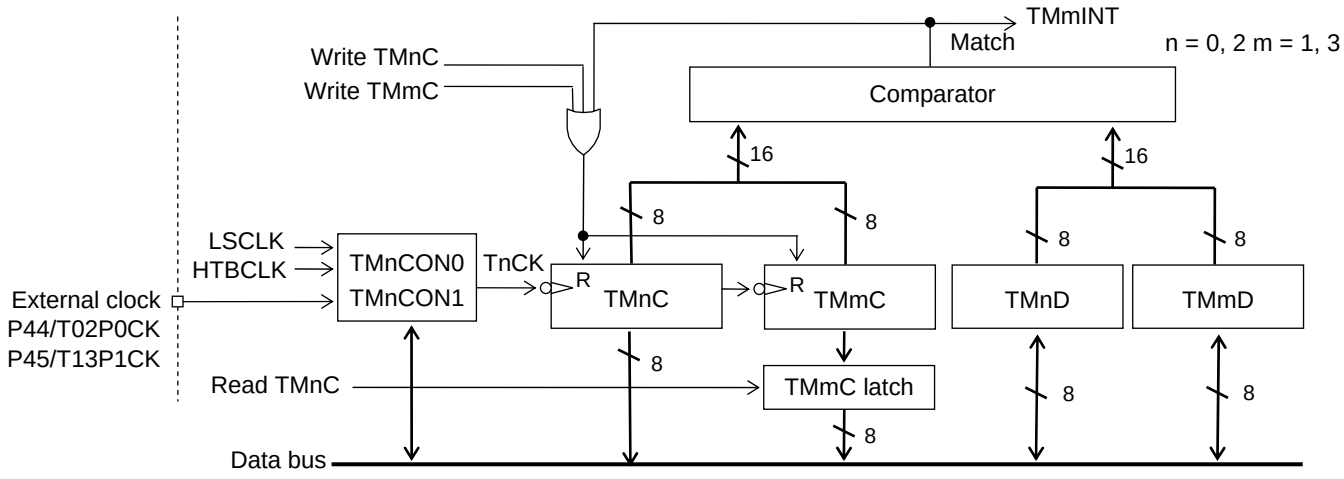
- The timer interrupt (TMnINT) is generated when the values of timer counter register (TMnC, n=0 to 3) and timer data register (TMnD) coincide.
- A timer configured by combining timer 0 and timer 1 or timer 2 and timer 3 can be used as a 16-bit timer.
- For the timer clock, the low-speed clock (LSCLK), high-speed time base clock (HTBCLK), or external clock can be selected.
- A 16bit-timer 2 & 3 has clock frequency measurement mode, which can count HTBCLK and generates the timer interrupt (TM3INT) when the count ends. Using the count data to know the frequency by software can determine more accurate baud-rate.

10.1.2 Configuration

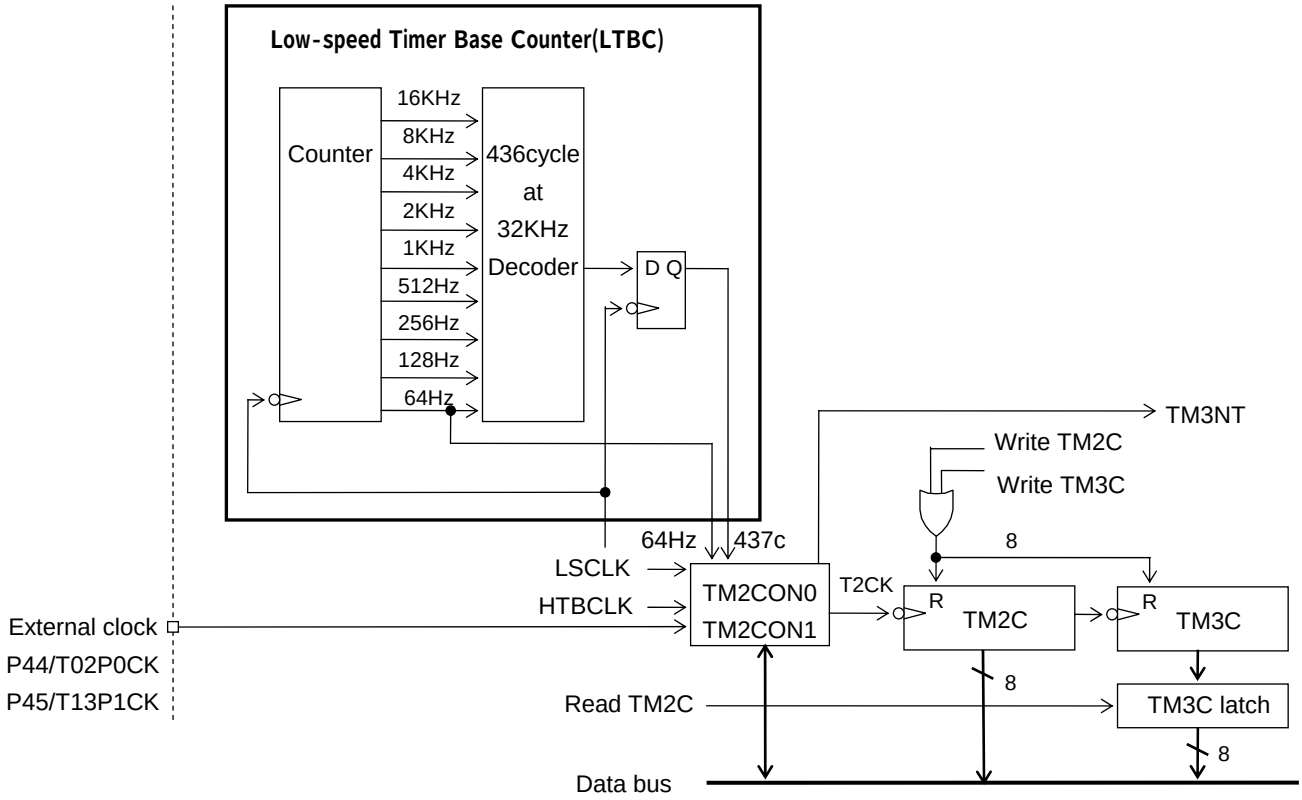
Figure 10-1 shows the configuration of the timers.



(a) In 8-bit Timer Mode (Timers 0 to 3)



(b) 16-bit Timer Mode (Timers 0 to 3)



(c) Frequency measurement mode with 16bit timer(Timer2 to 3)

Figure 10-1 Configuration of Timers

10.2 Description of Registers

10.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F030H	Timer 0 data register	TM0D	TM0DC	R/W	8/16	0FFH
0F031H	Timer 0 counter register	TM0C		R/W	8	00H
0F032H	Timer 0 control register 0	TM0CON0	TM0CON	R/W	8/16	00H
0F033H	Timer 0 control register 1	TM0CON1		R/W	8	00H
0F034H	Timer 1 data register	TM1D	TM1DC	R/W	8/16	0FFH
0F035H	Timer 1 counter register	TM1C		R/W	8	00H
0F036H	Timer 1 control register 0	TM1CON0	TM1CON	R/W	8/16	00H
0F037H	Timer 1 control register 1	TM1CON1		R/W	8	00H
0F038H	Timer 2 data register	TM2D	TM2DC	R/W	8/16	0FFH
0F039H	Timer 2 counter register	TM2C		R/W	8	00H
0F03AH	Timer 2 control register 0	TM2CON0	TM2CON	R/W	8/16	0A0H
0F03BH	Timer 2 control register 1	TM2CON1		R/W	8	00H
0F03CH	Timer 3 data register	TM3D	TM3DC	R/W	8/16	0FFH
0F03DH	Timer 3 counter register	TM3C		R/W	8	00H
0F03EH	Timer 3 control register 0	TM3CON0	TM3CON	R/W	8/16	00H
0F03FH	Timer 3 control register 1	TM3CON1		R/W	8	00H

10.2.2 Timer 0 Data Register (TM0D)

Address: 0F030H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM0D	T0D7	T0D6	T0D5	T0D4	T0D3	T0D2	T0D1	T0D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM0D is a special function register (SFR) to set the value to be compared with the timer 0 counter register (TM0C) value.

Note:
Set TM0D when the timer stops(When T0STAT bit of TM0CON1 register is "0").
When "00H" is written in TM0D, TM0D is set to "01H".

10.2.3 Timer 1 Data Register (TM1D)

Address: 0F034H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM1D	T1D7	T1D6	T1D5	T1D4	T1D3	T1D2	T1D1	T1D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM1D is a special function register (SFR) to set the value to be compared with the value of the timer 1 counter register (TM1C).

Note:
Set TM1D when the timer stops(When T1STAT bit of TM1CON1 register is "0").
When "00H" is written in TM1D, TM1D is set to "01H".

10.2.4 Timer 2 Data Register (TM2D)

Address: 0F038H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM2D	T2D7	T2D6	T2D5	T2D4	T2D3	T2D2	T2D1	T2D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM2D is a special function register (SFR) to set the value to be compared with the value of the timer 2 counter register (TM2C).

Note:
Set TM2D when the timer stops(When T2STAT bit of TM2CON1 register is "0").
When "00H" is written in TM2D, TM2D is set to "01H".

10.2.5 Timer 3 Data Register (TM3D)

Address: 0F03CH
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM3D	T3D7	T3D6	T3D5	T3D4	T3D3	T3D2	T3D1	T3D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM3D is a special function register (SFR) to set the value to be compared with the value of the timer 3 counter register (TM3C).

Note:
Set TM3D when the timer stops(When T3STAT bit of TM3CON1 register is "0").
When "00H" is written in TM3D, TM3D is set to "01H".

10.2.6 Timer 0 Counter Register (TM0C)

Address: 0F031H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM0C	T0C7	T0C6	T0C5	T0C4	T0C3	T0C2	T0C1	T0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM0C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM0C is performed, TM0C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode and 16-bit timer frequency measurement mode, if write operation is performed to either the low-order TM0C or high-order TM1C, both the low-order and the high-order are set to "0000H".

During timer operation, the contents of TM0C may not be read depending on the conditions of the timer clock and the system clock.
Table 10-1 shows whether a TM0C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 10-1 TM0C Read Enable/Disable during Timer Operation

Timer clock T0CK	System clock SYSCLK	TM0C read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read TM0C twice and check that the results match.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

10.2.7 Timer 1 Counter Register (TM1C)

Address: 0F035H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM1C	T1C7	T1C6	T1C5	T1C4	T1C3	T1C2	T1C1	T1C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM1C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM1C is performed, TM1C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode and 16-bit timer frequency measurement mode, if write operation is performed to either the low-order TM0C or high-order TM1C, both the low order and the high order are set to "0000H".
When reading TM1C in 16-bit timer mode, be sure to read TM0C first since the count value of TM1C is stored in the TM1C latch when TM0C is read.

During timer operation, the contents of TM1C may not be read depending on the conditions of the timer clock and the system clock.
Table 10-2 shows whether a TM1C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 10-2 TM1C Read Enable/Disable during Timer Operation

Timer clock T1CK	System clock SYSCLK	TM1C read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read TM1C twice and check that the results match.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

10.2.8 Timer 2 Counter Register (TM2C)

Address: 0F039H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM2C	T2C7	T2C6	T2C5	T2C4	T2C3	T2C2	T2C1	T2C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM2C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM2C is performed, TM2C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode and 16-bit timer frequency measurement mode, if write operation is performed to either the low-order TM2C or high-order TM3C, both the low order and the high order are set to "0000H".

During timer operation, the contents of TM2C may not be read depending on the conditions of the timer clock and the system clock.
Table 10-3 shows whether a TM2C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 10-3 TM2C Read Enable/Disable during Timer Operation

Timer clock T2CK	System clock SYSCLK	TM2C read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read TM2C twice and check that the results match.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

10.2.9 Timer 3 Counter Register (TM3C)

Address: 0F03DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM3C	T3C7	T3C6	T3C5	T3C4	T3C3	T3C2	T3C1	T3C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM3C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM3C is performed, TM3C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode and 16-bit timer frequency measurement mode, if write operation is performed to either the low-order (TM2C) or high-order (TM3C), both the low order and the high order are set to "0000H".
When reading TM3C in 16-bit timer mode, be sure to read TM2C first since the count value of TM3C is stored in the TM3C latch when TM2C is read.

During timer operation, the contents of TM3C may not be read depending on the conditions of the timer clock and the system clock.
Table 10-4 shows whether a TM3C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 10-4 TM3C Read Enable/Disable during Timer Operation

Timer clock T3CK	System clock SYSCLK	TM3C read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read TM3C twice and check that the results match.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

10.2.10 Timer 0 Control Register 0 (TM0CON0)

Address: 0F032H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM0CON0	—	—	—	—	—	T01M16	T0CS1	T0CS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM0CON0 is a special function (SFR) to control a timer 0.
Rewrite TM0CON0 while the timer 0 is stopped (T0STAT of the TM0CON1 register is "0").

[Description of Bits]

- **T0CS1, T0CS0** (bits 1, 0)
  The T0CS1 and T0CS0 bits are used for selecting the operation clock of timer 0. LSCLK, HTBCLK, or the external clock (P44/T02P0CK) can be selected by these bits.

T0CS1	T0CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited (timer 0 does not operate)
1	1	External clock (P44/T02P0CK)

- **T01M16** (bit 2)
  The T01M16 bit is used for selecting the operating mode of timer 0 and timer 1.
  In 8-bit timer mode, each of timer 0 and timer 1 operates independently as a 8-bit timer.
  In 16-bit timer mode, timer 0 and timer 1 are connected and they operate as a 16-bit timer.
  In 16-bit timer mode, timer 1 is incremented by a timer 0 overflow signal. A timer 0 interrupt (TM0INT) is not generated.

T01M16	Description
0	8-bit timer mode (initial value)
1	16-bit timer mode

10.2.11 Timer 1 Control Register 0 (TM1CON0)

Address: 0F036H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM1CON0	—	—	—	—	—	—	T1CS1	T1CS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM1CON0 is a special function (SFR) to control a timer 1.
Rewrite TM1CON0 while the timer 1 is stopped (T1STAT of the TM1CON1 register is "0").

[Description of Bits]

- **T1CS1, T1CS0** (bits 1, 0)
  The T1CS1 and T1CS0 bits are used for selecting the operation clock of timer 1. LSCLK, HTBCLK, or the external clock (P45/T13P0CK) can be selected by these bits.
  In cases where the 16-bit timer mode has been selected by setting T01M16 of TM0CON to "1", the values of T1CS1 and T1CS0 are invalid.

T1CS1	T1CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited (timer 1 does not operate)
1	1	External clock (P45/T13P1CK)

10.2.12 Timer 2 Control Register 0 (TM2CON0)

Address: 0F03AH
Access: R/W
Access size: 8 bits
Initial value: 0A0H

	7	6	5	4	3	2	1	0
TM2CON0	T2FMA7	T2FMA6	T2FMA5	T2FMA4	T23MFM	T23M16	T2CS1	T2CS0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	1	0	1	0	0	0	0	0

TM2CON0 is a special function (SFR) to control a timer 2.
Rewrite TM2CON0 while the timer 2 is stopped (T2STAT of the TM2CON1 register is "0").

[Description of Bits]

- **T2CS1, T2CS0** (bits 1, 0)
  The T2CS1 and T2CS0 bits are used for selecting the operation clock of timer 2. LSCLK, HTBCLK, or the external clock (P44/T02P0CK) can be selected by these bits.

T2CS1	T2CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited (timer 2 does not operate)
1	1	External clock (P44/T02P0CK)

- **T23MFM, T23M16** (bit 3, 2)
  The T23MFM bit and T23M16 bit is used for selecting the operating mode of timer 2 and timer 3..
  In 8-bit timer mode, each of timer 0 and timer 1 operates independently as a 8-bit timer.
  In 16-bit timer mode, timer 2 and timer 3 are connected and they operate as a 16-bit timer.
  In 16-bit timer mode, timer 3 is incremented by a timer 2 overflow signal. A timer 2 interrupt (TM2INT) is not generated.
  In 16-bit timer frequency measurement mode, timer 2 and timer 3 are connected and they operate as a 16-bit clock counter to measure the frequency. A timer 2 interrupt (TM2INT) is not generated.

T23MFM	T23M16	Description
0	0	8-bit timer mode (initial value)
0	1	16-bit timer mode
1	0	Prohibited (timer 2 and timer 3 does not operate)
1	1	16-bit timer frequency measurement mode

- **T2FMA7~T2FMA4** (bit 7~4)
  The T2FMA7 bit ~T2FMA4 bit shows the LSI has the frequency measurement mode.
  Those bits are read-only and always return 1010b on ML610Q421/ML610Q422/ML610421/ML610422.

T2FMA7	T2FMA6	T2FMA5	T2FMA4	Description
1	0	1	0	The frequency measurement mode is available.

10.2.13 Timer 3 Control Register 0 (TM3CON0)

Address: 0F03EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM3CON0	—	—	—	—	—	—	T3CS1	T3CS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM3CON0 is a special function (SFR) to control a timer 3.
Rewrite TM3CON0 while the timer 3 is stopped (T3STAT of the TM3CON1 register is "0").

[Description of Bits]

- **T3CS1, T3CS0** (bits 1, 0)
  The T3CS1 and T3CS0 bits are used for selecting the operation clock of timer 3. LSCLK, HTBCLK, or the external clock (P44/T13P1CK) can be selected by these bits.
  In cases where the 16-bit timer mode has been selected by setting T23M16 of TM2CON to "1", the values of T3CS1 and T3CS0 are invalid.

T3CS1	T3CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited (timer 3 does not operate)
1	1	External clock (P45/T13P1CK)

10.2.14 Timer 0 Control Register 1 (TM0CON1)

Address: 0F033
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM0CON1	T0STAT	—	—	—	—	—	—	T0RUN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM0CON1 is a special function register (SFR) to control a timer 0.

[Description of Bits]

- **T0RUN** (bit 0)
  The T0RUN bit is used for controlling stop/start of timer 0.

T0RUN	Description
0	Stops counting.
1	Starts counting.

- **T0STAT** (bit 7)
  The T0STAT bit is used for indicating "counting stopped"/"counting in progress" of timer 0.

T0STAT	Description
0	Counting stopped.
1	Counting in progress.

10.2.15 Timer 1 Control Register 1 (TM1CON1)

Address: 0F037H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM1CON1	T1STAT	—	—	—	—	—	—	T1RUN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM1CON1 is a special function register (SFR) to control a timer 1.

[Description of Bits]

- **T1RUN** (bit 0)
  The T1RUN bit is used for controlling count stop/start of timer 1.
  In 16-bit timer mode, be sure to set this bit to "0". Timer 1 is incremented caused by a timer 0 overflow signal regardless of the value of T1RUN.

T1RUN	Description
0	Stops counting.
1	Starts counting.

- **T1STAT** (bit 7)
  The T1STAT bit is used for indicating "counting stopped"/"counting in progress" of timer 1.
  In 16-bit timer mode, this bit will read "0".

T1STAT	Description
0	Counting stopped.
1	Counting in progress.

10.2.16 Timer 2 Control Register 1 (TM2CON1)

Address: 0F03BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM2CON1	T2STAT	—	—	—	—	—	—	T2RUN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM2CON1 is a special function register (SFR) to control a timer 2.

[Description of Bits]

- **T2RUN** (bit 0)
  The T2RUN bit is used for controlling stop/start of timer 2.
  Setting the T2RUN bit can forcely cancel the counting in the 16-bit timer frequency measurement mode. In that case, TM3INT does not occur.

T2RUN	Description
0	Stops counting.
1	Starts counting.

- **T2STAT** (bit 7)
  The T2STAT bit is used for indicating "counting stopped"/"counting in progress" of timer 2.

T2STAT	Description
0	Counting stopped.
1	Counting in progress.

10.2.17 Timer 3 Control Register 1 (TM3CON1)

Address: 0F03FH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM3CON1	T3STAT	—	—	—	—	—	—	T3RUN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM3CON1 is a special function register (SFR) to control a timer 3.

[Description of Bits]

- **T3RUN** (bit 0)
  The T3RUN bit is used for controlling stop/start of timer 3.
  In 16-bit timer mode and 16-bit timer frequency measurement mode, be sure to set this bit to "0". Timer 3 is incremented caused by a timer 2 overflow signal regardless of the value of T3RUN.

T3RUN	Description
0	Stops counting.
1	Starts counting.

- **T3STAT** (bit 7)
  The T3STAT bit is used for indicating "counting stopped"/"counting in progress" of timer 3.
  In 16-bit timer mode and 16-bit timer frequency measurement mode, this bit will return "0".

T3STAT	Description
0	Counting stopped.
1	Counting in progress.

10.3 Description of Operation

10.3.1 Timer mode operation

The timer counters (TMnC) are set to an operating state (TnSTAT are set to "1") on the first falling edge of the timer clocks (TnCK) that are selected by the Timer 0 to 3 control register 0 (TMnCON0) when the TnRUN bits of timer 0 to 3 control register 1 (TMnCON1) are set to "1" and increment the count value on the 2nd falling.

When the count value of TM0 to TM3C and the timer 0 to 3 data register (TMnD) coincide, timer 0 to 3 interrupt (TMnINT) occurs on the next timer clock falling edge, TMnC are reset to "00H" and incremental counting continues.

When the TnRUN bits are set to "0", TMnC stop counting after counting once the falling of the timer clock (TnCK). Confirm that TMnC has been stopped by checking that the TnSTAT bit of the Timer 0–3 control register 1 (TMnCON1) is "0". When the TnRUN bits are set to "1" again, TMn restart incremental counting from the previous values. To initialize TMnC to "00H", perform write operation in TMnC.
The timer interrupt period (TTMI) is expressed by the following equation.

$$TTMI = \frac{TMnD + 1}{TnCK\ (Hz)} \quad (n = 0 \text{ to } 3)$$

TMnD: Timer 0 to 3 data register (TMnD) setting value (01H to 0FFH)
TnCK: Clock frequency selected by the Timer 0 to 3 control register 0 (TMnCON0)

After the TnRUN bits are set to "1", timers are synchronized by the timer clock and counting starts so that an error of a maximum of 1 clock period occurs until the first timer interrupt. The timer interrupt periods from the second time are constant.
Figure 10-2 shows the operation timing diagram of Timer 0 to 3.

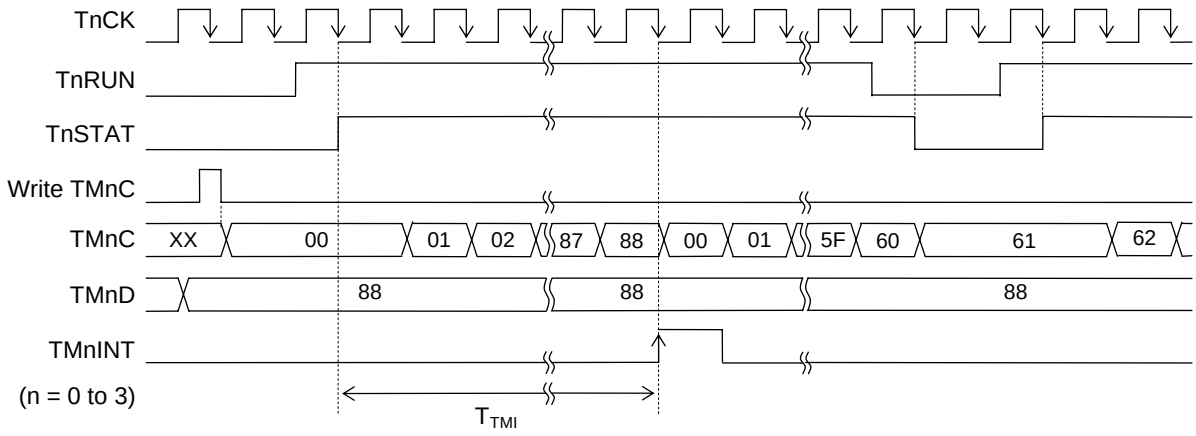


Figure 10-2 Operation Timing Diagram of Timer 0 to 3

Note:
Even if "0" is written to the TnRUN bits, counting operation continues up to the falling edge (the timer 0 to 3 status flag (TnSTA) is in a "1" state) of the next timer clock pulse. Therefore, the timer 0 to 3 interrupt (TMnINT) may occur.

10.3.2 16-bit timer frequency measurement mode operation

The frequency measurement mode in 16-bit timer 2&3, is used to count the frequency of 500kHz RC oscillation clock which typically has temperature variation and production tolerance.

Using the frequency measurement mode can make better accuracy for uart baud-rate clock or timer function.
(1) Reading the count data, caluculating and setting it to uart communication baud-rate registers, can make more accurate baud-rate clock.
(2) Reading the count data, caluculating and setting it to a timer data register, can make more accurate timing in normal timer mode.

Figure 10-3 shows the operation timing in frequency measurement mode.

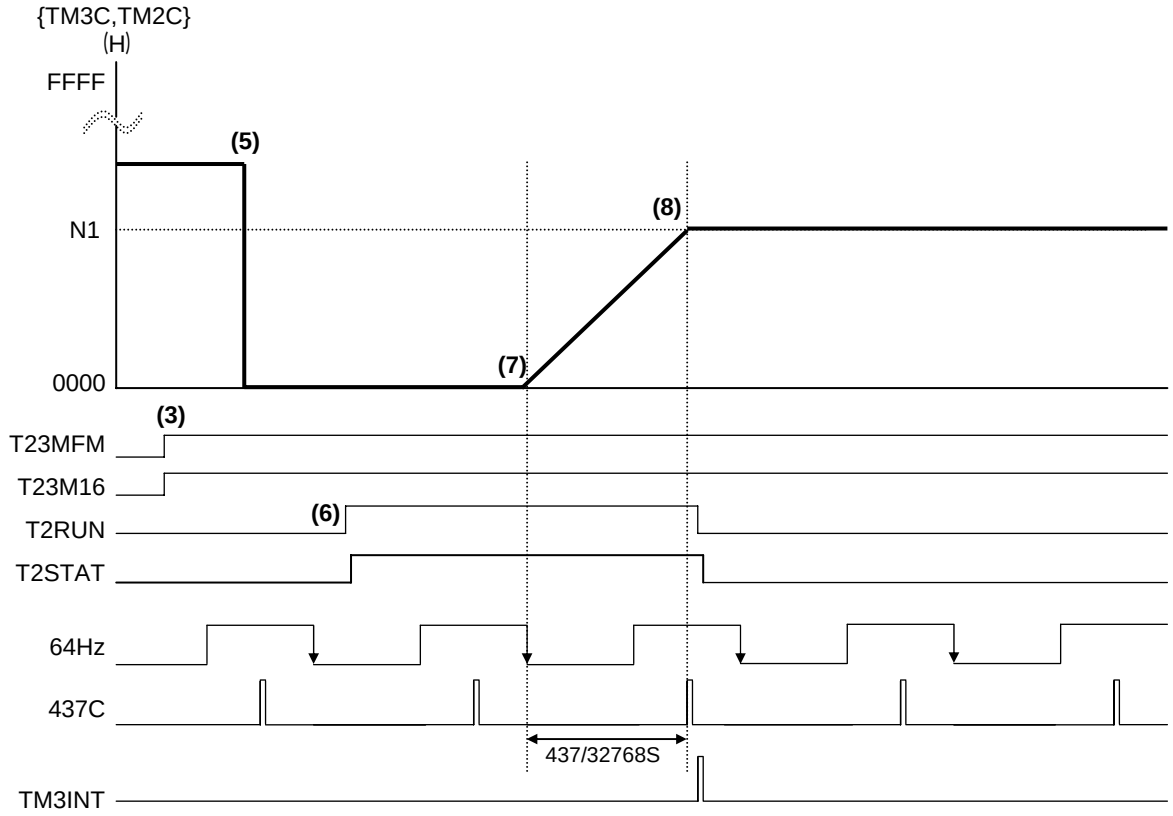


Figure 10-3 Operation Timing in frequency measurement mode

(1) High-speed clock (HSCLK, HTBCLK) has to be in oscillating state by conrolling with FCONn registers. And also select 1/1 devide ratio of the high-speed time base counter by setting HTBDR (High-speed Time Base counter Devide Register) register to 0FH.

(2) Reset both T2RUN bit (bit0 of TM2CON1 register) and T3RUN bit (bit0 of TM3CON1 register) to "0" to stop the timer. And then, check both T2STAT bit (bit7 of TM2CON1 register) and T3STAT bit (bit7 of TM3CON1 register) are "0" for making certain the timer stops.

(3) Set T23MFM bit (bit3 of TM2CON0 register) to "1" (Frequency measurement mode), set T23M16 bit (bit2of TM2CON0 register) to "1" (16bit mode) and set T2CS1-0 bits(bit1/0 of TM2CON0 register) to "01"(HTBCLK mode).

(4) Set "FFH" to both TM2D register and TM3D register.

(5) Clear both TM2C register and TM3C register to "00H".

(6) Set T2RUN bit (bit0 of TM2CON1 register) to "1" to start counting the timer.

(7) On the condition of (T23MFM ビット=="1") & ((TM23M16 ビット=="1") & (T2RUN ビット=="1"), the count-up starts at rising edge of 64Hz clock signal.

(8) The count-up stops at the falling edge of the next timer clock (HTBCLK) after 437C signal becomes "1". Also, at the same time, T2RUN bit and T2STAT bit become "0" and the interrupt signal TM3INT activates.

(9) After checking T2STAT bit or TM3INT interrupt occurs, read out the data (N1) of TM2C register and TM3C register.

For example of utilizing N1, to occur 9600Hz timer interrupt.

Assuming the HTBCLK is 600kHz,

N1 = 600000 * 437 / 32768
= 8001 (Decimal)
= 1F41 (Hexadecimal)
= 0001 1111 0100 0001 (Binary)

As (437 / 32768) sec is equivalent to 128 clocks at 9600Hz (more precisely, 9598Hz), a division of the count N1 by 128 equals frequency ratio (N2) between the frequency of HTBCLK and 9600Hz.
Because $128 = 2^7$, that caluculation can be determined by truncating the righthand seven digits of N1(Binary).

N2 = 8001(Decimal) / 128 (Decimal)
=0001 1111 0 (Binary)
=3E (Hexadecimal)
=62 (Decimal)

This indicates that 9600Hz is about 62 times the cycle of HTBCLK.
Therefore, if 3DH(=3EH-1) set to the timer register and the timer start counting, the cycle of TMnINT interrupt that can occur every 62 counts of HTBCLK is:

tTMnINT = (1 / 600000) * 62 = 0.10333ms (9677Hz)

10.3.3 16-bit timer frequency measurement mode application for setting uart baud-rate

For example, when the target baud-rate is 9600bps and the clock is HSCLK(500kHz), the UART0 baud-rate register (UA0BRTH, UA0BRTL) should be set as follows. See Section 14.3.2. in UART chapter.
UA0BRTH, UA0BRTL = 500000/9600 - 1 = 51 (decimal) = 33(Hexadecimal)

However, actual 500kHz RC oscillation clock has temperature variation and production tolerance, the calculation by using the fixed value of 500kHz can not make accurate baud-rate. To compensate it, count the frequency in the frequency measurement mode to set the baud-rate again before operating UART communication.

After finishing the clock count in the frequency measurement mode, assuming HTBCLK is 451kHz, data of TM2C register and TM3C register will be:

N1 = 451000 * 437 / 32768
= 6014 (Decimal)
= 177E (Hexadecimal)
= 1011101111110 (Binary)

As (437 / 32768) sec is equivalent to 128 clocks at 9600Hz (more precisely, 9598Hz), a division of the count (N1) by 128 equals frequency ratio (N2) between the frequency of HTBCLK and 9600Hz.
For the calculation, the accuracy of baud-rate depends on truncating (1) or rounding (2) the data.

UA0BRTH regiser and UA0BRTL register have to be set as follows. See the previous secntion 10.3.2. and section 14.3.2. in UART chapter.
UA0BRTH, UA0BRTL = (the frequency ratio of HTBCLK and 9600Hz) - 1 = (N1/128)-1 = N2 -1

(1) Round data in caluculation
N1 = 1011101111110 (binary)
N2 = 101111 (binary) = 47 (decimal) = 2F (hexadecimal)
Set N2-1 (= 2E) to UA0BRTH and UA0BRTL registers.
In this case, the acual baud-rate will be 9595.744681.. [bps], so the accuracy = ((9595.744681/9600) -1)* 100= -0.04..[%].

(2) Trancate data in calucuation (the accuracy of baud-rate becomes worse)
N1 = 1011101111110 (binary)
N2 = 101110 (binary) = 46 (decimal) = 2E (hexadecimal)
Set N2-1 (= 2D) to UA0BRTH and UA0BRTL registers.
In this case, the acual baud-rate will be 9804.347826.. [bps], so the accuracy = ((9804.347826/9600) -1)* 100= 2.12..[%].

Table 10-5 shows a baud-rate and theoretical accuracy, and Table 10-6 shows a baud-rate and theoretical accuracy for P Version.

Table 10-5 Baud-rate and theoretical accuracy

Baud-rate[bps]	Data setting to UA0BRTH register and UA0BRTH register	Theoretical accuracy
300	Round off {N1/4 (2bit right-shift) } - (minus) 1.	~ +/- 2%
600	Round off {N1/8 (3bit right-shift) } - (minus) 1.	
1200	Round off {N1/16 (4bit right-shift) } - (minus) 1.	
2400	Round off {N1/32 (5bit right-shift) } - (minus) 1.	
4800	Round off {N1/64 (6bit right-shift) } - (minus) 1.	
9600	Round off {N1/128 (7bit right-shift) } - (minus) 1.	
19200	Round off {N1/256 (8bit right-shift) } - (minus) 1.	+/- 2% ~ 2.5%
38400	Round off {N1/512 (9bit right-shift) } - (minus) 1.	±2.5% ~
57600	Round off {N1/768} - (minus) 1.	

Table 10-6 Baud-rate and theoretical accuracy for P Version

Baud-rate[bps]	Data setting to UA0BRTH register and UA0BRTH register	Theoretical accuracy
300	Round off {N1/4 (2bit right-shift) } - (minus) 1.	~ +/- 2%
600	Round off {N1/8 (3bit right-shift) } - (minus) 1.	
1200	Round off {N1/16 (4bit right-shift) } - (minus) 1.	
2400	Round off {N1/32 (5bit right-shift) } - (minus) 1.	
4800	Round off {N1/64 (6bit right-shift) } - (minus) 1.	
9600	Round off {N1/128 (7bit right-shift) } - (minus) 1.	
19200	Round off {N1/256 (8bit right-shift) } - (minus) 1.	±2.5% ~
38400	Round off {N1/512 (9bit right-shift) } - (minus) 1.	
57600	Round off {N1/768} - (minus) 1.	

Chapter 11

PWM

11. PWM

11.1 Overview

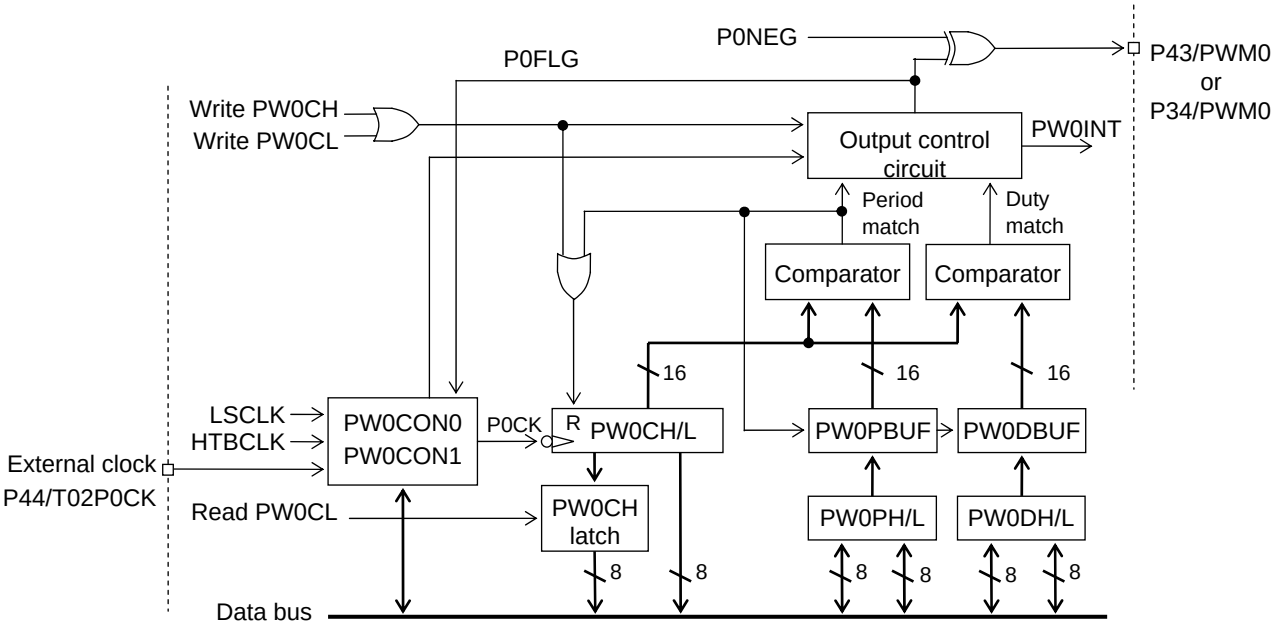
This LSI includes one channel of 16-bit PWM (Pulse Width Modulation).
The PWM output (PWM0) function is assigned to P43(Port 4) and P34(Port 3) as the tertiary function. For the functions of port 4 and port3, see Chapter 21, "Port 4" and Chapter 20, "Port 3".

11.1.1 Features

- The PWM signals with the periods of approximately 488 ns (HTBCLK=4.096MHz) to 2s (@LSCLK=32.768kHz) can be generated and output outside of the LSI.
- The output logic of the PWM signal can be switched to the positive or negative logic.
- At the coincidence of PWM signal period, duties, and period & duty, a PWM interrupt (PW0INT) occurs.
- For the PWM clock, a low-speed clock (LSCLK), a high-speed time base clock (HTBCLK), and an external clock are available.

11.1.2 Configuration

Figure 11 - 1 shows the configuration of the PWM circuit.



PW0PL: PWM0 period register L
PW0PH: PWM0 period register H
PW0PBUF: PWM0 period buffer
PW0DL: PWM0 duty register L
PW0DH: PWM0 duty register H
PW0DBUF: PWM0 duty buffer
PW0CL: PWM0 counter register L
PW0CH: PWM0 counter register H
PW0CON0: PWM0 control register 0
PW0CON1: PWM0 control register 1

Figure 11-1 Configuration of PWM Circuit

11.1.3 List of Pins

Pin name	I/O	Description
P43/PWM0	O	PWM0 output pin Used for the secondary function of the P43 pin.
P34/PWM0	O	PWM0 output pin Used for the secondary function of the P34 pin.

11.2 Description of Registers

11.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F0A0H	PWM0 period register L	PW0PL	PW0P	R/W	8/16	0FFH
0F0A1H	PWM0 period register H	PW0PH		R/W	8	0FFH
0F0A2H	PWM0 duty register L	PW0DL	PW0D	R/W	8/16	00H
0F0A3H	PWM0 duty register H	PW0DH		R/W	8	00H
0F0A4H	PWM0 counter register L	PW0CL	PW0C	R/W	8/16	00H
0F0A5H	PWM0 counter register H	PW0CH		R/W	8	00H
0F0A6H	PWM0 control register 0	PW0CON0	PW0CON	R/W	8/16	00H
0F0A7H	PWM0 control register 1	PW0CON1		R/W	8	40H

11.2.2 PWM0 Period Registers (PW0PL, PW0PH)

Address: 0F0A0H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PW0PL	P0P7	P0P6	P0P5	P0P4	P0P3	P0P2	P0P1	P0P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	1	1	1	1	1	1	1	1

Address: 0F0A1H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PW0PH	P0P15	P0P14	P0P13	P0P12	P0P11	P0P10	P0P9	P0P8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	1	1	1	1	1	1	1	1

PW0PH and PW0PL are special function registers (SFRs) to set the PWM0 periods.

Note:
When PW0PH or PW0PL is set to "0000H", the PWM0 period buffer (PW0PBUF) is set to "0001H".

11.2.3 PWM0 Duty Registers (PW0DL, PW0DH)

	7	6	5	4	3	2	1	0
PW0DL	P0D7	P0D6	P0D5	P0D4	P0D3	P0D2	P0D1	P0D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F0A2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW0DH	P0D15	P0D14	P0D13	P0D12	P0D11	P0D10	P0D9	P0D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F0A3H
Access: R/W
Access size: 8 bits
Initial value: 00H

PW0DH and PW0DL are special function registers (SFRs) to set the duties of PWM0.

Note:
Set PW0DH and PW0DL to values smaller than those to which PW0PH and PW0PL are set.

11.2.4 PWM0 Counter Registers (PW0CH, PW0CL)

	7	6	5	4	3	2	1	0
PW0CL	P0C7	P0C6	P0C5	P0C4	P0C3	P0C2	P0C1	P0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F0A4H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW0DH	P0C15	P0C14	P0C13	P0C12	P0C11	P0C10	P0C9	P0C8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F0A5H
Access: R/W
Access size: 8 bits
Initial value: 00H

PW0CL and PW0CH are special function registers (SFRs) that function as 16-bit binary counters.
When data is written to either PW0CL or PW0CH, PW0CL and PW0CH is set to "0000H". The data that is written is meaningless.
When data is read from PW0CL, the value of PW0CH is latched. When reading PW0CH and PW0CL, use a word type instruction or pre-read PW0CL.

The contents of PW0CH and PW0CL during PWM operation cannot be read depending on the combination of the PWM clock and system clock. Table 11-1 shows PW0CH and PW0CL read enable/disable for each combination of the PWM clock and system clock.

Table 11-1 PW0CH and PW0CL Read Enable/Disable during PWM0 Operation

PWM clock P0CK	System clock SYSCLK	PW0CH and PW0CL read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting, read consecutively PW0CH or PW0CL twice until the last data coincides the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

11.2.5 PWM0 Control Register 0 (PW0CON0)

	7	6	5	4	3	2	1	0
PW0CON0	—	—	—	P0NEG	P0IS1	P0IS0	P0CS1	P0CS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F0A6H
Access: R/W
Access size: 8 bits
Initial value: 00H

PW0CON0 is a special function register (SFR) to control PWM.

[Description of Bits]

- **P0CS1, P0CS0** (bits 1, 0)
  The P0CS1 and P0CS0 bits are used to select the PWM0 operation clocks. LSCLK, HTBCLK, or the external clock (P44/T02P0CK) can be selected.

P0CS1	P0CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited (the PWM circuit does not operate)
1	1	External clock (P44/T02P0CK)

- **P0IS1, P0IS0** (bits 3, 2)
  The P0IS1 and P0IS0 bits are used to select the point at which the PWM0 interrupt occurs. "When the periods coincide", "when the duties coincide", or "when the periods and duties coincide" can be selected.

P0IS1	P0IS0	Description
0	0	When the periods coincide. (Initial value)
0	1	When the duties coincide.
1	*	When the periods and duties coincide.

- **P0NEG** (bit 4)
  The P0NEG bit is used to select the output logic. When the positive logic is selected, the initial value of PWM0 output is "1", and when the negative logic is selected, the initial value of PWM0 output is "0".

P0NEG	Description
0	Positive logic (initial value)
1	Negative logic

11.2.6 PWM0 Control Register 1 (PW0CON1)

	7	6	5	4	3	2	1	0
PW0CON1	P0STAT	P0FLG	—	—	—	—	—	P0RUN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	1	0	0	0	0	0	0

Address: 0F0A7H
Access: R/W
Access size: 8 bits
Initial value: 40H

PW0CON1 is a special function register (SFR) to control PWM0.

[Description of Bits]

- **P0RUN** (bit 0)
  The P0RUN bit is used to control count stop/start of PWM0.

P0RUN	Description
0	Stops counting. (Initial value)
1	Starts counting.

- **P0FLG** (bit 6)
  The P0FLG bit is used to read the output flag of PWM0.
  This bit is set to "1" when write operation to PW0CH or PW0CL is performed,

P0FLG	Description
0	PWM0 output flag = "0"
1	PWM0 output flag = "1" (initial value)

- **P0STAT** (bit 7)
  The P0STAT bit indicates "counting stopped or "counting in progress" of PWM0.

P0STAT	Description
0	Counting stopped. (Initial value)
1	Counting in progress.

11.3 Description of Operation

The PWM0 counter registers (PW0CH, PW0CL) are set to an operating state (P0STAT is set to "1") on the first falling edge of the PWM clock (P0CK) that are selected by the PWM0 control register 0 (PW0CON0) when the P0RUN bit of PWM0 control register 1 (PW0CON1) is set to "1" and increment the count value on the 2nd falling edge.

When the count value of PWM0 counter registers and the value of the PWM0 duty buffer (PW0DBUF) coincide, the PWM flag (P0FLG) is set to "0" on the next timer clock falling edge of P0CK.
When the count value of PWM0 counter registers and the value of the PWM0 period buffer (PW0PBUF) coincide, the PWM flag (P0FLG) is set to "1" on the next falling edge of P0CK and PWM0 counter registers is set to "0000H" and incremental counting continues. At the same time, the value of the PWM0 duty register (PW0DH, PW0DL) is transferred to the PWM0 duty buffer (PW0DBUF) and the value of PWM0 period register (PW0PH, PW0PL) to the PWM0 period buffer (PW0PBUF).

When the P0RUN bit is set to "0", PWM0 counter registers stop counting after counting once the falling of the PWM clock (P0CK). Confirm that PW0CH and PW0CL are stopped by checking that the PnSTAT bit of the PWM0 control register 1 (PW0CON1) is "0". When the P0RUN bit is set to "1" again, PWM0 counter registers restarts incremental counting from the previous value on the falling edge of P0CK.

To initialize PWM0 counter registers to "0000H", perform write operation in either of PW0CH or PW0CL. At that time, P0FLG is also set to "1". When data is written in the PWM0 duty register (PW0DH, PW0DL) during count stop (P0RUN is in a "1" state), the data is transferred to the PWM0 duty buffer (PW0DBUF) and when data is written in the PWM0 period register (PW0PH, PW0PL), the data is transferred to the PWM0 period buffer (PW0PBUF).

The PWM clock, the point at which an interrupt of PWM0 occurs, and the logic of the PWM output are selected by PWM0 control register 0 (PW0CN0).

The period of the PWM0 signal (TPWP) and the first half duration (TPWD) of the duty are expressed by the following equations.

$$T_{PWP} = \frac{PW0P + 1}{P0CK\ (Hz)}$$

$$T_{PWP} = \frac{PW0D + 1}{P0CK\ (Hz)}$$

PW0P: PWM0 period registers (PW0PH, PW0PL) setting value (0001H to 0FFFFH)
PW0D: PWM0 duty registers (PW0DH, PW0DL) setting value (0000H to 0FFFEH)
P0CK: Clock frequency selected by the PWM0 control register 0 (PW0CON0)

After the P0RUN bit is set to "1", counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. The PWM interrupt period from the second time is fixed.
Figure 11-2 shows the operation timing of PWM0.

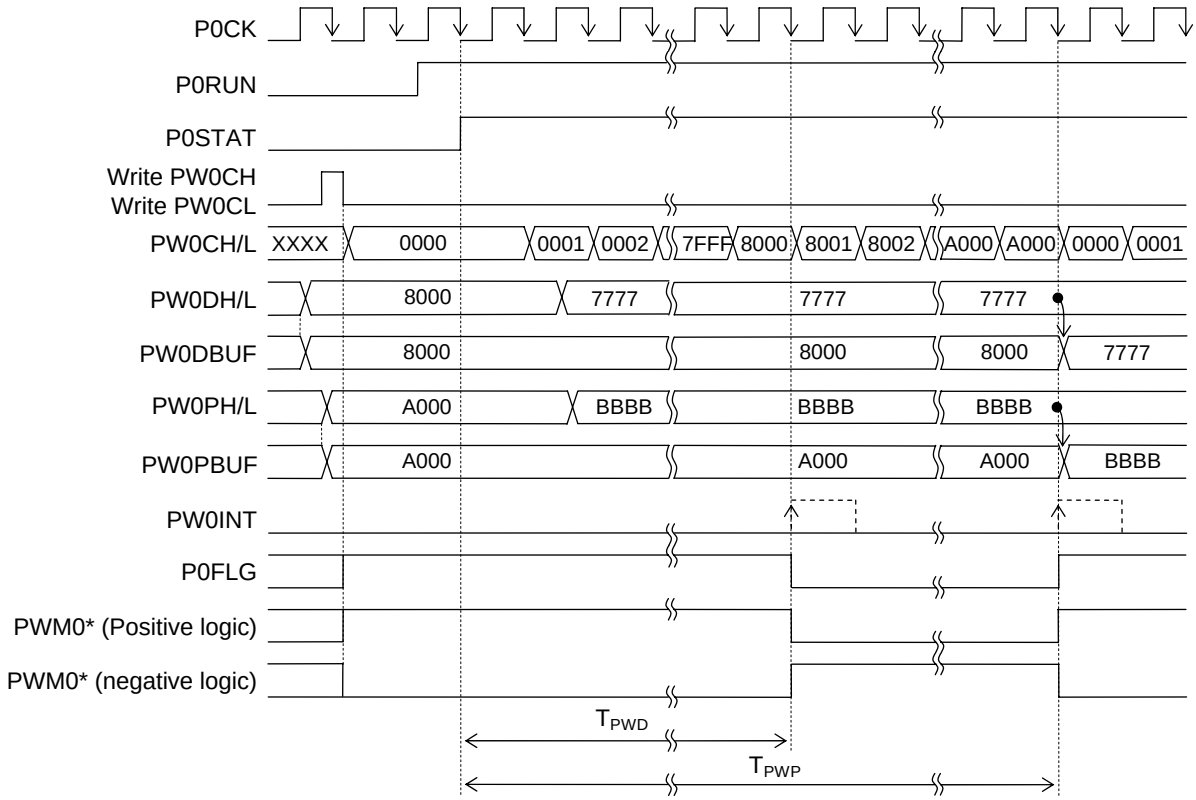


Figure 11-2 (1/2) Operation Timing Diagram of PWM0

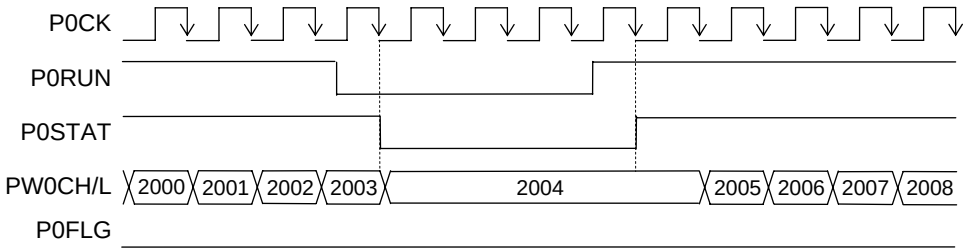


Figure 11-2 (2/2) Operation Timing Diagram of PWM0

Note:
Even if "0" is written to the P0RUN bit, counting operation continues up to the falling edge (the PWM0 status flag (P0STAT) is in a "1" state) of the next PWM clock pulse. Therefore, the PWM0 interrupt (PW0INT) may occur.

11.4 Specifying port registers

When you want to make sure the PWM function is working, please check related port registers are specified. See Chapter 21, "Port 4" and Chapter 20, "Port 3" for detail about the port registers.

11.4.1 Functioning P43 (PWM0) as the PWM output

Set P43MD1 bit (bit3 of P4MOD1 register) to "1" and set P43MD0 bit (bit3 of P4MOD0 register) to "0", for specifying the PWM output as the tertiary function of P43.

Reg. name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	**P43MD1**	P42MD1	P41MD1	P40MD1
Data	*	*	*	*	**1**	*	*	*

Reg. name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47MD0	P46MD0	P45MD0	P44MD0	**P43MD0**	P42MD0	P41MD0	P40MD0
Data	*	*	*	*	**0**	*	*	*

Set P43C1 bit (bit3 of P4CON1 register) to "1", set P43C0 bit(bit3 of P4CON0 register) to "1" and set P43DIR bit(bit3 of P4DIR register) to "0", for specifying the P43 as CMOS output.

Reg. name	P4CON1 register (Address: 0F223H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47C1	P46C1	P45C1	P44C1	**P43C1**	P42C1	P41C1	P40C1
Data	*	*	*	*	**1**	*	*	*

Reg. name	P4CON0 register (Address: 0F222H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47C0	P46C0	P45C0	P44C0	**P43C0**	P42C0	P41C0	P40C0
Data	*	*	*	*	**1**	*	*	*

Reg. name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	**P43DIR**	P42DIR	P41DIR	P40DIR
Data	*	*	*	*	**0**	*	*	*

Data of P43D bit (bit3 of P4D register) does not affect to the PWM output function, so don't care the data for the function.

Reg. name	P4D register (Address: 0F220H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47D	P46D	P45D	P44D	**P43D**	P42D	P41D	P40D
Data	*	*	*	*	******	*	*	*

* : Bit not related to the PWM function
** : Don't care the data.

11.4.2 Functioning P34 (PWM0) as the PWM output

Set P34MD1 bit (bit4 of P3MOD1 register) to "1" and set P34MD0 bit (bit4 of P3MOD0 register) to "0", for specifying the PWM output as the tertiary function of P34.

Reg. name	P3MOD1 register (Address: 0F21DH)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	-	-	P35MD1	**P34MD1**	P33MD1	P32MD1	P31MD1	P30MD1
Data	-	-	*	**1**	*	*	*	*

Reg. name	P3MOD0 register (Address: 0F21CH)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	-	-	P35MD0	**P34MD0**	P33MD0	P32MD0	P31MD0	P30MD0
Data	-	-	*	**0**	*	*	*	*

Set P34C1 bit (bit4 of P3CON1 register) to "1", set P34C0 bit(bit4 of P3CON0 register) to "1" and set P34DIR bit(bit4 of P3DIR register) to "0", for specifying the P34 as CMOS output.

Reg. name	P3CON1 register (Address: 0F21BH)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	-	-	P35C1	**P34C1**	P33C1	P32C1	P31C1	P30C1
Data	-	-	*	**1**	*	*	*	*

Reg. name	P3CON0 register (Address: 0F21AH)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	-	-	P35C0	**P34C0**	P33C0	P32C0	P31C0	P30C0
Data	-	-	*	**1**	*	*	*	*

Reg. name	P3DIR register (Address: 0F219H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	-	-	P35DIR	**P34DIR**	P33DIR	P32DIR	P31DIR	P30DIR
Data	-	-	*	**0**	*	*	*	*

Data of P34D bit (bit4 of P3D register) does not affect to the PWM output function, so don't care the data for the function.

Reg. name	P3D register (Address: 0F218H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	-	-	P35D	**P34D**	P33D	P32D	P31D	P30D
Data	-	-	*	******	*	*	*	*

- : Bit does not exist.
* : Bit not related to the PWM function
** : Don't care the data.

Chapter 12

Watchdog Timer

12. Watchdog Timer

12.1 Overview

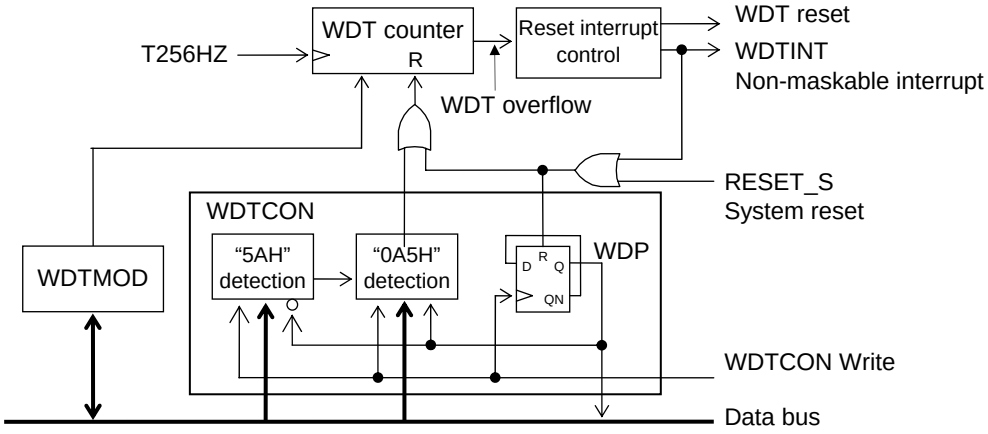
This LSI incorporates a watchdog timer (WDT) that operates at a system reset unconditionally (free-run operation) in order to detect an undefined state of the MCU and return from that state.
If the WDT counter overflows due to the failure of clearing of the WDT counter within the WDT overflow period, the watchdog timer requests a WDT interrupt (non-maskable interrupt). When the second overflow occurs, the watchdog timer generates a WDT reset signal and shifts the mode to a system reset mode.
For interrupts see Chapter 5, "Interrupts," and for WDT interrupt see Chapter 3, "Reset Function".

12.1.1 Features

- Free running (cannot be stopped)
- One of four types of overflow periods (125ms, 500ms, 2s, and 8s) selectable by software
- Non-maskable interrupt by the first overflow
- Reset generated by the second overflow

12.1.2 Configuration

Figure 12-1 shows the configuration of the watchdog timer.



WDTCON : Watchdog timer control register
WDTMOD : Watchdog timer mode register

Figure 12-1 Configuration of Watchdog Timer

12.2 Description of Registers

12.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F00EH	Watchdog timer control register	WDTCON	—	R/W	8	00H
0F00FH	Watchdog timer mode register	WDTMOD	—	R/W	8	02H

12.2.2 Watchdog Timer Control Register (WDTCON)

Address: 0F00EH
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
WDTCON	d7	d6	d5	d4	d3	d2	d1	WDP/d0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

WDTCON is a special function register (SFR) to clear the WDT counter.
When WDTCON is read, the value of the internal pointer (WDP) is read from bit 0.

[Description of Bits]

- **WDP/d0** (bit 0)
  The value of the internal pointer (WDP) is read from this bit. The WDP is reset to "0" at the system reset or Watch Dog Timer overflow and is inverted every writing to WDTCON.

- **d7-d0** (bits 7-0)
  This bit is used to write data to clear the WDT counter. Write "5AH" on the condition of WDP is "0" and write "0A5H" on the condition of WDP is "1".

Note:
When the WDT interrupt (WDTINT) occurs by the first WDT counter overflow, the counter and the internal pointer (WDP) are initialiaed for a half cycle of low speed clock (about 15us). During the time period that they are initialized, writing to WDTCON is disable and the logic of WDP does not change. Therefore, in the case of that you have program codes handle to clear the WDT when the first overflow WDT interrupt occurs and also the codes run at high-speed system clock, please check the WDP gets reversed after writing to WDTCON to see if the writing was surely successful. For example of the program code, see Section 12.3.1, "Handling example when you do not want to use the watch dog timer".

12.2.3 Watchdog Timer Mode Register (WDTMOD)

Address: 0F00FH
Access: W
Access size: 8 bits
Initial value: 02H

	7	6	5	4	3	2	1	0
WDTMOD	—	—	—	—	—	—	WDT1	WDT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	1	0

WDTMOD is a special function register to set the overflow period of the watchdog timer.

[Description of Bits]

- **WDT1-0** (bits 1-0)
  These bits are used to select an overflow period of the watchdog timer.
  The WDT1 and WDT0 bits set a overflow period (TWOV) of the WDT counter. One of 125ms, 500ms, 2s, and 8s can be selected.

WDT1	WDT0	Description
0	0	125 ms
0	1	500 ms
1	0	2 s (initial value)
1	1	8 s

12.3 Description of Operation

The WDT counter starts counting after the system reset has been released and the low-speed clock oscillation start..
Write "5AH" when the internal pointer (WDP) is "0"and then the WDT counter is cleared by writing "0A5H" when WDP is "1".
WDP is reset to "0" at the time of system reset or when the WDT counter overflows and is inverted whenever data is written to WDTCON.
When the WDT counter cannot be cleared within the WDT counter overflow period (T_{WOV}), a watchdog timer interrupt (WDTINT) occurs. If the WDT counter is not cleared even by the software processing performed following the watchdog timer interrupt and overflow occurs again, WDT reset occurs and the mode shifts to a system reset mode.
For the overflow period (TWOV) of the WDT counter, one of 125ms, 500ms, 2s, and 8s can be selected by the watchdog mode register (WDTMOD).
Clear the WDT counter within the clear period of the WDT counter shown in Table 12-1.

Table 12-1 Clear Period of WDT Counter

WDT1	WDT0	T_{WOV}	T_{WCL}
0	0	125 ms	Approx. 121 ms
0	1	500 ms	Approx. 496 ms
1	0	2000 ms	Approx. 1996 ms
1	1	8000 ms	Approx. 7996 ms

Figure 12-2 shows an example of watchdog timer operation.

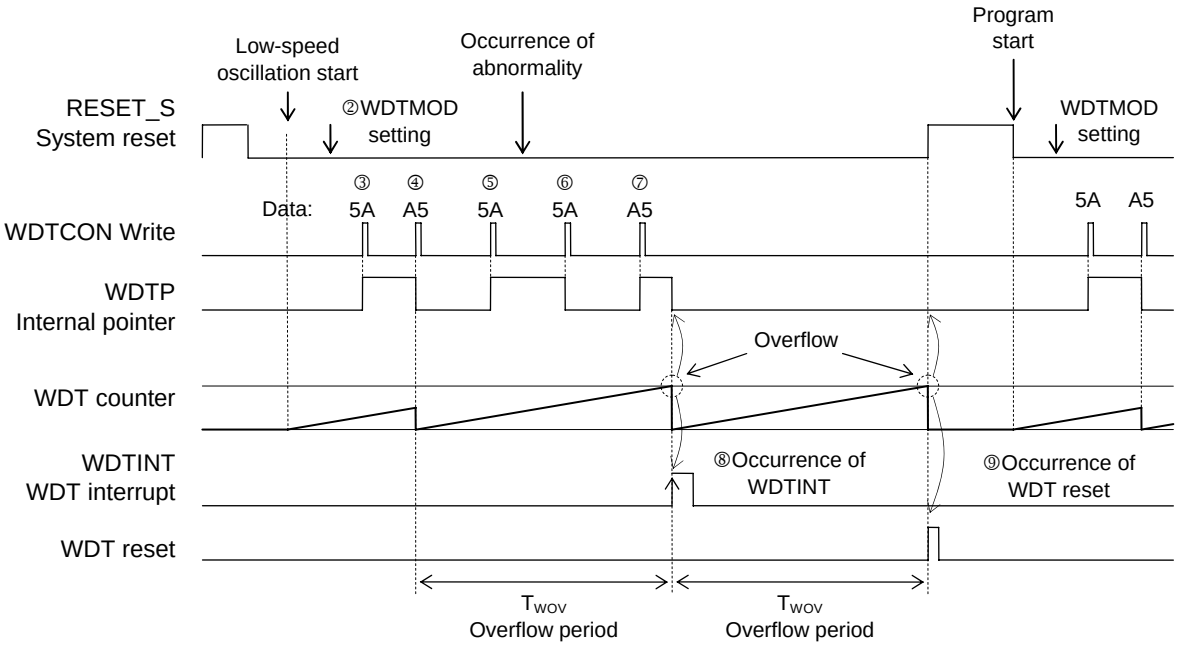


Figure 12-2 Example of Watchdog Timer Operation

① The WDT counter starts counting after the system reset has been released and the low-speed clock oscillation start.
② The overflow period of the WDT counter (TWOV) is set to WDTMOD.
③ "5AH" is written to WDTCON. (Internal pointer 0→1)
④ "0A5H" is written to WDTCON and the WDT counter is cleared. (Internal pointer 1→0)
⑤ "5AH" is written o WDTCON. (Internal pointer 0→1)
⑥ When "5AH" is written to WDTCON after the occurrence of abnormality, it cannot be accepted as the internal pointer is set to "1". (Internal pointer 1→0)
⑦ Although "0A5H" is written to WDTCON, the WDT counter is not cleared since the internal pointer is "0" and the writing of "5AH" is not accepted in ⑥. (Internal pointer 0→1)
⑧ The WDT counter overflows and a watchdog timer interrupt request (WDTINT) is generated. In this case,, the WDT counter and the internal pointer (WDP) are initialiaed for a half cycle of low speed clock (about 15.26us).
⑨ If the WDT counter is not cleared even by the software processing performed following a watchdog timer interrupt and the WDT counter overflows again, WDT reset occurs and the mode is shifted to a system reset mode.

Note:
- In STOP mode, the watchdog timer operation also stops.
- In HALT mode, the watchdog timer operation does not stop. When the WDT interrupt occurs, the HALT mode is released.
- The watchdog timer cannot detect all the abnormal operations. Even if the CPU loses control, the watchdog timer cannot detect the abnormality in the operation state in which the WDT counter is cleared.

12.3.1 Handling example when you do not want to use the watch dog timer

WDT counter is a free-run counter that starts count-up automatically after the system reset released and the low-speed clock (LSCLK) starts oscillating. If the WDT counter gets overflow, the WDT non-maskable interrupt occurs and then a system reset occurs. Therefore, it is needed to clear the WDT counter even if you do not want to use the WDT as a fale-safe function.
See following example programming codes to clear the WDT counter in the interrupt routine.

Example programming code:

```
__DI();                    // Disable multi-interrupts
do
{
   WDTCON = 0x5a;
} while(WDP != 1)
WDTCON = 0xa5;
__EI();
```

Chapter 13

Synchronous Serial Port

13. Synchronous Serial Port

13.1 Overview

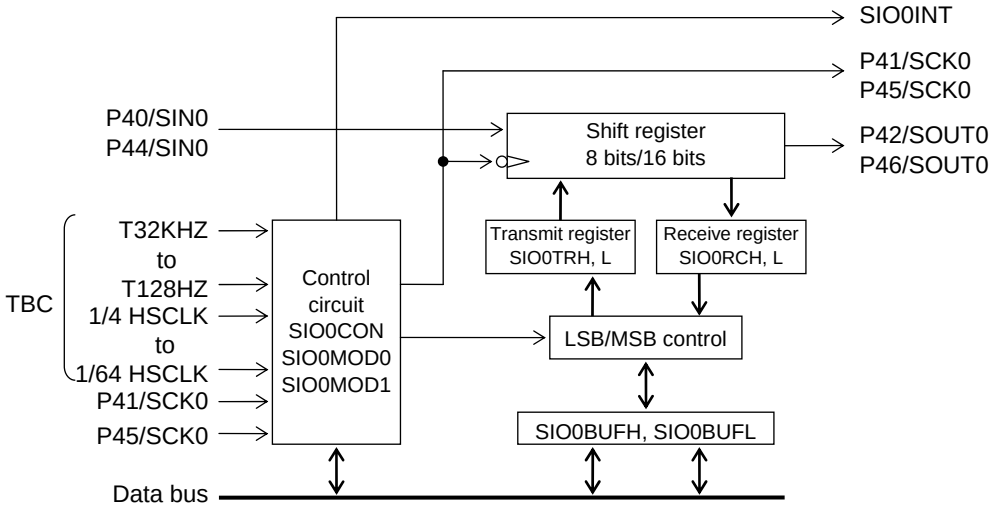
This LSI includes one channel of the 8/16-bit synchronous serial port (SSIO) and can also be used to control the device incorporated with the SPI interface by using one GPIO as the chip enable pin.
For the input clock, see Chapter 6, "Clock Generation Circuit".
When the synchronous serial port is used, the tertiary functions of port 4 must be set. For the tertiary functions of port 4, see Chapter 21, "Port 4".

13.1.1 Features

- Master or slave selectable
- MSB first or LSB first selectable
- 8-bit length or 16-bit length selectable fro the data length

13.1.2 Configuration

Figure 13-1 shows the configuration of the synchronous serial port.



SIO0BUFL: Serial port transmit/receive buffer L
SIO0BUFH: Serial port transmit/receive buffer H
SIO0CON: Serial port control register
SIO0MOD0: Serial port mode register 0
SIO0MOD1: Serial port mode register 1

Figure 13-1 Configuration of Synchronous Serial Port

13.1.3 List of Pins

Pin name	I/O	Description
P40/SIN0 P44/SIN0	I	Receive data input. Used for the tertiary function of the P40 and P44 pins.
P41/SCK0 P45/SCK0	I/O	Synchronous clock input/output. Used for the tertiary function of the P41 and P45 pins.
P42/SOUT0 P46/SOUT0	O	Transmit data output. Used for the tertiary function of the P42 and P46 pins.

13.2 Description of Registers

13.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F280H	Serial port 0 transmit/receive buffer L	SIO0BUFL	SIO0BUF	R/W	8/16	00H
0F281H	Serial port 0 transmit/receive buffer H	SIO0BUFH		R/W	8	00H
0F282H	Serial port 0 control register	SIO0CON	—	R/W	8	00H
0F284H	Serial port 0 mode register 0	SIO0MOD0	SIO0MOD	R/W	8/16	00H
0F285H	Serial port 0 mode register 1	SIO0MOD1		R/W	8	00H

13.2.2 Serial Port Transmit/Receive Buffers (SIO0BUFL, SIO0BUFH)

Address: 0F280H
Access: R/W
Access size: 8 bits/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0BUFL	S0B7	S0B6	S0B5	S0B4	S0B3	S0B2	S0B1	S0B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F281H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0BUFH	S0B15	S0B14	S0B13	S0B12	S0B11	S0B10	S0B9	S0B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0BUFL and SIO0BUFH are special function registers (SFRs) to write transmit data and to read receive data of the synchronous serial port.
When data is written in SIO0BUFL and SIO0BUFH, the data is written in the transmit registers (SIO0TRL and SIO0TRH) and when data is read from SIO0BUFL and SIO0BUFH, the contents of the receive registers (SIO0RCL and SIO0RCH) are read.

13.2.3 Serial Port Control Register (SIO0CON)

Address: 0F282H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0CON	—	—	—	—	—	—	—	S0EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0CON is a special function register (SFR) to control the synchronous serial port.

[Description of Bits]

- **S0EN** (bit 0)
  The S0EN bit is used to specify start of synchronous serial communication. Writing a "1" to this bit starts 8-/16-bit data communication. This bit is set to "0" automatically when 8-/16-bit data communication is terminated.
  The S0EN bit is set to "0" at a system reset.

S0EN	Description
0	Stops communication. (Initial value)
1	Starts communication

13.2.4 Serial Port Mode Register 0 (SIO0MOD0)

Address: 0F284H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0MOD0	—	—	—	—	S0LG	S0MD1	S0MD0	S0DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0MOD0 is a special function register (SFR) to set mode of the synchronous serial port.

[Description of Bits]

- **S0DIR** (bit 0)
  The S0DIR is used to select LSB first or MSB first.

S0DIR	Description
0	LSB first (initial value)
1	MSB first

- **S0MD1, S0MD0** (bits 2, 1)
  The S0MD1 and S0MD0 bits are used to select transmit, receive, or transmit/receive mode of the synchronous serial port.

S0MD1	S0MD0	Description
0	0	Stops transmission/reception (initial value)
0	1	Receive mode
1	0	Transmit mode
1	1	Transmit/receive mode

- **S0LG** (bit 3)
  The S0LG bit is used to specify the bit length of the transmit/receive buffer, 8-bit or 16-bit length.
  The S0LG bit is set to "0" at a system reset.

S0LG	Description
0	8-bit length (initial value)
1	16-bit length

Note:
- Do not change any of the SIO0MOD0 register settings during transmission/reception.
- When the synchronous serial port is used, the tertiary functions of GPIO must be set. For the tertiary functions of Port 4, see Chapter 21, "Port 4".

13.2.5 Serial Port Mode Register 1 (SIO0MOD1)

Address: 0F285H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0MOD1	—	—	—	S0CKT	—	S0CK2	S0CK1	S0CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0MOD1 is a special function register (SFR) to set mode of the synchronous serial port.

[Description of Bits]

- **S0CK2 to S0CK0** (bits 2 to 0)
  The S0CK2 to S0CK0 bits are used to select the transfer clock of the synchronous serial port. When the internal clock is selected, this LSI is set to master mode and when the external clock is selected, it is set to slave mode.

S0CK2	S0CK1	S0CK0	Description
0	0	0	32 KHz (initial value)
0	0	1	16 KHz
0	1	0	1/4 HSCLK
0	1	1	1/8 HSCLK
1	0	0	1/16 HSCLK
1	0	1	1/32 HSCLK
1	1	0	External clock 0 (P41/SCK0)
1	1	1	External clock 1 (P45/SCK0)

- **S0CKT** (bit 4)
  The S0CKT bit is used to select a tansfer clock output phase.

S0CKT	Description
0	Clock type 0: Clock is output with a "H" level being the default. (Initial value)
1	Clock type 1: Clock is output with a "L" level being the default.

13.3 Description of Operation

13.3.1 Transmit Operation

When "1" is written to the S0MD1 bit and "0" is written to the S0MD0 bit of the serial mode register (SIO0MOD0), this LSI is set to a transmit mode.
When transmit data is written to the serial port transmit /receive buffer (SIO0BUFL and H) and the S0EN bit of the serial port control register (SIO0CON) is set to "1", transmission starts. When transmission of 8/16-bit data terminates, a synchronous serial port interrupt (SIO0INT) occurs and the S0EN bit is set to "0".
Transmit data is output from the tertiary function pins (P42/SOUT0 or P46/SOUT0) of GPIO.
When an internal clock is selected in the serial port mode register (SIO0MOD1), the LSI is set to a master mode and when an external clock (P41/SCK0 or P45/SCK0) is selected, the LSI is set to a slave mode.
The serial port mode register (SIO0MOD0) enables selection of MSB first/LSB first.
The transmit data output pin (P42/SOUT0 or P46/SOUT0) and transfer clock input/output pin (P41/SCK0 or P45/SCK0) must be set to the tertiary functions.
Figures 13-2 and 13-3 show the transmit operation waveforms of the synchronous serial ports for clock type 0 and clock type 1, respectively (8-bit length, LSB first, clock types 0 and 1).

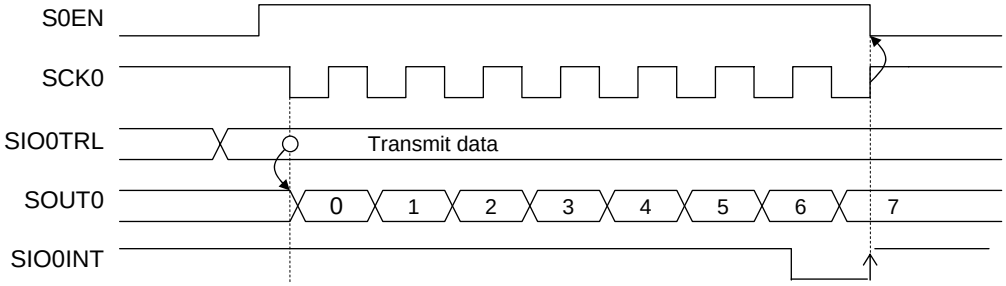


Figure 13-2 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8-bit Length, LSB first)

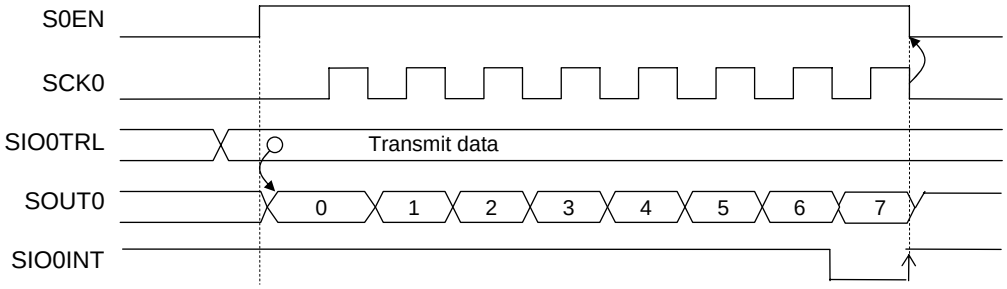


Figure 13-3 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8-bit Length, LSB first)

13.3.2 Receive Operation

When "0" is written to the S0MD1 bit and "1" is written to the S0MD0 bit of the serial mode register (SIO0MOD0), this LSI is set to a receive mode.
When the S0EN bit of the serial port control register (SIO0CON) is set to "1", reception starts. When reception of 8/16-bit data terminates, a synchronous serial port interrupt (SIO0INT) occurs and the S0EN bit is set to "0".
Receive data is input from the tertiary function pins (P40/SIN0 or P44/SIN0) of GPIO.
When an internal clock is selected in the serial port mode register (SIO0MD1), the LSI is set to a master mode and when an external clock (P41/SCK0 or P45/SCK0) is selected, the LSI is set to a slave mode.
The serial port mode register (SIO0MOD0) enables selection of MSB first or LSB first.
The receive data input pin (P40/SIN0 or P44/SIN0) and transfer clock input/output pin (P41/SCK0 or P45/SCK0) must be set to the tertiary function.
Figures 13-4 and 13-5 show the receive operation waveforms of the synchronous serial ports for clock type 0 and clock type 1, respectively (8-bit length, MSB first, clock types 0 and 1).

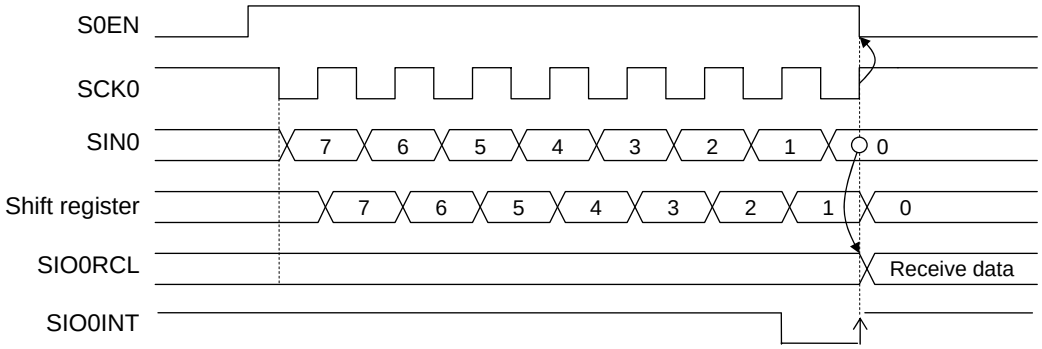


Figure 13-4 Receive Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8-bit Length, MSB first)

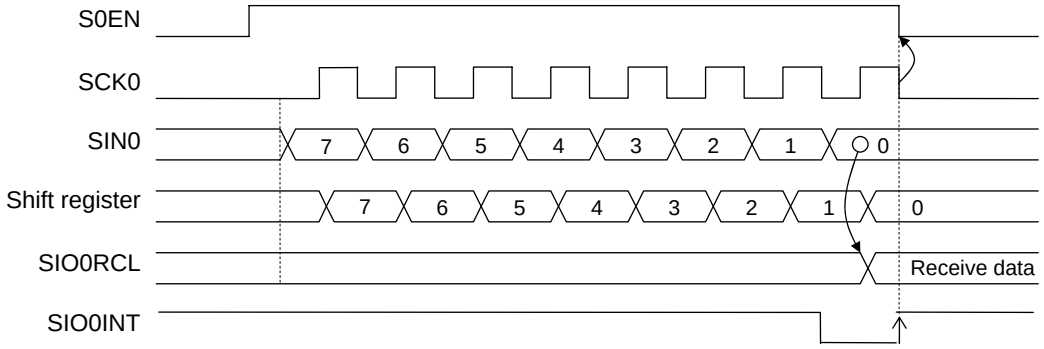


Figure 13-5 Receive Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8-bit Length, MSB first)

Note:
When the SOUT0 pin is set to the tertiary function output in receive mode, a "H" level is output from the SOUT0 output pin.

13.3.3 Transmit/Receive Operation

When "1" is written to the S0MD1 bit and "1" is written to the S0MD0 bit of the serial mode register (SIO0MOD0), this LSI is set to a transmit/receive mode.
When the S0EN bit of the serial port control register (SIO0CON) is set to "1", transmission/reception starts. When transmission/reception of 8/16-bit data terminates, a synchronous serial port interrupt (SIO0INT) occurs and the S0EN bit is set to "0".
Receive data is input from the tertiary function pins (P40/SIN0 or P44/SIN0) of GPIO, and transmit data is output from the tertiary function pins (P42/SOUT0 or P46/SOUT0) of GPIO
When an internal clock is selected in the serial port mode register (SIO0MD1), the LSI is set to a master mode and when an external clock (P41/SCK0 or P45/SCK0) is selected, the LSI is set ot a slave mode.
The serial port mode register (SIO0MOD0) enables selection of MSB first or LSB first.
The receive data input pin (P40/SIN0 or P44/SIN0), the transmit data output pin (P42/SOUT0 or P46/SOUT0), and transfer clock input/output pin (P41/SCK0 or P45/SCK0) must be set to the tertiary function.
Figure 13-6 shows the transmit/receive operation waveforms of the synchronous serial port (16-bit length, LSB first, clock types 0).

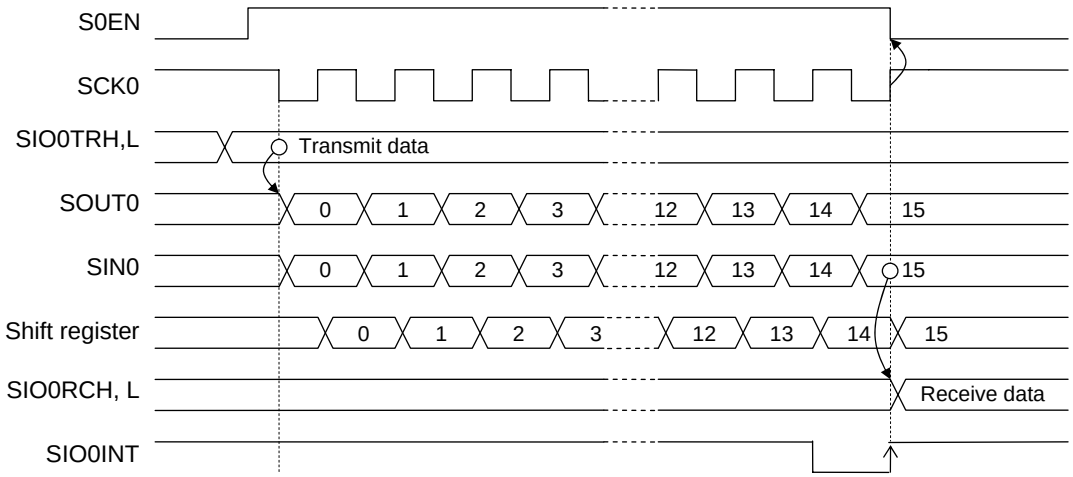


Figure 13-6 Transmit/Receive Operation Waveforms of Synchronous Serial Port (16-bit Length, LSB first, Clock Type 0)

13.4 Specifying port registers

When you want to make sure the SSIO function is working, please check related port registers are specified. See Chapter 21, "Port 4" for detail about the port registers.

13.4.1 Functioning P42 (SOUT0), P41 (SCK0) and P40 (SIN0) as the SSIO/ "Master mode"

Set P42MD1-P40MD1 bits(bit2-bit0 of P4MOD1 register) to "1" and set P42MD0-P40MD0(bit2-bit0 of P4MOD0 register) to "0", for specifying the SSIO as the secondary function of P42, P41 and P40.

Reg. name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	4	**3**	**2**	**1**	**0**
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	P43MD1	**P42MD1**	**P41MD1**	**P40MD1**
Data	*	*	*	*	*	**1**	**1**	**1**

Reg. name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	**P42MD0**	**P41MD0**	**P40MD0**
Data	*	*	*	*	*	**0**	**0**	**0**

Set P42C1-P41MC1 bits(bit2-bit1 of P4CON1 register) to "1", set P42C0-P41C0 bits(bit2-bit1 of P4CON0 register) to "1", and set P42DIR-P41DIR bits(bit2-bit1 of P4DIR register) to "0", for specifying the P42-P41 as CMOS output.
Set P40DIR bit(bit0 of P4DIR register) to "1" for specifying the P40 as an input pin.
Data setting to P40C1 bit and P40C0 bit depend on the application circuit connected to P40.

Reg. name	P4CON1 register (Address: 0F223H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47C1	P46C1	P45C1	P44C1	P43C1	**P42C1**	**P41C1**	**P40C1**
Data	*	*	*	*	*	**1**	**1**	**$**

Reg. name	P4CON0 register (Address: 0F222H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47C0	P46C0	P45C0	P44C0	P43C0	**P42C0**	**P41C0**	**P40C0**
Data	*	*	*	*	*	**1**	**1**	**$**

Reg. name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	P43DIR	**P42DIR**	**P41DIR**	**P40DIR**
Data	*	*	*	*	*	**0**	**0**	**1**

Data of P42D-P40D bits (bit2-0 of P4D register) do not affect to the SSIO function, so don't care the data for the function.

Reg. name	P4D register (Address: 0F220H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47D	P46D	P45D	P44D	P43D	**P42D**	**P41D**	**P40D**
Data	*	*	*	*	*	******	******	******

* : Bit not related to the SSIO function
** : Don't care the data
$: Arbitrarily

13.4.2 Functioning P42 (SOUT0), P41 (SCK0) and P40 (SIN0) as the SSIO/ "Slave mode"

Set P42MD1-P40MD1 bits(bit2-bit0 of P4MOD1 register) to "1" and set P42MD0-P40MD0(bit2-bit0 of P4MOD0 register) to "0", for specifying the SSIO as the secondary function of P42, P41 and P40. They are the same setting as those in the case of master mode.

Reg. name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	4	**3**	**2**	**1**	**0**
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	P43MD1	**P42MD1**	**P41MD1**	**P40MD1**
Data	*	*	*	*	*	**1**	**1**	**1**

Reg. name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	**P42MD0**	**P41MD0**	**P40MD0**
Data	*	*	*	*	*	**0**	**0**	**0**

Set P42C1 bit(bit2 of P4CON1 register) to "1", set P42C0 bit(bit2 of P4CON0 register) to "1", and set P42DIR bit(bit2 of P4DIR register) to "0", for specifying the P42 as CMOS output.

Set P41DIR-P40DIR bits(bit1-0 of P4DIR register) to "1" for specifying the P41 and P40 as input pins.

Data setting to P41C1 bit, P40C1 bit, P41C0 bit and P40C0 bit, depend on the application circuit connected to P41 and P40.

Reg. name	P4CON1 register (Address: 0F223H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47C1	P46C1	P45C1	P44C1	P43C1	**P42C1**	**P41C1**	**P40C1**
Data	*	*	*	*	*	**1**	**$**	**$**

Reg. name	P4CON0 register (Address: 0F222H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47C0	P46C0	P45C0	P44C0	P43C0	**P42C0**	**P41C0**	**P40C0**
Data	*	*	*	*	*	**1**	**$**	**$**

Reg. name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	P43DIR	**P42DIR**	**P41DIR**	**P40DIR**
Data	*	*	*	*	*	**0**	**1**	**1**

Data of P42D-P40D bits (bit2-0 of P4D register) do not affect to the SSIO function, so don't care the data for the function.

Reg. name	P4D register (Address: 0F220H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47D	P46D	P45D	P44D	P43D	**P42D**	**P41D**	**P40D**
Data	*	*	*	*	*	******	******	******

* : Bit not related to the SSIO(using P42, P41, and P40) function
** : Don't care the data
$: Arbitrarily

13.4.3 Functioning P46 (SOUT0), P45 (SCK0) and P44 (SIN0) as the SSIO/ "Master mode"

Set P46MD1-P44MD1 bits(bit6-bit4 of P4MOD1 register) to "1" and set P46MD0-P44MD0(bit6-bit4 of P4MOD0 register) to "0", for specifying the SSIO as the secondary function of P46, P45 and P44.

Reg. name	P4MOD1 register (Address: 0F225H)							
Bit	7	**6**	**5**	**4**	**3**	2	1	0
Bit name	P47MD1	**P46MD1**	**P45MD1**	**P44MD1**	P43MD1	P42MD1	P41MD1	P40MD1
Data	*	**1**	**1**	**1**	*	*	*	:

Reg. name	P4MOD0 register (Address: 0F224H)							
Bit	7	**6**	**5**	**4**	3	2	1	0
Bit name	P47MD0	**P46MD0**	**P45MD0**	**P44MD0**	P43MD0	P42MD0	P41MD0	P40MD0
Data	*	**0**	**0**	**0**	*	*	*	*

Set P46C1-P45MC1 bits(bit6-bit5 of P4CON1 register) to "1", set P46C0-P45C0 bits(bit6-bit5 of P4CON0 register) to "1", and set P46DIR-P45DIR bits(bit6-bit5 of P4DIR register) to "0", for specifying the P46-P45 as CMOS output.
Set P44DIR bit(bit4 of P4DIR register) to "1" for specifying the P44 as an input pin.
Data setting to P44C1 bit and P44C0 bit depend on the application circuit connected to P44.

Reg. name	P4CON1 register (Address: 0F223H)							
Bit	7	**6**	**5**	**4**	3	2	1	0
Bit name	P47C1	**P46C1**	**P45C1**	**P44C1**	P43C1	P42C1	P41C1	P40C1
Data	*	**1**	**1**	**$**	*	*	*	*

Reg. name	P4CON0 register (Address: 0F222H)							
Bit	7	**6**	**5**	**4**	3	2	1	0
Bit name	P47C0	**P46C0**	**P45C0**	**P44C0**	P43C0	P42C0	P41C0	P40C0
Data	*	**1**	**1**	**$**	*	*	*	*

Reg. name	P4DIR register (Address: 0F221H)							
Bit	7	**6**	**5**	**4**	3	2	1	0
Bit name	P47DIR	**P46DIR**	**P45DIR**	**P44DIR**	P43DIR	P42DIR	P41DIR	P40DIR
Data	*	**0**	**0**	**1**	*	*	*	*

Data of P46D-P44D bits (bit6-4 of P4D register) do not affect to the SSIO function, so don't care the data for the function.

Reg. name	P4D register (Address: 0F220H)							
Bit	7	**6**	**5**	**4**	3	2	1	0
Bit name	P47D	**P46D**	**P45D**	**P44D**	P43D	P42D	P41D	P40D
Data	*	**	**	**	*	*	*	*

- : Bit not related to the SSIO(using P46, P45, and P44) function
** : Don't care the data
$: Arbitrarily

13.4.4 Functioning P46 (SOUT0), P45 (SCK0) and P44 (SIN0) as the SSIO/ "Slave mode"

Set P46MD1-P44MD1 bits(bit6-bit4 of P4MOD1 register) to "1" and set P46MD0-P44MD0(bit6-bit4 of P4MOD0 register) to "0", for specifying the SSIO as the secondary function of P46, P45 and P44. They are the same setting as those in the case of master mode.

Reg. name	P4MOD1 register (Address: 0F225H)							
Bit	7	**6**	**5**	**4**	**3**	2	1	0
Bit name	P47MD1	**P46MD1**	**P45MD1**	**P44MD1**	P43MD1	P42MD1	P41MD1	P40MD1
Data	*	**1**	**1**	**1**	*	*	*	:

Reg. name	P4MOD0 register (Address: 0F224H)							
Bit	7	**6**	**5**	**4**	3	2	1	0
Bit name	P47MD0	**P46MD0**	**P45MD0**	**P44MD0**	P43MD0	P42MD0	P41MD0	P40MD0
Data	*	**0**	**0**	**0**	*	*	*	*

Set P46C1 bit(bit6 of P4CON1 register) to "1", set P46C0 bit(bit6 of P4CON0 register) to "1", and set P46DIR bit(bit6 of P4DIR register) to "0", for specifying the P46 as CMOS output.

Set P45DIR-P44DIR bits(bit5-4 of P4DIR register) to "1" for specifying the P45 and P44 as input pins.

Data setting to P45C1 bit, P44C1 bit, P45C0 bit and P44C0 bit, depend on the application circuit connected to P45 and P44.

Reg. name	P4CON1 register (Address: 0F223H)							
Bit	7	**6**	**5**	**4**	3	2	1	0
Bit name	P47C1	**P46C1**	**P45C1**	**P44C1**	P43C1	P42C1	P41C1	P40C1
Data	*	**1**	**$**	**$**	*	*	*	*

Reg. name	P4CON0 register (Address: 0F222H)							
Bit	7	**6**	**5**	**4**	3	2	1	0
Bit name	P47C0	**P46C0**	**P45C0**	**P44C0**	P43C0	P42C0	P41C0	P40C0
Data	*	**1**	**$**	**$**	*	*	*	*

Reg. name	P4DIR register (Address: 0F221H)							
Bit	7	**6**	**5**	**4**	3	2	1	0
Bit name	P47DIR	**P46DIR**	**P45DIR**	**P44DIR**	P43DIR	P42DIR	P41DIR	P40DIR
Data	*	**0**	**1**	**1**	*	*	*	*

Data of P46D-P44D bits (bit6-4 of P4D register) do not affect to the SSIO function, so don't care the data for the function.

Reg. name	P4D register (Address: 0F220H)							
Bit	7	**6**	**5**	**4**	3	2	1	0
Bit name	P47D	**P46D**	**P45D**	**P44D**	P43D	P42D	P41D	P40D
Data	*	**	**	**	*	*	*	*

- : Bit not related to the SSIO(using P46, P45, and P44) function
** : Don't care the data
$: Arbitrarily

Chapter 14

UART

14. UART

14.1 Overview

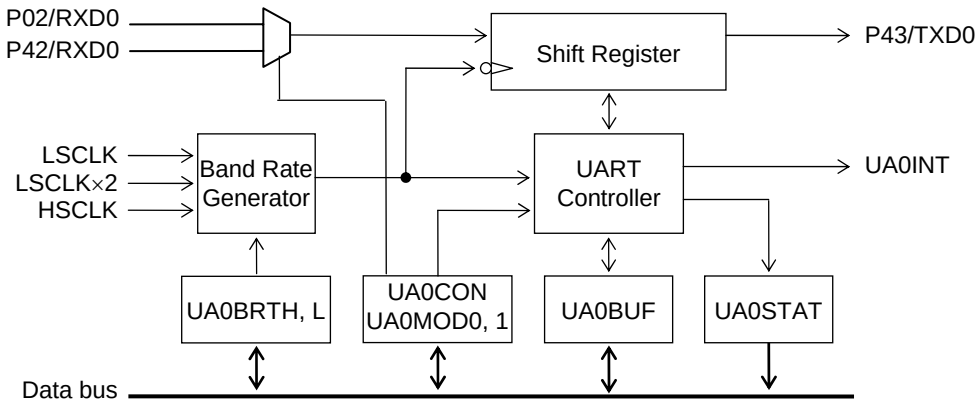
This LSI includes 1 channel of UART (Universal Asynchronous Receiver Transmitter) which is an asynchrnous serial interface.
For the input clock, see Chapter 6, "Clock Generation Circuit".
The use of UART requires setting of the secondary functions of Port 4. For setting of the secondary functions of Port 4, see Chapter 21, "Port 4".

14.1.1 Features

- 5-bit/6-bit/7-bit/8-bit data length selectable
- Odd parity, even parity, or no parity selectable
- 1 stop bit or 2 stop bits selectable
- Provided with parity error flag, overrun error flag, framing error flag, and transmit buffer status flag.
- Positive logic or negative logic selectable as communication logic
- LSB first or MSB first slectable as a communication direction
- Communication speed: Settable within the range of 200bps to 115200bps
- Built-in baud rate generator

14.1.2 Configuration

Figure 14-1 shows the configuration of the UART.



UA0BUF:	UART0 transmit/receive buffer
UA0BRTH, L:	UART0 baud rate registers H, L
UA0CON:	UART0 control register
UA0MOD0, 1:	UART0 mode registers 0, 1
UA0STAT:	UART0 status register

Figure 14-1 Configuration of UART

14.1.3 List of Pins

Pin name	I/O	Description
P02/RXD0	I	UART0 data input pin Used for the secondary function of the P02 pin.
P42/RXD0	I	UART0 data input pin Used for the secondary function of the P42 pin.
P43/TXD0	O	UART0 data output pin Used for the secondary function of the P43 pin.

14.2 Description of Registers

14.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F290H	UART0 transmit/receive buffer	UA0BUF	—	R/W	8	00H
0F291H	UART0 control register	UA0CON	—	R/W	8	00H
0F292H	UART0 mode register 0	UA0MOD0	UA0MOD	R/W	8/16	00H
0F293H	UART0 mode register 1	UA0MOD1		R/W	8	00H
0F294H	UART0 baud rate register L	UA0BRTL	UA0BRT	R/W	8/16	0FFH
0F295H	UART0 baud rate register H	UA0BRTH		R/W	8	0FH
0F296H	UART0 status register	UA0STAT	—	R/W	8	00H

14.2.2 UART0 Transmit/Receive Buffer (UA0BUF)

Address: 0F290H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0BUF	U0B7	U0B6	U0B5	U0B4	U0B3	U0B2	U0B1	U0B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0BUF is a special function register (SFR) to store the transmit/receive data of the UART.
In transmit mode, write transmission data to UA0BUF. To tranmit data continuously, write the next data to UA0BUF after making sure that the U0FUL flag of the UART0 status register (UA0STAT) is "0". Any value written to UA0BUF can be read.
In receive mode, since data received at termination of reception is stored in UA0BUF, read the contents of UABUF using the UART0 interrupt at termination of reception. At continuous reception, BA0BUF is updated whenever reception terminates. Any write to BA0BUF is disabled in receive mode.
The bits not required when 5-bit, 6-bit, 7-bit, or 8-bit data length is slected become invalid in transmit mode and are set to "0" in receive mode.

Note:
For operation in transmit mode, be sure to set the transmit mode (UA0MOD0 and UA0MOD1) before setting transmit data in UAOBUF.

14.2.3 UART0 Control Register (UA0CON)

Address: 0F291H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0CON	—	—	—	—	—	—	—	U0EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0CON is a special function register (SFR) to start/stop communication of the UART.

[Description of Bits]

- **U0EN** (bit 0)
  The U0EN bit is used to specify the UART communication operation start. When U0EN is set to "1", UART communication starts. In transmit mode, this bit is automatically set to "0" at termination of transmission. In receive mode, receive operation is continued. To terminate reception, set the bit to "0" by software.

U0EN	Description
0	Stops communication. (Initial value)
1	Starts communication.

14.2.4 UART0 Mode Register 0 (UA0MOD0)

Address: 0F292H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0MOD0	—	—	—	U0RSEL	—	U0CK1	U0CK0	U0IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0MOD0 is a special function register (SFR) to set the transfer mode of the UART.

[Description of Bits]

- **U0IO** (bit 0)
  The U0IO bit is used to select transmit or receive mode.

U0IO	Description
0	Transmit mode (initial value)
1	Receive mode

- **U0CK1, U0CK0** (bits 2, 1)
  The U0CK1 and U0CK0 bits are used to select the clock to be input to the baud rate generator of the UART0.

U0CK1	U0CK0	Description
0	0	LSCLK (initial value)
0	1	LSCLK×2
1	*	HSCLK

- **U0RSEL** (bit 4)
  The U0RSEL bit is used to select the receive data input pin for the UART0.

U0RSEL	Description
0	Selects the P02 pin. (Initial value)
1	Selects the P42 pin.

Notes:
- Always set the UA0MOD0 register while communication is stopped, and do not rewrite it during communication.
- When specifying LSCLK×2 for the clock, enable the operation of the 2×low-speed clock by setting bit 2 (ENMLT) of the frequency control register 1 (FCON1) to "1".
- When selecting the P42 pin as the receive data input pin, it is necessary to configure settings for the Port 4 secondary functions. For the details of the Port 4 secondary function settings, see Chapter 21, "Port 4".

14.2.5 UART0 Mode Register 1 (UA0MOD1)

Address: 0F293H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0MOD1	—	U0DIR	U0NEG	U0STP	U0PT1	U0PT0	U0LG1	U0LG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0MOD1 is a special function register (SFR) to set the transfer mode of the UART.

[Description of Bits]

- **U0LG1, U0LG0** (bits 1, 0)
  The U0LG1 and U0LG0 bits are used to specify the data length in the communication of the UART.

U0LG1	U0LG0	Description
0	0	8-bit length (initial value)
0	1	7-bit length
1	0	6-bit length
1	1	5-bit length

- **U0PT1, U0PT0** (bits 3, 2)
  The U0PT1 and U0PT0 bits are used to select "even parity", odd parith", or "no parity" in the communication of the UART.

U0PT1	U0PT0	Description
0	0	Even parity (initial value)
0	1	Odd parity
1	*	No parity bit

- **U0STP** (bit 4)
  The U0STP bit is used to select the stop bit length in the communication of the UART.

U0STP	Description
0	1 stop bit (initial value)
1	2 stop bits

- **U0NEG** (bit 5)
  The U0NEG bit is used to select positive logic or negative logic in the communication of the UART.

U0NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **U0DIR** (bit 6)
  The U0DIR bit is used to select LSB first or MSB first in the communication of the UART.

U0DIR	Description
0	LSB first (initial value)
1	MSB first

Note:
Always set the UA0MOD1 register while communication is stopped, and do not rewrite it during communication.

14.2.6 UART0 Baud Rate Registers L, H (UA0BRTL, UA0BRTH)

Address: 0F294H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
UA0BRTL	U0BR7	U0BR6	U0BR5	U0BR4	U0BR3	U0BR2	U0BR1	U0BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F295H
Access: R/W
Access size: 8 bits
Initial value: 0FH

	7	6	5	4	3	2	1	0
UA0BRTH	—	—	—	—	U0BR11	U0BR10	U0BR9	U0BR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	1	1

UA0BRTL and UA0BRTH are special function registers (SFRs) to set the count value of the baud rate generator which generates baud rate clocks.
For the relationship between the count value of the baud rate generator and baud rate, see Section 14.3.2, "Baud Rate".

Note:
Always set the UA0BRTL and UA0BRTH registers while communication is stopped, and do not rewrite them during communication.

14.2.7 UART0 Status Register (UA0STAT)

Address: 0F296H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0STAT	—	—	—	—	U0FUL	U0PER	U0OER	U0FER
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0STAT is a special function register (SFR) to indicate the state of transmit or receive operation of the UART.
When any data is written to UA0STAT, all the flags are initialized to "0".

[Description of Bits]

- **U0FER** (bit 0)
  The U0FER bit is used to indicate occurrence of a framing error of the UART.
  When an error occurs in the start or stop bit, the U0FER bit is set to "1". This bit is updated each time reception is completed.
  The U0FER bit is fixed to "0" in transmit mode.

U0FER	Description
0	No framing error (initial value)
1	Framing error

- **U0OER** (bit 1)
  The U0OER bit is used to indicate occurrence of an overrun error of the UART.
  If the received data in the transmit/receive buffer (UA0BUF) is received again before it is read, this bit is set to "1". Even if reception is stopped by the U0EN bit and then reception is restarted, this bit is set to "1" unless the previous receive data is not read. Therefore, make sure that data is always read from the transmit/receive buffer even if the data is not required.
  The U0OER bit is fixed to "0" in transmit mode.

U0OER	Description
0	No overrun error (initial value)
1	Overrun error

- **U0PER** (bit 2)
  The U0PER bit is used to indicate occurrence of a parity error of the UART.
  When the parity of the received data and the parity bit attached to the data do not coincide, this bit is set to "1". U0PER is updated whenever data is received.
  The U0PER bit is fixed to "0" in transmit mode.

U0PER	Description
0	No parity error (initial value)
1	Parity error

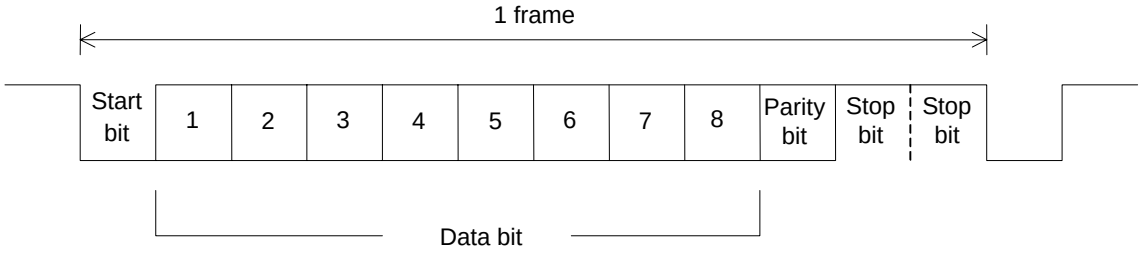
- **U0FUL** (bit 3)
  The U0FUL bit is used to indicate the state of the transmit/receive buffer of the UART.
  When transmit data is written in UA0BUF in transmit mode, this bit is set to "1" and when transmit data is transferred to the shift register, this bit is set to "0". To transmit data consecutively, write the next transmit data to UA0BUF after checking that the U0FUL flag has been set to "0".
  The U0FUL bit is fixed to "0" in receive mode.

U0FUL	Description
0	There is no data in the transmit/receive buffer. (Initial value)
1	There is data in the transmit/receive buffer.

14.3 Description of Operation

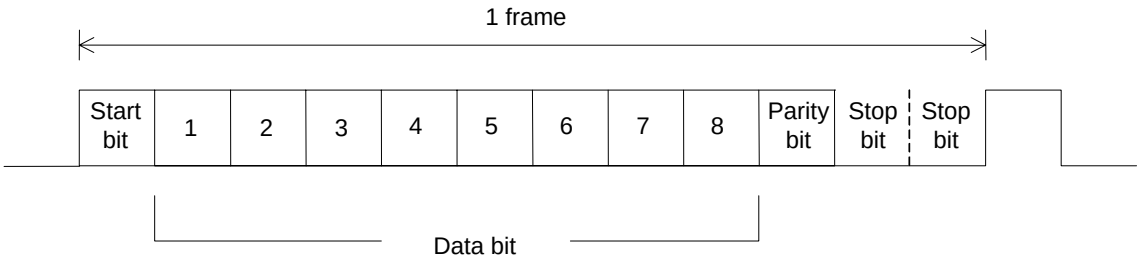
14.3.1 Transfer Data Format

In the transfer data format, one frame contains a start bit, a data bit, a parity bit, and a stop bit. In this format, 5 to 8 bits can be selected as data bit. For the parity bit, "with parity bit", "without parity bit", "even parity", or "odd parity" can be selected. For the stop bit, "1 stop bit" or "2 stop bits" are available and for the transfer direction, "LSB first" or "MSB first" are available for selection. For serial input/output logic, positive logic or negative logic can be selected. All these options are set with the UART0 mode register (UA0MOD1).
Figure 14-2 and Figure 14-3 show the positive logicc input/output format and negative logic input/output format, respectively.



- 1 frame
  Max. ……. 12 bits
  Min. ……. 7 bits
- Data bit length……. 8 to 5 bits variable
- Parity bit…….... With or without parity bit selectable
  Odd or even parity selectable
- Stop bit…….... 1 or 2 stop bits selectable

Figure 14-2 Positive Logic Input/Output Format



- 1 frame
  Max. …… 12 bits
  Min. …… 7 bits
- Data bit length…….8 to 5 bits variable
- Parity bit…….....With or without parity bit selectable
  Odd or even parity selectable
- Stop bit…….....1 or 2 stop bits selectable

Figure 14-3 Negative Logic Input/Output Format

14.3.2 Baud Rate

Baud rates are generated by the baud generator.
The baud rate generator generates a baud rate by counting the clock selected by the baud rate clock selection bits (U0CK1, U0CK0) of the UART0 mode register 0 (UA0MOD0). The count value of the baud rate generator can be set by writing it in the UART0 baud rate register H or L (UA0BRTH, UA0BRTL). The maximum count is 4096.
The setting values of UA0BRTH and UA0BRTL are expressed by the following equation.

$$\text{UA0BRTH, L} = \frac{\text{Clock frequency (Hz)}}{\text{Baud rate (bps)}} - 1$$

Table 14-2 lists the count values for typical baud rates.

Table 14-2 Count Values for Typical Baud Rates

Baud rate	Baud rate generator clock selection			Count value of the baud rate generator			
	Baud rate clock	U0CK1	U0CK0	Count value	Period of 1 bit	UA0BRTH	UA0BRTL
1200 bps	32.768 kHz	0	0	27	Approx. 824 μs	00H	1AH
2400 bps	65.536 kHz	0	1	27	Approx. 412 μs	00H	1AH
4800 bps	4.096 MHz	1	*	853	Approx. 208 μs	03H	054H
9600 bps	4.096 MHz	1	*	427	Approx. 104 μs	01H	0AAH
19200 bps	4.096 MHz	1	*	213	Approx. 52 μs	00H	0D4H
38400 bps	4.096 MHz	1	*	107	Approx. 26 μs	00H	06AH
57600 bps	4.096 MHz	1	*	71	Approx. 17.3 μs	00H	046H
115200 bps	4.096 MHz	1	*	36	Approx. 8.8 μs	00H	023H

Note:
When UA0BRTH or UA0BRTL is set to a value equal to less than "0007H", the value set is read from UA0BRTH or UA0BRTL but the value of the baud rate clock counter is the same as the value when UA0BRTH or UA0BRTL is set to "0008H".
When specifying 65.536 kHz (LSCLK×2) for the clock, enable the operation of the 2×low-speed clock by setting bit 2 (ENMLT) of the frequency control register 1 (FCON1) to "1".
Compensating tolerant of RC oscillation 500kHz with Timer can support errors of +/- 2% or less at 9600bps. See Section 10.3.2., "Frequency measurement mode".

14.3.3 Transmit Data Direction

Figure 14-4 shows the relationship between the transmit/receive buffer and the transmit/receive data.

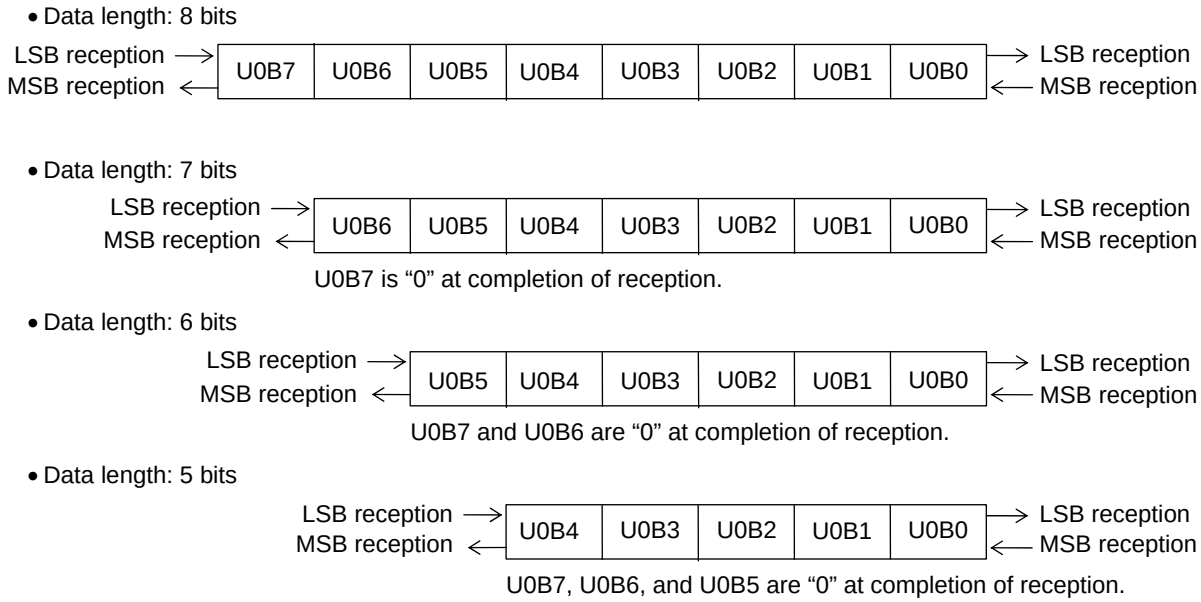


Figure 14-4 Relationship between Transmit/Receive Buffer and Transmit/Receive Data

Note:
When the TXD0 pin is set to serve the secondary function output in receive mode, "H" level is output from the TXD0 pin.

14.3.4 Transmit Operation

Transmission is started by setting the U0IO bit of the UART0 mode register 0 (UA0MOD0) to "0" to select transmit mode and setting the U0EN bit of the UART0 control register (UA0CON) to "1".
Figure 14-5 shows the operation timing for transmission.

When the U0EN bit is set to "1" (①), the baud rate generator generates an internal transfer clock of the baud rate set and starts transmission.
The start bit is output to the TXD0 pin by the falling edge of the internal transfer clock (②). Subsequently, transmit data, a parity bit, and a stop bit are output.
When the start bit is output (②), a UART0 interrupt is requested. In the UART0 interrupt routine, the next data to be transmitted is written to the transmit/receive buffer (UA0BUF).
When the next data to be transmitted is written to the transmit/receive buffer (UA0OBUF), the transmit buffer status flag (U0FUL) is set to "1" (③) and a UART0 interrupt is requested on the falling edge of the internal transfer clock (④) after transmission of the stop bit. If the UART0 interrupt routine is terminated without writing the next data to the transmit/receive buffer, the U0FUL bit is not set to "1" (⑤) and transmission continues up to the transmission of the stop bit, then the U0EN bit is reset to "0" and a UART0 interrupt is requested.
The valid period for the next transmit data to be written to the transmit/receive buffer is from the generation of an interrupt to the termination of stop bit transmission. (⑥)

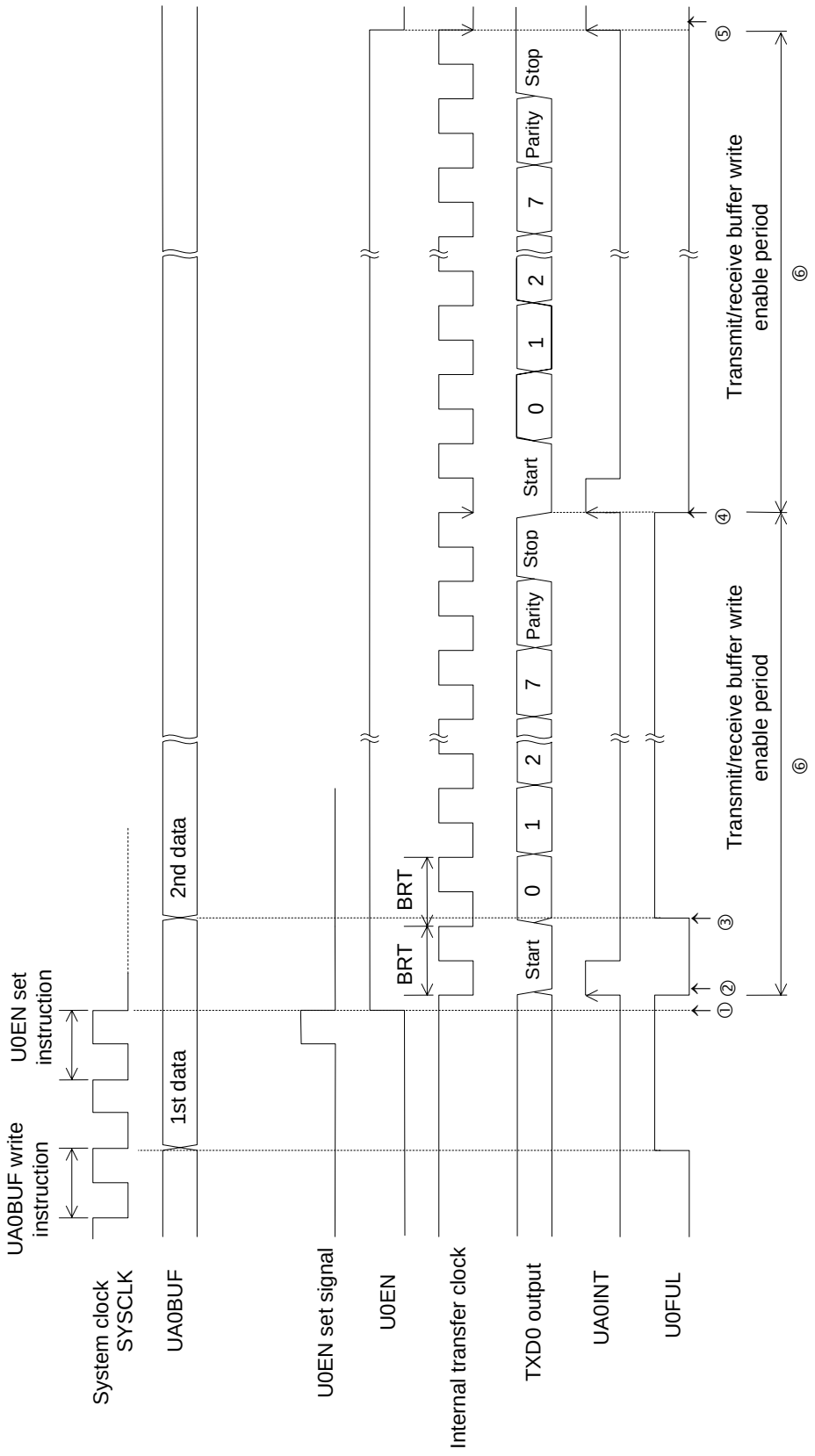


Figure 14-5 Operation Timing in Transmission

14.3.5 Receive Operation

Reception is started by selecting a receive data input pin using the U0RSEL bit of the UART0 mode register 0 (UA0MOD0), then setting the U0IO bit of UA0MOD0 to "0" to select receive mode, and then setting the U0EN bit of the UART0 control register (UA0CON) to "1".
Figure 14-6 shows the operation timing for reception.

When receive operation starts, the LSI checks the data sent to the input pin RXD0 and waits for the arrival of a start bit. When detecting a start bit (②), the LSI generates the internal transfer clock of the baud rate set with the start bit detect point as a reference and performs receive operation.
The shift register shifts in the data input to RXD on the rising edge of the internal transfer clock. The data and parity bit are shifted into the shift register and 5- to 8- bit receive data is transferred to the transmit/receive buffer (UA0BUF) concurrently with the fall of the internal transfer clock of ③.
The LSI requests a UART0 interrupt on the rising edge of the internal transfer clock subsequent to the internal transfer clock by which the receive data was fetched (④) and checks for a stop bit error and a parity bit error. When an error is detected, the LSI sets the corresponding bit of the UART0 status register (UA0STAT) to "1".

Parity error : S0PER = "1"
Overrun error : S0OER = "1"
Framing error : S0FER = "1"

As shown in Figure 14-6, the rise of the internal transfer clock is set so that it may fall into the middle of the bit interval of the receive data.
Reception continues until the U0EN bit is reset to "0" by the program. When the U0EN bit is reset to "0" during reception, the data received may be destroyed. When the U0EN bit is reset to "0" during the "U0EN reset enable period" in Figure 14.6, the data received is protected.

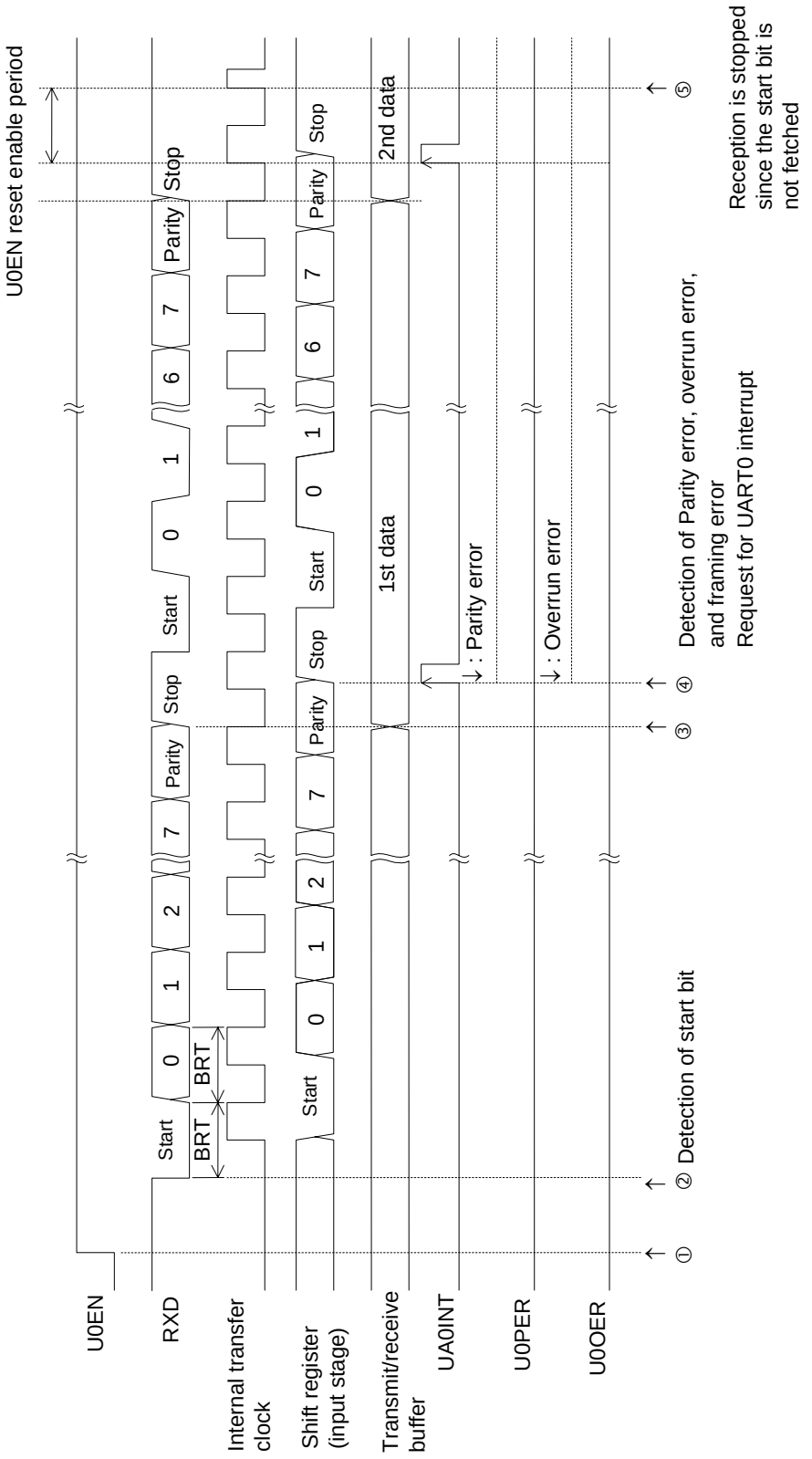


Figure 14-6 Operation Timing in Reception

14.4 Specifying port registers

When you want to make sure the UART function is working, please check related port registers are specified. See Chapter 21, "Port 4" and Chapter 18, "Port 0" for detail about the port registers.

14.4.1 Functioning P43(TXD0) and P42(RXD0) as the UART.

Set P43MD1-P42MD1 bits(bit3-bit2 of P4MOD1 register) to "0" and set P43MD0-P42MD0(bit3-bit2 of P4MOD0 register) to "1", for specifying the UART as the secondary function of P43 and P42.

Reg. name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	4	**3**	**2**	1	0
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	**P43MD1**	**P42MD1**	P41MD1	P40MD1
Data	*	*	*	*	**0**	**0**	*	*

Reg. name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	4	**3**	**2**	1	0
Bit name	P47MD0	P46MD0	P45MD0	P44MD0	**P43MD0**	**P42MD0**	P41MD0	P40MD0
Data	*	*	*	*	**1**	**1**	*	*

Set P43C1 bit(bit3 of P4CON1 register) to "1", set P43C0 bit(bit3 of P4CON0 register) to "1", and set P43DIR bit(bit3 of P4DIR register) to "0", for specifying the P43 as CMOS output.
Set P42DIR bit(bit2 of P4DIR register) to "1" for specifying the P42 as an input pin.
Data setting to P42C1 bit and P42C0 bit, depend on the application circuit connected to P42.

Reg. name	P4CON1 register (Address: 0F223H)							
Bit	7	6	5	4	**3**	**2**	1	0
Bit name	P47C1	P46C1	P45C1	P44C1	**P43C1**	**P42C1**	P41C1	P40C1
Data	*	*	*	*	**1**	**$**	*	*

Reg. name	P4CON0 register (Address: 0F222H)							
Bit	7	6	5	4	**3**	**2**	1	0
Bit name	P47C0	P46C0	P45C0	P44C0	**P43C0**	**P42C0**	P41C0	P40C0
Data	*	*	*	*	**1**	**$**	*	*

Reg. name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	4	**3**	**2**	1	0
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	**P43DIR**	**P42DIR**	P41DIR	P40DIR
Data	*	*	*	*	**0**	**1**	*	*

Data of P43D-P42D bits (bit3-2 of P4D register) do not affect to the UART function, so don't care the data for the function.

Reg. name	P4D register (Address: 0F220H)							
Bit	7	6	5	4	**3**	**2**	1	0
Bit name	P47D	P46D	P45D	P44D	**P43D**	**P42D**	P41D	P40D
Data	*	*	*	*	******	******	*	*

* : Bit not related to the UART(using P43 and P42) function
** : Don't care the data
$: Arbitrarily

Note:
The receive pin (RXD) is selected by U0RSEL bit(bit4 of UA0MOD0 register). Reseting the bit to "0" (initial value) selects P02 pin and setting the bit to "1" selects P43 pin.

14.4.2 Functioning P43(TXD0) and P02(RXD0) as the UART.

Set P43MD1 bit(bit3 of P4MOD1 register) to "0" and set P43MD0(bit3 of P4MOD0 register) to "1", for specifying the UART as the secondary function of P43.

Reg. name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	**P43MD1**	P42MD1	P41MD1	P40MD1
Data	*	*	*	*	**0**	$	*	*

Reg. name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47MD0	P46MD0	P45MD0	P44MD0	**P43MD0**	P42MD0	P41MD0	P40MD0
Data	*	*	*	*	**1**	$	*	*

Set P43C1 bit(bit3 of P4CON1 register) to "1", set P43C0 bit(bit3 of P4CON0 register) to "1", and set P43DIR bit(bit3 of P4DIR register) to "0", for specifying the P43 as CMOS output.

Reg. name	P4CON1 register (Address: 0F223H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47C1	P46C1	P45C1	P44C1	**P43C1**	P42C1	P41C1	P40C1
Data	*	*	*	*	**1**	*	*	*

Reg. name	P4CON0 register (Address: 0F222H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47C0	P46C0	P45C0	P44C0	**P43C0**	P42C0	P41C0	P40C0
Data	*	*	*	*	**1**	*	*	*

Reg. name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	**P43DIR**	P42DIR	P41DIR	P40DIR
Data	*	*	*	*	**0**	*	*	*

Data of P43D bit (bit3 of P4D register) do not affect to the UART function, so don't care the data for the function.

Reg. name	P4D register (Address: 0F220H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47D	P46D	P45D	P44D	**P43D**	P42D	P41D	P40D
Data	*	*	*	*	**	*	*	*

P02 is an input-only port, so there is no need to specify data direction (i.e. input or output).
Data setting to P02C1 bit and P02C0 bit, depend on the application circuit connected to P02.

Reg. name	P0CON1 register (Address: 0F207H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	-	P03C1	**P02C1**	P01C1	P00C1
Data	-	-	-	-	*	**$**	*	*

Reg. name	P0CON0 register (Address: 0F206H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	-	P03C0	**P02C0**	P01C0	P00C0
Data	-	-	-	-	*	**$**	*	*

Data of P02D bit (bit2 of P0D register) do not affect to the UART function, so don't care the data for the function.

Reg. name	P0D register (Address: 0F204H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	-	P03D	**P02D**	P01D	P00D
Data	-	-	-	-	*	******	*	*

* : Bit not related to the UART(using P43 and P02) function
** : Don't care the data
$: Arbitrarily

Note:
The receive pin (RXD0) is selected by U0RSEL bit(bit4 of UA0MOD0 register). Setting the bit to "0" (initial value) selects P02 pin and setting the bit to "1" selects P43 pin.

Even if P42 is specified as RXD0 by P42MD1 bit, P42MD0 bit, P42C1 bit, P42C0 bit and P42IDR bit, setting "0" to U0RSEL bit has priority to select P02 pin as the RXD0.

P02(Port 0) is an input-only port, does not have registers that can select data direction(input or output) or mode(primary or secondary function).

Chapter 15

I^2C Bus Interface

15. I²C Bus Interface

15.1 Overview

This LSI includes 1 channel of I²C bus interface (master).
The secondary functions of Port 4 are assigned to the I²C bus interface data input/output pin and the I²C bus interface clock input/output pin. For Port4, see Chapter 21, "Port 4".

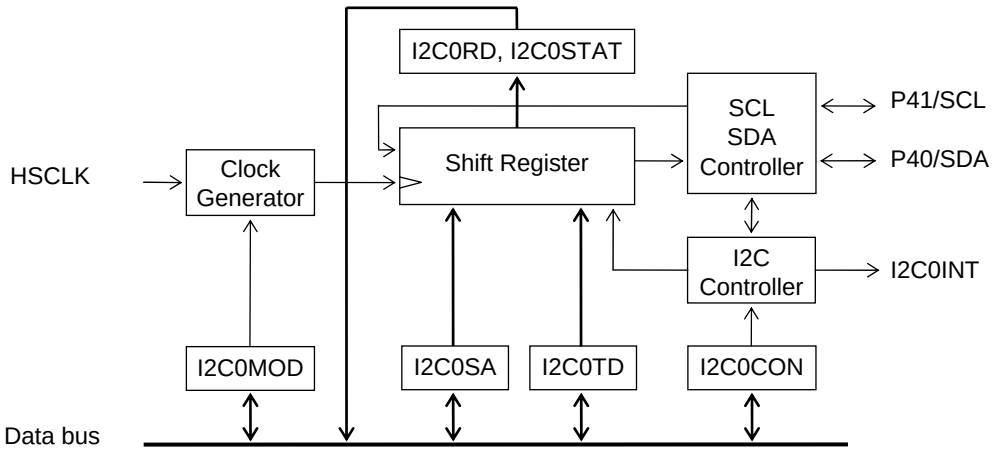
15.1.1 Features

- Master function
- Communication speeds supported include standard mode (100 kbps@1MHz HSCLK, 50kbps@500kHz HSCLK) and fast mode (400kbps@4MHz HSCLK).
- 7-bit address format (10-bit address can be supported)

Note:
This LSI does not support arbitration function (multi-master) and clock synchronization (handshake).

15.1.2 Configuration

Figure 15-1 shows the configuration of the I²C bus interface.



I2C0RD : I²C bus 0 receive register
I2C0SA : I²C bus 0 slave address register
I2C0TD : I²C bus 0 transmit data register
I2C0CON : I²C bus 0 control register
I2C0MOD : I²C bus 0 mode register
I2C0STAT : I²C bus 0 status register

Figure 15-1 Configuration of I²C Bus Interface

15.1.3 List of Pins

Pin name	I/O	Description
P40/SDA	I/O	I²C bus interface data input/output pin. Used for the secondary function of the P40 pin.
P41/SCL	I/O	I²C bus interface clock input/output pin. Used for the secondary function of the P41 pin.

15.2 Description of Registers

15.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2A0H	I^2C bus 0 receive register	I2C0RD	—	R	8	00H
0F2A1H	I^2C bus 0 slave address register	I2C0SA	—	R/W	8	00H
0F2A2H	I^2C bus 0 transmit data register	I2C0TD	—	R/W	8	00H
0F2A3H	I^2C bus 0 control register	I2C0CON	—	R/W	8	00H
0F2A4H	I^2C bus 0 mode register	I2C0MOD	—	R/W	8	00H
0F2A5H	I^2C bus 0 status register	I2C0STAT	—	R	8	00H

15.2.2 I^2C Bus 0 Receive Register (I2C0RD)

Address: 0F2A0H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0RD	I20R7	I20R6	I20R5	I20R4	I20R3	I20R2	I20R1	I20R0
R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

I2C0RD is a read-only special function register (SFR) to store receive data.
I2C0RD is updataed after completion of each reception.

[Description of Bits]

- **I20R7-I20R0** (bits 7-0)
  The I20R7 to I20R0 bits are used to store receive data. The signal input to the SDA pin is received at transmission of a slave address and at data transmission/reception in sync with the rising edge of the signal on the SCL pin. Since data that has been output to the SDA and SCL pins is received not only at data reception but also at slave address data transmission and data transmission, it is possible to check whether transmit data has certainly been transmitted.

15.2.3 I^2C Bus 0 Slave Address Register (I2C0SA)

Address: 0F2A1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0SA	I20A6	I20A5	I20A4	I20A3	I20A2	I20A1	I20A0	I20RW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0SA is a special function register (SFR) to set the address and the transmit/receive mode of the slave device.

[Description of Bits]

- **I20RW** (bit 0)
  The I20RW bit is used to select the data transmit mode (write) or data receive mode (read).

I20RW	Description
0	Data transmit mode (initial value)
1	Data receive mode

- **I20A6-I20A0** (bits 7-1)
  The I20A6 to I20A0 bits are used to set the address of the communication destination.

15.2.4 I^2C Bus 0 Transmit Data Register (I2C0TD)

Address: 0F2A2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0TD	I20T7	I20T6	I20T5	I20T4	I20T3	I20T2	I20T1	I20T0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0TD is a special function register (SFR) to set transmit data.

[Description of Bits]

- **I20T7-0** (bits 7-0)
  The I20T7 to 0 bits are used to set transmit data.

15.2.5 I²C Bus 0 Control Register (I2C0CON)

Address: 0F2A3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0CON	I20ACT	—	—	—	—	I20RS	I20SP	I20ST
R/W	R/W	R/W	R/W	R/W	R/W	W	W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0CON is a special function register (SFR) to control transmit and receive operations.

[Description of Bits]

- **I20ST** (bit 0)
  The I20ST bit is used to control the communication operation of the I²C bus interface. When the I20ST bit is set to "1", communication starts. When "1" is overwritten to the I20ST bit in a control register setting wait state after transmission/reception of acknowledgment, communication starts again. When the I20ST bit is set to "0", communication is stopped forcibly.
  The I20ST bit can be set to "1" only when the I2C bus interface is in an operation enable state (I20EN = "1").
  When the I20SP bit is set to "1", the I20ST bit is set to "0".

I20ST	Description
0	Stops communication (initial value)
1	Starts communication

- **I20SP** (bit 1)
  The I20SP bit is a write-only bit used to request a stop condition. When the I20SP bit is set to "1", the I²C bus shifts to the stop condition and communication stops. When the I20SP bit is read, "0" is always read.

I20SP	Description
0	No stop condition request (initial value)
1	Stop condition request

- **I20RS** (bit 2)
  The I20RS bit is a write-only bit used to request a repeated start. When this bit is set to "1" during data communication, the I²C bus shifts to the repeated start condition and communication restarts from the slave address. I20RS can be set to "1" only while communication is active (I20ST ="1"). When the I20RS bit is read, "0" is always read.

I20RS	Description
0	No repeated start request (initial value)
1	Repeated start request

- **I20ACT** (bit 7)
  The I20ACT bit is used to set the acknowledge signal to be output at completion of reception.

I20ACT	Description
0	Acknowledgment data "0" (initial value)
1	Acknowledgment data "1"

15.2.6 I²C Bus 0 Mode Register (I2C0MOD)

Address: 0F2A4H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0MOD	—	—	—	I20SYN	I20DW1	I20DW0	I20MD	I20EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0MOD is a special function register (SFR) to set operating mode.

[Description of Bits]

- **I20EN** (bit 0)
  The I20EN bit is used to enable the operation of the I²C bus interface. Only when the I20EN bit is set to "1", the I20ST bit can be set and the I20BB flag starts operation. When the I20EN bit is set to "0", all the SFRs related to the I²C bus 0 are initialized.

I20EN	Description
0	Stops I²C operation. (Initial value)
1	Enables I²C operation.

- **I20MD** (bit 1)
  The I20MD bit is used to set the communication speed of the I²C bus interface. Standard mode or fast mode can be selected.

I20MD	Description
0	Standard mode (initial value)/ 100kbps@1MHz HSCLK
1	Fast mode / Max. 400kbps@4MHz HSCLK

- **I20DW1, I20DW0** (bits 3, 2)
  The I20DW1 and I20DW0 bits are used to set the communication speed reduction rate of the I²C bus interface. Set this bit so that the communication speed does not exceed 100kpbs/400kpbs.

I20DW1	I20DW0	Description
0	0	No communication speed reduction (initial value)
0	1	10% communication speed reduction
1	0	20% communication speed reduction
1	1	30% communication speed reduction

- **I20SYN** (bit 4)
  The I20SYN bit is used to select whether or not to use the clock synchronization function (handshake function).

Note: This LSI does not support the clock synchronization function or multi-master. Please always set the bit to "0".

I20SYN	Description
0	Clock synchronization is not used. (Initial value)
1	Do not use.

Note:
The I²C bus is set so that the communication speed may become 100kbps/400kbps when HSCLK is 4 MHz. Therefore, when using PLL oscillation (approx. 8.192 MHz) for high-speed oscillation, select 1/2HSCLK at selection of the HSCLK frequency of FCON0 and select 10% communication speed reduction at selection of I2C0MOD communication speed reduction. When 500 kHz RC oscillation is used, communication in standard mode (50kbps) is available with the fast mode by setting I20MD bit to "1".

15.2.7 I^2C Bus 0 Status Register (I2C0STAT)

Address: 0F2A5H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0STAT	—	—	—	—	—	I20ER	I20ACR	I20BB
R	R	R	R	R	R	R	R	R
Initial value:	0	0	0	0	0	0	0	0

I2C0STAT is a read-only special function register (SFR) to indicate the state of the I^2C bus interface.

[Description of Bits]

- **I20BB** (bit 0)
  The I20BB bit is used to indicate the state of use of the I^2C bus interface. When the start condition is generated on the I^2C bus, this bit is set to "1" and when the stop condition is generated, the bit is set to "0". The I20BB bit is set to "0" when the I20EN bit of I2C0MOD is "0".

I20BB	Description
0	I^2C bus-free state (Initial value)
1	I^2C bus-busy state

- **I20ACR** (bit 1)
  The I20ACR bit is used to store the acknowledgment signal received. Acknowledgment signals are received each time the slave address is received and data transmission or reception is completed. The I20ACR bit is set to "0" when the I20EN bit of I2C0MOD is "0".

I20ACR	Description
0	Receives acknowledgment "0". (Initial value)
1	Receives acknowledgment "1".

- **I20ER** (bit 2)
  The I20ER bit is a flag to indicate a transmit error. When the value of the bit transmitted and the value of the SDA pin do not coincide, this bit is set to "1". The SDA remains the output until the subsequent byte data communication terminates even if I20ER is set to "1".
  The I20ER bit is set to "0" when a write operation to I2C0CON is performed. The I20ER bit is set to "0" when the I20EN bit of I2C0MOD is set to "0".

I20ER	Description
0	No transmit error (initial value)
1	Transmit error

15.3 Description of Operation

15.3.1 Communication Operating Mode

Communication is started when communication mode is selected by using the I²C bus 0 mode register (I2C0MOD), the I²C function is enabled by using the I20EN bit, a slave address and a data communication direction are set in the I²C bus 0 slave address register, and "1" is written to the I20ST bit of the I2C bus 0 control register (I2C0CON).

15.3.1.1 Start Condition

When "1" is written to the I20ST bit of the I²C bus 0 control register ((I2C0CON) while communication is stopped (the I20ST bit is "0"), communication is started and the start condition waveform is output to the SDA and SCL pins.
After execution of the start condition, the LSI shifts to slave address transmit mode.

15.3.1.2 Repeated Start Condition

When "1" is written to the I20RS and I20ST bits of the I²C bus 0 control register ((I2C0CON) during communication (the I20ST bit is "0"), the repeated start condition waveform is output to the SDA and SCL pins. If you want to continue the communication without making the stop condition, executing the repeated start condition enables to specify another slave addresses or change the data direction (transmit or receive) See Figure 15-4.

After execution of the repeated start condition, the LSI shifts to slave address transmit mode.

15.3.1.3 Slave Address Transmit Mode

In slave address transmit mode, the values (slave address and data communication direction) of the I²C bus 0 slave address register (I2C0SA) are transmitted in MSB first, and finally, the acknowledgment signal is received in the I20ACR bit of the I²C bus 0 status register (I2CSTAT). The I20ACR bit is reset to "0" when receving an acknowledgment "0" and set to "1" when receving an acknowledgment "1".
At completion of acknowledgment reception, the LSI shifts to the I²C bus 0 control register (I2C0CON) setting wait state (control register setting wait state).
The value of I2C0SA output from the SDA pin is stored in I2C0RD during aftermentioned Control Register Setting Wait State.

15.3.1.4 Data Transmit Mode

In data transmit mode, the value of I2C0TD is transmitted in MSB first, and finally, the acknowledgment signal is received in the I20ACR bit of the I²C bus 0 status register (I2CSTAT). The I20ACR bit is reset to "0" when receving an acknowledgment "0" and set to "1" when receving an acknowledgment "1".
At completion of acknowledgment reception, the LSI shifts to the I²C bus 0 control register (I2C0CON) setting wait state (control register setting wait state).
The value of I2C0TD output from the SDA pin is stored in I2C0RD.

15.3.1.5 Data Receive Mode

In data receive mode, the value input in the SDA pin is received synchronously with the rising edge of the serial clock output to the SCL pin, and finally, the value of the I20ACT bit of the I2C bus 0 control register (I2C0CON) is output as an acknowledge signal. For example, as shown in Figure 15-3 and Figure 15-4, the acknowlege slot after I20ACT bit is reset to "0" (I2CON="01H") will have the acknowlege "0" (Shown as "A" in the Figure). In the same way, the acknowlege slot after I20ACT bit is set to "1" (I2CON="81H") will have the non-acknowlege "1" (Shown as "A" in the Figure).
At completion of acknowledgment transmission, the LSI shifts to the I²C bus 0 control register (I2C0CON) setting wait state (control register setting wait state).
The data received is stored in I2C0RD after the acknowledgment signal is output. The acknowledgment signal output is received in the I20ACR bit of the I²C bus 0 status register (I2CSTAT).

15.3.1.6 Control Register Setting Wait State

When the LSI shifts to the control register setting wait state, an I²C bus interface interrupt (I2C0INT) is generated.
In the control register setting wait state, the transmit flag (I20ER) of the I²C bus 0 status register (I2C0STAT) and acknowledgment receive data (I20ACR) are confirmed and at data reception, the contents of I2C0RD are read in the CPU and the next operation mode is selected.

When "1" is written to the I20ST bit in the control register setting wait state, the LSI shifts to the data transmit or receive mode. When "1" is written to the I20SP bit, the LSI shifts to the stop condition. When "1" is written to the I20RS bit and I20ST bit, the operation shifts to the repeated start condition.

15.3.1.7 Stop Condition

In the stop condition, the stop condition waveform is output to the SDA and SCL pins. After the stop condition waveform is output, an I^2C bus interface interrupt (I2C0INT) is generated.

15.3.2 Communication Operation Timing

Figures 15-2 to 15-4 show the operation timing and control method for each communication mode.

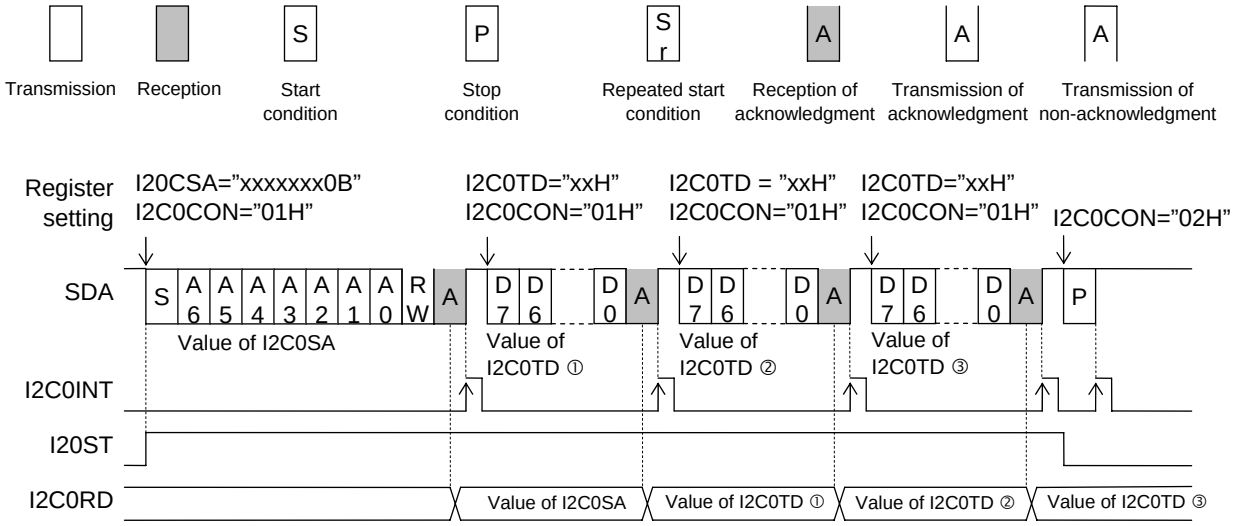


Figure 15-2 Operation Timing in Data Transmit (Write)

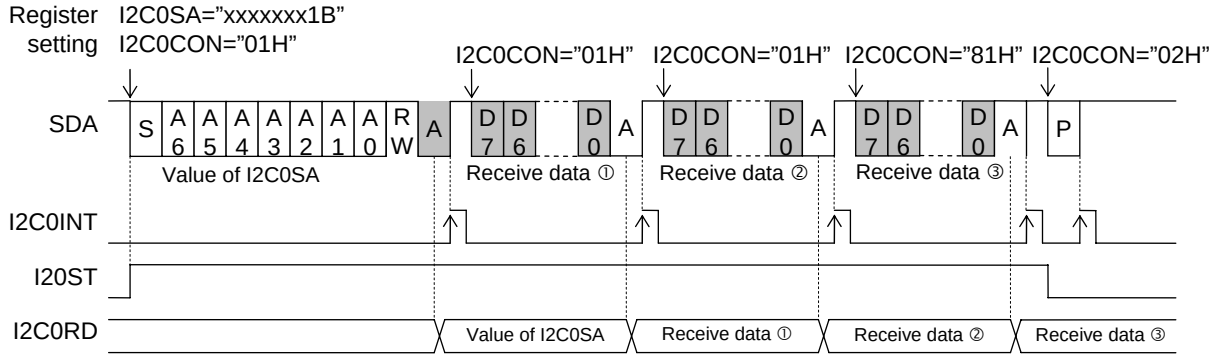


Figure 15-3 Operation Timing in Data Receive (Read)

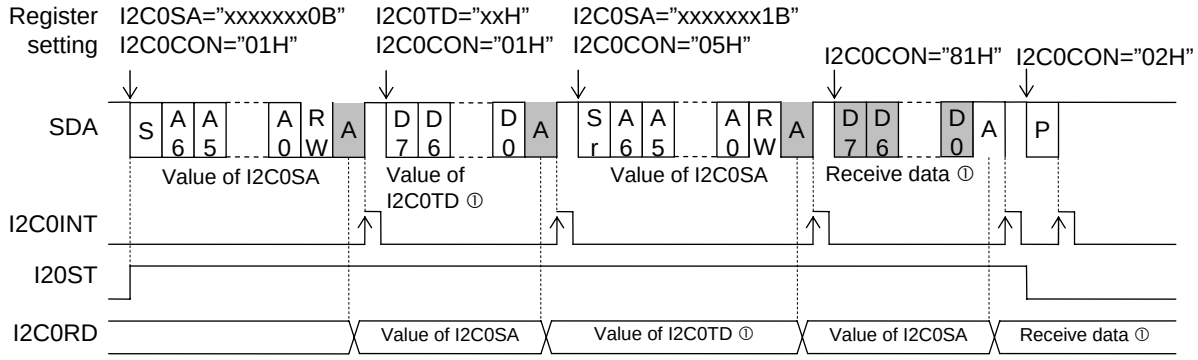


Figure 15-4 Operation Timing at Data Transmit/Receive (Write/Read) Switching

Figure 15-5 shows the operation timing and control method when an acknowledgment error occurs.

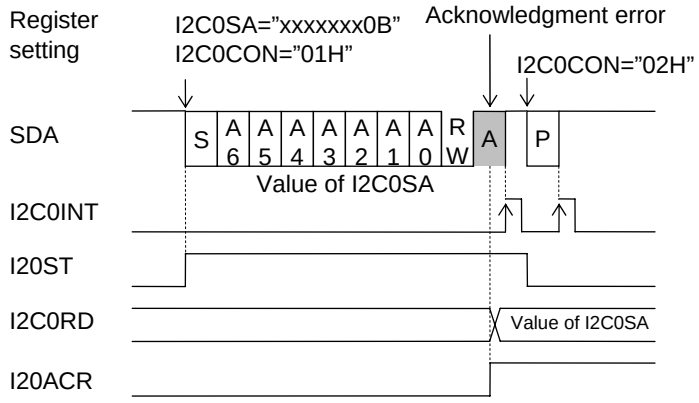


Figure 15-5 Operation Suspend Timing at Occurrence of Acknowledgment Error

When the values of the transmitted bit and the SDA pin do not coincide, the I20ER bit of the I2C bus 0 status register (I2C0STAT) is set to "1" and SDA pin remains the output until termination of the subsequent byte data communication. I20ER bit is initialized to "0" by writing I²C Bus 0 Control Register (I2C0COCON).
Figure 15-6 shows the operation timing and control method when transmission fails.

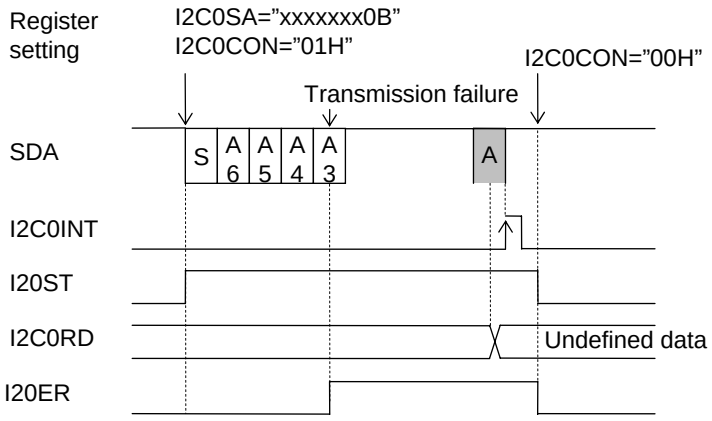


Figure 15-6 Operation Timing When Transmission Fails

15.3.3 Operation Waveforms

Figure 15-7 shows the operation waveforms of the SDA and SCL signals and the I20BB flag. Table 15-1 shows the relationship between communication speeds and HSCLK clock counts.

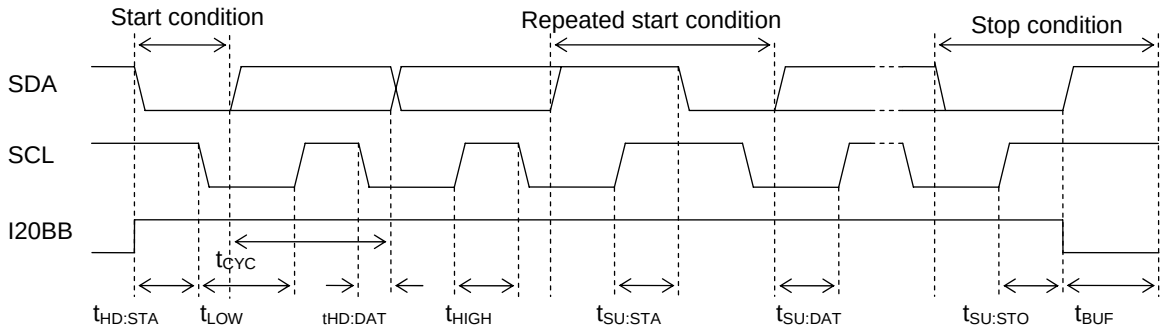


Figure 15-7 Operation Waveforms of SDA and SCL Signals and I20BB Flag

Table 15-1 Relationship between Communication Speeds and HSCLK Clock Counts

Communication speed (I20SP)	Speed reduction (I20DW1, 0)	t_{CYC}	$t_{HD:STA}$	t_{LOW}	$t_{HD:DAT}$	t_{HIGH}	$t_{SU:STA}$	$t_{SU:DAT}$	$t_{SU:STO}$	t_{BUF}
Standard mode 100 kbps	No reduction	40ϕ	18ϕ	22ϕ	4ϕ	18ϕ	22ϕ	18ϕ	18ϕ	22ϕ
	10% reduction	44ϕ	20ϕ	24ϕ	4ϕ	20ϕ	24ϕ	20ϕ	20ϕ	24ϕ
	20% reduction	48ϕ	22ϕ	26ϕ	4ϕ	22ϕ	26ϕ	22ϕ	22ϕ	26ϕ
	30% reduction	52ϕ	24ϕ	28ϕ	4ϕ	24ϕ	28ϕ	24ϕ	24ϕ	28ϕ
Fast mode 400 kbps	No reduction	10ϕ	4ϕ	6ϕ	2ϕ	4ϕ	6ϕ	4ϕ	4ϕ	6ϕ
	10% reduction	11ϕ	4ϕ	7ϕ	2ϕ	4ϕ	7ϕ	5ϕ	4ϕ	7ϕ
	20% reduction	12ϕ	5ϕ	7ϕ	2ϕ	5ϕ	7ϕ	5ϕ	5ϕ	7ϕ
	30% reduction	13ϕ	5ϕ	8ϕ	2ϕ	5ϕ	8ϕ	6ϕ	5ϕ	8ϕ

ϕ: Period of high-speed clock (HSCLK)

Note
The HSCLK clock count is set so that the communication speed may be set to 100kbps/400kbps when HSCLK is 4 MHz. When the high-speed clock frequency is not 4 MHz, select an I2C0MOD communication speed reduction rate and an FCON0 HSCLK frequency so that the communication speed may not exceed 100kbps/400kbps.

15.4 Specifying port registers

When you want to make sure the I2C bus interface function is working, please check related port registers are specified. See Chapter 21, "Port 4" for detail about the port registers.

15.4.1 Functioning P41(SCL) and P40(SDA) as the I2C

Set P41MD1-P40MD1 bits(bit1-bit0 of P4MOD1 register) to "0" and set P41MD0-P40MD0(bit1-bit0 of P4MOD0 register) to "1", for specifying the I2C as the secondary function of P41 and P40.

Reg. name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	4	**3**	2	**1**	**0**
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	P43MD1	P42MD1	**P41MD1**	**P40MD1**
Data	*	*	*	*	*	*	**0**	**0**

Reg. name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	P42MD0	**P41MD0**	**P40MD0**
Data	*	*	*	*	*	*	**1**	**1**

Set P41C1-P40C1 bit(bit1-0 of P4CON1 register) to "1", set P41C0-P40C0 bit(bit1-0 of P4CON0 register) to "0", and set P41DIR-P40DIR bit(bit1-0 of P4DIR register) to "0", for specifying the P41 and P40 as Nch open-drain output. The open-drain/open-collector outputs are required on the I2C bus line to avoid collision between H level and L level.

Reg. name	P4CON1 register (Address: 0F223H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47C1	P46C1	P45C1	P44C1	P43C1	P42C1	**P41C1**	**P40C1**
Data	*	*	*	*	*	*	**1**	**1**

Reg. name	P4CON0 register (Address: 0F222H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47C0	P46C0	P45C0	P44C0	P43C0	P42C0	**P41C0**	**P40C0**
Data	*	*	*	*	*	*	**0**	**0**

Reg. name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	P43DIR	P42DIR	**P41DIR**	**P40DIR**
Data	*	*	*	*	*	*	**0**	**0**

Data of P41D-P40D bits (bit1-0 of P4D register) do not affect to the I2C function, so don't care the data for the function.

Reg. name	P4D register (Address: 0F220H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47D	P46D	P45D	P44D	P43D	P42D	**P41D**	**P40D**
Data	*	*	*	*	*	*	******	******

* : Bit not related to the I2C bus interface function
** : Don't care the data

Chapter 16

NMI Pin

16. NMI Pin

16.1 Overview

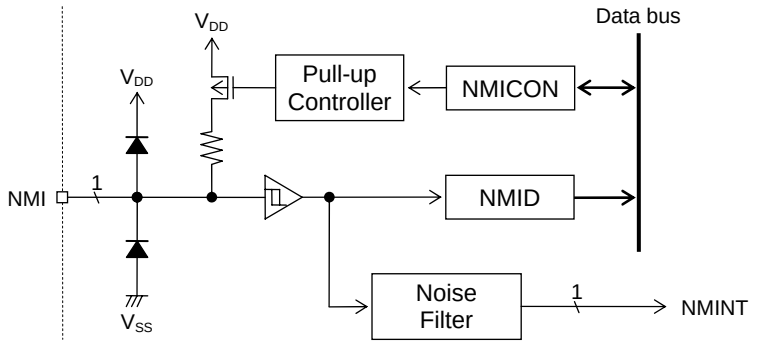
This LSI includes an input port (NMI) which generates a non-maskable interrupt.
For interrupts see Chapter 5, "Interrupts".

16.1.1 Features

- Non-maskable interrupt pin.
- Allows selection of an input with a pull-up resistor or a high-impedance input.
- Applies a noise filter to NMI interrupt (NMINT).

16.1.2 Configuration

Figure 16-1 shows the configuration of the NMI pin.



NMID: NMI data register
NMICON: NMI control register

Figure 16-1 Configuration of NMI Pin

16.1.3 List of Pins

Pin name	Input/output	Description
NMI	I	Non-maskable interrupt input port

16.2 Description of Registers

16.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F200H	NMI data register	NMID	—	R	8	Depends on pin state
0F201H	NMI control register	NMICON	—	R/W	8	00H

16.2.2 NMI Data Register (NMID)

Address: 0F200H
Access: R
Access size: 8 bits
Initial value: Depends on the pin state

	7	6	5	4	3	2	1	0
NMID	—	—	—	—	—	—	—	NMI
R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	x

NMID is a read-only special function register (SFR) for reading the NMI pin level.

[Description of Bits]

- **NMI** (bit 0)
  The NMI bit is used to read the level of the NMI pin.

NMI	Description
0	"0" level
1	"1" level

16.2.3 NMI Control Register (NMICON)

Address: 0F201H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
NMICON	—	—	—	—	—	—	—	NMIC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

NMICON is a special function register (SFR) to select the input mode of the NMI pin.

[Description of Bits]

- **NMIC** (bit 0)
  The NMIC bit is used to select the input mode with or without a pull-up resistor.

NMIC	Description
0	Input mode with a pull-up resistor (initial value)
1	High-impedance input mode

16.3 Description of Operation

The non-maskable NMI interrupt (NMIINT) is assigned to the NMI pin.
The NMI pin allows selection of an input mode with a pull-up resistor or a high-impedance input mode by using the NMI control register (NMICON). At a system reset, the input mode with a pull-up resistor is selected.
The level of the NMI pin can be read by reading the NMI data register (MMID).

16.3.1 Interrupt Request

When a level change occurs at the NMI pin after the duration longer than the minimum NMI interrupt pulse width, a non-maskable interrupt which does not depend on the master interrupt enable flag (MIE) is generated.
Figure 16-2 shows the NMI interrupt generation timing.

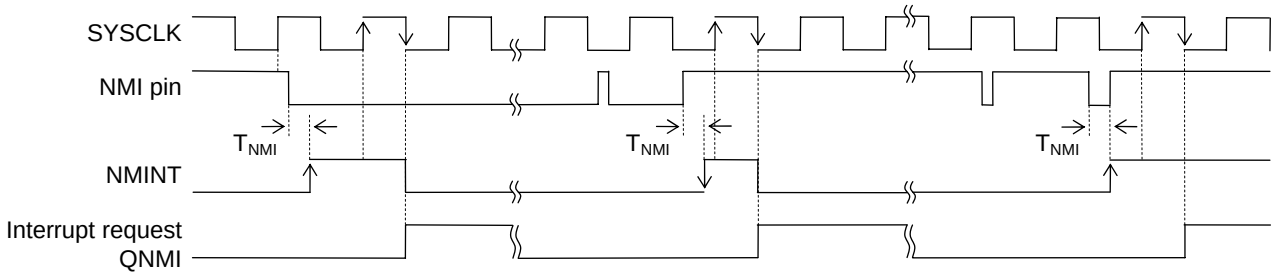


Figure 16-2 NMI Interrupt Generation Timing

Chapter 17

Port 0

17. Port 0

17.1 Overview

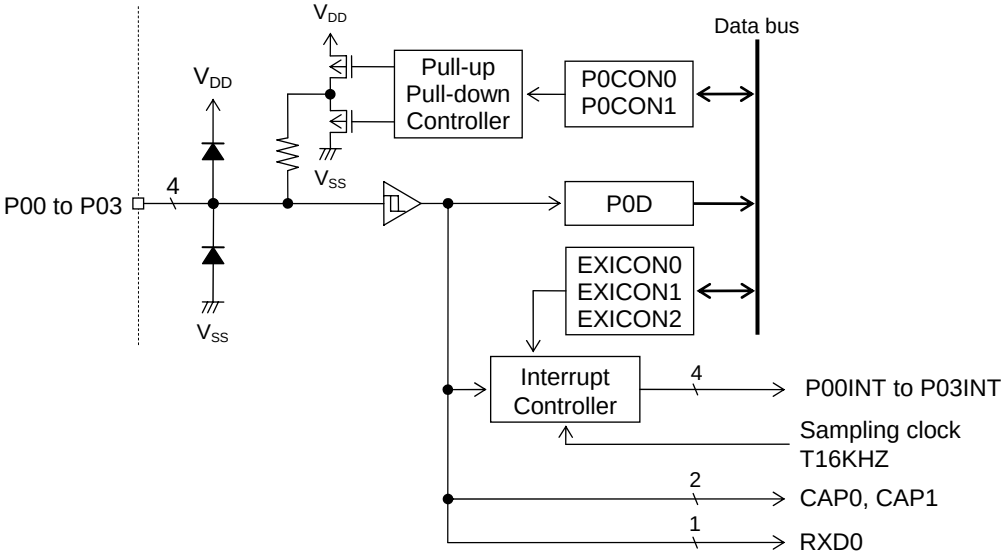
This LSI includes Port 0 (P00 to P03) which is a 4-bit input port.

17.1.1 Features

- All bits support a maskable interrupt function.
- Allows selection of interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode for each bit.
- Allows selection of with/without interrupt sampling for each bit.(Sampling frequency: T16KHZ)
- Allows selection of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor for each bit.
- The P00 and P01 pins can be used as the trigger input pins of the capture circuit and the P02 pin can be used as the RXD0 input pin of UART0.

17.1.2 Configuration

Figure 17-1 shows the configuration of Port 0.



P0D	: Port 0 data register
P0CON0	: Port 0 control register 0
P0CON1	: Port 0 control register 1
EXICON0	: External interrupt control register 0
EXICON1	: External interrupt control register 1
EXICON2	: External interrupt control register 2

Figure 17-1 Configuration of Port 0

17.1.3 List of Pins

Pin name	I/O	Description
P00/EXI0/CAP0	I	Input port, External 0 interrupt, Capture 0 trigger signal input
P01/EXI1/CAP1	I	Input port, External 1 interrupt, Capture 1 trigger signal input
P02/EXI2/RXD0	I	Input port, External 2 interrupt, UART0 data input (RXD0)
P03/EXI3	I	Input port, External 3 interrupt

17.2 Description of Registers

17.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F204H	Port 0 data register	P0D	—	R	8	Depends on pin status
0F206H	Port 0 control register 0	P0CON0	P0CON	R/W	8/16	00H
0F207H	Port 0 control register 1	P0CON1		R/W	8	00H
0F020H	External interrupt control register 0	EXICON0	—	R/W	8	00H
0F021H	External interrupt control register 1	EXICON1	—	R/W	8	00H
0F022H	External interrupt control register 2	EXICON2	—	R/W	8	00H

17.2.2 Port 0 Data Register (P0D)

Address: 0F204H
Access: R
Access size: 8 bits
Initial value: Depends on pin status

	7	6	5	4	3	2	1	0
P0D	—	—	—	—	P03D	P02D	P01D	P00D
R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	x	x	x	x

P0D is a special function register (SFR) to only read the pin level of Port 0.

[Description of Bits]

- **P03D-P00D** (bits 3-0)
  The P03D to P00D bits are used to read the pin level of Port 0.

P00D	Description
0	P00 pin input: "L" level
1	P00 pin input: "H" level

P01D	Description
0	P01 pin input: "L" level
1	P01 pin input: "H" level

P02D	Description
0	P02 pin input: "L" level
1	P02 pin input: "H" level

P03D	Description
0	P03 pin input: "L" level
1	P03 pin input: "H" level

17.2.3 Port 0 Control Registers 0, 1 (P0CON0, P0CON1)

Address: 0F206H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P0CON0	—	—	—	—	P03C0	P02C0	P01C0	P00C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F207H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P0CON1	—	—	—	—	P03C1	P02C1	P01C1	P00C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P0CON0 and P0CON1 are special function registers (SFRs) to select the input mode of Port 0.

[Description of Bits]

- **P03C0-P00C0, P03C1-P00C1** (bits 3-0)
  The P03C0 to P00C0 bits and the P03C1 to P00C1 bits are used to select high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor. The P0nC0 bit and the P0nC1 bit determine the input mode of P0n (Example: When P02C0 = "0" and P02C1 = "1", P02 is in input mode with a pull-up resistor).

P03C1-P00C1	P03C0-P00C0	Description
0	0	High-impedance input mode (initial value)
0	1	Input mode with a pull-down resistor
1	0	Input mode with a pull-up resistor
1	1	High-impedance input mode

17.2.4 External Interrupt Control Registers 0, 1 (EXICON0, EXICON1)

Address: 0F020H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
EXICON0	—	—	—	—	P03E0	P02E0	P01E0	P00E0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F021H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
EXICON1	—	—	—	—	P03E1	P02E1	P01E1	P00E1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

EXICON0 and EXICON1 are special function registers (SFRs) to select an interrupt edge of Port 0.

[Description of Bits]

- **P03E0-P00E0, P03E1-P00E1** (bits 3-0)
  The P03E0 to P00E0 bits and the P03E1 to P00E1 bits are used to select interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode. The P0nE0 bit and the P0nE1 bit determine the interrupt mode of P0n (Example: When P02E0 = "0" and P02E1 = "1", P02 is in rising-edge interrupt mode).

P03E1-P00E1	P03E0-P00E0	Description
0	0	Interrupt disabled mode (initial value)
0	1	Falling-edge interrupt mode
1	0	Rising-edge interrupt mode
1	1	Both-edge interrupt mode

17.2.5 External Interrupt Control Register 2 (EXICON2)

Address: 0F022H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
EXICON2	—	—	—	—	P03SM	P02SM	P01SM	P00SM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

EXICON2 is a special function register (SFR) to select detection of signal edge for interrupts with or without sampling.

[Description of Bits]

- **P03SM-P00SM** (bits 3-0)
  The P03SM to P00SM bits are used to select detection of signal edge for Port 0 interrupts with or without sampling. The sampling clock is T16KHZ of the low-speed time base counter (LTBC).

P00SM	Description
0	Detects the input signal edge for a P00 interrupt without sampling (initial value).
1	Detects the input signal edge for a P00 interrupt with sampling.

P01SM	Description
0	Detects the input signal edge for a P01 interrupt without sampling (initial value).
1	Detects the input signal edge for a P01 interrupt with sampling.

P02SM	Description
0	Detects the input signal edge for a P02 interrupt without sampling (initial value).
1	Detects the input signal edge for a P02 interrupt with sampling.

P03SM	Description
0	Detects the input signal edge for a P03 interrupt without sampling (initial value).
1	Detects the input signal edge for a P03 interrupt with sampling.

Note:
In STOP mode, since the 16 kHz sampling clock stops, no sampling is performed regardless of the values set in P00SM to P03SM.

17.3 Description of Operation

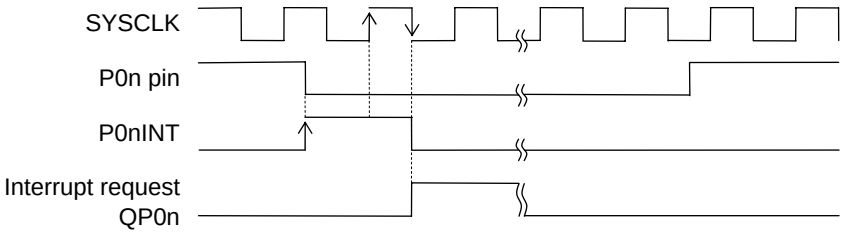
For each pin of Port 0, the setting of the Port 0 control registers 0 and 1 (P0CON0 and P0CON1) allows selection of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor. High-impedance input mode is selected at system reset.
The pin level of Port 0 can be read by reading the Port 0 data register (P0D)

17.3.1 External Interrupt/Capture Function

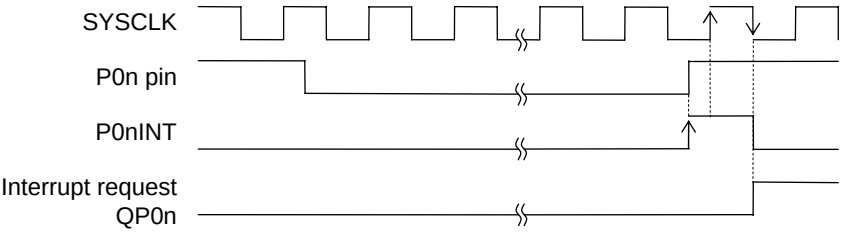
The Port 0 pins (P00, P01, P02, P03) can be used for P00 to P03 interrupts (P00INT to P03INT). The P00 to P03 interrupts are maskable and interrupt enable or disable can be selected. For details of interrupts, see Chapter 5, "Interrupts".
The P00 and P01 pins can be used as the trigger input for the capture circuit and the P02 pin can be used as the RXD0 input pin of UART0.
For the capture function and the UART function, see Chapter 8, "Capture," and Chapter 14, "UART," respectively.

17.3.2 Interrupt Request

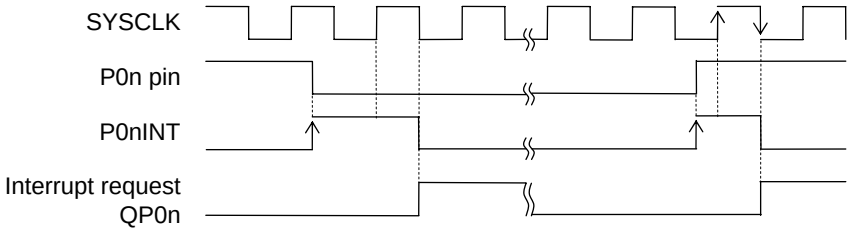
When an interrupt edge selected with the external interrupt control register 0, 1, or 2 (EXICON0, EXICON1, or EXICON2) occurs at a Port 0 pin, a maskable P00 (P01, P02, or P03) interrupt (P00INT, P01INT, P02INT, or P03INT). Figure 17-2 shows the P00 to P03 interrupt generation timing in rising-edge interrupt mode, in falling-edge interrupt mode, and in both-edge interrupt mode without sampling and the P00 to P03 interrupt generation timing in rising-edge interrupt mode with sampling.



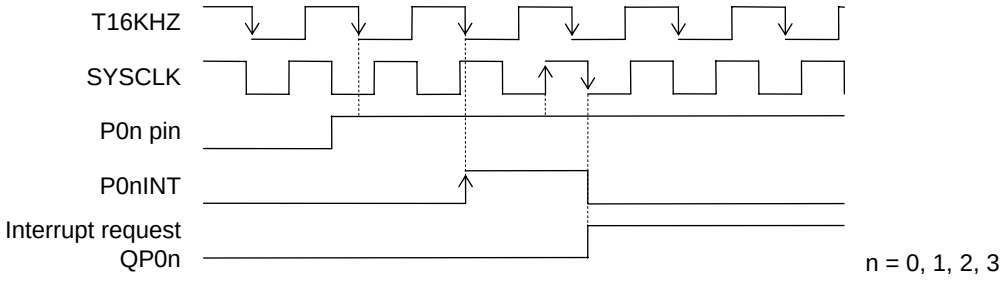
(a) When Falling-Edge Interrupt Mode without Sampling is Selected



(b) When Rising-Edge Interrupt Mode without Sampling is Selected



(c) When Both-Edge Interrupt Mode without Sampling is Selected



(d) When Rising-Edge Interrupt Mode with Sampling is Selected

Figure 17-2 P00 to P03 Interrupt Generation Timing

Chapter 18

Port 1

18. Port 1

18.1 Overview

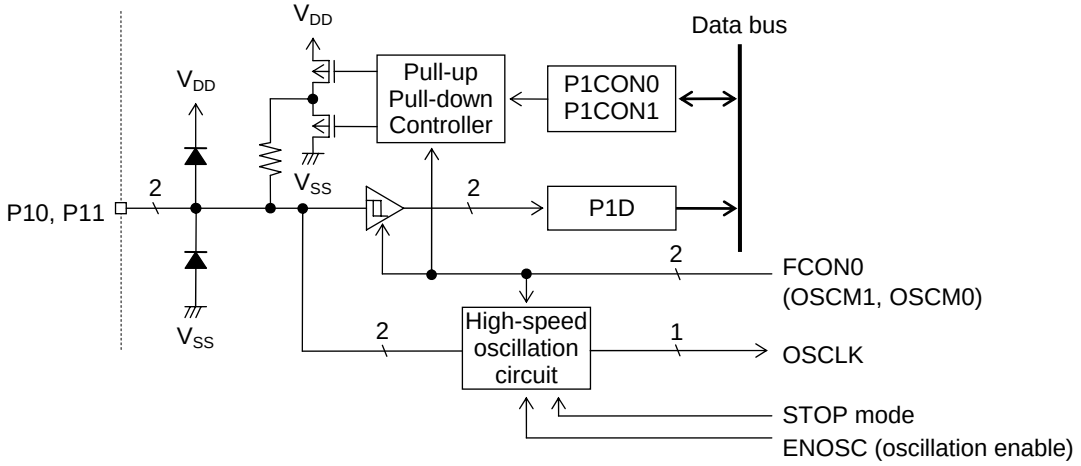
This LSI incorporates a 2-bit input port, Port 1 (P10, P11).
Port 1 can have a high-speed oscillation pin or an external clock input pin as a secondary function. When the port is used as a high-speed oscillation pin, the P11 pin functions as an output pin if crystal/ceramic oscillation mode is selected with the OSCM1–0 bits of the FCON0 register.
For high-speed oscillation and external clock input, see Chapter 6, "Clock Generation Circuit".

18.1.1 Features

- Allows selection of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor for each bit.
- Allows selection of a high-speed crystal/ceramic resonator pin or an external clock input pin as a secondary function.

18.1.2 Configuration

Figure 18-1 shows the configuration of Port 1.



P1D : Port 1 data register
P1CON0 : Port 1 control register 0
P1CON1 : Port 1 control register 1

Figure 18-1 Configuration of Port 1

18.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function
P10/OSC0	I	Input port	High-speed crystal/ceramic oscillation pin, external clock input pin
P11/OSC1	I/O	Input port	High-speed crystal/ceramic oscillation pin

18.2 Description of Registers

18.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F208H	Port 1 data register	P1D	—	R	8	Depends on pin status
0F20AH	Port 1 control register 0	P1CON0	P1CON	R/W	8/16	00H
0F20BH	Port 1 control register 1	P1CON1		R/W	8	00H

18.2.2 Port 1 Data Register (P1D)

Address: 0F208H
Access: R
Access size: 8 bits
Initial value: Depends on pin status

	7	6	5	4	3	2	1	0
P1D	—	—	—	—	—	—	P11D	P10D
R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	x	x

P1D is a special function register (SFR) dedicated to read the input level of the Port 1 pin.

[Description of Bits]

- **P11D, P10D** (bits 1, 0)
  The P11D and P10D bits are used to read the input level of the Port 1 pin.

P11D	Description
0	Input level of the P11 pin: "L"
1	Input level of the P11 pin: "H"

P10D	Description
0	Input level of the P10 pin: "L"
1	Input level of the P10 pin: "H"

18.2.3 Port 1 Control Registers 0, 1 (P1CON0, P1CON1)

Address: 0F20AH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P1CON0	—	—	—	—	—	—	P11C0	P10C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F20BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P0CON1	—	—	—	—	—	—	P11C1	P10C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P1CON0 and P1CON1 are special function registers (SFRs) to select the input mode of Port 1.

[Description of Bits]

- **P11C0, P10C0, P11C1, P00C1** (bits 1-0)
  The P11C0, P10C0, P11C1 and P00C1 bits are used to select high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor.

P11C1	P11C0	Description
0	0	P11 pin: high-impedance input mode (initial value)
0	1	P11 pin: input mode with a pull-down resistor
1	0	P11 pin: input mode with a pull-up resistor
1	1	P11 pin: high-impedance input mode

P10C1	P10C0	Description
0	0	P10 pin: high-impedance input mode (initial value)
0	1	P10 pin: input mode with a pull-down resistor
1	0	P10 pin: input mode with a pull-up resistor
1	1	P10 pin: high-impedance input mode

Note:
When using P10 and P11 as crystal/ceramic oscillation pins, be sure to set the P10 and P11 pins to high-impedance input mode.
When using the P10 pin as an external clock input pin, set the P10 pin to high-impedance input mode so that the pull-up or pull-down resistor will not carry current.

18.3 Description of Operation

18.3.1 Input Port Function

For each pin of Port 1, one of high-impedance input mode, input mode with a pull-down resistor, and input mode with a pull-up resistor can be selected by setting the Port 1 control registers 0 and 1 (P1CON0 and P1CON1). At system reset, high-impedance input mode is selected as the initial state.
The input level of the Port 1 pin can be read by reading the Port 1 data register (P1D).

18.3.2 Secondary Function

A high-speed crystal/ceramic oscillation pin or an external clock input pin is assigned to Port 1 as a secondary function. Select high-speed crystal/ceramic oscillation mode or external clock input mode by using the high-speed clock mode select function of the OSCM1 and 0 bits of the frequency control register 0 (FCON0). In crystal/ceramic oscillation mode, both P10 and P11 pins are used as the pins for crystal/ceramic oscillation.
In external clock input mode, the P10 pin is used as the input pin of external clock and the P11 pin can be used as a general-purpose input port.

Note:
No port mode register is provided for switching between the primary function and the secondary function of Port 1. When using the Port 1 pins as high-speed oscillation pins, pin mode is switched according to the values set in the OSCM1 and OSCM0 bits of the FCON0 register.
See Chapter 6, "Clock Generation Circuit," for the details of the FCON0 register, high-speed oscillation, and external clock input.

Chapter 19

Port 2

19. Port 2

19.1 Overview

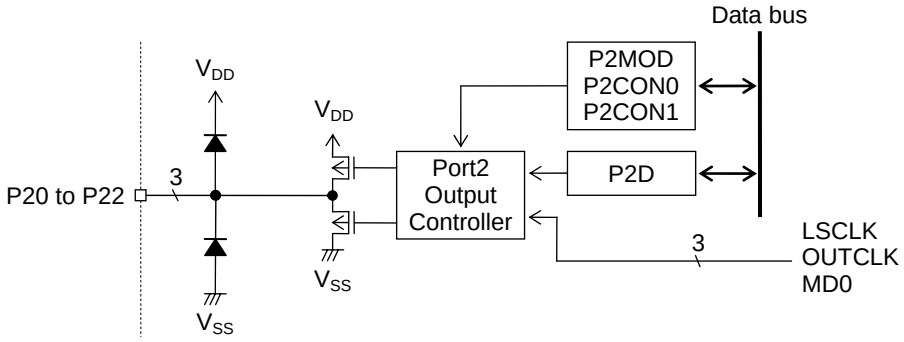
This LSI includes 3-bit Port 2 (P20 to P22) dedicated to output.
Port 2 can output low-speed clock (LSCLK), high-speed output clock (OUTCLK), and melody as a secondary function. For clock output and melody 0 (MD0) output, see Chapter 6, "Clock Generation Circuit" and Chapter 23, "Melody Driver", respectively.

19.1.1 Features

- Allows direct LED drive.
- Allows selection of high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode for each bit.
- Allows output of low-speed clock (LSCLK), high-speed clock (OUTCLK), or melody 0 (MD0) as a secondary function.

19.1.2 Configuration

Figure 19-1 shows the configuration of Port 2.



P2D : Port 2 data register
P2CON0 : Port 2 control register 0
P2CON1 : Port 2 control register 1
P2MOD : Port 2 mode register

Figure 19-1 Configuration of Port 2

19.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function
P20/LED0/LSCLK	O	Output port, Direct LED drive	Low-speed clock output (LSCLK)
P21/LED1/OUTCLK	O	Output port, Direct LED drive	High-speed clock output (OUTCLK)
P22/LED2/MD0	O	Output port, Direct LED drive	Melody 0 output (MD0)

19.2 Description of Registers

19.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F210H	Port 2 data register	P2D	—	R/W	8	00H
0F212H	Port 2 control register 0	P2CON0	P2CON	R/W	8/16	00H
0F213H	Port 2 control register 1	P2CON1		R/W	8	00H
0F214H	Port 2 mode register	P2MOD	—	R/W	8	00H

19.2.2 Port 2 Data Register (P2D)

Address: 0F210H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2D	—	—	—	—	—	P22D	P21D	P20D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2D is a special function register (SFR) to set the output value of Port 2. The value of this register is output to Port 2. The value written to P2D is readable.

[Description of Bits]

- **P22D-P20D** (bits 2-0)
  The P22D to P20D bits are used to set the output value of the Port 2 pin.

P22D	Description
0	Output level of the P22 pin: "L"
1	Output level of the P22 pin: "H"

P21D	Description
0	Output level of the P21 pin: "L"
1	Output level of the P21 pin: "H"

P20D	Description
0	Output level of the P20 pin: "L"
1	Output level of the P20 pin: "H"

19.2.3 Port 2 control registers 0, 1 (P2CON0, P2CON1)

Address: 0F212H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2CON0	—	—	—	—	—	P22C0	P21C0	P20C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F213H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2CON1	—	—	—	—	—	P22C1	P21C1	P20C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2CON0 and P2CON1 are special function registers (SFRs) to select the output state of the output pin Port 2.

[Description of Bits]

- **P22C0-P20C0, P22C1-P20C1** (bits 2-0)
  The P22C0 to P20C0 and P22C1 to P20C1 bits are used to select high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode.
  To directly drive LEDs, select N-channel open drain output mode.

P22C1	P22C0	Description
0	0	P22 pin: In high-impedance output mode (initial value)
0	1	P22 pin: In P-channel open drain output mode
1	0	P22 pin: In N-channel open drain output mode
1	1	P22 pin: In CMOS output mode

P21C1	P21C0	Description
0	0	P21 pin: In high-impedance output mode (initial value)
0	1	P21 pin: In P-channel open drain output mode
1	0	P21 pin: In N-channel open drain output mode
1	1	P21 pin: In CMOS output mode

P20C1	P20C0	Description
0	0	P20 pin: In high-impedance output mode (initial value)
0	1	P20 pin: In P-channel open drain output mode
1	0	P20 pin: In N-channel open drain output mode
1	1	P20 pin: In CMOS output mode

19.2.4 Port 2 Mode Register (P2MOD)

Address: 0F214H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2MOD	—	—	—	—	—	P22MD	P21MD	P20MD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2MOD is a special function register (SFR) to select the primary function or the secondary function of Port 2

[Description of Bits]

- **P22MD** (bit 2)
  The P22MD bit is used to select the primary function or the secondary function of the P22 pin.

P22MD	Description
0	General-purpose output port function (initial value)
1	Melody 0 (MD0) output function

- **P21MD** (bit 1)
  The P21MD bit is used to select the primary function or the secondary function of the P21 pin.

P21MD	Description
0	General-purpose output port function (initial value)
1	High-speed output clock (OUTCLK) output function

- **P20MD** (bit 0)
  The P20MD bit is used to select the primary function or the secondary function of the P20 pin.

P20MD	Description
0	General-purpose output port function (initial value)
1	Low-speed clock (LSCLK) output function

Note:
The output characteristics of port2(P20, P21 and P22) corresponds to VOL1 and VOH1 when each bit (P20MD, P21MD, P22MD) is "1" , and corresponds to VOL2 and VOH2 when the bit is "0", which are shown in Appendix C, "Electrical Characteristics".

19.3 Description of Operation

19.3.1 Output Port Function

For each pin of Port 2, any one of high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, and CMOS output mode can be selected by setting the Port 2 control registers 0 and 1 (P2CON0 and P2CON1). At a system reset, high-impedance output mode is selected as the initial state.
Depending of the value set in the Port 2 data register (P2D), a "L" level or "H" level signal is output to each pin of Port 2.

19.3.2 Secondary Function

Low-speed clock (LSCLK) output, High-speed output clock (OUTCLK) output, or melody 0 (MD0) output is assigned to Port 2 as a secondary function. The secondary function can be used by setting the P22MD to P20MD bits of the Port 2 mode register (P2MOD) to "1".

Chapter 20

Port 3

20. Port 3

20.1 Overview

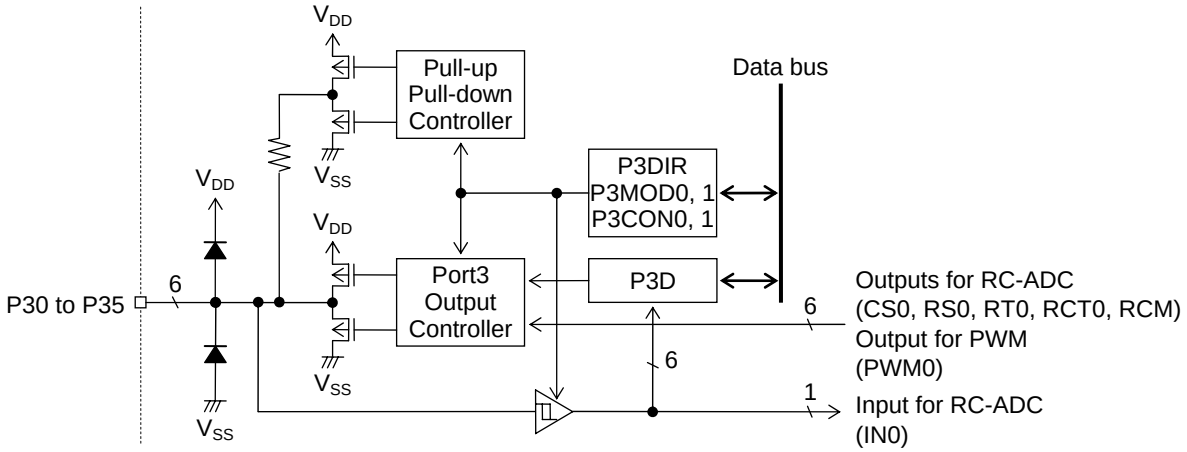
This LSI includes Port 3 (P30 to P35), which is a 6-bit input/output port.
This port can also be used as the RC-ADC (channel 0) oscillation pins (IN0, CS0, RS0, RT0, RCT0, RCM) and the PWM output pin in secondary and tertiary modes.
For RC-ADC and PWM, see Chapter 24, "RC Oscillation Type A/D converter", and Chapter 11, "PWM".

20.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode for each bit.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode for each bit.
- The RC-ADC (channel 0) oscillation pins (IN0, CS0, RS0, RT0, RCT0, RCM) and the PWM output pin (PWM0) can be used as the secondary functions.

20.1.2 Configuration

Figure 20-1 shows the configuration of Port 3.



P3D	: Port 3 data register
P3DIR	: Port 3 direction register
P3CON0	: Port 3 control register 0
P3CON1	: Port 3 control register 1
P3MOD0	: Port 3 mode register 0
P3MOD1	: Port 3 mode register 1

Figure 20-1 Configuration of Port 3

20.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function
P30/IN0	I/O	Input/output port	Oscillation waveform input pin for RC-ADC	—
P31/CS0	I/O	Input/output port	Reference capacitor connection pin for RC-ADC	—
P32/RS0	I/O	Input/output port	Reference resistor connection pin for RC-ADC	—
P33/RT0	I/O	Input/output port	Resistor sensor connection pin for measurement for RC-ADC	—
P34/RCT0/PWM0	I/O	Input/output port	Resistor/capacitor sensor connection pin for measurement for RC-ADC	PWM0 output pin
P35/RCM	I/O	Input/output port	RC oscillation monitor pin for RC-ADC	—

20.2 Description of Registers

20.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F218H	Port 3 data register	P3D	—	R/W	8	00H
0F219H	Port 3 direction register	P3DIR	—	R/W	8	00H
0F21AH	Port 3 control register 0	P3CON0	P3CON	R/W	8/16	00H
0F21BH	Port 3 control register 1	P3CON1		R/W	8	00H
0F21CH	Port 3 mode register 0	P3MOD0	P3MOD	R/W	8/16	00H
0F21DH	Port 3 mode register 1	P3MOD1		R/W	8	00H

20.2.2 Port 3 data register (P3D)

Address: 0F218H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3D	—	—	P35D	P34D	P33D	P32D	P31D	P30D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3D is a special function register (SFR) to set the value to be output to the Port 3 pin or to read the input level of the Port 3. In output mode, the value of this register is output to the Port 3 pin. The value written to P3D is readable. In input mode, the input level of the Port 3 pin is read when P3D is read. Output mode or input mode is selected by using the port direction register (P3DIR) described later.

[Description of Bits]

- **P35D-P30D** (bits 5-0)
  The P35D to P30D bits are used to set the output value of the Port 3 pin in output mode and to read the pin level of the Port 3 pin in input mode.

P35D	Description
0	Output or input level of the P35 pin: "L"
1	Output or input level of the P35 pin: "H"

P34D	Description
0	Output or input level of the P34 pin: "L"
1	Output or input level of the P34 pin: "H"

P33D	Description
0	Output or input level of the P33 pin: "L"
1	Output or input level of the P33 pin: "H"

P32D	Description
0	Output or input level of the P32 pin: "L"
1	Output or input level of the P32 pin: "H"

P31D	Description
0	Output or input level of the P31 pin: "L"
1	Output or input level of the P31 pin: "H"

P30D	Description
0	Output or input level of the P30 pin: "L"
1	Output or input level of the P30 pin: "H"

20.2.3 Port 3 Direction Register (P3DIR)

Address: 0F219H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3DIR	—	—	P35DIR	P34DIR	P33DIR	P32DIR	P31DIR	P30DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3DIR is a special function register (SFR) to select the input/output mode of Port 3.

[Description of Bits]

- **P35DIR-P30DIR** (bits 5-0)
  The P35DIR to P30DIR pins are used to set the input/output direction of the Port 3 pin.

P35DIR	Description
0	P35 pin: Output (initial value)
1	P35 pin: Input

P34DIR	Description
0	P34 pin: Output (initial value)
1	P34 pin: Input

P33DIR	Description
0	P33 pin: Output (initial value)
1	P33 pin: Input

P32DIR	Description
0	P32 pin: Output (initial value)
1	P32 pin: Input

P31DIR	Description
0	P31 pin: Output (initial value)
1	P31 pin: Input

P30DIR	Description
0	P30 pin: Output (initial value)
1	P30 pin: Input

20.2.4 Port 3 control registers 0, 1 (P3CON0, P3CON1)

Address: 0F21AH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3CON0	—	—	P35C0	P34C0	P33C0	P32C0	P31C0	P30C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F21BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3CON1	—	—	P35C1	P34C1	P33C1	P32C1	P31C1	P30C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3CON0 and P3CON1 are special function registers (SFRs) to select input/output state of the Port 3 pin. The input/output state is different between input mode and output mode. Input or output is selected by using the P3DIR register.

[Description of Bits]

- **P35C1-P30C1, P35C0-P30C0** (bits 5-0)
  The P35C1 to P30C1 pins and the P35C0 to P30C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

		When output mode is selected (P35DIR bit = "0")	When input mode is selected (P35DIR bit = "1")
P35C1	**P35C0**	Description	
0	0	P35 pin: High-impedance output (initial value)	P35 pin: High-impedance input
0	1	P35 pin: P-channel open drain output	P35 pin: Input with a pull-down resistor
1	0	P35 pin: N-channel open drain output	P35 pin: Input with a pull-up resistor
1	1	P35 pin: CMOS output	P35 pin: High-impedance input

		When output mode is selected (P34DIR bit = "0")	When input mode is selected (P34DIR bit = "1")
P34C1	**P34C0**	Description	
0	0	P34 pin: High-impedance output (initial value)	P34 pin: High-impedance input
0	1	P34 pin: P-channel open drain output	P34 pin: Input with a pull-down resistor
1	0	P34 pin: N-channel open drain output	P34 pin: Input with a pull-up resistor
1	1	P34 pin: CMOS output	P34 pin: High-impedance input

		When output mode is selected (P33DIR bit = "0")	When input mode is selected (P33DIR bit = "1")
P33C1	**P33C0**	Description	
0	0	P33 pin: High-impedance output (initial value)	P33 pin: High-impedance input
0	1	P33 pin: P-channel open drain output	P33 pin: Input with a pull-down resistor
1	0	P33 pin: N-channel open drain output	P33 pin: Input with a pull-up resistor
1	1	P33 pin: CMOS output	P33 pin: High-impedance input

		When output mode is selected (P32DIR bit = "0")	When input mode is selected (P32DIR bit = "1")
P32C1	**P32C0**	Description	
0	0	P32 pin: High-impedance output (initial value)	P32 pin: High-impedance input
0	1	P32 pin: P-channel open drain output	P32 pin: Input with a pull-down resistor
1	0	P32 pin: N-channel open drain output	P32 pin: Input with a pull-up resistor
1	1	P32 pin: CMOS output	P32 pin: High-impedance input

		When output mode is selected (P31DIR bit = "0")	When input mode is selected (P31DIR bit = "1")
P31C1	**P31C0**	Description	
0	0	P31 pin: High-impedance output (initial value)	P31 pin: High-impedance input
0	1	P31 pin: P-channel open drain output	P31 pin: Input with a pull-down resistor
1	0	P31 pin: N-channel open drain output	P31 pin: Input with a pull-up resistor
1	1	P31 pin: CMOS output	P31 pin: High-impedance input

		When output mode is selected (P30DIR bit = "0")	When input mode is selected (P30DIR bit = "1")
P30C1	**P30C0**	Description	
0	0	P30 pin: High-impedance output (initial value)	P30 pin: High-impedance input
0	1	P30 pin: P-channel open drain output	P30 pin: Input with a pull-down resistor
1	0	P30 pin: N-channel open drain output	P30 pin: Input with a pull-up resistor
1	1	P30 pin: CMOS output	P30 pin: High-impedance input

20.2.5 Port 3 mode registers 0, 1 (P3MOD0, P3MOD1)

Address: 0F21CH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3MOD0	—	—	P35MD0	P34MD0	P33MD0	P32MD0	P31MD0	P30MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F21DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3MOD1	—	—	P35MD1	P34MD1	P33MD1	P32MD1	P31MD1	P30MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3MOD0 and P3MOD1 are special function registers (SFRs) to select the primary, secondary, or tertiary function of Port 3.

[Description of Bits]

- **P35MD1, P35MD0** (bit 5)
  The P35MD1 and P35MD0 bits are used to select the primary or secondary function of the P35 pin.

P35MD1	P35MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	RC oscillation monitor pin for RC-ADC
1	0	Prohibited
1	1	Prohibited

- **P34MD1, P34MD0** (bit 4)
  The P34MD1 and P34MD0 bits are used to select the primary, secondary, or tertiary function of the P34 pin.

P34MD1	P34MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Resistor/capacitor sensor connection pin for measurement for RC-ADC (channel 0)
1	0	PWM0 output pin
1	1	Prohibited

- **P33MD1, P33MD0** (bit 3)
  The P33MD1 and P33MD0 bits are used to select the primary or secondary function of the P33 pin.

P33MD1	P33MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Resistor/capacitor sensor connection pin for measurement for RC-ADC (channel 0)
1	0	Prohibited
1	1	Prohibited

- **P32MD1, P32MD0** (bit 2)
  The P32MD1 and P32MD0 bits are used to select the primary or secondary function of the P32 pin.

P32MD1	P32MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Reference resistor connection pin for RC-ADC (channel 0)
1	0	Prohibited
1	1	Prohibited

- **P31MD1, P31MD0** (bit 1)
  The P31MD1 and P31MD0 bits are used to select the primary or secondary function of the P31 pin.

P31MD1	P31MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Reference capacitor connection pin for RC-ADC (channel 0)
1	0	Prohibited
1	1	Prohibited

- **P30MD1, P30MD0** (bit 0)
  The P30MD1 and P30MD0 bits are used to select the primary or secondary function of the P30 pin.

P30MD1	P30MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	RC oscillation waveform input pin for RC-ADC (channel 0)
1	0	Prohibited
1	1	Prohibited

Note:
If any bit combination out of the above is set to "Prohibited" and the corresponding bit of the port 3 is sepecified to output mode (selected in port3 control register), status of corresponding pin is fixed, regardless the contents of Port3 register (P3D)

High-impedance output mode: High-impedance
P-channel open drain output mode: High-impedance
N-channel open drain output mode: Fixed to "L"
CMOS output mode: High-impedance: Fixed to "L"

When using RC-ADC as the secondary function, specify each pin be "High-impedance input" even the RC oscillation monitor pin. Pull-up or Pull-down input makes drawing the current.

20.3 Description of Operation

20.3.1 Input/Output Port Functions

For each pin of Port 3, either output or input is selected by setting the Port 3 direction register (P3DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 3 control registers 0 and 1 (P3CON0 and P3CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 3 control registers 0 and 1 (P3CON0 and P3CON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port 3 depending on the value set by the Port 3 data register (P3D).
In input mode, the input level of each pin of Port 3 can be read from the Port 3 data register (P3D).

20.3.2 Secondary and Tertiary Functions

Secondary and tertiary functions are assigned to Port 3 as the RC-ADC (channel 0) oscillation pins (IN0, CS0, RS0, RT0, RCT0, RCM) and the PWM output pin (PWM0). These pins can be used in a secondary or tertiary function mode by setting the P35MD0 to P30MD0 bits and the P35MD1 to P30MD1 bits of the Port 3 mode registers (P3MOD0, P3MOD1).

Note:
All the port 3 pins except P35/RCM are configured as pins dedicated to the RC-ADC function during A/D conversion. Therefore, if there is any unused pin, that pin cannot be used as its primary function during A/D conversion. For the RC-ADC, see Chapter 24, "RC Oscillation Type A/D Converter".

Chapter 21

Port 4

21. Port 4

21.1 Overview

This LSI includes Port 4 (P40 to P47) which is an 8-bit input/output port.
This port can have the I2C bus, RC-ADC, synchronous serial port, and PWM output functions as secondary and tertiary functions.
See the following chapters for reference:

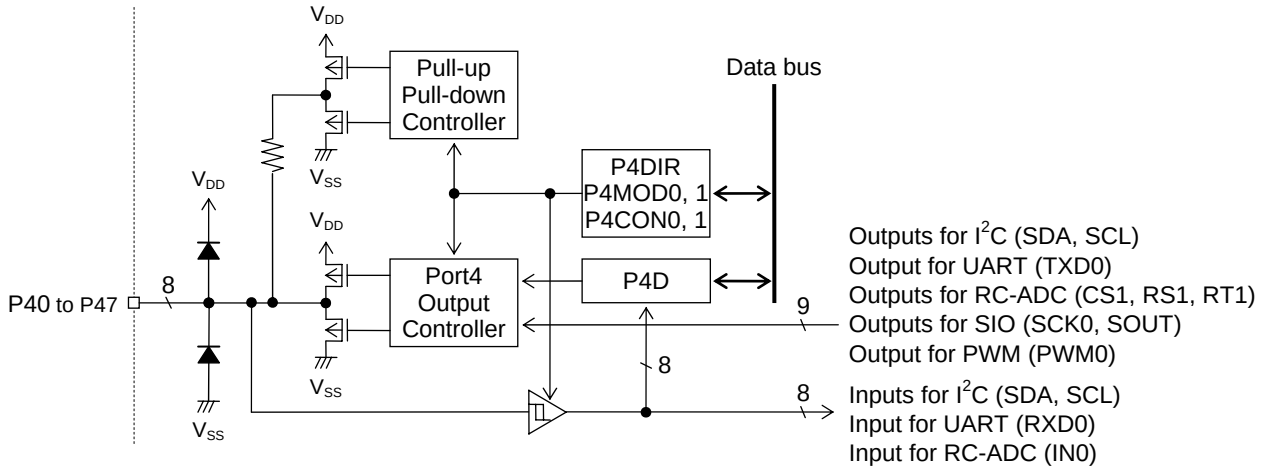
I2C bus:	Chapter 15 "I2C Bus Interface"
UART:	Chapter 14 "UART"
RC-ADC:	Chapter 24 "RC Oscillation Type A/D Converter"
Synchronous serial port:	Chapter 13 "Synchronous Serial Port"
PWM:	Chapter 11 "PWM"

21.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- The P44 and P45 pins can be used as external clock input pins for the timer and PWM.
- The I2C bus interface pins (SDA, SCL), UART pins (RXD0, TXD0), RC-ADC (channel 1) oscillation pins (IN1, CS1, RS1, RT1), synchronous serial port pins (SIN0, SCK0, SOUT0), and PWM output pin (PWM0) can be used as the secondary functions.

21.1.2 Configuration

Figure 21-1 shows the configuration of Port 4.



P4D	: Port 4 data register
P4DIR	: Port 4 direction register
P4CON0	: Port 4 control register 0
P4CON1	: Port 4 control register 1
P4MOD0	: Port 4 mode register 0
P4MOD1	: Port 4 mode register 1

Figure 21-1 Configuration of Port 4

21.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function
P40/SDA/SIN0	I/O	Input/output port	I^2C bus 0 data input/output pin	SSIO0 data input pin
P41/SCL/SCK0	I/O	Input/output port	I^2C bus 0 clock input/output pin	SSIO0 clock input/output pin
P42/RXD0/SOUT0	I/O	Input/output port	UART0 data input pin	SSIO0 data output pin
P43/TXD0/PWM0	I/O	Input/output port	UART0 data output pin	PWM0 output pin
P44/ T02P0CK /IN1/SIN0/	I/O	Input/output port, Timer 0/Timer 2/ PWM0 external clock	RC oscillation waveform input pin for RC-ADC	SSIO0 data input pin
P45/ T13P1CK /CS1/SCK0/	I/O	Input/output port, Timer 1/Timer 3 external clock	Reference capacitor connection pin for RC-ADC	SSIO0 clock input/output pin
P46/RS1/SOUT0	I/O	Input/output port	Reference resistor connection pin for RC-ADC	SSIO0 data output pin
P47/RT1	I/O	Input/output port	Resistor sensor connection pin for measurement for RC-ADC	—

21.2 Description of Registers

21.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F220H	Port 4 data register	P4D	—	R/W	8	00H
0F221H	Port 4 direction register	P4DIR	—	R/W	8	00H
0F222H	Port 4 control register 0	P4CON0	P4CON	R/W	8/16	00H
0F223H	Port 4 control register 1	P4CON1		R/W	8	00H
0F224H	Port 4 mode register 0	P4MOD0	P4MOD	R/W	8/16	00H
0F225H	Port 4 mode register 1	P4MOD1		R/W	8	00H

21.2.2 Port 4 Data Register (P4D)

Address: 0F220H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4D	P47D	P46D	P45D	P44D	P43D	P42D	P41D	P40D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4D is a special function register (SFR) to set the value to be output to the Port 4 pin or to read the input level of the Port 4. In output mode, the value of this register is output to the Port 4 pin. The value written to P4D is readable. In input mode, the input level of the Port 4 pin is read when P4D is read. Output mode or input mode is selected by using the port direction register (P4DIR) described later.

[Description of Bits]

- **P47D-P40D** (bits 7-0)
  The P47D to P40D bits are used to set the output value of the Port 4 pin in output mode and to read the pin level of the Port 4 pin in input mode.

P47D	Description
0	Output or input level of the P47 pin: "L"
1	Output or input level of the P47 pin: "H"

P46D	Description
0	Output or input level of the P46 pin: "L"
1	Output or input level of the P46 pin: "H"

P45D	Description
0	Output or input level of the P45 pin: "L"
1	Output or input level of the P45 pin: "H"

P44D	Description
0	Output or input level of the P44 pin: "L"
1	Output or input level of the P44 pin: "H"

P43D	Description
0	Output or input level of the P43 pin: "L"
1	Output or input level of the P43 pin: "H"

P42D	Description
0	Output or input level of the P42 pin: "L"
1	Output or input level of the P42 pin: "H"

P41D	Description
0	Output or input level of the P41 pin: "L"
1	Output or input level of the P41 pin: "H"

P40D	Description
0	Output or input level of the P40 pin: "L"
1	Output or input level of the P40 pin: "H"

21.2.3 Port 4 Direction Register (P4DIR)

Address: 0F221H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4DIR	P47DIR	P46DIR	P45DIR	P44DIR	P43DIR	P42DIR	P41DIR	P40DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4DIR is a special function register (SFR) to select the input/output mode of Port 4.

[Description of Bits]

- **P47DIR-P40DIR** (bits 7-0)
  The P47DIR to P40DIR pins are used to set the input/output direction of the Port 4 pin.

P47DIR	Description
0	P47 pin: Output (initial value)
1	P47 pin: Input

P46DIR	Description
0	P46 pin: Output (initial value)
1	P46 pin: Input

P45DIR	Description
0	P45 pin: Output (initial value)
1	P45 pin: Input

P44DIR	Description
0	P44 pin: Output (initial value)
1	P44 pin: Input

P43DIR	Description
0	P43 pin: Output (initial value)
1	P43 pin: Input

P42DIR	Description
0	P42 pin: Output (initial value)
1	P42 pin: Input

P41DIR	Description
0	P41 pin: Output (initial value)
1	P41 pin: Input

P40DIR	Description
0	P40 pin: Output (initial value)
1	P40 pin: Input

21.2.4 Port 4 Control Registers 0, 1 (P4CON0, P4CON1)

Address: 0F222H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4CON0	P47C0	P46C0	P45C0	P44C0	P43C0	P42C0	P41C0	P40C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F223H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4CON1	P47C1	P46C1	P45C1	P44C1	P43C1	P42C1	P41C1	P40C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4CON0 and P4CON1 are special function registers (SFRs) to select input/output state of the Port 4 pin. The input/output state is different between input mode and output mode. Input or output is selected by using the P4DIR register.

[Description of Bits]

- **P47C1-P40C1, P47C0-P40C0** (bits 7-0)
  The P47C1 to P40C1 pins and the P47C0 to P40C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P47 pin		When output mode is selected (P47DIR bit = "0")	When input mode is selected (P47DIR bit = "1")
P47C1	**P47C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P46 pin		When output mode is selected (P46DIR bit = "0")	When input mode is selected (P46DIR bit = "1")
P46C1	**P46C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P45 pin		When output mode is selected (P45DIR bit = "0")	When input mode is selected (P45DIR bit = "1")
P45C1	**P45C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P44 pin		When output mode is selected (P44DIR bit = "0")	When input mode is selected (P44DIR bit = "1")
P44C1	**P44C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P43 pin		When output mode is selected (P43DIR bit = "0")	When input mode is selected (P43DIR bit = "1")
P43C1	**P43C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P42 pin		When output mode is selected (P42DIR bit = "0")	When input mode is selected (P42DIR bit = "1")
P42C1	**P42C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P41 pin		When output mode is selected (P41DIR bit = "0")	When input mode is selected (P41DIR bit = "1")
P41C1	**P41C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P40 pin		When output mode is selected (P40DIR bit = "0")	When input mode is selected (P40DIR bit = "1")
P40C1	**P40C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

21.2.5 Port 4 Mode Registers 0, 1 (P4MOD0, P4MOD1)

Address: 0F224H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4MOD0	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	P42MD0	P41MD0	P40MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F225H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4MOD1	P47MD1	P47MD1	P45MD1	P44MD1	P43MD1	P42MD1	P41MD1	P40MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4MOD0 and P4MOD1 are special function registers (SFRs) to select the primary, secondary, or tertiary function of Port 4.

[Description of Bits]

- **P47MD1, P47MD0** (bit 7)
  The P47MD1 and P47MD0 bits are used to select the primary or secondary function of the P47 pin.

P47MD1	P47MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Resistor sensor connection pin for measurement for RC-ADC (channel 1)
1	0	Prohibited
1	1	Prohibited

- **P46MD1, P46MD0** (bit 6)
  The P46MD1 and P46MD0 bits are used to select the primary, secondary, or tertiary function of the P46 pin.

P46MD1	P46MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Reference resistor connection pin for RC-ADC (channel 1)
1	0	SIO0 data output pin
1	1	Prohibited

- **P45MD1, P45MD0** (bit 5)
  The P45MD1 and P45MD0 bits are used to select the primary, secondary, or tertiary function of the P45 pin.

P45MD1	P45MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Reference capacitor connection pin for RC-ADC (channel 1)
1	0	SIO0 clock input/output pin
1	1	Prohibited

- **P44MD1, P44MD0** (bit 4)
  The P44MD1 and P44MD0 bits are used to select the primary, secondary, or tertiary function of the P44 pin.

P44MD1	P44MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	RC oscillation waveform input pin for RC-AD (channel 1)
1	0	SIO0 data input pin
1	1	Prohibited

- **P43MD1, P43MD0** (bit 3)
  The P43MD1 and P43MD0 bits are used to select the primary, secondary, or tertiary function of the P43 pin.

P43MD1	P43MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	UART0 data output pin
1	0	PWM0 output pin
1	1	Prohibited

- **P42MD1, P42MD0** (bit 2)
  The P42MD1 and P42MD0 bits are used to select the primary, secondary, or tertiary function of the P42 pin.

P42MD1	P42MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	UART0 input pin
1	0	SIO0 data output pin
1	1	Prohibited

- **P41MD1, P41MD0** (bit 1)
  The P41MD1 and P41MD0 bits are used to select the primary, secondary, or tertiary function of the P41 pin.

P41MD1	P41MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	I^2C bus 0 clock input/output pin
1	0	SIO0 clock input/output pin
1	1	Prohibited

- **P40MD1, P40MD0** (bit 0)
  The P40MD1 and P40MD0 bits are used to select the primary, secondary, or tertiary function of the P40 pin.

P40MD1	P40MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	I^2C bus 0 data input/output pin
1	0	SIO0 data input pin
1	1	Prohibited

Note:
If any bit combination out of the above is set to "Prohibited" and the corresponding bit of the port 4 is specified to output mode (selected in port4 control register), status of corresponding pin is fixed, regardless the contents of Port4 register (P4D)

High-impedance output mode: High-impedance
P-channel open drain output mode: High-impedance
N-channel open drain output mode: Fixed to "L"
CMOS output mode: High-impedance: Fixed to "L"

When using RC-ADC as the secondary function, specify each pin be "High-impedance input" even the RC oscillation monitor pin. Pull-up or Pull-down input makes drawing the current.

21.3 Description of Operation

21.3.1 Input/Output Port Functions

For each pin of Port 4, either output or input is selected by setting the Port 4 direction register (P4DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 4 control registers 0 and 1 (P4CON0 and P4CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 4 control registers 0 and 1 (P4CON0 and P4CON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port 4 depending on the value set by the Port 4 data register (P4D).
In input mode, the input level of each pin of Port 4 can be read from the Port 4 data register (P4D).

21.3.2 Secondary and Tertiary Functions

Secondary and tertiary functions are assigned to Port 4 as the I2C bus 0 pins (SDA, SCL), UART 0 pins (RXD0, TXD0), RC-ADC (channel 1) oscillation pins (IN1, CS1, RS1, RT1), synchronous serial port 0 pins (SIN0, SCK0, SOUT), and the PWM output pin (PWM0). These pins can be used in a secondary or tertiary function mode by setting the P47MD0 to P40MD0 bits and the P47MD1 to P40MD1 bits of the Port 4 mode registers (P4MOD0, P4MOD1).

Note:
The P44 to P47 pins of port 4 are configured as pins dedicated to the RC-ADC function during A/D conversion. Therefore, if there is any unused pin, that pin cannot be used during A/D conversion. For the RC-ADC, see Chapter 24, "RC Oscillation Type A/D Converter".

Chapter 22

Port A

22. Port A

22.1 Overview

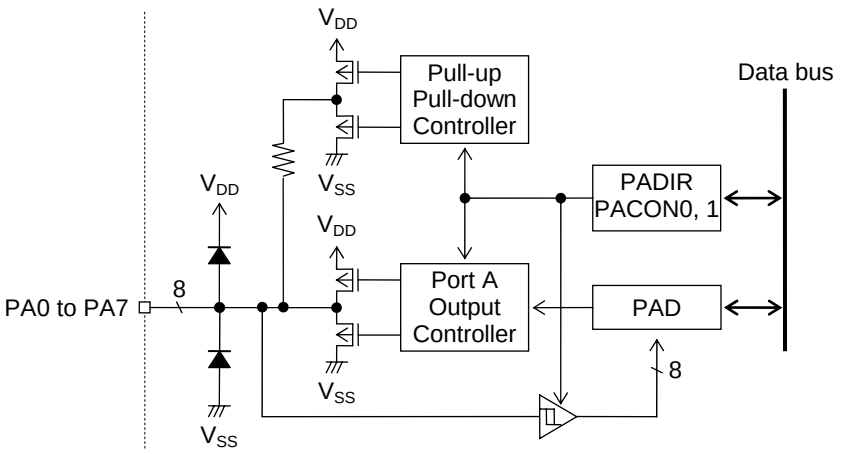
This LSI (ML610Q421/ML610421 only) includes Port A (PA0 to PA7) which is an 8-bit input/output port.
This function is not included in the ML610Q422/ML610422.

22.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.

22.1.2 Configuration

Figure 22-1 shows the configuration of Port A.



PAD : Port A data register
PADIR : Port A direction register
PACON0 : Port A control register 0
PACON1 : Port A control register 1

Figure 22-1 Configuration of Port A

22.1.3 List of Pins

Pin name	I/O	Description
PA0	I/O	Input/output port
PA1	I/O	Input/output port
PA2	I/O	Input/output port
PA3	I/O	Input/output port
PA4	I/O	Input/output port
PA5	I/O	Input/output port
PA6	I/O	Input/output port
PA7	I/O	Input/output port

22.2 Description of Registers

22.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F250H	Port A data register	PAD	—	R/W	8	00H
0F251H	Port A direction register	PADIR	—	R/W	8	00H
0F252H	Port A control register 0	PACON0	PACON	R/W	8/16	00H
0F253H	Port A control register 1	PACON1		R/W	8	00H

22.2.2 Port A Data Register (PAD)

Address: 0F250H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PAD	PA7D	PA6D	PA5D	PA4D	PA3D	PA2D	PA1D	PA0D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PAD is a special function register (SFR) to set the value to be output to the Port A pin or to read the input level of the Port A. In output mode, the value of this register is output to the Port A pin. The value written to PAD is readable. In input mode, the input level of the Port A pin is read when PAD is read. Output mode or input mode is selected by using the port direction register (PADIR) described later.

[Description of Bits]

- **PA7D-PA0D** (bits 7-0)
  The PA7D to PA0D bits are used to set the output value of the Port A pin in output mode and to read the pin level of the Port A pin in input mode.

PA7D	Description
0	Output or input level of the PA7 pin: "L"
1	Output or input level of the PA7 pin: "H"

PA6D	Description
0	Output or input level of the PA6 pin: "L"
1	Output or input level of the PA6 pin: "H"

PA5D	Description
0	Output or input level of the PA5 pin: "L"
1	Output or input level of the PA5 pin: "H"

PA4D	Description
0	Output or input level of the PA4 pin: "L"
1	Output or input level of the PA4 pin: "H"

PA3D	Description
0	Output or input level of the PA3 pin: "L"
1	Output or input level of the PA3 pin: "H"

PA2D	Description
0	Output or input level of the PA2 pin: "L"
1	Output or input level of the PA2 pin: "H"

PA1D	Description
0	Output or input level of the PA1 pin: "L"
1	Output or input level of the PA1 pin: "H"

PA0D	Description
0	Output or input level of the PA0 pin: "L"
1	Output or input level of the PA0 pin: "H"

22.2.3 Port A Direction Register (PADIR)

Address: 0F251H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PADIR	PA7DIR	PA6DIR	PA5DIR	PA4DIR	PA3DIR	PA2DIR	PA1DIR	PA0DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PADIR is a special function register (SFR) to select the input/output mode of Port A.

[Description of Bits]

- **PA7DIR-PA0DIR** (bits 7-0)
  The PA7DIR to PA0DIR pins are used to set the input/output direction of the Port A pin.

PA7DIR	Description
0	PA7 pin: Output (initial value)
1	PA7 pin: Input

PA6DIR	Description
0	PA6 pin: Output (initial value)
1	PA6 pin: Input

PA5DIR	Description
0	PA5 pin: Output (initial value)
1	PA5 pin: Input

PA4DIR	Description
0	PA4 pin: Output (initial value)
1	PA4 pin: Input

PA3DIR	Description
0	PA3 pin: Output (initial value)
1	PA3 pin: Input

PA2DIR	Description
0	PA2 pin: Output (initial value)
1	PA2 pin: Input

PA1DIR	Description
0	PA1 pin: Output (initial value)
1	PA1 pin: Input

PA0DIR	Description
0	PA0 pin: Output (initial value)
1	PA0 pin: Input

22.2.4 Port A Control Registers 0, 1 (PACON0, PACON1)

Address: 0F252H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PACON0	PA7C0	PA6C0	PA5C0	PA4C0	PA3C0	PA2C0	PA1C0	PA0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F253H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PACON1	PA7C1	PA6C1	PA5C1	PA4C1	PA3C1	PA2C1	PA1C1	PA0C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PACON0 and PACON1 are special function registers (SFRs) to select input/output state of the Port A pin. The input/output state is different between input mode and output mode. Input or output is selected by using the PADIR register.

[Description of Bits]

- **PA7C1-PA0C1, PA7C0-PA0C0** (bits 7-0)
  The PA7C1 to PA0C1 pins and the PA7C0 to PA0C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of PA7 pin		When output mode is selected (PA7DIR bit = "0")	When input mode is selected (PA7DIR bit = "1")
PA7C1	**PA7C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PA6 pin		When output mode is selected (PA6DIR bit = "0")	When input mode is selected (PA6DIR bit = "1")
PA6C1	**PA6C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PA5 pin		When output mode is selected (PA5DIR bit = "0")	When input mode is selected (PA5DIR bit = "1")
PA5C1	**PA5C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PA4 pin		When output mode is selected (PA4DIR bit = "0")	When input mode is selected (PA4DIR bit = "1")
PA4C1	**PA4C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PA3 pin		When output mode is selected (PA3DIR bit = "0")	When input mode is selected (PA3DIR bit = "1")
PA3C1	**PA3C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PA2 pin		When output mode is selected (PA2DIR bit = "0")	When input mode is selected (PA2DIR bit = "1")
PA2C1	**PA2C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PA1 pin		When output mode is selected (PA1DIR bit = "0")	When input mode is selected (PA1DIR bit = "1")
PA1C1	**PA1C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PA0 pin		When output mode is selected (PA0DIR bit = "0")	When input mode is selected (PA0DIR bit = "1")
PA0C1	**PA0C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

22.3 Description of Operation

22.3.1 Input/Output Port Functions

For each pin of Port A, either output or input is selected by setting the Port A direction register (PADIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port A control registers 0 and 1 (PACON0 and PACON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port A control registers 0 and 1 (PACON0 and PACON1).
At system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port A depending on the value set by the Port A data register (PAD).
In input mode, the input level of each pin of Port A can be read from the Port A data register (PAD).

Chapter 23

Melody Driver

23. Melody Driver

23.1 Overview

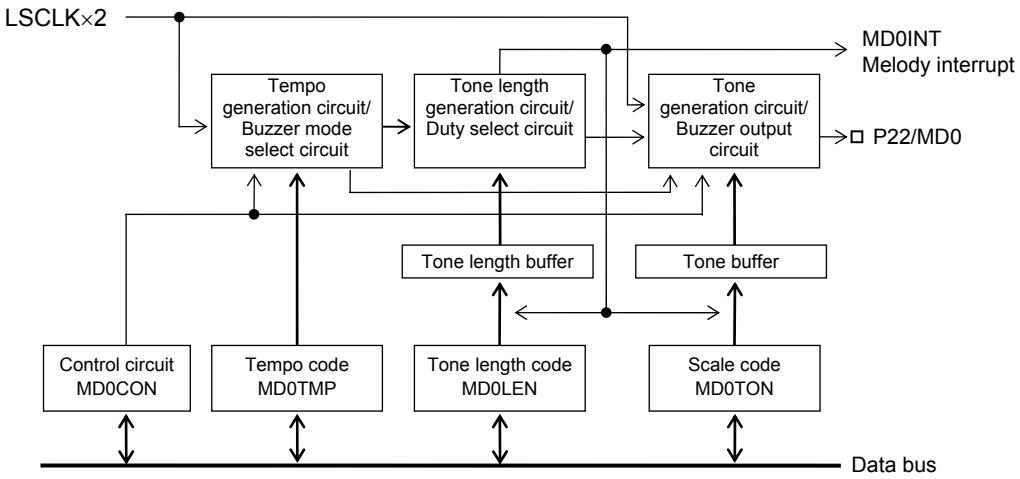
This LSI includes one channel of the melody driver.
To use the melody driver, the secondary function of port 2 should be set. For the secondary function of port 2, see Chapter 19, "Port 2". For the clock to be used in this melody driver, see Chapter 6, "Clock Generation Circuit".

23.1.1 Features

- In melody output mode, 29 scales (melody audio frequency: 508Hz to 32.768kHz), 63 tone lengths, and 15 tempos) are available.
- In buzzer output mode, 4 output modes, 8 frequencies, and 15 duties can be set.

23.1.2 Configuration

Figure 23-1 shows the configuration of the melody driver.



MD0CON : Melody 0 control register
MD0TMP : Melody 0 tempo code register
MD0TON : Melody 0 scale code register
MD0LEN : Melody 0 tone length code register

Figure 23-1 Configuration of Melody Driver

23.1.3 List of Pins

Pin name	I/O	Description
P22/MD0	O	Melody 0 signal output pin Used as the secondary of the P22 pin.

23.2 Description of Registers

23.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2C0H	Melody 0 control register	MD0CON	—	R/W	8	00H
0F2C1H	Melody 0 tempo code register	MD0TMP	—	R/W	8	00H
0F2C2H	Melody 0 scale code register	MD0TON	MD0TL	R/W	8/16	00H
0F2C3H	Melody 0 tone length code register	MD0LEN		R/W	8	00H

23.2.2 Melody 0 Control Register (MD0CON)

Address: 0F2C0H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
MD0CON	—	—	—	—	—	—	BZMD	M0RUN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

MD0CON is a special function register (SFR) to control a melody and the buzzer.

[Description of Bits]

- **BZMD** (bit 1)
  The BZMD bit is used to select melody mode or buzzer mode.

BZMD	Description
0	Melody mode (initial value)
1	Buzzer mode

- **M0RUN** (bit 0)
  The M0RUN bit is used to control start/stop of the MD0 output.

M0RUN	Description
0	Stops MD0 output. (Initial value)
1	Starts MD0 output.

Note:
For melody output, use the 2×low-speed clock (LSCLK×2).
Enable the 2×low-speed clock by setting bit 2 (ENMLT) of frequency control register 1 (FCON1) to "1" and then start melody output by setting M0RUN to "1".

23.2.3 Melody 0 Tempo Code Register (MD0TMP)

Address: 0F2C1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
MD0TMP	—	—	—	—	M0TM3	M0TM2	M0TM1	M0TM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

MD0TMP is a special function register (SFR) to set the tempo code of a melody when melody mode is selected and the output mode of a buzzer sound waveform when buzzer mode is selected.

[Description of Bits]

- **M0TM3, M0TM2, M0TM1, M0TM0** (bits 3-0)

When melody mode is selected (BZMD bit = "0")				
M0TM3	**M0TM2**	**M0TM1**	**M0TM0**	Description
0	0	0	0	♪ = 480 (initial value)
0	0	0	1	♪ = 480
0	0	1	0	♪ = 320
0	0	1	1	♪ = 240
0	1	0	0	♪ = 192
0	1	0	1	♪ = 160
0	1	1	0	♪ ≅ 137
0	1	1	1	♪ = 120
1	0	0	0	♪ ≅ 107
1	0	0	1	♪ = 96
1	0	1	0	♪ ≅ 87
1	0	1	1	♪ = 80
1	1	0	0	♪ ≅ 74
1	1	0	1	♪ ≅ 69
1	1	1	0	♪ = 64
1	1	1	1	♪ = 60

When buzzer mode is selected (BZMD bit = "1")				
M0TM3	**M0TM2**	**M0TM1**	**M0TM0**	Description
*	*	0	0	Intermittent 1 output (initial value)
*	*	0	1	Intermittent 2 output
*	*	1	0	Single sound output
*	*	1	1	Continuous sound output

23.2.4 Melody 0 Scale Code Register (MD0TON)

Address: 0F2C2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
MD0TON	—	M0TN6	M0TN5	M0TN4	M0TN3	M0TN2	M0TN1	M0TN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

MD0TON is a special function register (SFR) to set the scale code of a melody when melody mode is selected and a buzzer output frequency when buzzer mode is selected.

[Description of Bits]

- **M0TN6, M0TN5, M0TN4, M0TN3, M0TN2, M0TN1, M0TN0** (bits 6-0)

When melody mode is selected (BZMD bit = "0")	
M0TN6 to 0	Description
	Sets the corresponding scale code.

For scale codes, see Section 23.3.4, "Scale Codes".

When buzzer mode is selected (BZMD bit = "1")				
M0TN6 to 3	**M0TN2**	**M0TN1**	**M0TN0**	Description
*	0	0	0	4.096 kHz (initial value)
*	0	0	1	2.048 kHz
*	0	1	0	1.365 kHz
*	0	1	1	1.024 kHz
*	1	0	0	819 Hz
*	1	0	1	683 Hz
*	1	1	0	585 Hz
*	1	1	1	512 Hz

Note: In buzzer mode, the M0TN6 to M0TN3 bits are not used.(Don't care)

23.2.5 Melody 0 Tone Length Code Register (MD0LEN)

Address: 0F2C3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
MD0LEN	—	—	M0LN5	M0LN4	M0LN3	M0LN2	M0LN1	M0LN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

MD0LEN is a special function register (SFR) to set the tone length code of a melody when melody mode is selected and buzzer output duty when buzzer mode is selected.

[Description of Bits]

- **M0LN5, M0LN4, M0LN3, M0LN2, M0LN1, M0LN0** (bits 5-0)

When melody mode is selected (BZMD bit = "0")	
M0LN5 to 0	Description
	Sets the corresponding tone length code.

For tone length codes, see Section 23.3.3, "Tone Length Codes".

When buzzer mode is selected (BZMD bit = "1")					
M0LN5 to 4	**M0LN3**	**M0LN2**	**M0LN1**	**M0LN0**	Description
*	0	0	0	0	1/16 DUTY (initial value)
*	0	0	0	1	1/16 DUTY
*	0	0	1	0	2/16 DUTY
*	0	0	1	1	3/16 DUTY
*	0	1	0	0	4/16 DUTY
*	0	1	0	1	5/16 DUTY
*	0	1	1	0	6/16 DUTY
*	0	1	1	1	7/16 DUTY
*	1	0	0	0	8/16 DUTY
*	1	0	0	1	9/16 DUTY
*	1	0	1	0	10/16 DUTY
*	1	0	1	1	11/16 DUTY
*	1	1	0	0	12/16 DUTY
*	1	1	0	1	13/16 DUTY
*	1	1	1	0	14/16 DUTY
*	1	1	1	1	15/16 DUTY

Note: In buzzer mode, the M0LN5 to M0LN4 bits are not used.(Don't care)

23.3 Description of Operation

23.3.1 Operation of Melody Output

Melody is output in the following procedure.

(1) Select melody mode by setting the BZMD bit of the melody 0 control register (MD0CON) to "0".
(2) Set a melody tempo in the melody 0 tempo code register (MD0TMP).
(3) Set a tone length code in the melody 0 tone length code register (MD0LEN).
(4) Set a scale code in the melody 0 scale code register (MD0TON).
(5) Set bit 2 (ENMLT) of the frequency control register 1(FCON1) to "1" to enable the 2×low-speed clock.
(6) When the M0RUN bit of the melody 0 control register (MD0CON) is set to "1", the tone length code and scale code are transferred to the tone length buffer and scale buffer and melody output is started from the MD0 pin. At the same time, a melody 0 interrupt (MD0INT) is requested. When an interrupt occurs and program is passed to the interrupt routine, the interrupt request flag is cleared.

The melody 0 signal output pin (MD0) is assigned as the secondary function of Port 2. See Chapter 19, "Port 2," for the secondary function settings of Port 2.
In the software processing after melody 0 interrupt, the tone length code and the scale code of the note that are output next are set to MD0LEN and MD0TON, respectively. When there is no next note to be output, rest data "00H" is set in MD0TON, the M0RUN bit is set to "0" by the software processing after the next melody 0 interrupt, and melody output is terminated.
By setting the M0RUN bit to "0", melody can be terminated forcibly during melody output.
In the case the melody is forcibly terminated, meldy circuit must be reset once by setting DMD0 bit of BLKCON3 register to "1". Then if you want continue to use the melody function, reset the DMD0 bit to "0" and restart operating from the aforementioned procedure (1).

Figure 23-2 shows the operation waveform of the melody driver.

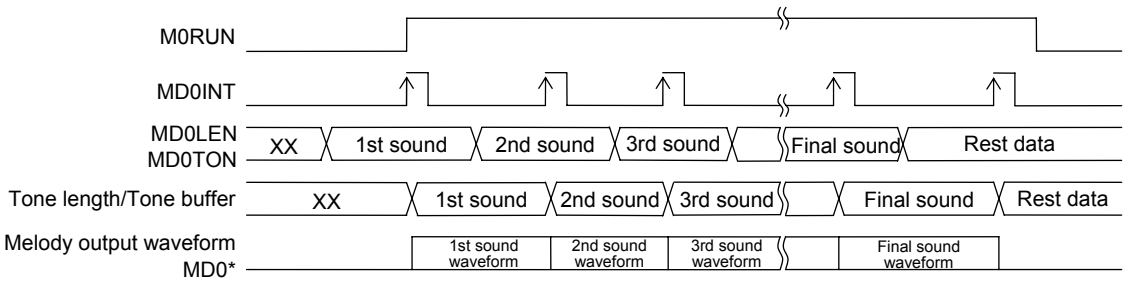


Figure 23-2 Operation Waveform of Melody Driver

23.3.2 Tempo Codes

A tempo code is set in the melody 0 tempo code register (MD0TEM).
Table 23-1 shows the correspondence between tempos and tempo codes.
The tempo when all the bits are set to "0" is equal to the shortest tone length (the tempo when the only M0TP0 bit is set to "1").

Table 23-1 Correspondence between Tempos and Tempo Codes

Tempo	Tempo code (MD0TMP)				
	M0TP3	M0TP2	M0TP1	M0TP0	M0TP3 to 0
♩ = 480	0	0	0	0	0H
♩ = 480	0	0	0	1	1H
♩ = 320	0	0	1	0	2H
♩ = 240	0	0	1	1	3H
♩ = 192	0	1	0	0	4H
♩ = 160	0	1	0	1	5H
♩ ≅ 137	0	1	1	0	6H
♩ = 120	0	1	1	1	7H
♩ ≅ 107	1	0	0	0	8H
♩ = 96	1	0	0	1	9H
♩ ≅ 87	1	0	1	0	AH
♩ = 80	1	0	1	1	BH
♩ ≅ 74	1	1	0	0	CH
♩ ≅ 69	1	1	0	1	DH
♩ = 64	1	1	1	0	EH
♩ = 60	1	1	1	1	FH

23.3.3 Tone Length Codes

A tone length code is set in the melody 0 tone length code register (MD0LEN).
Table 23-2 shows the correspondence between tone lengths and tone length codes.
The tone length when all the bits are set to "0" is equal to the shortest tone length (the tone length when the only M0LN0 bit is set to "1").

Table 23-2 Correspondence between Tone Lengths and Tone Length Codes

Tone length	Tone length code (MD0LEN)						
	M0LN5	M0LN4	M0LN3	M0LN2	M0LN1	M0LN1	M0LN5–0
	1	1	1	1	1	1	3FH
	1	0	1	1	1	1	2FH
	0	1	1	1	1	1	1FH
	0	1	0	1	1	1	17H
	0	0	1	1	1	1	0FH
	0	0	1	0	1	1	0BH
	0	0	0	1	1	1	07H
	0	0	0	1	0	1	05H
	0	0	0	0	1	1	03H
	0	0	0	0	1	0	02H
	0	0	0	0	0	1	01H

The tone length set by a tone length code and a tempo code is expressed by the following equation.

$$\text{Tone length} = 1.953125 \times (TP + 1) \times (LN + 1) \text{ ms}$$

where TP is an integer of 1 to 15, and LN is an integer of 1 to 63.

The bit correspondence between TP and tempo codes is expressed by the following equation.

$$TP = 2^3\text{M0TP3} + 2^2\text{M0TP2} + 2^1\text{M0TP1} + 2^0\text{M0TP0}$$

The bit correspondence between LN and tone length codes is expressed by the following equation.

$$LN = 2^5\text{M0LN5} + 2^4\text{M0LN4} + 2^3\text{M0LN3} + 2^2\text{M0LN2} + 2^1\text{M0LN1} + 2^0\text{M0LN0}$$

23.3.4 Scale Codes

A scale code is set in the melody 0 scale code register (MD0TON).
In the melody driver, a frequency that can be output is expressed by the following equation.

$$\frac{65536}{(TN + 1)} \text{ Hz} \qquad \text{(where TN is an integer of 4 to 127.)}$$

The bit correspondence between TN and scale codes is expressed by the following equation.

$$TN = 2^6M0TN6 + 2^5M0TN5 + 2^4M0TN4 + 2^3M0TN3 + 2^2M0TN2 + 2^1M0TN1 + 2^0M0TN0$$

Table 23-3 shows the correspondence between scales and scale codes.
When the M0TN6 to M0TN2 bits are set to "0", scale becomes a rest. The rest length is set by the tone length code (MD0LEN).

Table 23-3 Correspondence between Scales and Scale Codes

Scale	Frequency (Hz)	Scale code (MD0TON)							
		M0TN6	M0TN5	M0TN4	M0TN3	M0TN2	M0TN1	M0TN0	M0TN6–0
C^1	529	1	1	1	1	0	1	1	7BH
Cis^1	560	1	1	1	0	1	0	0	74H
D^1	590	1	1	0	1	1	1	0	6EH
Dis^1	624	1	1	0	1	0	0	0	68H
E^1	662	1	1	0	0	0	1	0	62H
F^1	705	1	0	1	1	1	0	0	5CH
Fis^1	745	1	0	1	0	1	1	1	57H
G^1	790	1	0	1	0	0	1	0	52H
Gis^1	840	1	0	0	1	1	0	1	4DH
A^1	886	1	0	0	1	0	0	1	49H
Ais^1	936	1	0	0	0	1	0	1	45H
B^1	993	1	0	0	0	0	0	1	41H
C^2	1057	0	1	1	1	1	0	1	3DH
Cis^2	1111	0	1	1	1	0	1	0	3AH
D^2	1192	0	1	1	0	1	1	0	36H
Dis^2	1260	0	1	1	0	0	1	1	33H
E^2	1338	0	1	1	0	0	0	0	30H
F^2	1394	0	1	0	1	1	1	0	2EH
Fis^2	1490	0	1	0	1	0	1	1	2BH
G^2	1560	0	1	0	1	0	0	1	29H
Gis^2	1680	0	1	0	0	1	1	0	26H
A^2	1771	0	1	0	0	1	0	0	24H
Ais^2	1872	0	1	0	0	0	1	0	22H
B^2	1986	0	1	0	0	0	0	0	20H
C^3	2114	0	0	1	1	1	1	0	1EH
D^3	2341	0	0	1	1	0	1	1	1BH
Dis^3	2521	0	0	1	1	0	0	1	19H
E^3	2621	0	0	1	1	0	0	0	18H
Fis^3	2979	0	0	1	0	1	0	1	15H

23.3.5 Example of Using Melody Circuit

Figure 23-3 shows an example of a melody notation, and Table 23-4 shows note codes of melody examples.

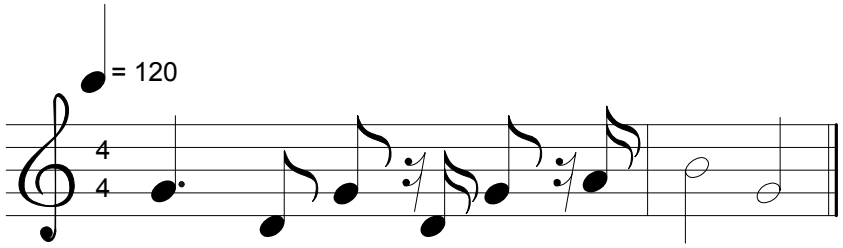



Figure 23-3 Example of Melody Notation

Table 23-4 Note Codes of Melody Examples

Note	Note code													hexadecimal
	MD0LEN						MD0TON							
	5	4	3	2	1	0	6	5	4	3	2	1	0	
G^2	1	0	1	1	1	1	0	1	0	1	0	0	0	2F28H
D^2	0	0	1	1	1	1	0	1	1	0	1	0	1	0F35H
G^2	0	0	1	1	1	1	0	1	0	1	0	0	0	0F28H
—	0	0	0	1	1	1	0	0	0	0	0	0	0	0700H
D^2	0	0	0	1	1	1	0	1	1	0	1	0	1	0735H
G^2	0	0	1	1	1	1	0	1	0	1	0	0	0	0F28H
—	0	0	0	1	1	1	0	0	0	0	0	0	0	0700H
A^2	0	0	0	1	1	1	0	1	0	0	0	1	1	0723H
B^2	1	1	1	1	1	1	0	0	1	1	1	1	1	3F1FH
G^2	1	1	1	1	1	1	0	1	0	1	0	0	0	3F28H

23.3.6 Operations of Buzzer Output

A buzzer sound is output in the following procedure.

(1) Select a buzzer mode by setting the BZMD bit of the melody 0 control register (MD0CON) to "1".
(2) Select a buzzer output mode using the melody 0 tempo code register (MD0TMP).
(3) Select a duty of the High level width of the buzzer output waveform using the melody 0 tone length code register (MD0LEN).
(4) Set the buzzer output frequency in the melody 0 scale code register (MD0TON).
(5) Set bit 2 (ENMLT) of the frequency control register 1(FCON1) to "1" to enable the 2×low-speed clock.
(6) When the M0RUN bit of the melody 0 control register (MD0CON) is set to "1", the waveform equivalent to the buzzer sound that is set from the MD0 pin is output.

Figure 23-4 shows the output waveform of each buzzer output mode.

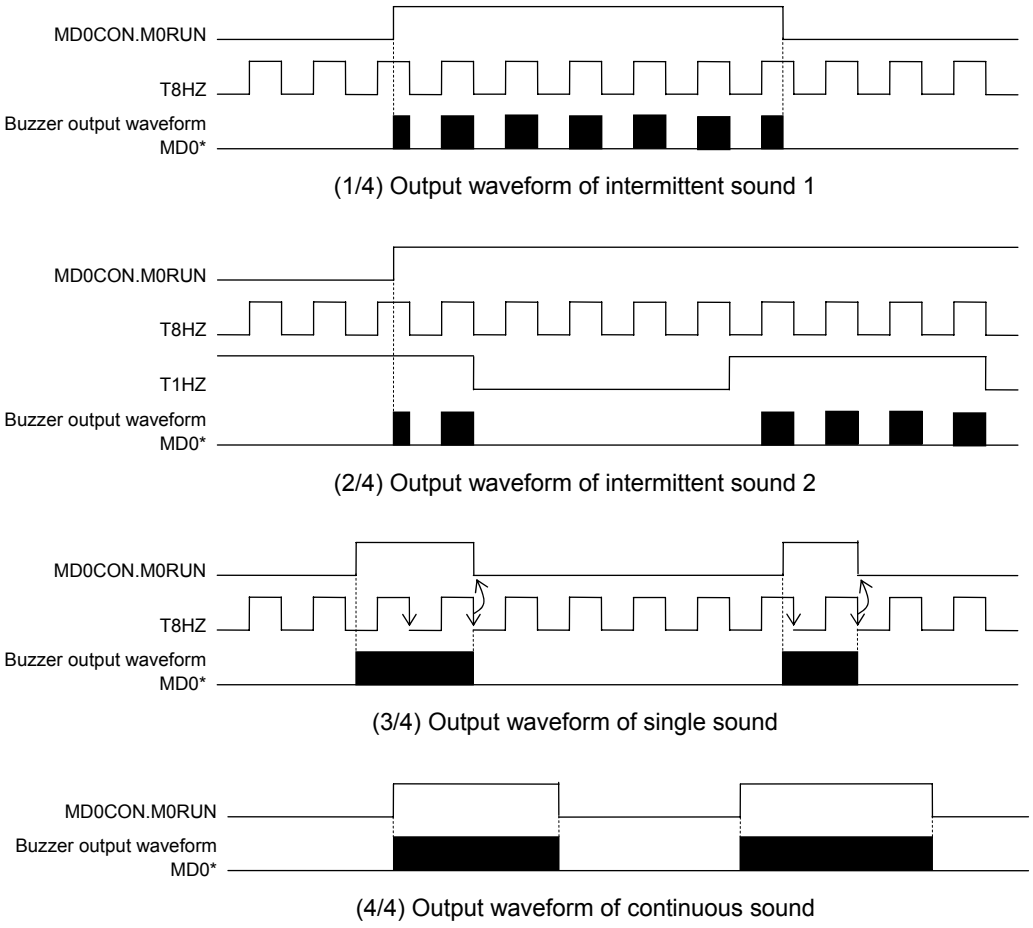


Figure 23-4 Output Waveform of Each Buzzer Output Mode

23.4 Specifying port registers

When you want to make sure the Melody/Buzzer function is working, please check related port registers are specified. See Chapter 19, "Port 2" for detail about the port registers.

23.4.1 Functioning P22 (MD0) as the Melody or Buzzer output

Set P22MD bit (bit2 of P2MOD register) to "1" for specifying the melody or buzzer output as the secondary function of P22.

Reg. name	P2MOD register (Address: 0F214H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	-	-	**P22MD**	P21MD	P20MD
Data	-	-	-	-	-	**1**	*	*

Set P22C1 bit (bit2 of P2CON1 register) to "1" and set P22C0 bit(bit2 of P2CON0 register) to "1", for specifying the P22 as CMOS output.

Reg. name	P2CON1 register (Address: 0F213H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	-	-	**P22C1**	P21C1	P20C1
Data	-	-	-	-	-	**1**	*	*

Reg. name	P2CON0 register (Address: 0F212H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	-	-	**P22C0**	P21C0	P20C0
Data	-	-	-	-	-	**1**	*	*

Data of P22D bit (bit2 of P2D register) does not affect to the melody or buzzer function, so don't care the data for the function.

Reg. name	P2D register (Address: 0F210H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	-	-	**P22D**	P21D	P20D
Data	-	-	-	-	-	******	*	*

- : Bit does not exist.
* : Bit not related to the melody or buzzer function
** : Don't care the data.

Note:
- Port2 is an output-only port, does not have an register to select the data direction(input or output).
- The output characteristics of port22 corresponds to VOL1 and VOH1 when P22MD bit is "1" (melody/buzzer is selected as the 2nd function), and corresponds to VOL2 and VOH2 when the P22MD bit is "0", which are shown in Appendix C, "Electrical Characteristics".

Chapter 24

RC Oscillation Type A/D Converter

24. RC Oscillation Type A/D Converter

24.1 Overview

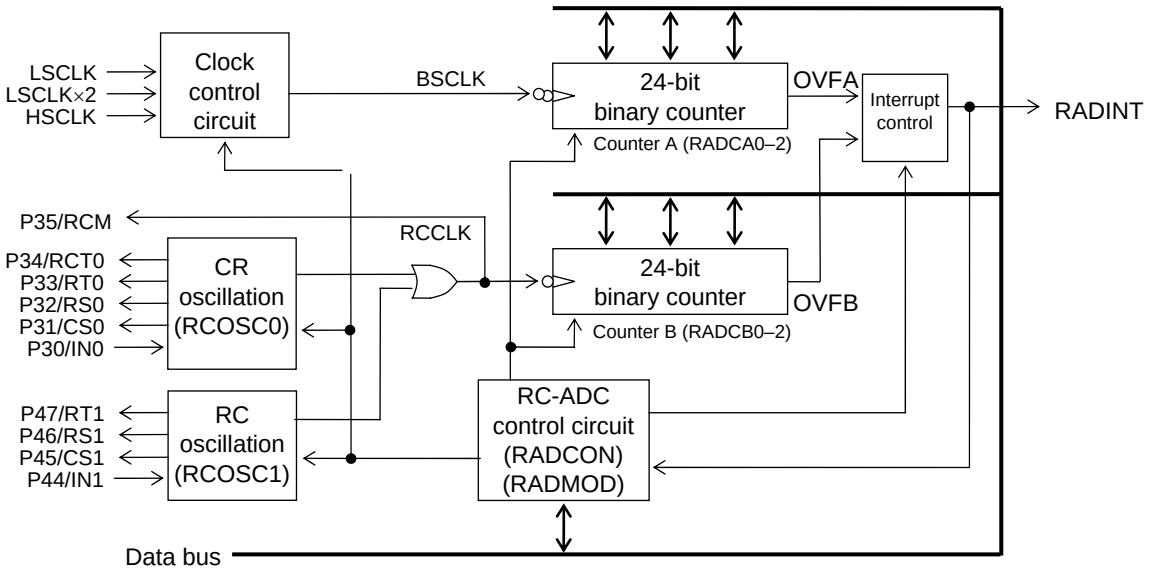
This LSI has a built-in 2-channel RC oscillation type A/D converter (RC-ADC).
The RC-ADC converts resistance values or capacitance values to digital values by counting the oscillator clock whose frequency changes according to the resistor or capacitor connected to the RC oscillator circuits. By using a thermistor or humidity sensor as a resistor, a thermometer or hygrometer can be formed.
In addition, a different sensor for each of the two channels of RC-ADC's RC oscillator circuit can be used to broaden RC-ADC applications; for example, the conveter can be used for expansion of measurement range or measurement at two points.
For input clock, see Chapter 6, "Clock Generation Circuit."

24.1.1 Features

- 2-channel system by time division

24.1.2 Configuration

The RC-ADC consists of two RC oscillator circuits to form two channels, Counter A (RADCA0–2) and Counter B (RADCB0–2) as 24-bit binary counters, and an RC-ADC control circuit (RADCON, RADMOD). Figure 24-1 shows the configuration of the RC-ADC.



RADMOD: RC-ADC mode register
RADCON: RC-ADC control register
RADCA0–2: RC-ADC Counter A registers 0–2
RADCB0–2: RC-ADC Counter B registers 0–2

Figure 24-1 Configuration of RC-ADC

24.1.3 List of Pins

Pin name	I/O	Description
P30/IN0	I	Channel 0 oscillation input pin. Used for the secondary function of the P30 pin.
P31/CS0	O	Channel 0 reference capacitor connection pin. Used for the secondary function of the P31 pin.
P32/RS0	O	Channel 0 reference resistor connection pin. Used for the secondary function of the P32 pin.
P33/RT0	O	Pin for connection with a resistive sensor for measurement on Channel 0. Used for the secondary function of the P33 pin.
P34/RCT0	O	Pin for connection with a resistive/capacitive sensor for measurement on Channel 0. Used for the secondary function of the P34 pin.
P35/RCM	O	RC oscillation monitor pin. Used for the secondary function of the P35 pin.
P44/IN1	I	Channel 1 oscillation input pin. Used for the secondary function of the P44 pin.
P45/CS1	O	Channel 1 reference capacitor connection pin. Used for the secondary function of the P45 pin.
P46/RS1	O	Channel 1 reference resistor connection pin. Used for the secondary function of the P46 pin.
P47/RT1	O	Pin for connection with a resistive sensor for measurement on Channel 1. Used for the secondary function of the P47 pin.

24.2 Description of Registers

24.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F300H	RC-ADC Counter A register 0	RADCA0	—	R/W	8	00H
0F301H	RC-ADC Counter A register 1	RADCA1	—	R/W	8	00H
0F302H	RC-ADC Counter A register 2	RADCA2	—	R/W	8	00H
0F304H	RC-ADC Counter B register 0	RADCB0	—	R/W	8	00H
0F305H	RC-ADC Counter B register 1	RADCB1	—	R/W	8	00H
0F306H	RC-ADC Counter B register 2	RADCB2	—	R/W	8	00H
0F308H	RC-ADC mode register	RADMOD	—	R/W	8	00H
0F309H	RC-ADC control register	RADCON	—	R/W	8	00H

24.2.2 RC-ADC Counter A Registers (RADCA0–2)

Address: 0F300H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
RADCA0	RAA7	RAA6	RAA5	RAA4	RAA3	RAA2	RAA1	RAA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F301H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
RADCA1	RAA15	RAA14	RAA13	RAA12	RAA11	RAA10	RAA9	RAA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F302H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
RADCA2	RAA23	RAA22	RAA21	RAA20	RAA19	RAA18	RAA17	RAA16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

RADCA0–2, which serve as a 24-bit binary counter (Counter A), are special function registers (SFRs) used to perform read/write operations to Counter A itself.

Note:
After writing data into the RC-ADC counter A register, be sure to read it to check that the data has been written correctly.
When A/D conversion starts after data is written, the value that has been written is read during A/D conversion (RARUN = 1).
When A/D conversion terminates (RARUN = 0), the count value is read.

24.2.3 RC-ADC Counter B Registers (RADCB0–2)

Address:0F304H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
RADCB0	RAB7	RAB6	RAB5	RAB4	RAB3	RAB2	RAB1	RAB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address:0F305H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
RADCB1	RAB15	RAB14	RAB13	RAB12	RAB11	RAB10	RAB9	RAB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address:0F306H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
RADCB2	RAB23	RAB22	RAB21	RAB20	RAB19	RAB18	RAB17	RAB16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

RADCB0–2, which serve as a 24-bit binary counter (Counter B), are special function registers (SFRs) used to perform read/write operations to Counter B itself.

Note:
After writing data into the RC-ADC counter B register, be sure to read it to check that the data has been written correctly.
When A/D conversion starts after data is written, the value that has been written is read during A/D conversion (RARUN = 1).
When A/D conversion terminates (RARUN = 0), the count value is read.

24.2.4 RC-ADC Mode Register (RADMOD)

Address: 0F308H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
RADMOD	RACK2	RACK1	RACK0	RADI	OM3	OM2	OM1	OM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

RADMOD is a special function register (SFR) used to select an A/D conversion mode of the RC-ADC.

[Description of Bits]

- **OM3-0** (bits 3-0)
  The OM3–0 bits are used to select an oscillation mode for the RC oscillator circuits.

OM3	OM2	OM1	OM0	Description
0	0	0	0	IN0 pin external clock input mode (initial value)
0	0	0	1	RS0–CS0 oscillation mode
0	0	1	0	RT0–CS0 oscillation mode
0	0	1	1	$RT_{0\text{-}1}$–CS0 oscillation mode
0	1	0	0	RS0–CT0 oscillation mode
0	1	0	1	RS1–CS1 oscillation mode
0	1	1	0	RT1–CS1 oscillation mode
0	1	1	1	IN1 pin external clock input mode
1	*	*	*	Setting prohibited

- **RADI** (bit 4)
  The RADI bit is used to choose whether to generate the RC-ADC interrupt request signal (RADINT) by an overflow at Counter A or Counter B.

RADI	Description
0	Generates an interrupt request by Counter A overflow (initial value).
1	Generates an interrupt request by Counter B overflow.

- **RACK2-0** (bits 7-5)
  The RACK2–0 bits are used to select the base clock of Conter A (BSCLK).

RACK2	RACK1	RACK0	Description
0	0	0	LSCLK (initial value)
0	0	1	LSCLK×2
0	1	0	HSCLK
0	1	1	1/2HSCLK
1	0	0	1/4HSCLK
1	0	1	1/8HSCLK
1	1	*	Setting prohibited (no clock is supplied)

Note:
When specifying LSCLK×2 for the base clock, enable the operation of the 2×low-speed clock by setting bit 2 (ENMLT) of the frequency control register 1 (FCON1) to "1".

24.2.5 RC-ADC Control Register (RADCON)

Address: 0F309H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
RADCON	—	—	—	—	—	—	—	RARUN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

RADCON is a special function register (SFR) used to control A/D conversion operation of the RC-ADC.

[Description of Bits]

- **RARUN** (bit 0)
  The RARUN bit is used to start or stop A/D conversion of the RC-ADC. When RARUN is set to "1", A/D conversion starts and when set to "0", A/D conversion stops. If Counter A or Counter B overflows with RARUN set to "1", the bit is automatically reset to "0".
  RARUN is set to "0" at system reset.

RARUN	Description
0	Stops A/D conversion (initial value).
1	Starts A/D conversion.

24.3 Description of Operation

Counter A (RADCA0–2) is a 24-bit binary counter for counting the base clock (BSCLK), which is used as the standard of time. Counter A can count up to 0FFFFFFH.
Counter B (RADCB0–2) is a 24-bit binary counter for counting the oscillator clock (RCCLK) of the RC oscillator circuits. Counter B can count up to 0FFFFFFH.
Counters A and B are provided with overflow flags (OVFA and OVFB, respectively). Each overflow output results in generation of an RC-ADC interrupt request signal (RADINT). Use the RADI bit of the RC-AC mode register (RADMOD) to select whether to generate an overflow interrupt by an overflow on Counter A or Counter B: setting RADI to "0" specifies Counter A overflow and setting it to "1" specifies Counter B overflow.

The RARUN bit of the RC-AD control register (RADCON) is used to start or stop RC-ADC conversion operation. When RARUN is set to "0", the oscillator circuits stop, so that counting will not be performed. When RARUN is set to "1", RC oscillation starts, when the RC oscillator clock (RCCLK) and the base clock (BSCLK) start counting through Counter B and Counter A.

The RC oscillation section has a total of eight types of oscillation modes based on the two oscillator circuits of RCOSC0 and RCOSC1, and mode selection is made by the RC-ADC mode register (RADMOD).
P30–34, P44–47, and P35 must be configured as their secondary function input or output when using 1) the RC oscillator circuit RCOSC0, 2) the RC oscillator circuit RCOSC1, and 3) the RC monitor pin (RCM) that outputs RC oscillation waveforms, respectively. For the configuration of the RC oscillator circuits, see Section 24.1.2, "Configuration"; for the secondary functions of Port 3, see Chapter 20, "Port 3"; for the secondary functions of Port 4, see Chapter 21, "Port 4".

24.3.1 RC Oscillator Circuits

RC-ADC performs A/D conversion by converting the oscillation frequency ratio between a reference resistor (or capacitor) and a resistive sensor (or capacitive sensor) such as a thermistor to digital data.
By making RC oscillation occur both on the reference side and on the sensor side with the reference capacitor the error factor that the RS oscillator circuit itself is eliminated, thereby making it possible to perform the A/D conversion of the characteristics of the sensor itself.
Also, by calculating the ratio between the oscillation frequency on the reference side and that on the sensor side and then calculating the correlation between the calculated ratio and temperatures that the sensor characteristics have in advance, a temperature can be obtained based on that calculated ratio.
Table 24-1 lists the eight types of oscillation modes, one of which is selected by the RC-ADC mode register (RADMOD) OM3–0 bits.

Table 24-1 Oscillation Modes from Which Selection Is Made by OM3–0 Bits

Mode No.	RADMOD				RCOSC0 output pin				RCOSC1 output pin			Mode	
	OM3	OM2	OM1	OM0	RS0	RT0	RCT0	CS0	RS1	RT1	CS1		
0	0	0	0	0	Z	Z	Z	Z	Z	Z	Z	IN0 external clock input mode	
1	0	0	0	1	1/0	Z	Z	0/1	Z	Z	Z	RS0–CS0 oscillation	RCOSC0 oscillation mode
2	0	0	1	0	Z	1/0	Z	0/1	Z	Z	Z	RT0–CS0 oscillation	
3	0	0	1	1	Z	Z	1/0	0/1	Z	Z	Z	$RT_{0\text{-}1}$–CS0 oscillation	
4	0	1	0	0	1/0	Z	0/1	Z	Z	Z	Z	RS0–CT0 oscillation	
5	0	1	0	1	Z	Z	Z	Z	1/0	Z	0/1	RS1–CS1 oscillation	RCOSC1 oscillation mode
6	0	1	1	0	Z	Z	Z	Z	Z	1/0	0/1	RT1–CS1 oscillation	
7	0	1	1	1	Z	Z	Z	Z	Z	Z	Z	IN1 external clock input mode	
8	1	*	*	*	Z	Z	Z	Z	Z	Z	Z	(Setting prohibited)	

Note) * : Indicates "arbitrary."
Z : Indicates high-impedance output.
1/0, 0/1 : Indicates active output.
(Setting prohibited) : The oscillator clock is not supplied even by setting the RARUN bit to "1" or by starting A/D conversion.

In Table 24-1, mode No.0 and mode No.7 are modes where external clocks to be input to the IN0 or IN1 pin are used for measurement with the RC oscillator circuit stopped.
As shown in Table 24-1, the two oscillator circuits, RCOSC0 and RCOSC1, are so specified that they cannot operate concurrenty in order to prevent interference in oscillation from occurring when they oscillate concurrently.
The relationship between an oscillation frequency f_{RCCLK} and an RC constant is expressed by the following equation:

$$\frac{1}{f_{RCCLK}} = t_{RCCLK} = k_{RCCLK} \cdot R \cdot C$$

where t_{RCCLK} is the period of the oscillator clock, k_{RCCLK} the proportional constant, and R•C the product of capacitances CS, CT, (CS+CVR) and (CT+CVR) and resistances RS and RT. CS, CT, (CS+CVR), (CT+CVR), RS, and RT concern oscillation. The value of k_{RCCLK} slightly changes depending on the value of the supply voltage VDD, RI, R, or C.
Table 24-2 lists the typical k_{RCCLK} values.

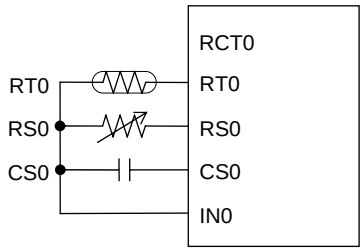
Table 24-2 Typical Values of the Proportional Constant k_{RCCLK} of RC Oscillator Circuits

V_{DD} (V)	CSn, CTn (pF)	CVRn (pF)	RSn, RTn (kΩ)	k_{RCCLK} (Typ.)
3	560	820	100	1.2
	560	820	10	1.2
1.5	560	820	100	1.2
	560	820	10	1.3

Note) n = 0, 1

Notes:
- Out of the Port 3 and Port 4 pins, pins that are to be used for the RC-ADC function must be configured as secondary function input or output using the mode register (P3MOD0, P3MOD1, P4MOD0, P4MOD1) of the corresponding port.
- All the Port 3 pins except P35/RCM (see Section 24.1.3, "List of Pins") are configured as pins dedicated to the RC-ADC function during A/D conversion. Therefore, during A/D conversion, all the Port 3 pins except P35 cannot be used as their primary functions in oscillation mode No. 0, 1, 2, 3 or 4, which is selected by the RADMOD register. In the same way, the P44 to P47 pins of Port 4 cannot be used as their primary functions in oscillation mode No. 5, 6 or 7.

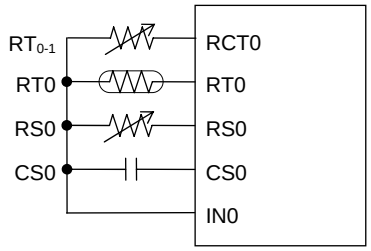
Figures 24-2 to 24-5 show the oscillator circuit configurations, the modes of oscillation for each configuration, and the OM3–0 bit settings.



OM3	OM2	OM1	OM0	Mode of oscillation
0	0	0	1	Oscillates with the reference resistor RS0 and CS0
0	0	1	0	Oscillates with the sensor RT0 and CS0

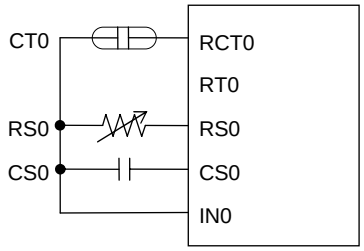
Figure 24-2 When RCOSC0 Is Used for Measurement with One Resistive Sensor

Note:
The unused pin RCT0 shown in the figure above is configured as a pin dedicated to the RC-ADC function during A/D conversion; therefore, during A/D conversion, RCT0 cannot be used as a port (P34).



OM3	OM2	OM1	OM0	Mode of oscillation
0	0	0	1	Oscillates with the reference resistor RS0 and CS0
0	0	1	0	Oscillates with the sensor RT0 and CS0
0	0	1	1	Oscillates with the reference resistor RT_{0-1} and CS0

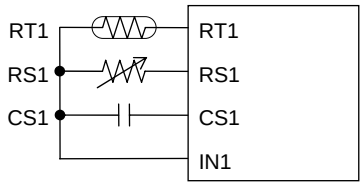
Figure 24-3 When RCOSC0 Is Used for Measurement with One Resistive Sensor (Two points are adjusted with two reference resistors)



OM3	OM2	OM1	OM0	Mode of oscillation
0	0	0	1	Oscillates with the reference resistor RS0 and CS0
0	1	0	0	Oscillates with the sensor RS0 and CT0

Figure 24-4 When RCOSC0 Is Used for Measurement with One Capacitive Sensor

Note:
The unused pin RT0 shown in the figure above is configured as a pin dedicated to the RC-ADC function during A/D conversion; therefore, during A/D conversion, RT0 cannot be used as a port (P33).



OM3	OM2	OM1	OM0	Mode of oscillation
0	1	0	1	Oscillates with the reference resistor RS1 and CS1
0	1	1	0	Oscillates with the sensor RT1 and CS1

Figure 24-5 When RCOSC1 Is Used for Measurement with One Resistive Sensor

24.3.2 Counter A/Counter B Reference Modes

There are the following two modes of RC-ADC conversion operation:

- Counter A reference mode (RADMOD RADI = "0")
  In this mode, a gate time is determined by Counter A and the base clock (BSCLK), which is used as the time reference, then the RC oscillator clock (RCCLK) is counted by Counter B within the gate time to make the content of Counter B an A/D conversion value.
  The A/D conversion value is proportional to RC oscillation frequency.

- Counter B reference mode (RADMOD RADI = "1")
  In this mode, a gate time is determined by Counter B and the RC oscillator clock (RCCLK), and the base clock (BSCLK), which is used as the time reference, is counted by Counter A within the gate time to make the content of Counter A an A/D conversion value.
  The /D conversion value is inversely proportional to RC oscillation frequency.

(1) Operation in Counter A reference mode

Figure 24-6 shows the operation timing in Counter A reference mode.
Following is an example of operation procedure in Counter A reference mode:

① Preset to Counter A (RADCA2–0) the value obtained by subtracting the count value "nA0" from the maximum value + 1 (1000000H). The product of the count value "nA0" and the BSCLK clock period indicates the gate time.
② Preset "000000H" to Counter B (RADCB2–0).
③ Set the OM3–OM0 bits of RADMOD to desired oscillation mode (see Table 24-1).
④ Set the RADI bit of RADMOD to "0" to specify generating of an interrupt request signal by Counter A overflow.
⑤ Set the RARUN bit of RADCON to "1" to start A/D conversion.

Counter A starts counting of the base clock (BSCLK) when RARUN is set to "1" and the RCON signal (signal synchronized with the fall of the base clock) is set to "1". When Counter A overflows, the RARUN bit is automatically reset to "0" (⑥) and counting is terminated. At the same time, an RC-ADC interrupt request (RADIN) occurs (⑦).

When the RCON signal is set to "1", the RC oscillator circuit starts operation and Counter B starts counting of the RC oscillator clock (RCCLK). When the RARUN bit is reset to "0" due to overflow of Counter A, RC oscillation stops and Counter B stops counting.
The final count value "nB0" of Counter B is the RCCLK count value during the gate time "$nA0 \cdot t_{BSCLK}$" and is expressed by the following expression:

$$nB0 \quad \cong \quad nA0 \cdot \frac{t_{BSCLK}}{t_{RCCLK}} \quad \propto \quad f_{RCCLK}$$

where t_{BSCLK} indicates the BSCLK period and t_{RCCLK} the RCCLK period. That is, "nB0" is a value proportional to the RC oscillation frequency f_{RCCLK}.

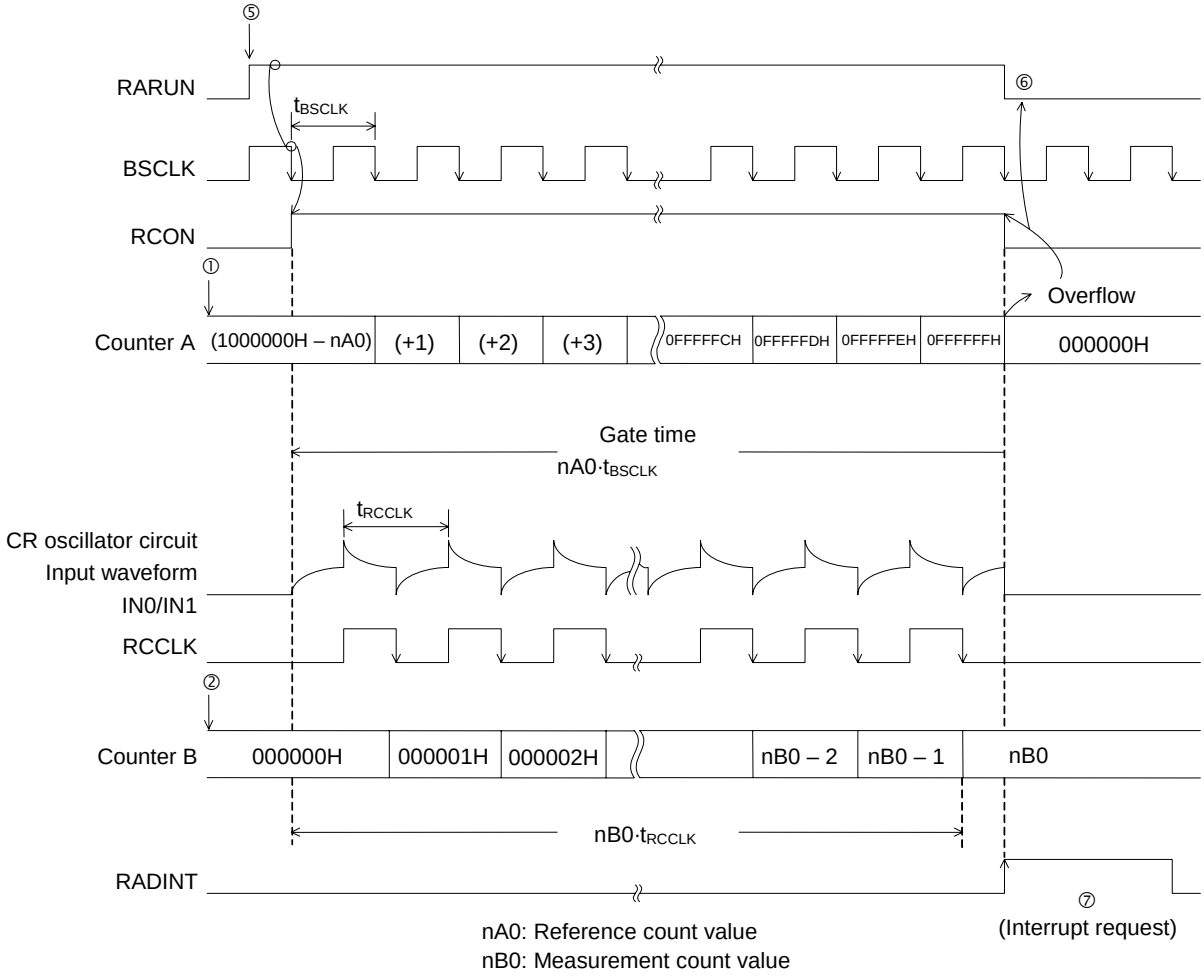


Figure 24-6 Operation Timing in Counter A Reference Mode

(2) Operation in Counter B reference mode

Figure 24-7 shows the operation timing in Counter B reference mode.
Following is an example of operation procedure in Counter B reference mode:

① Preset to Counter B (RADCB2–0) the value obtained by subtracting the count value "nB1" from the maximum value + 1 (1000000H). The product of the count value "nB1" and the RCCLKclock period indicates the gate time.
② Preset "000000H" to Counter A (RADCA2–0).
③ Set the OM3–OM0 bits of RADMOD to desired oscillation mode (see Table 24-1).
④ Set the RADI bit of RADMOD to "1" to specify generating of an interrupt request signal by Counter B overflow.
⑤ Set the RARUN bit of RADCON to "1" to start A/D conversion.

When the RARUN bit is set to "1" and the RCON signal (signal synchronized with the fall of the base clock) is set to"1", the RC oscillator circuit starts operation and Counter B starts counting of the RC oscillator clock (RCCLK). When Counter B overflows, the RARUN bit is automatically reset (⑥) and conversion operation terminates. At the same time, an RC-ADC interrupt request (RADINT) occurs. (⑦)

When the RCON signal is set to "1", Counter A starts counting of the base clock (BSCLK). When the RARUN bit is reset due to overflow of Counter B, Counter A stops counting.
The final count "nA1" of Counter A is the CLK count value during the gate time "$nB1 \cdot t_{RCCLK}$" and is expressed by the following expression:

$$nA1 \quad \cong \quad nB1 \cdot \frac{t_{RCCLK}}{t_{BSCLK}} \propto \frac{1}{f_{RCCLK}}$$

That is, "nA1" is a value inversely proportional to the RC oscillation frequency f_{RCCLK}.

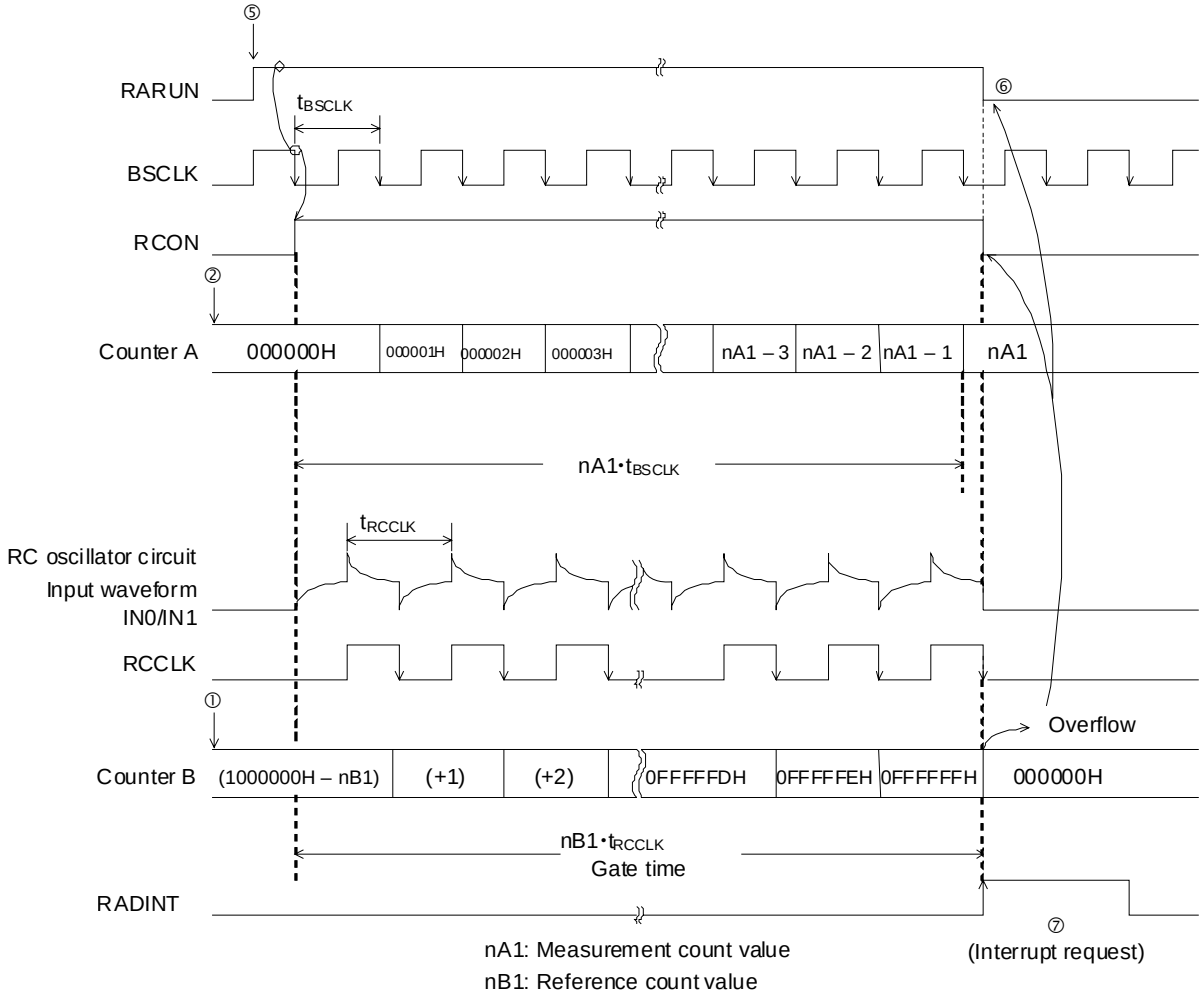


Figure 24-7 Operation Timing in Counter B Reference Mode

24.3.3 Example of Use of RC Oscillation Type A/D Converter

This section describes the method of performing A/D conversion for sensor values in Counter A and B reference modes by taking temperature measurement by a thermistor as an example.
Figure 24-8 shows the configuration of 1-thermistor RC oscillator circuit using RCOSC0.

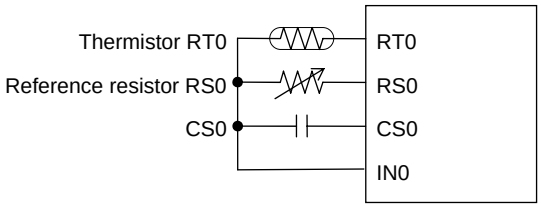


Figure 24-8 Configuration of 1-Thermistor RC Oscillator Circuit Using RCOSC0

Figure 24-9 shows the temperature characteristics of the thermistor resistance RT0.

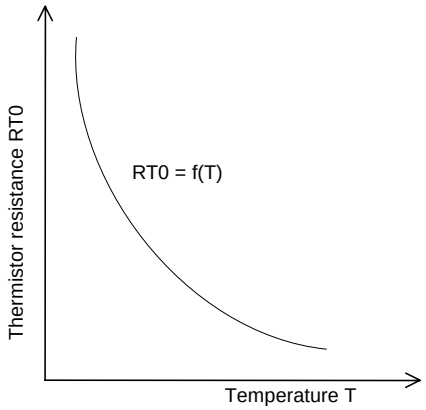


Figure 24-9 Temperature Characteristics of Thermistor

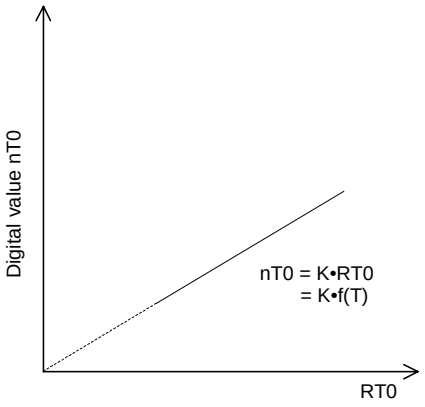


Figure 24-10 A/D Conversion Characteristics (Ideal characteristics when nT0 is proportional to RT0)

RT0 is expressed as a function of temperature T by the following equation:

$$RT0 = f(T)$$

Figure 24-10 shows the ideal characteristics of A/D conversion with the assumption that RT0 is an analog quantity. In the ideal characteristics, the A/D conversion value nT0 will purely depend on RT0 only. Assuming that nT0 is proportional to RT0, let proportional constant be K, then nT0 has the following relationship with temperature T:

$$nT0 = K \cdot RT0 = K \cdot f(T) \quad \ldots\ldots \text{Expression A}$$

Therefore, temperature T can be expressed as a digital value by performing the conversion processing that accords with the characteristics shown in Figure 24-9 for nT0 by software.

To convert from an RT0 value to a digital value, the ratio is used between a) the oscillation frequency by the thermistor connected to the RT0 pin and the capacitor connected to the CS0 pin and b) the oscillation frequency by the reference resistor (which ideally should have no temperature characteristics) connected to the RS0 pin and the capacitor connected to the CS0 pin. This is for making the conditions other than resistance equal to eliminate the error factor in oscillation characteristics.
As shown in Figures 24-9 and 24-11, the RT0 value depends on temperature T and the RS0 value is assumed to be constant regardless of temperature T. It is ideal if the characteristics of the oscillation frequency fOSC to temperature T using these resistances will be like the solid lines in Figures 24-12 and 24-13; however, in reality, it would appear that they will be like the dotted lines due to error factors such as IC temperature characteristics.
Since the condition of f_{RCCLK} (RT0) and that of f_{RCCLK} (RS0) are the same except for the resistances, the error ratios are almost the same; therefore, errors can almost be eliminated by using the ratio between f_{RCCLK} (RT0) and f_{RCCLK} (RS0).
The ratio between f_{RCCLK} (RT0) and f_{RCCLK} (RS0) is equivalent to the above-mentioned A/D conversion value nT0 that should ideally depend only on RT0.

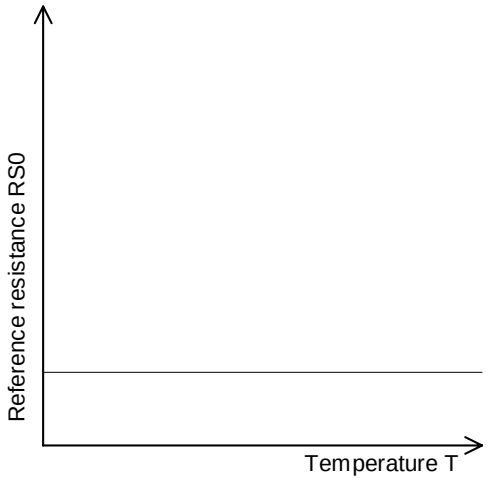


Figure 24-11 Temperature Characteristics of Reference Resistor

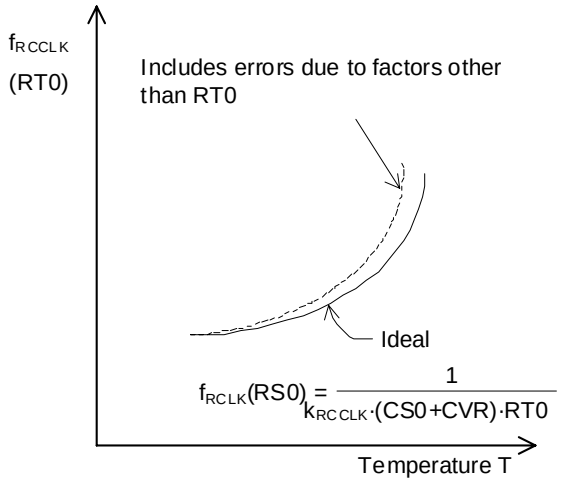


Figure 24-12 Oscillation Characteristics of Thermistor

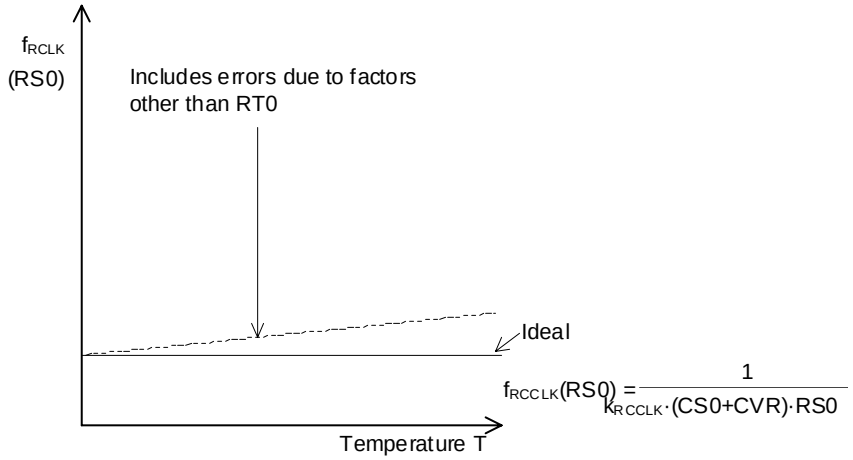


Figure 24-13 Oscillation Characteristics of Reference Resistor

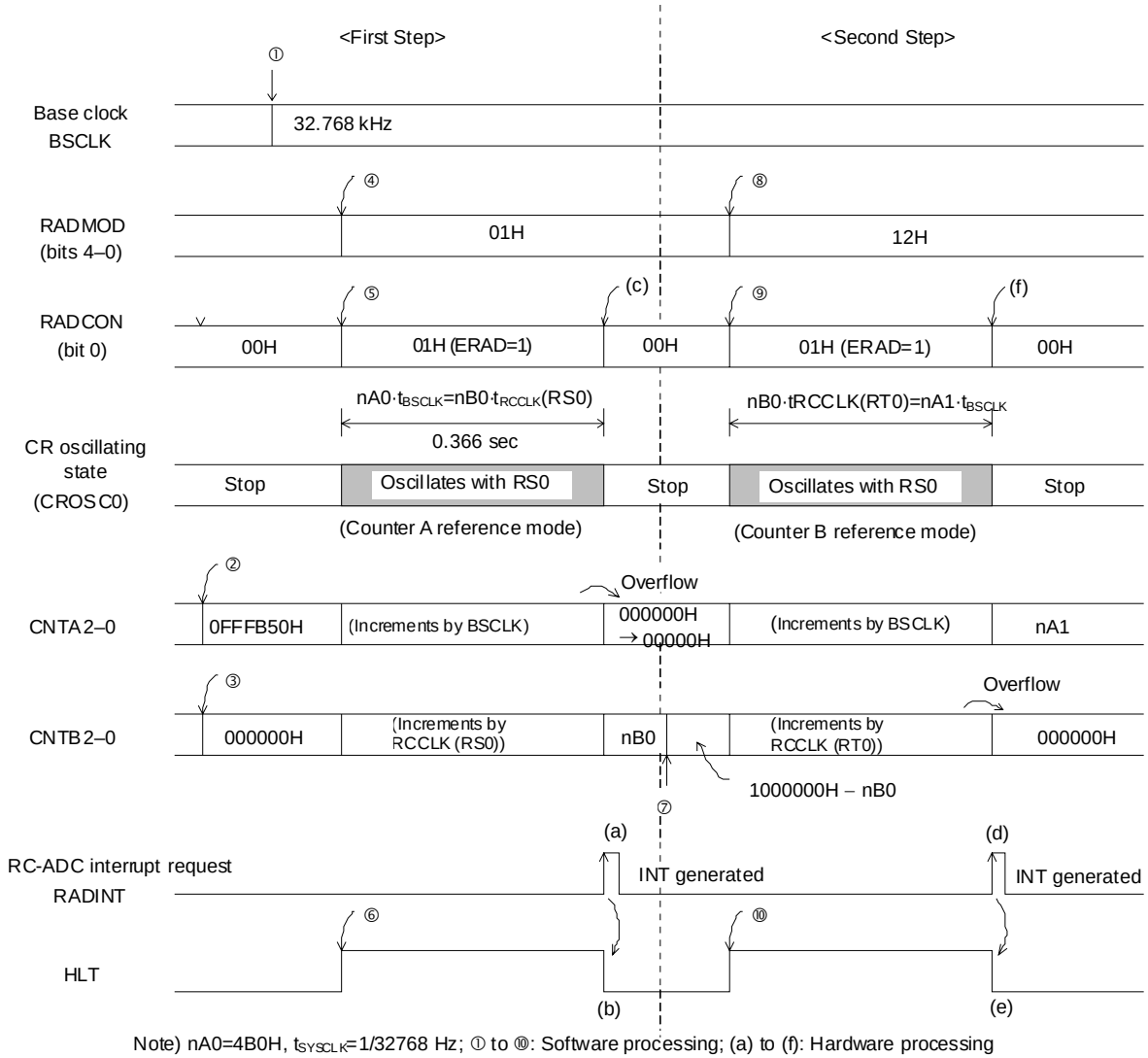
Figure 24-14 shows, as an example of method, a timing diagram of one cycle of conversion from analog value RT0 to a digital value, that is, A/D conversion.
Basically, one A/D conversion cycle must consist of two steps, as shown in Figure 24-14. The reason for requiring two steps is that the reference resistor and the thermistor must first be oscillated separately and then the ratio between the oscillation frequencies of them is used, as described above.
In the example below, operation for these two steps is performed using the following combination:

- First step = RC oscillation with RS0 in Counter A reference mode
- Second step = RC oscillation with RT0 in Counter B reference mode

Besides this, there would be several possible A/D conversion methods.
In the above method, the operation time (gate time) for the second step fluctuates depending on the value of thermistor RT0. To avoid the fluctuation of the operation time, using a method that uses the following combination is recommended:

- First step = RC oscillation with RS0 in Counter B reference mode
- Second step = RC oscillation with RT0 in Counter A reference mode

A/D conversion procedure is explained below by taking Figure 24-14 as an example.



Note) nA0=4B0H, t_{SYSCLK}=1/32768 Hz; ① to ⑩: Software processing; (a) to (f): Hardware processing

Figure 24-14 Timing Diagram for 1 Cycle of A/D Conversion (Example)

<First Step>

① Set the base clock to 32.768 kHz. (Write "00H" in FCON0.)
② Preset "1000000H – nA0" in Counter A.
③ Preset "000000H" in Counter B.
④ Write "01H" in RADMOD to select Counter A reference mode and the oscillation mode that uses reference resistance RS0.
⑤ Write "01H" in RADCON to start A/D conversion operation.
⑥ Write "1" in the HLT bit of SBYCON (see Chapter 4, "MCU") to set the device to HALT mode.

Note:
In this example, nA0 is set to 4B0H because the gate time "$nA0 \cdot t_{BSCLK}$" in oscillation mode with reference resistor RS0 is set to 0.3666 second. The value of nA0 is related to how much the margin of the quantizatoin error of the A/D conversion is: the greater the nA0 value is, the smaller the margin of error becomes.
To reduce noise contamination to the RC oscillator circuit caused by CPU operation, it is recommended to constantly put the device into HALT mode during operation of RC oscillation.

From this point of time, the RC oscillator circuit (RCOSC0) continues oscillation for about 0.366 second with the reference resistance RS0. Then, when Counter A overflows, the RADINT signal is set to "1" and an RC-ADC interrupt request is generated (section (a)). Also, the generation of interrupt request releases HALT mode (section (b)) and at the same time, A/D conversion operation stops (section (c), RARUN bit = "0"). At this time, Counter A is set to "000000H".
The content of Counter B at this time is expressed by the following expression:

$$nB0 = nA0 \cdot \frac{t_{BSCLK}}{t_{RCCLK}(RS0)} \quad \ldots\ldots \text{Expression B}$$

That completes the operations in First Step .

<Second Step>

⑦ Calculate "1000000H – nB0" from the content of Counter B "nB0" and set the obtained value in Counter B. At this point, Counter A needs to be cleared; however, no processing is required since the counter is already set to "000000H".
⑧ Write "12H" in RADMOD to select Counter B reference mode and the oscillation mode that uses thermistor RT0.
⑨ Write "01H" in RADCON to start A/D conversion operation.
⑩ Write "1" in the HLT bit of SBYCON (see Chapter 4, "MCU") to set the device to HALT mode.

The RC oscillator circuit (RCOSC0) oscillates with thermistor RT0 from this point until Counter B overflows. This period is equal to the product of "nB0" obtained in the First Step and the oscillation period t_{RCCLK} (RT0) using RT0.
When Counter B overflows, the RADINT signal is set to "1" and an RC-ADC interrupt request is generated (section (d)). Also, the generation of interrupt request releases HALT mode (section (e)) and at the same time, A/D conversion operation stops (section (f), RARUN bit = "0").
This completes the operations in Second Step .

The content of Counter A at this time becomes the A/D converison value nA1, which is expressed by the following expression:

$$nA1 = nB0 \cdot \frac{t_{RCCLK}\ (RT0)}{t_{BSCLK}} \quad \ldots\ldots \text{Expression C}$$

From expressions B and C, nA1 is expressed by the following expression:

$$nA1 = nA0 \cdot \frac{t_{RCCLK}\ (RT0)}{t_{RCCLK}\ (RS0)} \quad \ldots\ldots \text{Expression D}$$

where t_{RCCLK} (RS0) is the oscillator clock period by reference resistor RS0 and t_{RCCLK} (RT0) the oscillator clock period by thermistor RT0.
Since the oscillation period is expressed by "$t_{RCCLK} = k_{RCCLK} \cdot R \cdot C$", t_{RCCLK} (RS0) and t_{RCCLK} (RT0) are expressed by the following expressions:

$$t_{RCCLK}(RS0) = k_{RCCLK} \cdot (CS0+CVR) \cdot RS0$$
$$t_{RCCLK}(RT0) = k_{RCCLK} \cdot (CS0+CVR) \cdot RT0 \quad \ldots\ldots \text{Expression E}$$

When expression E is substituted for expression D, nA1 will be:

$$nA1 = nA0 \cdot \frac{RT0}{RS0}$$

Since "nA0" ("4B0H" in this example) and RS0 are constants whose values are fixed, "nA1" is a digital value proportional to RT0. This very "nA1" corresponds to "nT0" in expression A.

That concludes the description of the A/D conversion method using a thermistor. "nA1" that has been obtained must further be converted to a value such as a temperature indication value for thermometer by program according to the temperature-to-resistance characteristics of the themistor.

24.3.4 Monitoring RC Oscillation

The RC oscillator clock (RCCLK) can be output using the secondary function of the P35 pin of Port 3. See Chapter 20, "Port 3," for the details of the secondary function of P35.
Monitoring RC oscillation is useful for checking the characteristics of the RC oscillator circuit. That is, the relationship between a sensor, such as a thermistor, and the oscillation frequency can be measured. For instance, the coefficient for conversion from the above-described nA1 value to a temperature indication value can be obtained by checking the relationship between the ambient temperature of a themistor-incorporated RC oscillator, the oscillation frequency with thermistor RT0, and the oscillation frequency with reference resistor RS0.

Note:
- P35 (RCM) is a monitor pin for oscillation clock. The channel 0(P34-P30) and channel 1(P47-P44) share the monitor pin.
- Please use P35 (RCM) for the evaluation purpose and disable the output while operating in an actual application to minimize the noise.

24.4 Specifying port registers

When you want to make sure the RC-ADC function is working, please check related port registers are specified. See Chapter 20, "Port 3" and Chapter 21, "Port 4" for detail about the port registers.

24.4.1 Functioning P35(RCM), P34(RCT0), P33(RT0), P32(RS0), P31(CS0) and P30(IN0) as the RC-ADC(Ch0)

Set P35MD1-P30MD1 bits(bit5-bit0 of P3MOD1 register) to "0" and set P35MD0-P30MD0(bit5-bit0 of P3MOD0 register) to "1", for specifying the RC-ADC as the secondary function of P35, P34, P33, P32, P31 and P30.

Reg. name	P3MOD1 register (Address: 0F21DH)							
Bit	7	6	**5**	**4**	**3**	**2**	**1**	**0**
Bit name	P37MD1	P36MD1	**P35MD1**	**P34MD1**	**P33MD1**	**P32MD1**	**P31MD1**	**P30MD1**
Data	-	-	**0**	**0**	**0**	**0**	**0**	**0**

Reg. name	P3MOD0 register (Address: 0F21CH)							
Bit	7	6	**5**	**4**	**3**	**2**	**1**	**0**
Bit name	P37MD0	P36MD0	**P35MD0**	**P34MD0**	**P33MD0**	**P32MD0**	**P31MD0**	**P30MD0**
Data	-	-	**1**	**1**	**1**	**1**	**1**	**1**

Set P34C1-P30C1 bit(bit4-0 of P3CON1 register) to "0", set P34C0-P30C0 bit(bit4-0 of P3CON0 register) to "0", and set P34DIR-P30DIR bit(bit4-0 of P3DIR register) to "1", for specifying the P34-P30 as high-impedance inputs.
The P34C1-P30C1 bit and P34C0-P30C0 bit can be set to all "1" instead of all "0" to select the high-impedance inputs.
Set P35C1 bit(bit5 of P3CON1 register) to "1", set P35C0 bit(bit5 of P3CON0 register) to "1", and set P35DIR bit(bit5 of P3DIR register) to "0", for specifying the P35 as CMOS outputs.

Reg. name	P3CON1 register (Address: 0F21BH)							
Bit	7	6	**5**	**4**	**3**	**2**	**1**	**0**
Bit name	P37C1	P36C1	**P35C1**	**P34C1**	**P33C1**	**P32C1**	**P31C1**	**P30C1**
Data	-	-	**1**	**0**	**0**	**0**	**0**	**0**

Reg. name	P3CON0 register (Address: 0F21AH)							
Bit	7	6	**5**	**4**	**3**	**2**	**1**	**0**
Bit name	P37C0	P36C0	**P35C0**	**P34C0**	**P33C0**	**P32C0**	**P31C0**	**P30C0**
Data	-	-	**1**	**0**	**0**	**0**	**0**	**0**

Reg. name	P3DIR register (Address: 0F219H)							
Bit	7	6	**5**	**4**	**3**	**2**	**1**	**0**
Bit name	P37DIR	P36DIR	**P35DIR**	**P34DIR**	**P33DIR**	**P32DIR**	**P31DIR**	**P30DIR**
Data	-	-	**0**	**1**	**1**	**1**	**1**	**1**

Data of P35D-P30D bits (bit5-0 of P3D register) do not affect to the RC-ADC function, so don't care the data for the function.

Reg. name	P3D register (Address: 0F218H)							
Bit	7	6	**5**	**4**	**3**	**2**	**1**	**0**
Bit name	P37D	P36D	**P35D**	**P34D**	**P33D**	**P32D**	**P31D**	**P30D**
Data	-	-	**	**	**	**	**	**

- : Bit does not exist.
* : Bit not related to the RC-ADC channel 0(using P35,P34,P33,P32,P31 and P30) function
** : Don't care the data

24.4.2 Functioning P47(RT1), P46(RS1), P45(CS1) and P44(IN1) as the RC-ADC(Ch1)

Set P47MD1-P44MD1 bits(bit7-bit4 of P4MOD1 register) to "0" and set P47MD0-P44MD0(bit7-bit4 of P4MOD0 register) to "1", for specifying the RC-ADC as the secondary function of P47, P46, P45 and P44.

Reg. name	P4MOD1 register (Address: 0F225H)							
Bit	**7**	**6**	**5**	**4**	3	2	1	0
Bit name	**P47MD1**	**P46MD1**	**P45MD1**	**P44MD1**	P43MD1	P42MD1	P41MD1	P40MD1
Data	**0**	**0**	**0**	**0**	*	*	*	*

Reg. name	P4MOD0 register (Address: 0F224H)							
Bit	**7**	**6**	**5**	**4**	3	2	1	0
Bit name	**P47MD0**	**P46MD0**	**P45MD0**	**P44MD0**	P43MD0	P42MD0	P41MD0	P40MD0
Data	**1**	**1**	**1**	**1**	*	*	*	*

Set P47C1-P44C1 bit(bit7-4 of P4CON1 register) to "0", set P47C0-P44C0 bit(bit7-4 of P4CON0 register) to "0", and set P47DIR-P44DIR bit(bit7-4 of P4DIR register) to "1", for specifying the P47-P44 as high-impedance inputs.
The P47C1-P44C1 bit and P47C0-P44C0 bit can be set to all "1" instead of all "0" to select the high-impedance inputs.

Reg. name	P4CON1 register (Address: 0F223H)							
Bit	**7**	**6**	**5**	**4**	3	2	1	0
Bit name	**P47C1**	**P46C1**	**P45C1**	**P44C1**	P43C1	P42C1	P41C1	P40C1
Data	**0**	**0**	**0**	**0**	*	*	*	*

Reg. name	P4CON0 register (Address: 0F222H)							
Bit	**7**	**6**	**5**	**4**	3	2	1	0
Bit name	**P47C0**	**P46C0**	**P45C0**	**P44C0**	P43C0	P42C0	P41C0	P40C0
Data	**0**	**0**	**0**	**0**	*	*	*	*

Reg. name	P4DIR register (Address: 0F221H)							
Bit	**7**	**6**	**5**	**4**	3	2	1	0
Bit name	**P47DIR**	**P46DIR**	**P45DIR**	**P44DIR**	P43DIR	P42DIR	P41DIR	P40DIR
Data	**1**	**1**	**1**	**1**	*	*	*	*

Data of P47D-P44D bits (bit7-4 of P4D register) do not affect to the RC-ADC function, so don't care the data for the function.

Reg. name	P4D register (Address: 0F220H)							
Bit	**7**	**6**	**5**	**4**	3	2	1	0
Bit name	**P47D**	**P46D**	**P45D**	**P44D**	P43D	P42D	P41D	P40D
Data	******	******	******	******	*	*	*	*

* : Bit not related to the RC-ADC channel 1(using P47,P46,P45 and P44) function
** : Don't care the data

Note:
Status of output pins P31-P34 and P45-P47 changes according to the RC oscillation mode specified by OM0-OM3 bit of RADMOD register.

Chapter 25

Successive Approximation Type A/D Converter

25. Successive Approximation Type A/D Converter

25.1 Overview

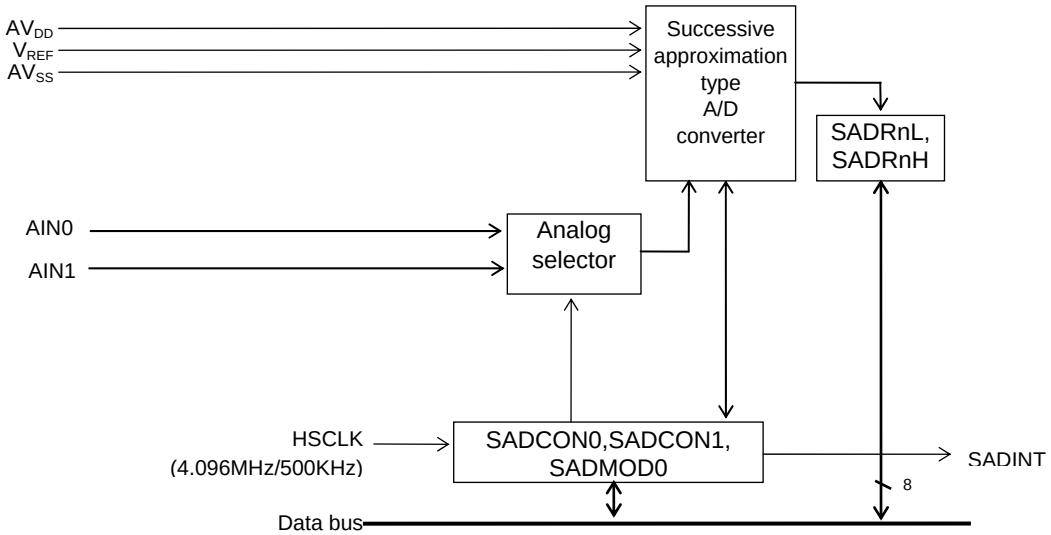
This LSI has a built-in 2-channel successive approximation type A/D converter (SA-ADC).

25.1.1 Features

- Built-in sample/hold 12-bit successive approximation type A-D converter, which enables channel selection from 2 channels

25.1.2 Configuration

Figure 25-1 shows the configuration of SA-ADC.



SADR0L: SA-ADC result register 0L
SADR0H: SA-ADC result register 0H
SADR1L: SA-ADC result register 1L
SADR1H: SA-ADC result register 1H
SADCON0: SA-ADC control register 0
SADCON1: SA-ADC control register 1
SADMOD0: SA-ADC mode register 0

Figure 25-1 Configuration of SA-ADC

25.1.3 List of Pins

Pin name	I/O	Description
AV_{DD}	—	Positive power supply pin for the successive approximation type A/D converter
V_{REF}	—	Reference power supply pin for the successive approximation type A/D converter
AV_{SS}	—	Negative power supply pin for the successive approximation type A/D converter
AIN0	I	Successive approximation type A/D converter input pin 0
AIN1	I	Successive approximation type A/D converter input pin 1

25.2 Description of Registers

25.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2D0H	SA-ADC result register 0L	SADR0L	SADR0	R	8/16	00H
0F2D1H	SA-ADC result register 0H	SADR0H		R	8	00H
0F2D2H	SA-ADC result register 1L	SADR1L	SADR1	R	8/16	00H
0F2D3H	SA-ADC result register 1H	SADR1H		R	8	00H
0F2F0H	SA-ADC control register 0	SADCON0	SADCON	R/W	8/16	02H
0F2F1H	SA-ADC control register 1	SADCON1		R/W	8	00H
0F2F2H	SA-ADC mode register 0	SADMOD0	—	R/W	8	00H

25.2.2 SA-ADC Result Register 0L (SADR0L)

Address: 0F2D0H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR0L	SAR03	SAR02	SAR01	SAR00	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR0L is a special function register (SFR) used to store SA-ADC conversion results on channel 0.
SADR0L is updated after A/D conversion.

[Description of Bits]

- **SAR03-SAR00** (bits 7-4)
  The SAR03–SAR00 bits are used to store the values of bit 3 to bit 0 of A/D conversion results (12 bits) on channel 0.

25.2.3 SA-ADC Result Register 0H (SADR0H)

Address: 0F2D1H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR0H	SAR0B	SAR0A	SAR09	SAR08	SAR07	SAR06	SAR05	SAR04
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR0H is a special function register (SFR) used to store SA-ADC conversion results on channel 0.
SADR0H is updated after A/D conversion.

[Description of Bits]

- **SAR0B-SAR04** (bits 7-0)
  The SAR0B3–SAR04 bits are used to store the values of bit 11 to bit 4 of A/D conversion results (12 bits) on channel 0.

25.2.4 SA-ADC Result Register 1L (SADR1L)

Address: 0F2D2H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR1L	SAR13	SAR12	SAR11	SAR10	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR1L is a special function register (SFR) used to store SA-ADC conversion results on channel 1.
SADR1L is updated after A/D conversion.

[Description of Bits]

- **SAR13-SAR10** (bits 7-4)
  The SAR13–SAR10 bits are used to store the values of bit 3 to bit 0 of A/D conversion results (12 bits) on channel 1.

25.2.5 SA-ADC Result Register 1H (SADR1H)

Address: 0F2D3H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR1H	SAR1B	SAR1A	SAR19	SAR18	SAR17	SAR16	SAR15	SAR14
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR1H is a special function register (SFR) used to store SA-ADC conversion results on channel 1.
SADR1H is updated after A/D conversion.

[Description of Bits]

- **SAR1B-SAR14** (bits 7-0)
  The SAR1B–SAR14 bits are used to store the values of bit 11 to bit 4 of A/D conversion results (12 bits) on channel 1.

25.2.6 SA-ADC Control Register 0 (SADCON0)

Address: 0F2F0H
Access: R/W
Access size: 8/16 bits
Initial value: 02H

	7	6	5	4	3	2	1	0
SADCON0	—	—	—	—	—	—	SACK	SALP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SADCON0 is a special function register (SFR) used to control the operation of the SA-ADC.

[Description of Bits]

- **SALP** (bit 0)

SALP	Description
0	Single A/D conversion only (Initial value)
1	Consecutive A/D conversion

This bit is used to select whether A/D conversion is performed once only for each channel or consecutively. When this bit is set to "0", A/D conversion is performed once only for each channel and when it is set to "1", A/D conversion is performed consecutively according to the settings of the SA-ADC mode register (SADMOD0).

- **SACK** (bit 1)

SACK	Description
0	HSCLK is set to the range of 375kHz to 625kHz.
1	HSCLK is set to the range of 1.5MHz to 4.2MHz (Initial value)

The SACK bit is used to set an A/D conversion time.
As a conversion time is set by counting HSCLK, set this bit to "0" when HSCLK is set in the range of 375kHz to 625kHz and when HSCLK is set in the range of 1.5MHz to 4.2MHz, set this bit to "1".

Note:
Set the SACK bit when the SARUN bit of the SADCON1 register is "0" (A/D conversion inactive).
SA-ADC is available only when VDD=1.8V to 3.6V and HSCLK is in the ranges of 375KHz to 625kHz and of 1.5MHz to 4.2MHz.

25.2.7 SA-ADC Control Register 1 (SADCON1)

Address: 0F2F1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADCON1	—	—	—	—	—	—	—	SARUN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SADCON1 is a special function register (SFR) used to control the operation of the SA-ADC.

[Description of Bits]

- **SARUN** (bit 0)

SARUN	Description
0	Stops conversion. (Initial value)
1	Starts conversion.

The SARUN bit is used to start or stop SA-ADC conversion. Setting this bit to "1" starts A/D conversion and setting it to "0" stops A/D conversion.
When SALP of SADCON0 is "0" and then A/D conversion on the channel with the largest channel number among the selected ones is terminated, the SARUN bit is automatically set to "0".

Notes:
Use the SA-ADC with high-speed clock oscillation (HSCLK) enabled in the frequency control register (FCON0).
The SA-ADC is available only when V_{DD} = 1.8 to 3.6 V and HSCLK is in the ranges of 3.75kHz to 625kHz and of 1.5MHz to 4.2 MHz.
Do not start A/D conversion in the state in which bits 1 (SACH1) and 0 (SACH0) of SA-ADC mode register 0 are "0" and "0" respectively. When A/D conversion is started in this state, A/D conversion is not done while the A/D converter is activated. Therefore, the SA-ADC result register is not updated, the A/D conversion termination interrupt is not generated, A/D conversion is not terminated automatically, and SARUN remains "1".

25.2.8 SA-ADC Mode Register 0 (SADMOD0)

Address: 0F2F2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADMOD0	—	—	—	—	—	—	SACH1	SACH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SADMOD0 is a special function register (SFR) used to choose A/D conversion channel(s).

[Description of Bits]

- **SACH0** (bit 0)

SACH0	Description
0	Stops conversion on channel 0. (Initial value)
1	Performs conversion on channel 0.

- **SACH1** (bit 1)

SACH1	Description
0	Stops conversion on channel 1. (Initial value)
1	Performs conversion on channel 1.

The SACH1 and SACH0 bits are used to select channel(s) on which A/D conversion is performed. If both channel 1 and channel 0 are set to "1", A/D conversion is performed on channel 0 first, and then channel 1.

Do not start A/D conversion both channel 1 and channel 0 set to 0. If conversion is started, the A/D conversion circuit is activated (ON), however, A/D conversion is not done. Therefore, the SA-ADC result register is not updated, A/D conversion termination interrupt does not occur, A/D conversion does not terminate automatically, and consequently, bit 0 (SARUN) of the SA-ADC control register (SADCON1) remains "1".

25.3 Description of Operation

25.3.1 Settings of A/D Conversion Channels

According to the setting of SA-ADC mode register 0 (SADMOD0), A/D conversion is performed as shown below and A/D conversion results are stored in the SA-ADC result register.

SA-ADC mode register 0		SA-ADC result register	Analog input
SACH0/1	0/1		
SACH0	0	SADR0	
SACH1	1	SADR1	AIN1 input
SACH0	1	SADR0	AIN0 input
SACH1	0	SADR1	
SACH0	1	SADR0	AIN0 input
SACH1	1	SADR1	AIN1 input

The values of the result register for the sections with a slash mark remain unchanged.
Do not start A/D conversion when bits 1 (SACH1) or 0 (SACH0) of SA-ADC mode register 0 (SADMOD0) is "0". If A/D conversion is started, the A/D conversion circuit is set to ON. However, as A/D conversion is not performed, the SA-ADC result register is not updated, an A/D conversion termination interrupt is not generated, A/D conversion does not terminate automatically, and bit 0 (SARUN) of the SA-ADC control register (SADCON1) remains "1".

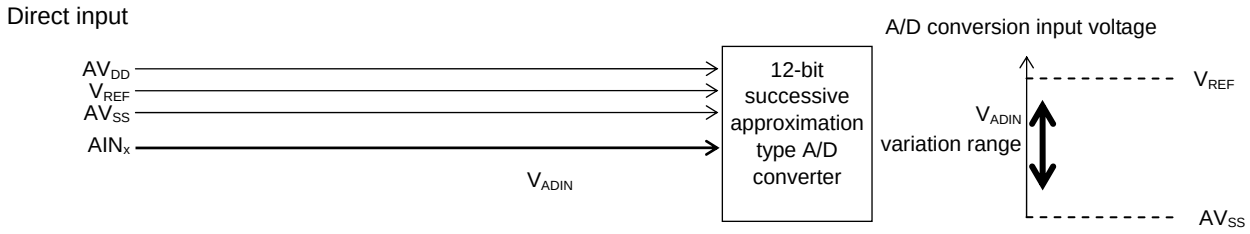


Figure 25-2 A/D conversion pins and conversion range

25.3.2 Operation of the Successive Approximation A/D Converter

For direct input, operate SA-ADC in the following procedure.

1. Before starting SA-ADC, start oscillation of the high-speed clock (HSCLK) and wait until the oscillator settles.
2. When HSCLK is within the range from 375KHz to 625kHz, set bit 1 (SACK) of the SA-ADC control register (SADCON0) to "0" and when HSCLK is within the range from 1.5MHz to 4.2MHz, set it to "1".
3. Set the SA-ADC mode register 0 (SADMOD0).
4. When bit 0 (SARUN) of SA-ADC control register 1 (SADCON1) is set to "1", the SA-ADC circuit becomes active and performs A/D conversion from the lower channel number that is selected in the SA-ADC mode register (SADMOD0).
5. A/D conversion results are stored in the applicable SA-ADC result registers (SADRnL, SADRnH) and when A/D conversion of the largest channel number that is selected terminates, an SA-ADC conversion termination interrupt (ADSINT) is generated.
6. Finally, using bit 0 (SALP) of the SADCON0 register, it is possible to select whether A/D conversion is terminated (SARUN bit is "0") or A/D conversion is automatically restarted at termination of A/D conversion of the last channel.

Even if a channel is switched during A/D conversion, the channel that is selected at the start of A/D conversion is maintained until an A/D conversion termination interrupt occurs.
Figure 25-3 shows the SA-ADC operation timing when channel 0 and channel 1 are selected.

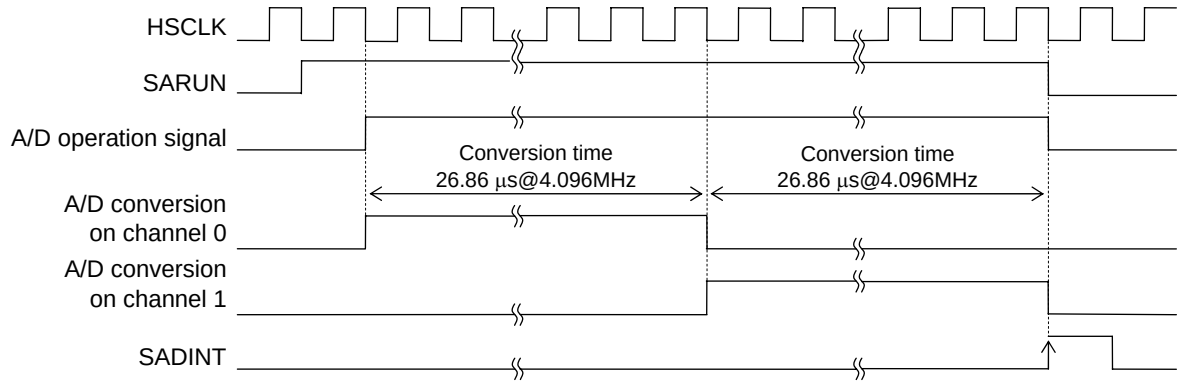


Figure 25-3 SA-ADC Operation Timing at Direct Input

Note:
A/D conversion time in 500kHzRC oscillation mode is 46 μs.

Chapter 26

LCD Drivers

26. LCD Drivers

26.1 Overview

This LSI includes LCD drivers that display the contents that are set in the display register.
The LCD drivers handle the LCD display functions with four blocks.

1. Display registers
2. Display allocation
3. Display control
4. Drivers

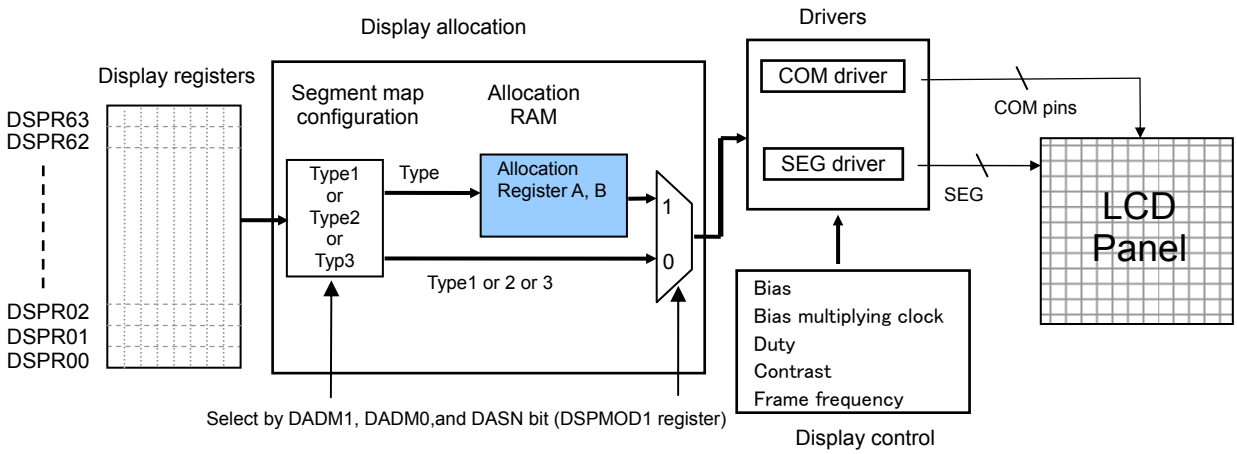


Figure 26-1 Configuration of LCD Display Function

The display registers are used to store the contents to be displayed as bit patterns.
The bit pattern storage method depends on the specification of the LCD panel to be used (display pattern and assignment of the COM pin and SEG pin) and the setting of the display allocation circuit.

The display allocation block controls mapping of the display register for the LCD common/segment.
Using the display allocation register A and B or not using them is selectable. When using them (Set DASN bit of DSPMOD1 register to "1"), the segment mapping of the display register can be specified in bit units by programming according to the contents of display allocation registers A and B. Therefore, the display register array can be changed in flexible and simplify the software process for display (This function is defined as the programmable display allocation function in the user's manual). Also, the data specified to the register A and B can be easily prepared by using LAPIS semiconductor LCD allocation Tool. Select type 3 for the display register segment map when using the programmable allocation function. The programmable display allocation function only generates table data can be used for the type 3.
When not using the display allocation register A and B (Set DASN bit of DSPMOD1 register to "0"), select type 2 or type 3 (type 1 is not available on ML610Q421/ML610Q422/ML610421/ML610422) for display registers segment map and control the display with the display register only.

The display control circuit generates LCD drive waveforms according to the characteristics of the LCD. A bias, a bias voltage multiplying clock, a duty, a frame frequency, and a contrast suitable for the LCD panel can be selected.

Note:
- The programmable display allocation function is available only when 1/1~1/8 duty is selected (when using eight COMs or less for display), it does not work when 1/9~1/16 duty is selected (when using nine COMs or more for display).
- Select type 3 for the display register segment map (Set DADM1 bit of DSPMOD1 register to "1") when using the programmable allocation function. LAPIS semiconductor LCD Tool only generates table data can be used for the type 3.
- When the programmable display function is not used (DASN = "0"), display allocation register A (0F400H to 0F5FFH) and display allocation register B (0F600H to 0F7FFH) can be used as 1K-byte data memory(RAM).

A) When not using Programmable display allocation function (DASN bit of DSPMOD1 register is "0")

Suitable for the dot matrix type LCD panel whose common/segment array is approximated to the bit array of the display register. One of two types for the display register segment mapping can be selected, the numbe of used COM pins determines the recommended type. See section 26.2.5, 26.2.9, and 26.3.2 for more detail.

When the programmable display function is not used, display allocation register A and display allocation register B (See section 26.2.7 and 26.2.8) can be used as 1K-byte data memory.

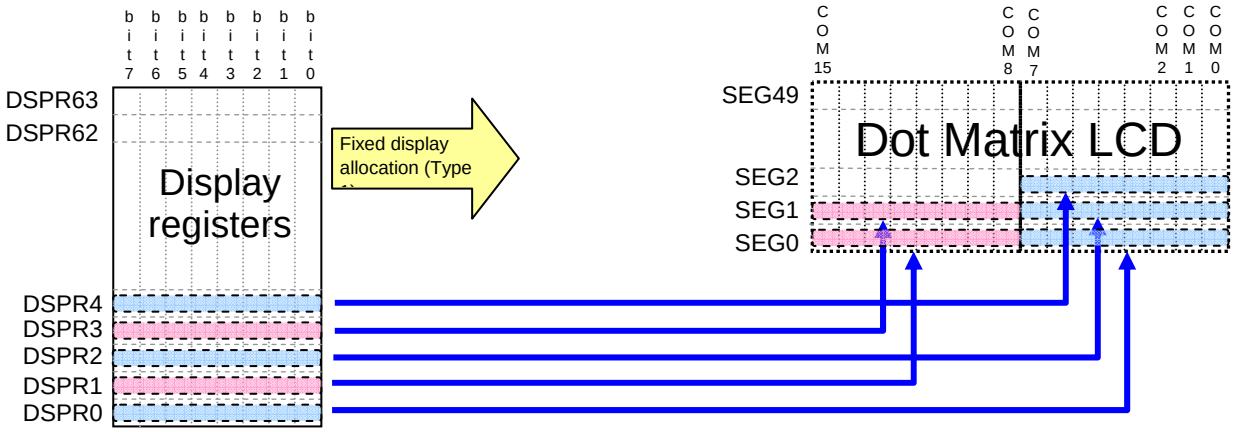
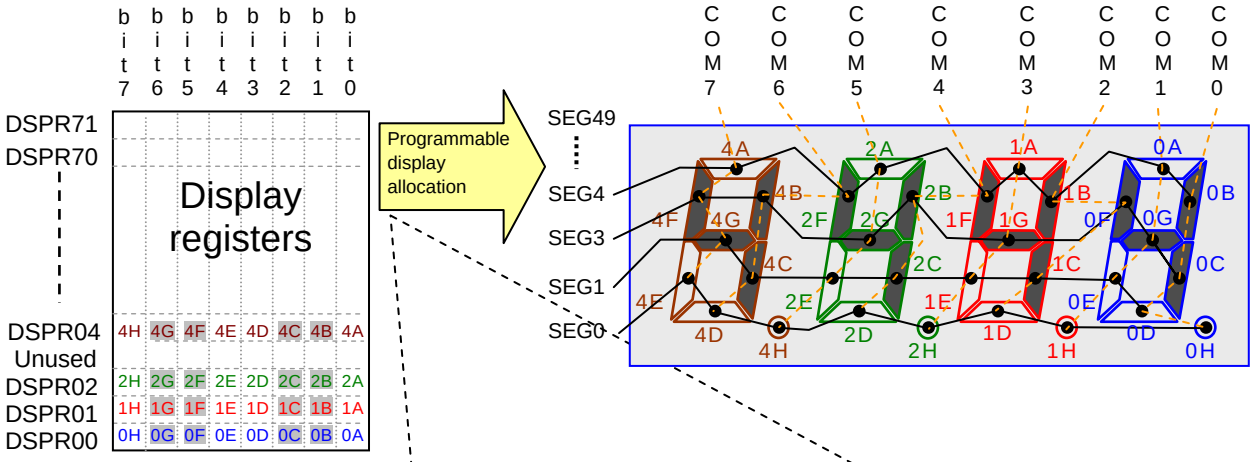


Figure 26-2 An example of correlation between display register and dot matrix type LCD

B) When using Programmable display allocation function (DASN bit of DSPMOD1 register is "1")

The programmable display allocation function is suitable for the LCD panel of segment type or character type whose common/segment array is restricted by the design or wiring. Segment mapping of the display register can be assigned in bit units by programming according to the contents of display allocation registers A and B. Therefore, the display register array can be changed in flexible and simplify the software process for display. Contents of the registers A(DSmCnA) specify addresses of the display registers (DSPR00 to 71) and contents of the registers B(DSmCnB) specify bits of the display registers, that are output to common "n" of segment "m".



DSPR	bit	Symbol	COM	SEG
…	…	…	…	…
DSPR4	6	4G	7	1
…	…	…	…	..
DSPR0	2	0C	0	3
DSPR0	1	0B	0	4
DSPR0	0	0A	1	4

Figure 26-3 An example of correlation between display registers and segment type LCD

26.1.1 Features

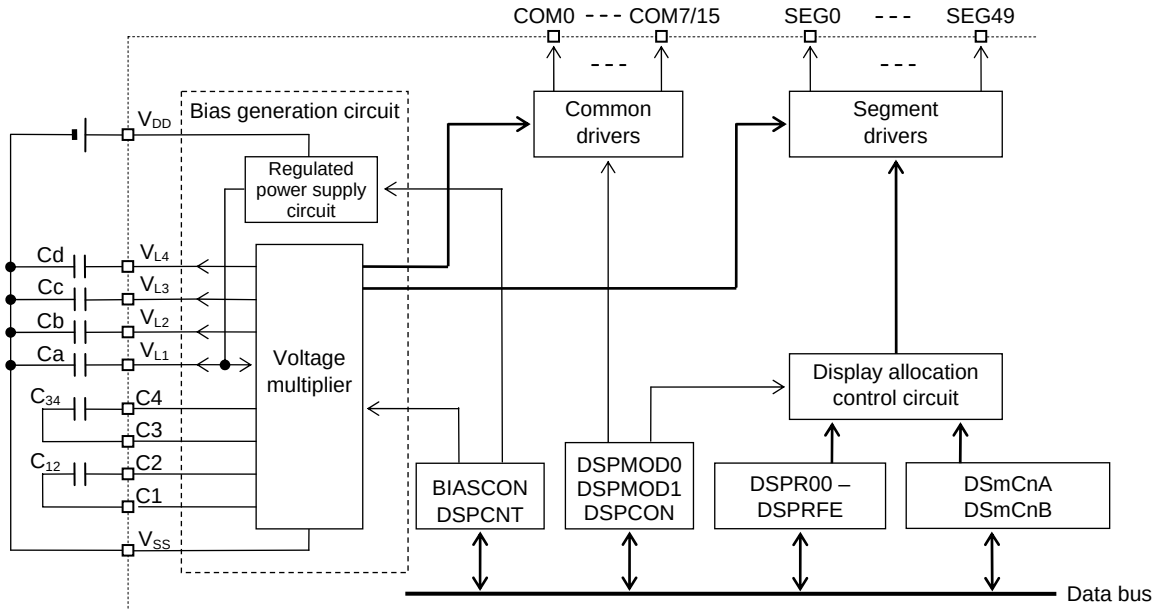
The LCD drivers are applicable to various types of LCD panels. The features include:

- ML610Q421/ML610421: 400 dots max. (50seg × 8com), 1/1 to 1/8 duty
- ML610Q422/ML610422: 800 dots max. (50seg × 16com), 1/1 to 1/16 duty
- 1/3 and 1/4 bias (4 types)
- Frame frequency selectable (4 types)
- Bias voltage multiplying clock selectable (8 types)
- Contrast adjustment (1/3 bias:32 steps, 1/4 bias: 20 steps)
- Programmable display allocation function (available only when 1/1~1/8 duty is selected)

The programmable display allocation function facilitates software display processing.
By using "ALL LCDs on mode" and "ALL LCDs off mode", LCD panel inspection processing software can be easily created.

26.1.2 Configuration of the LCD Drivers

Figure 26-4 shows the configuration of the LCD drivers and the bias generation circuit.



BIASCON : Bias circuit control register
DSPCNT : Display contrast register
DSPMOD0 : Display mode register 0
DSPMOD1 : Display mode register 1
DSPCON : Display control register
DSmCnA : Allocation register A (m = 0 to 63, n = 0 to 7)
DSmCnB : Allocation register B (m = 0 to 63, n = 0 to 7)
DSPR00 to DSPR71 : Display registers

Figure 26-4 Configuration of LCD Drivers and Bias Generation Circuit

26.1.3 Configuration of the Bias Generation Circuit

The bias generation circuit generates LCD drive voltages (V_{L1} to $V_{L4)}$ by multiplying the voltage (VL1) generated by the voltage regulator with the capacitors (C12 and C34).
When the BSON bit of the bias circuit control register (BIASCON) is set to "1", the bias generation circuit starts operation.
Display contrast adjustment is possible in 32 steps by using the display contrast register (DSPCNT).
Figure 26-5 shows the configurations of the bias generation circuit with 1/3 bias and with 1/4 bias.

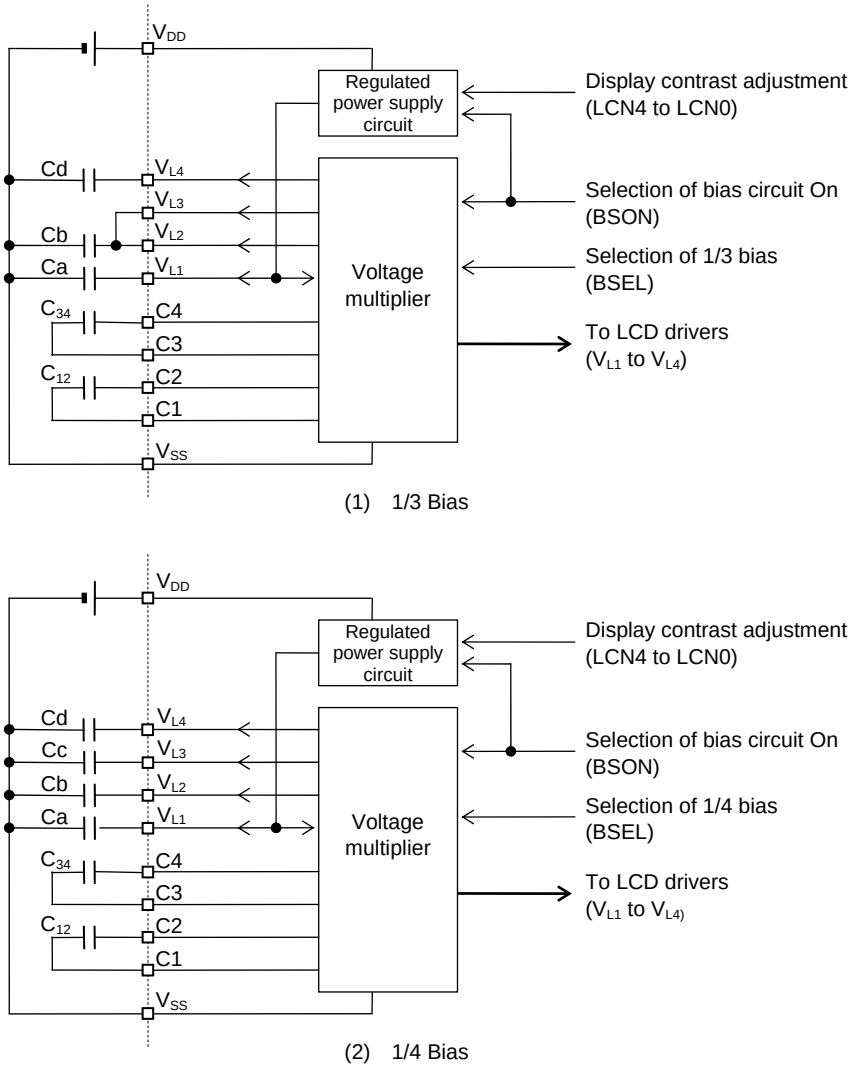


Figure 26-5 Configuration of Bias Generation Circuit

Note:
When using 1/3 bias, connect the V_{L2} pin and the V_{L3} pin externally.

26.1.4 List of Pins

Pin name	I/O	Description
V_{L1}	—	Power supply pin for LCD bias (internally generated)
V_{L2}	—	Power supply pin for LCD bias (internally generated)
V_{L3}	—	Power supply pin for LCD bias (internally generated)
V_{L4}	—	Power supply pin for LCD bias (internally generated)
C1	—	Capacitor connection pin for LCD bias generation
C2	—	Capacitor connection pin for LCD bias generation
C3	—	Capacitor connection pin for LCD bias generation
C4	—	Capacitor connection pin for LCD bias generation
COM0	O	LCD common pin
COM1	O	LCD common pin
COM2	O	LCD common pin
COM3	O	LCD common pin
COM4	O	LCD common pin
COM5	O	LCD common pin
COM6	O	LCD common pin
COM7	O	LCD common pin
COM8	O	LCD common pin
COM9	O	LCD common pin
COM10	O	LCD common pin
COM11	O	LCD common pin
COM12	O	LCD common pin
COM13	O	LCD common pin
COM14	O	LCD common pin
COM15	O	LCD common pin

Pin name	I/O	Description
SEG0	O	LCD segment pin
SEG1	O	LCD segment pin
SEG2	O	LCD segment pin
SEG3	O	LCD segment pin
SEG4	O	LCD segment pin
SEG5	O	LCD segment pin
SEG6	O	LCD segment pin
SEG7	O	LCD segment pin
SEG8	O	LCD segment pin
SEG9	O	LCD segment pin
SEG10	O	LCD segment pin
SEG11	O	LCD segment pin
SEG12	O	LCD segment pin
SEG13	O	LCD segment pin
SEG14	O	LCD segment pin
SEG15	O	LCD segment pin
SEG16	O	LCD segment pin
SEG17	O	LCD segment pin
SEG18	O	LCD segment pin
SEG19	O	LCD segment pin
SEG20	O	LCD segment pin
SEG21	O	LCD segment pin
SEG22	O	LCD segment pin
SEG23	O	LCD segment pin
SEG24	O	LCD segment pin
SEG25	O	LCD segment pin
SEG26	O	LCD segment pin
SEG27	O	LCD segment pin
SEG28	O	LCD segment pin
SEG29	O	LCD segment pin
SEG30	O	LCD segment pin
SEG31	O	LCD segment pin

Pin name	I/O	Description
SEG32	O	LCD segment pin
SEG33	O	LCD segment pin
SEG34	O	LCD segment pin
SEG35	O	LCD segment pin
SEG36	O	LCD segment pin
SEG37	O	LCD segment pin
SEG38	O	LCD segment pin
SEG39	O	LCD segment pin
SEG40	O	LCD segment pin
SEG41	O	LCD segment pin
SEG42	O	LCD segment pin
SEG43	O	LCD segment pin
SEG44	O	LCD segment pin
SEG45	O	LCD segment pin
SEG46	O	LCD segment pin
SEG47	O	LCD segment pin
SEG48	O	LCD segment pin
SEG49	O	LCD segment pin

26.2 Description of Registers

26.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F0F0H	Bias circuit control register	BIASCON	—	R/W	8	08H
0F0F1H	Display contrast register	DSPCNT	—	R/W	8	00H
0F0F2H	Display mode register 0	DSPMOD0	DSPMOD	R/W	8/16	00H
0F0F3H	Display mode register 1	DSPMOD1		R/W	8	00H
0F0F4H	Display control register	DSPCON		R/W	8	00H
0F100H to 0F171H	Display register 00 to Display register 71	DSPR00 to DSPR71	—	R/W	8	Undefined
0F400H to 0F5FFH	Display allocation register A	DS0C0A to DS63C7A	—	R/W	8	Undefined
0F600H to 0F7FFH	Display allocation register B	DS0C0B to DS63C7B	—	R/W	8	Undefined

26.2.2 Bias Circuit Control Register 0 (BIASCON)

Address: 0F0F0H
Access: R/W
Access size: 8 bits
Initial value: 08H

	7	6	5	4	3	2	1	0
BIASCON	—	—	—	BSEL	BSN2	BSN1	BSN0	BSON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	0	0	0

BIASCON is a special function register (SFR) to control the bias generation circuit.

[Description of Bits]

- **BSON** (bit 0)
  The BSON bit is used to control the operation of the bias generation circuit.
  When BSON is set to "1", the bias generation circuit generates the LCD drive voltages (VL1 to VL4).

BSON	Description
0	Bias circuit Off (initial value)
1	Bias circuit On

- **BSN2-BSN0** (bits 3-1)
  The BSN2 to BSN0 bits are used to select a clock for multiplying the bias voltage in the bias generation circuit.
  LSCLK to 1/128LSCLK can be selected.

BSN2	BSN1	BSN0	Description
0	0	0	1/1 LSCLK (32 kHz)
0	0	1	1/2 LSCLK (16 kHz)
0	1	0	1/4 LSCLK (8 kHz)
0	1	1	1/8 LSCLK (4 kHz)
1	0	0	1/16 LSCLK (2 kHz) (initial value)
1	0	1	1/32 LSCLK (1 kHz)
1	1	0	1/64 LSCLK (512 Hz)
1	1	1	1/128 LSCLK (256 Hz)

- **BSEL** (bit 4)
  The BSEL bit is used to set the bias in the bias generation circuit.
  1/3 bias or 1/4 bias can be selected.

BSEL	Description
0	1/3 bias (initial value)
1	1/4 bias

26.2.3 Display Control Register (DSPCNT)

Address: 0F0F1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
DSPCNT	—	—	—	LCN4	LCN3	LCN2	LCN1	LCN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSPCNT is a special function register (SFR) to adjust the contrast of display (32 steps).
For the setting value of DSPCNT and the LCD drive voltages (V_{L1}, V_{L2}, V_{L3}, V_{L4}), see Appendix C, "Electrical Characteristics".

[Description of Bits]

- **LCN4-LCN0** (bits 4-0)
  The LCN4 to LCN0 bits are used to adjust the contrast of display (32 steps).

LCN4	LCN3	LCN2	LCN1	LCN0	Description		V_{L1} voltage (typ.) V
0	0	0	0	0	Low		0.94 (initial value)
0	0	0	0	1	▲		0.96
0	0	0	1	0			0.98
0	0	0	1	1			1.00
0	0	1	0	0			1.02
0	0	1	0	1			1.04
0	0	1	1	0			1.06
0	0	1	1	1			1.08
0	1	0	0	0			1.10
0	1	0	0	1			1.12
0	1	0	1	0			1.14
0	1	0	1	1			1.16
0	1	1	0	0			1.18
0	1	1	0	1			1.20
0	1	1	1	0			1.22
0	1	1	1	1			1.24
1	0	0	0	0			1.26
1	0	0	0	1			1.28
1	0	0	1	0			1.30
1	0	0	1	1			1.32
1	0	1	0	0		V_{L1} = 1.32 when 1/4 bias is selected.	1.34
1	0	1	0	1			1.36
1	0	1	1	0			1.38
1	0	1	1	1			1.40
1	1	0	0	0			1.42
1	1	0	0	1			1.44
1	1	0	1	0			1.46
1	1	0	1	1			1.48
1	1	1	0	0			1.50
1	1	1	0	1			1.52
1	1	1	1	0	▼		1.54
1	1	1	1	1	High		1.56

Note: Only the 20-step adjustment is usable when 1/4 bias is selected (when the BSEL bit of the BIASCON register is "1").

26.2.4 Display Mode Register 0 (DSPMOD0)

Address: 0F0F2H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
DSPMOD0	—	FRM1	FRM0	—	DUTY3	DUTY2	DUTY1	DUTY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSPMOD0 is a special function register (SFR) to control the display mode of the LCD drivers.

[Description of Bits]

- **DUTY4-DUTY0** (bits 4-0)
  The DUTY4 to DUTY0 bits are used to specify the duty in 16 steps (1/1 to 1/16).

DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	Description
0	0	0	0	0	1/1 duty (initial value)
0	0	0	0	1	1/2 duty
0	0	0	1	0	1/3 duty
0	0	0	1	1	1/4 duty
0	0	1	0	0	1/5 duty
0	0	1	0	1	1/6 duty
0	0	1	1	0	1/7 duty
0	0	1	1	1	1/8 duty
0	1	0	0	0	1/9 duty
0	1	0	0	1	1/10 duty
0	1	0	1	0	1/11 duty
0	1	0	1	1	1/12 duty
0	1	1	0	0	1/13 duty
0	1	1	0	1	1/14 duty
0	1	1	1	0	1/15 duty
0	1	1	1	1	1/16 duty

- **FRM1-FRM0** (bits 6-5)
  The FRM1 to FRM0 bits are used to select a frame frequency of the LCD drivers.
  The reference frequency of a frame frequency (LLSCLK = 32.768 kHz) is selectable from 64 Hz, 73 Hz, 85 Hz, or 102 Hz.

FRM1	FRM0	Description
0	0	Reference frequency: 64 Hz (initial value)
0	1	Reference frequency: 73 Hz
1	0	Reference frequency: 85 Hz
1	1	Reference frequency: 102 Hz

The frame frequency for each duty is listed in Table 26-1.

Table 26-1 Frame Frequency for Each Duty

Duty	Frame frequency [Hz]			
	Reference frequency 64Hz	Reference frequency 73Hz	Reference frequency 85Hz	Reference frequency 102Hz
1/1 duty	64.00	73.14	85.33	102.40
1/2 duty	64.00	73.14	85.33	102.40
1/3 duty	64.25	73.31	85.33	103.04
1/4 duty	64.00	73.14	85.33	102.40
1/5 duty	64.25	73.64	86.23	102.40
1/6 duty	64.25	73.80	85.33	103.04
1/7 duty	64.13	73.14	86.69	104.03
1/8 duty	64.00	73.14	85.33	102.40
1/9 duty	86.69	98.40	113.78	140.03
1/10 duty	78.02	88.56	102.40	126.03
1/11 duty	70.93	80.51	93.09	114.57
1/12 duty	65.02	73.80	85.33	105.03
1/13 duty	78.77	90.02	105.03	126.03
1/14 duty	73.14	83.59	97.52	117.03
1/15 duty	68.27	78.02	91.02	109.23
1/16 duty	64.00	73.14	85.33	102.40
1/17 duty	77.10	87.61	101.45	120.47
1/18 duty	72.82	82.75	95.81	113.78
1/19 duty	68.99	78.39	90.77	107.79
1/20 duty	65.54	74.47	86.23	102.40
1/21 duty	74.30	86.69	97.52	120.03
1/22 duty	70.93	82.75	93.09	114.57
1/23 duty	67.84	79.15	89.04	109.59
1/24 duty	65.02	75.85	85.33	105.03

26.2.5 Display Mode Register 1 (DSPMOD1)

Address: 0F0F3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
DSPMOD1	—	—	—	—	—	DASN	DADM1	DADM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSPMOD1 is a special register (SFR) to control the display mode of the LCD drivers.
Use DSPMOD1 to select a type of display register segment map and determine to use or unuse the programmable display allocation function (display allocation RAM).

[Description of Bits]

- DADM1, DADM0 (bits 1-0)
  DADM1 and DADM0 are used to select a type of display register segment map. Two types are available; type 2, and type 3 (type 1 is not available on ML610Q421/ML610Q422/ML610421/ML610422) . See section 26.2.9 and section 26.3.2.

DADM1	DADM0	Description
0	*	Display register segment map type 2 (initial value)
1	*	Display register segment map type 3

- DASN (bit 2)
  The DASN bit is used to control the operation of the display allocation function.
  Setting the DASN bit to "1" enables the display allocation function.

DASN	Description
0	Not use Programmable display allocation (initial value)
1	Use Programmable display allocation

Note:
When using the programmable display allocation, select type 3 for the display register segment map. LAPIS semiconductor LCD Tool only generates table data can be used for the type 3.

26.2.6 Display Control Register (DSPCON)

Address: 0F0F4H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
DSPCON	—	—	—	—	—	—	LMD1	LMD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSPCON is a special function register (SFR) to control the LCD drivers.

[Description of Bits]

- **LMD1-LMD0** (bits 1, 0)
  The LMD1 and LMD0 bits are used to select an LCD display mode.
  LCD stop mode, all LCDs off mode, LCD display mode, and all LCDs on mode can be selected.
  In LCD stop mode, V_{ss} level is output to all the common drivers and segment drivers. The charge and discharge current to and from the display panel can be stopped.
  In all LCDs off mode, off waveform is output to all the segment drivers irrespective of the contents of the display registers.
  In LCD display mode, the contents of the display registers are output to each segment driver.
  In all LCDs on mode, on waveform is output to all the segment drivers irrespective of the contents of the display registers.

LMD1	LMD0	Description
0	0	LCD stop mode (initial value)
0	1	All LCDs off mode
1	0	LCD display mode
1	1	All LCDs on mode

26.2.7 Display Allocation Register A (DS0C0A to DS49C7A)

Address: 0F400H to 0F5FFH
Access: R/W
Access size: 8 bits
Initial value: Undefined

	7	6	5	4	3	2	1	0
DSmCnA	a7	a6	a5	a4	a3	a2	a1	a0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	x	x	x	x	x	x	x	x

DSmCnA (m= 0 to 49, n = 0 to 7) are special function registers (SFRs) that are used for the programmable display allocation function.
Each valid bit of DSmCnA becomes undefined at system reset.
When the programmable display allocation function is not used (DASN bit of DSPMOD1 reigster is reset to "0"), DSmCnA can be used as data memory space (512-byte RAM).
Table 26-2 shows a list of the display allocation register A.

[Description of Bits]

- **a7**-**a0** (bits 7-0)
  The a7 to a0 bits of DSmCnA (m= 0 to 49, n = 0 to 7) are used to select the lower 8 bits of the addresses of the display registers (DSPR00 to 71) that are output to common n of segment m.
  Set DSmCnA when the DASN bit of the display mode register 1 (DSPMOD1) is "0".
  When the DASN bit is "1", access from the CPU is invalid.

Table 26-2 Display Allocation Register A

Segment	Common	Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
SEG0	COM0	DS0C0A	0F400H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
SEG1	COM0	DS1C0A	0F401H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
SEG2	COM0	DS2C0A	0F402H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
SEG3	COM0	DS3C0A	0F403H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM0	DS49C0A	0F431H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
SEG0	COM1	DS0C1A	0F440H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM1	DS49C1A	0F471H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
SEG0	COM2	DS0C2A	0F480H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM2	DS49C2A	0F4B1H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
SEG0	COM3	DS0C3A	0F4C0H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM3	DS49C3A	0F4F1H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
SEG0	COM4	DS0C4A	0F500H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM4	DS49C4A	0F531H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
SEG0	COM5	DS0C5A	0F540H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM5	DS49C5A	0F571H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
SEG0	COM6	DS0C6A	0F580H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM6	DS49C6A	0F5B1H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
SEG0	COM7	DS0C7A	0F5C0H	a7	a6	a5	a4	a3	a2	a1	a0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM7	DS49C7A	0F5F1H	a7	a6	a5	a4	a3	a2	a1	a0	R/W

26.2.8 Display Allocation Register B (DS0C0B to DS49C7B)

Address: 0F600H to 0F7FFH
Access: R/W
Access size: 8 bits
Initial value: Undefined

	7	6	5	4	3	2	1	0
DSmCnB	b7	b6	b5	b4	b3	b2	b1	b0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	x	x	x	x	x	x	x	x

DSmCnB (m= 0 to 49, n = 0 to 7) are special function registers (SFRs) to store segment allocation data.
Each valid bit of DSmCnB becomes undefined at system reset.
When the programmable display allocation function is not used (DASN bit of DSPMOD1 reigster is reset to "0"), DSmCnB can be used as data memory space (512-byte RAM).
Table 26-3 shows a list of display allocation register B.

[Description of Bits]

- **b2-b0** (bits 2-0)
  The b2 to b0 bits of DSmCnB (m= 0 to 49, n = 0 to 7) are used to set the bits of the display registers (DSPR00 to 71) that are output to common n of segment m.
  Set DSmCnB when the DASN bit of the display control register 0 (DSPCON0) is "0".
  When the DASN bit is "1", access from the CPU is invalid.

b2	b1	b0	Description
0	0	0	Selects bit 0
0	0	1	Selects bit 1
0	1	0	Selects bit 2
0	1	1	Selects bit 3
1	0	0	Selects bit 4
1	0	1	Selects bit 5
1	1	0	Selects bit 6
1	1	1	Selects bit 7

Table 26-3 Display Allocation Register B

Segment	Common	Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
SEG0	COM0	DS0C0B	0F600H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
SEG1	COM0	DS1C0B	0F601H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
SEG2	COM0	DS2C0B	0F602H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
SEG3	COM0	DS3C0B	0F603H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM0	DS49C0B	0F631H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
SEG0	COM1	DS0C1B	0F640H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM1	DS49C1B	0F671H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
SEG0	COM2	DS0C2B	0F680H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM2	DS49C2B	0F6B1H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
SEG0	COM3	DS0C3B	0F6C0H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM3	DS49C3B	0F6F1H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
SEG0	COM4	DS0C4B	0F700H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM4	DS49C4B	0F731H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
SEG0	COM5	DS0C5B	0F740H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM5	DS49C5B	0F771H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
SEG0	COM6	DS0C6B	0F780H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM6	DS49C6B	0F7B1H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
SEG0	COM7	DS0C7B	0F7C0H	b7	b6	b5	b4	b3	b2	b1	b0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG49	COM7	DS49C7B	0F7F1H	b7	b6	b5	b4	b3	b2	b1	b0	R/W

26.2.9 Display Registers (DSPR00 to DSPR71)

Address: 0F100H to 0F171H
Access: R/W
Access size: 8 bits
Initial value: Undefined

	7	6	5	4	3	2	1	0
DSPRxx	c15/7	c14/6	c13/5	c12/4	c11/3	c10/2	c9/1	c8/0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	x	x	x	x	x	x	x	x

DSPRxx (xx = 00 to 71) are special function registers (SFRs) to store display data.
Each valid bit of DSPRxx becomes undefined at system reset.
The display registers that are not used for LCD display can be used for data memories.
Set data in DSPRxx before setting LCD display mode.
Tables 26-4 to 26-6 list display registers segment map type 2 to type 3 respectively. The type can be selected by the DADM1 and DADM0 bits of the display mode register 1 (DSPMOD1).

[Description of Bits]

- **c15-c0** (bits 7-0)
  The c15 to c0 bits are used to set display data.

C15 to c0	Description
0	off waveform
1	on waveform

Table 26-4 Segment Map Type 2 of Display Registers (1/2)

Register name	Address	Corresponding segment	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
DSPR00	0F100H	SEG0	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR01	0F101H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR02	0F102H	SEG1	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR03	0F103H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR04	0F104H	SEG2	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR05	0F105H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR06	0F106H	SEG3	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR07	0F107H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR08	0F108H	SEG4	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR09	0F109H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR0A	0F10AH	SEG5	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0B	0F10BH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR0C	0F10CH	SEG6	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0D	0F10DH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR0E	0F10EH	SEG7	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0F	0F10FH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR10	0F110H	SEG8	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR11	0F111H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR12	0F112H	SEG9	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR13	0F113H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR14	0F114H	SEG10	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR15	0F115H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR16	0F116H	SEG11	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR17	0F117H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR18	0F118H	SEG12	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR19	0F119H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR1A	0F11AH	SEG13	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR1B	0F11BH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR1C	0F11CH	SEG14	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR1D	0F11DH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR1E	0F11EH	SEG15	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR1F	0F11FH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR20	0F120H	SEG16	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR21	0F121H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR22	0F122H	SEG17	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR23	0F123H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR24	0F124H	SEG18	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR25	0F125H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR26	0F126H	SEG19	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR27	0F127H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR28	0F128H	SEG20	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR29	0F129H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR2A	0F12AH	SEG21	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR2B	0F12BH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR2C	0F12CH	SEG22	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR2D	0F12DH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR2E	0F12EH	SEG23	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR2F	0F12FH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR30	0F130H	SEG24	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR31	0F131H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR32	0F132H	SEG25	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR33	0F133H		c15	c14	c13	c12	c11	c10	c9	c8	R/W

Table 26-4 Segment Map Type 2 of Display Registers (2/2)

Register name	Address	Corresponding segment	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
DSPR34	0F134H	SEG26	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR35	0F135H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR36	0F136H	SEG27	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR37	0F137H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR38	0F138H	SEG28	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR39	0F139H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR3A	0F13AH	SEG29	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR3B	0F13BH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR3C	0F13CH	SEG30	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR3D	0F13DH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR3E	0F13EH	SEG31	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR3F	0F13FH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR40	0F140H	SEG32	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR41	0F141H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR42	0F142H	SEG33	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR43	0F143H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR44	0F144H	SEG34	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR45	0F145H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR46	0F146H	SEG35	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR47	0F147H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR48	0F148H	SEG36	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR49	0F149H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR4A	0F14AH	SEG37	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR4B	0F14BH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR4C	0F14CH	SEG38	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR4D	0F14DH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR4E	0F14EH	SEG39	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR4F	0F14FH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR50	0F150H	SEG40	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR51	0F151H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR52	0F152H	SEG41	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR53	0F153H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR54	0F154H	SEG42	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR55	0F155H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR56	0F156H	SEG43	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR57	0F157H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR58	0F158H	SEG44	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR59	0F159H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR5A	0F15AH	SEG45	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR5B	0F15BH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR5C	0F15CH	SEG46	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR5D	0F15DH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR5E	0F15EH	SEG47	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR5F	0F15FH		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR60	0F160H	SEG48	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR61	0F161H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR62	0F162H	SEG49	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR63	0F163H		c15	c14	c13	c12	c11	c10	c9	c8	R/W
Not used	0F164H ~ 0F171H	—	—	—	—	—	—	—	—	—	—

Table 26-5 Segment Map Type 3 of Display Registers (1/2)

Register name	Address	Corresponding segment	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
DSPR00	0F100H	SEG0	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR01	0F101H	SEG1	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR02	0F102H	SEG2	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR03	0F103H	SEG3	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR04	0F104H	SEG4	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR05	0F105H	SEG5	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR06	0F106H	SEG6	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR07	0F107H	SEG7	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR08	0F108H	SEG8	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR09	0F109H	SEG9	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0A	0F10AH	SEG10	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0B	0F10BH	SEG11	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0C	0F10CH	SEG12	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0D	0F10DH	SEG13	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0E	0F10EH	SEG14	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0F	0F10FH	SEG15	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR10	0F110H	SEG16	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR11	0F111H	SEG17	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR12	0F112H	SEG18	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR13	0F113H	SEG19	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR14	0F114H	SEG20	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR15	0F115H	SEG21	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR16	0F116H	SEG22	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR17	0F117H	SEG23	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR18	0F118H	SEG24	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR19	0F119H	SEG25	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR1A	0F11AH	SEG26	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR1B	0F11BH	SEG27	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR1C	0F11CH	SEG28	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR1D	0F11DH	SEG29	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR1E	0F11EH	SEG30	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR1F	0F11FH	SEG31	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR20	0F120H	SEG32	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR21	0F121H	SEG33	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR22	0F122H	SEG34	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR23	0F123H	SEG35	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR24	0F124H	SEG36	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR25	0F125H	SEG37	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR26	0F126H	SEG38	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR27	0F127H	SEG39	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR28	0F128H	SEG40	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR29	0F129H	SEG41	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR2A	0F12AH	SEG42	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR2B	0F12BH	SEG43	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR2C	0F12CH	SEG44	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR2D	0F12DH	SEG45	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR2E	0F12EH	SEG46	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR2F	0F12FH	SEG47	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR30	0F130H	SEG48	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR31	0F131H	SEG49	c7	c6	c5	c4	c3	c2	c1	c0	R/W
Not used	0F132H ~ 0F13FH	—	—	—	—	—	—	—	—	—	—

Table 26-5 Segment Map Type 3 of Display Registers (2/2)

Register name	Address	Corresponding segment	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
DSPR40	0F140H	SEG0	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR41	0F141H	SEG1	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR42	0F142H	SEG2	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR43	0F143H	SEG3	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR44	0F144H	SEG4	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR45	0F145H	SEG5	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR46	0F146H	SEG6	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR47	0F147H	SEG7	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR48	0F148H	SEG8	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR49	0F149H	SEG9	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR4A	0F14AH	SEG10	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR4B	0F14BH	SEG11	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR4C	0F14CH	SEG12	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR4D	0F14DH	SEG13	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR4E	0F14EH	SEG14	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR4F	0F14FH	SEG15	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR50	0F150H	SEG16	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR51	0F151H	SEG17	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR52	0F152H	SEG18	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR53	0F153H	SEG19	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR54	0F154H	SEG20	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR55	0F155H	SEG21	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR56	0F156H	SEG22	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR57	0F157H	SEG23	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR58	0F158H	SEG24	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR59	0F159H	SEG25	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR5A	0F15AH	SEG26	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR5B	0F15BH	SEG27	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR5C	0F15CH	SEG28	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR5D	0F15DH	SEG29	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR5E	0F15EH	SEG30	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR5F	0F15FH	SEG31	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR60	0F160H	SEG32	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR61	0F161H	SEG33	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR62	0F162H	SEG34	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR63	0F163H	SEG35	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR64	0F164H	SEG36	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR65	0F165H	SEG37	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR66	0F166H	SEG38	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR67	0F167H	SEG39	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR68	0F168H	SEG40	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR69	0F169H	SEG41	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR6A	0F16AH	SEG42	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR6B	0F16BH	SEG43	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR6C	0F16CH	SEG44	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR6D	0F16DH	SEG45	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR6E	0F16EH	SEG46	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR6F	0F16FH	SEG47	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR70	0F170H	SEG48	c15	c14	c13	c12	c11	c10	c9	c8	R/W
DSPR71	0F171H	SEG49	c15	c14	c13	c12	c11	c10	c9	c8	R/W

26.3 Description of Operation

26.3.1 Operation of LCD Drivers and Bias Generation Circuit

Figure 26-6 shows the operation of the LCD drivers and the bias generation circuit.

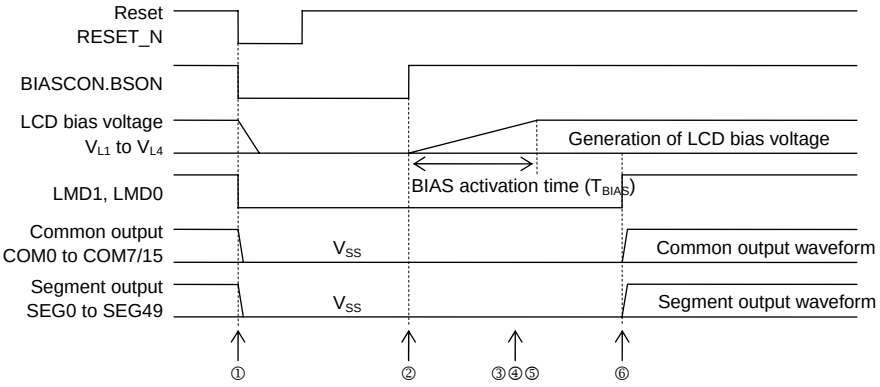
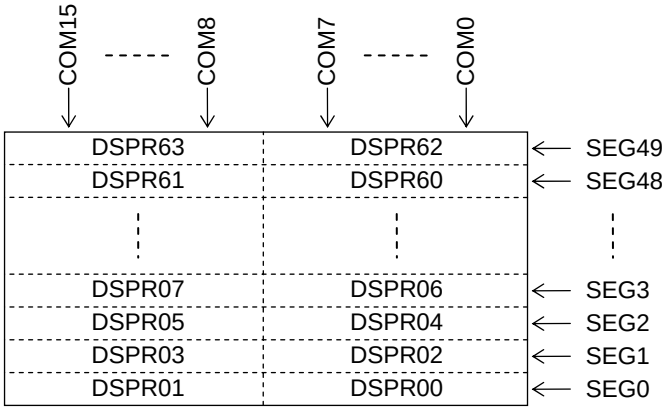


Figure 26-6 Operation of LCD Drivers and Bias Generation Circuit

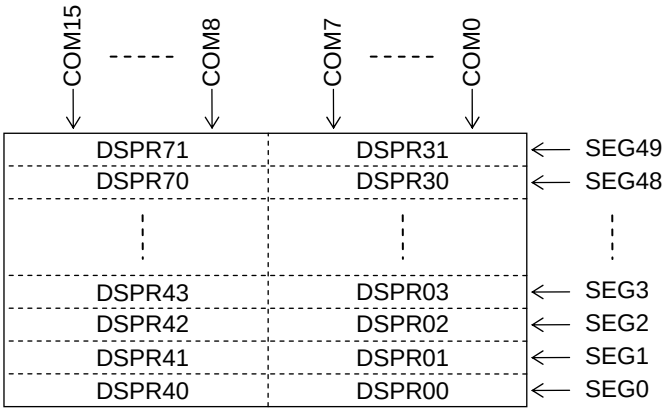
① System reset causes the bias generation circuit and the LCD drivers to stop operation and Vss level to be output to each of the common and segment pins.
② By using the bias circuit control register (BIASCON), select 1/3 bias or 1/4 bias and lock of bias voltage multiplying, and set the bias generation circuit to on (BSON = "1").
③ When the programmable display allocation function is used, set LCD allocation data in the display allocation registers A and B (DS0C0A to DS49C7A and DS0C0B to DS49C7B).
④ Set a frame frequency and a duty by using the display mode register 0 (DSPMOD0). When using the programmable display allocation function, set the DASN bit of DSPMOD1 register to "1" and set DADM1 bit to "1" to select type 3 for the display register segment map. When not using the programmable display allocation function, set the DASN bit to "0" and select a type of segment map for display registers.
⑤ Set display data in the display registers (DSPR00 to DSPR71).
⑥ After elapse of the bias activation time (T_{BIAS}) or longer, set the mode to display mode by using the LMD1 and LMD0 bits of the display control register (DSPCON). (Display waveform is output to each segment pin.)
For the bias activation time (T_{BIAS}), see the "Electrical Characteristics" Section in Appendix C.

26.3.2 Segment Mapping When the Programmable Display Allocation Function is Not Used

When not using the programmable display function (DASN bit of DSPMOD1 register is "0"), three types of segment map are available for the display registers (DSPR00 to 71), selected by the DADM1 bit and DADM0 bit.



(1) Type 2: Recommended for when using COM9 to COM15 (1/9 to 1/16 duty)



(2) Type 3: Recommended for when using COM0 to COM7 (1/1 to 1/8 duty)

Figure 26-7 Configurations of Display register segment map types

Note:
When the programmable display function is not used (DASN = "0"), display allocation register A (0F400H to 0F5FFH) and display allocation register B (0F600H to 0F7FFH) can be used as 1K-byte data memory(RAM).

26.3.3 Segment Mapping When the Programmable Display Allocation Function is Used

When the programmable display allocation function is used (DASN bit of DSPMOD1 register is "1"), display registers (DSPR00 to 71) segment mapping can be set in bit units according to the contents of display allocation registers A and B (DSmCnA, DSmCnB: m = 0 to 49, n = 0 to 7).
Table 26-7 shows the frame frequencies and the duty conditions that allow the use of the programmable allocation function.

Table 26-6 Conditions That Allow the Use of Programmable Allocation Function

Frame frequency	Duty that allows the use of duty
Approx. 64 Hz	1/1 to 1/8 Duty
Approx. 73 Hz	1/1 to 1/8 Duty
Approx. 85 Hz	1/1 to 1/7 Duty
Approx. 102 Hz	1/1 to 1/6 Duty

Note:
- When the duty is other than those indicated in Table 26-6, the programmable allocation function can not be used regardless of the content of the DASN bit of DSPMOD1. The programmable display allocation function is available only when 1/1~1/8 duty is selected (when using eight COMs or less for display), it does not work when 1/9~1/16 duty is selected (when using nine COMs or more for display).
- Select type 3 for the display register segment map (Set DADM1 bit of DSPMOD1 register to "1") when using the programmable allocation function.

Figure 26-8 shows the configuration when using the programmable display allocation function.

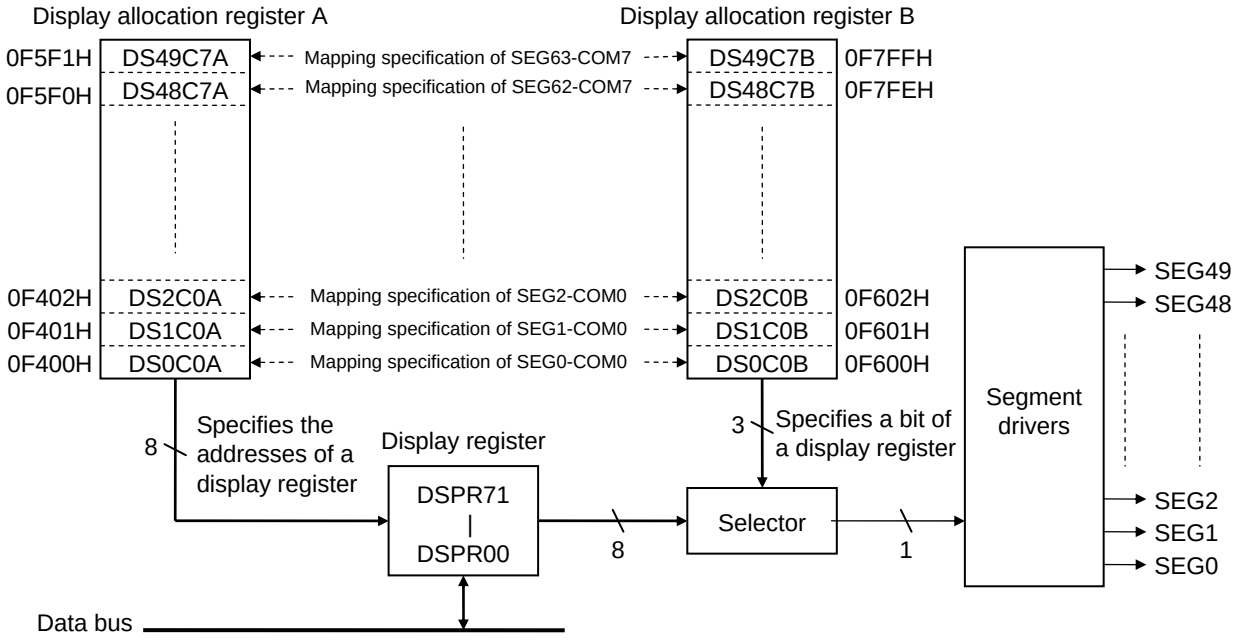
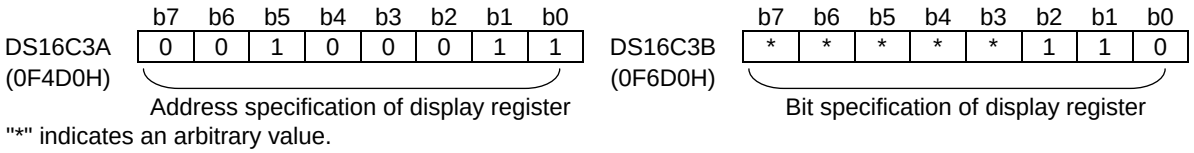


Figure 26-8 Configuration When Using the Programmable Display Allocation Function

In display allocation register A (DSmCnA: m = 0 to 49, n = 0 to 8), set the lower 8 bits (00H to 71H) of the addresses of the display registers (DSPR00 to DSPR71) that are output to common n of segment n. In display allocation register B (DSmCnB: m = 0 to 49, n = 0 to 8), set the bits of the display registers (DSPR00 to DSPR71) that are output to common n of segment m.
For instance, to display bit 6 of display register 23 to common 3 of segment 16, set as follows.



"*" indicates an arbitrary value.

Note:
- Set display allocation data to display allocation registers A and B when the DASN bit of display control register 0 (DSPMOD1) is "0". When the DASN bit is "1", access from the CPU is invalid.
- Select type 3 for the display register segment map (Set DADM1 bit of DSPMOD1 register to "1") when using the programmable allocation function.

26.3.4 Common Output Waveforms

Figure 26-9 shows the common output waveforms for 1/8 duty and 1/3 bias and for 1/16 duty and 1/4 bias.

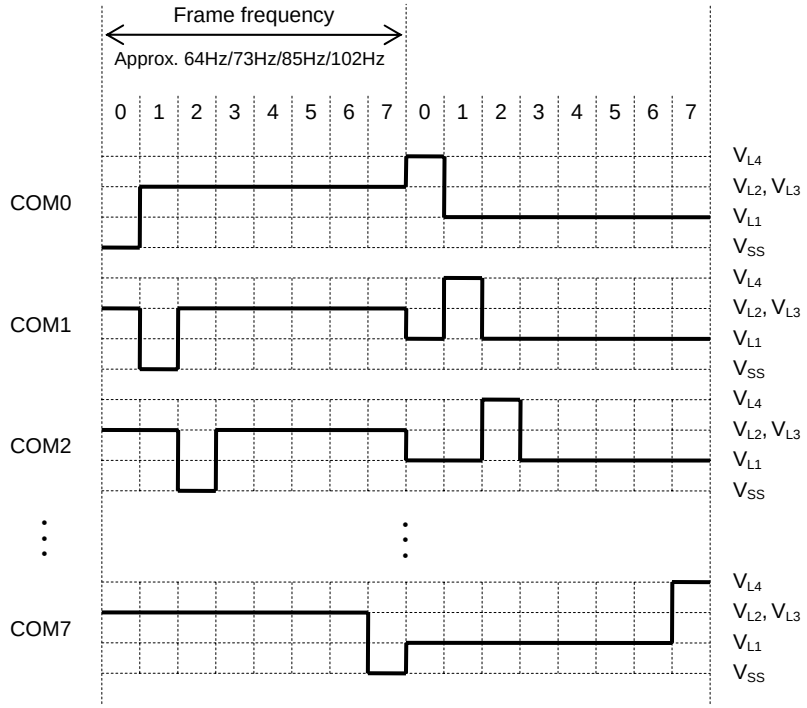


Figure 26-9 (1) Common Output Waveforms for 1/8 Duty and 1/3 Bias

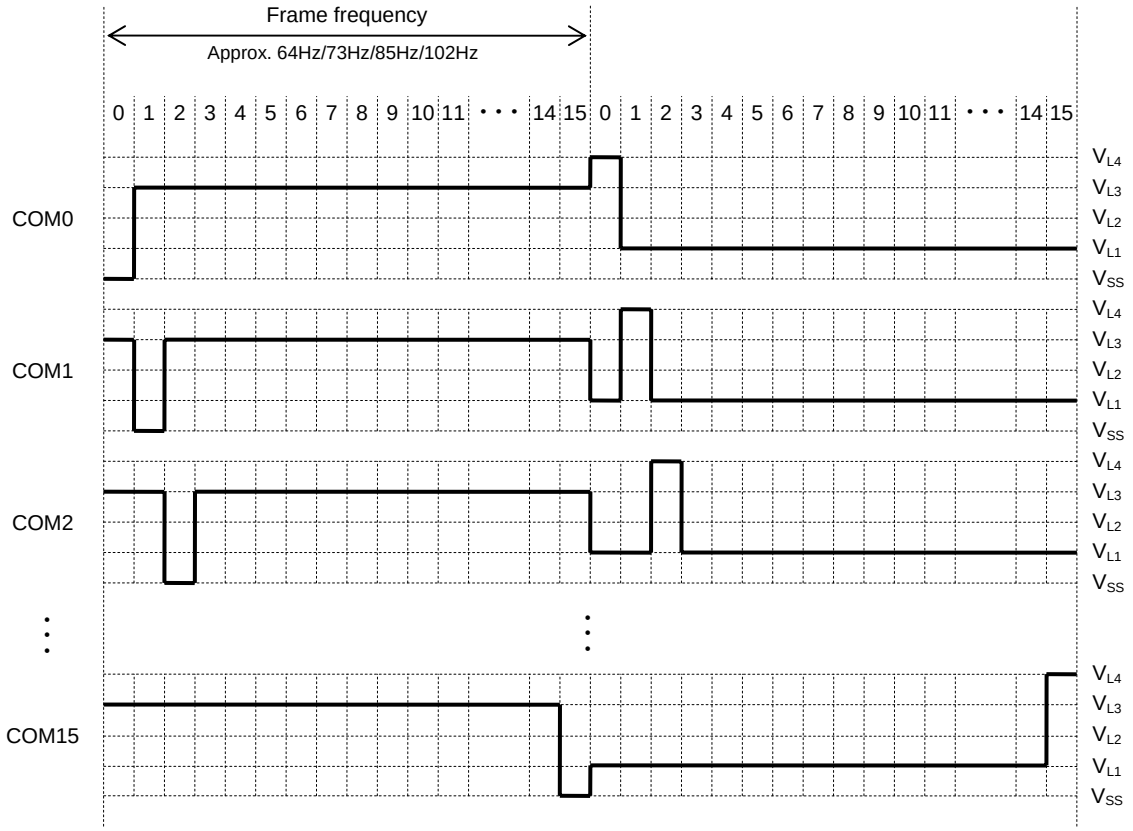


Figure 26-9 (2) Common Output Waveforms for 1/16 Duty and 1/4 Bias

26.3.5 Segment Output Waveforms

Figure 26-10 shows the segment output waveforms for 1/8 duty and 1/3 bias and for 1/16 duty and 1/4 bias.

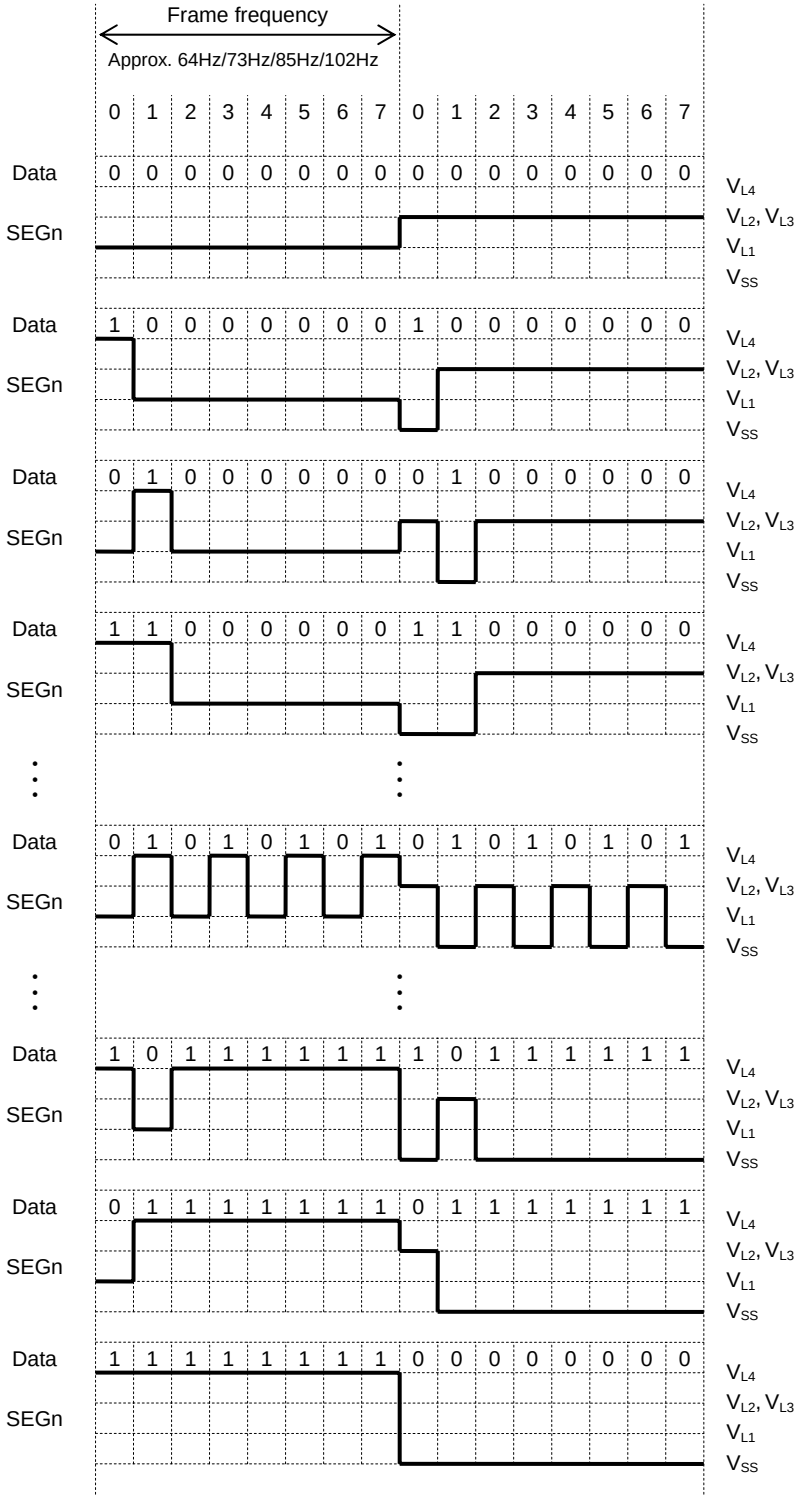


Figure 26-10 (1) Segment Output Waveforms for 1/8 Duty and 1/3 Bias

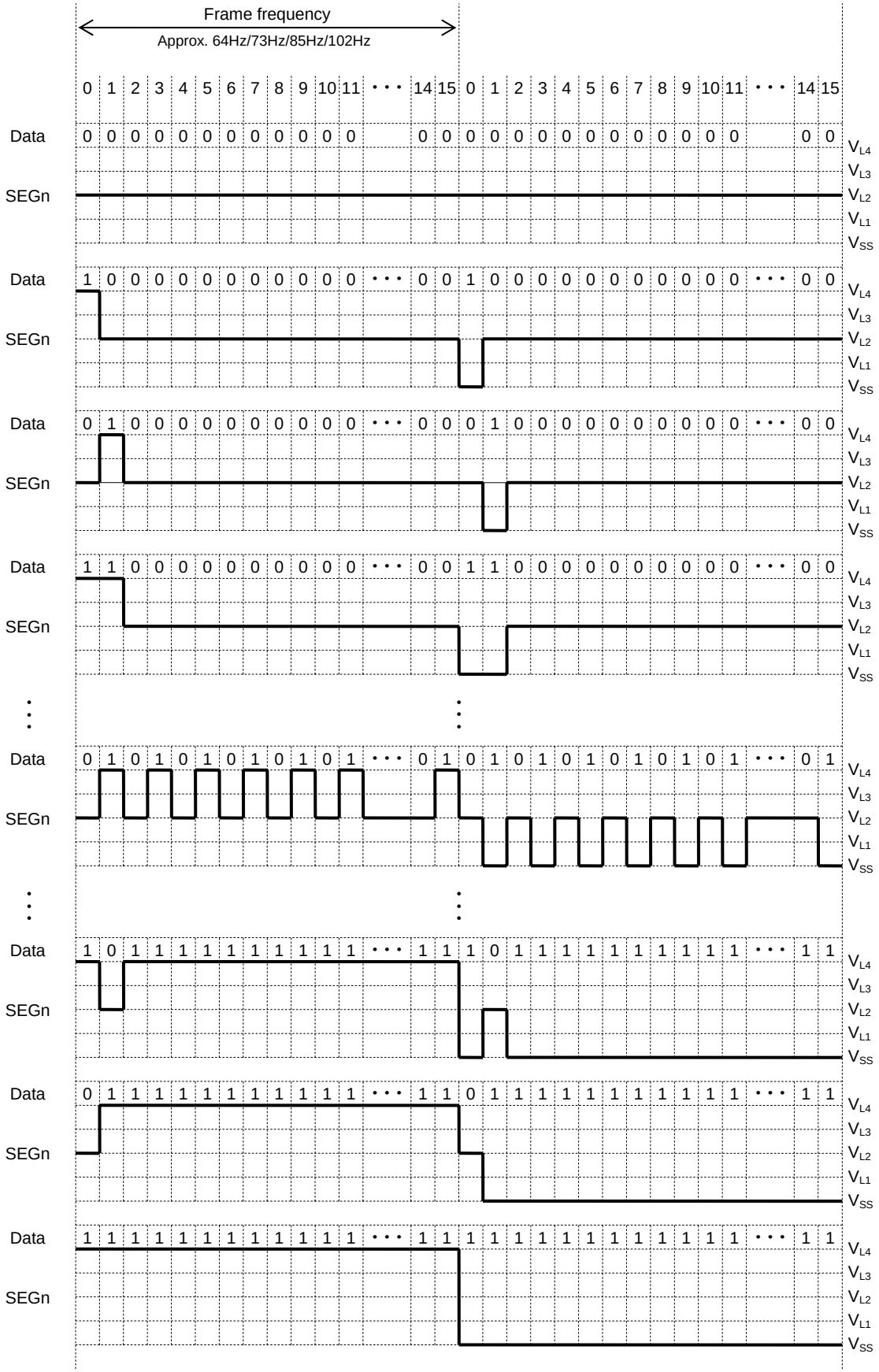


Figure 26-10 (2) Segment Output Waveforms for 1/16 Duty and 1/4 Bias

Chapter 27

Battery Level Detector

27. Battery Level Detector

27.1 Overview

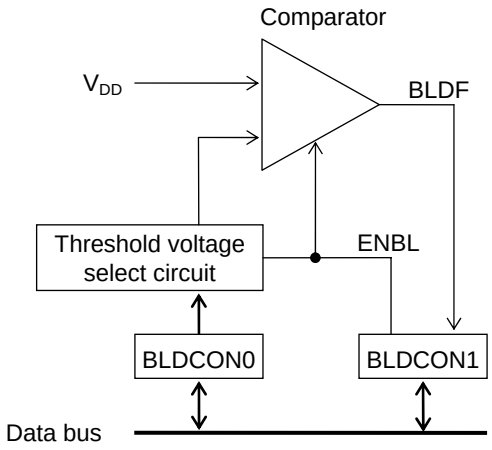
This LSI includes a Battery Level Detector (BLD).
16 levels of threshold voltages can be selected by setting Battery Level Detector control register 0 (BLDCON0).

27.1.1 Features

- Threshold voltages: One out of the 16 levels can be selected
- Accuracy: ±2% (Typ.)
- Temperature deviation: ±0.1%/°C

27.1.2 Configuration

BLD consists of the comparator and threshold voltage select circuits.
Figure 27-1 shows the configuration of the Battery Level Detector.



BLDCON0 : Battery Level Detector control register 0
BLDCON1 : Battery Level Detector control register 1

Figure 27-1 Configuration of Battery Level Detector

27.2 Description of Registers

27.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F0D0H	Battery Level Detector control register 0	BLDCON0	BLDCON	R/W	8/16	00H
0F0D1H	Battery Level Detector control register 1	BLDCON1		R/W	8	00H

27.2.2 Battery Level Detector Control Register 0 (BLDCON0)

Address: 0F0D0H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLDCON0	—	—	—	—	LD3	LD2	LD1	LD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLDCON0 is a special function register (SFR) to control the Battery Level Detector

[Description of Bits]

- **LD3, LD2, LD1, LD0** (bits 3-0)
  The LD3, LD2, LD1, and LD0 bits are used to select a threshold voltage (VCMP) of the Battery Level Detector. 16 levels of threshold voltages can be selected.

LD3	LD2	LD1	LD0	Description
0	0	0	0	1.35 V ±2% (initial value)
0	0	0	1	1.40 V ±2%
0	0	1	0	1.45 V ±2%
0	0	1	1	1.50 V ±2%
0	1	0	0	1.60 V ±2%
0	1	0	1	1.70 V ±2%
0	1	1	0	1.80 V ±2%
0	1	1	1	1.90 V ±2%
1	0	0	0	2.00 V ±2%
1	0	0	1	2.10 V ±2%
1	0	1	0	2.20 V ±2%
1	0	1	1	2.30 V ±2%
1	1	0	0	2.40 V ±2%
1	1	0	1	2.50 V ±2%
1	1	1	0	2.70 V ±2%
1	1	1	1	2.90 V ±2%

27.2.3 Battery Level Detector Control Register 1 (BLDCON1)

Address: 0F0D1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLDCON1	—	—	—	—	—	—	BLDF	ENBL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0

BLDCON1 is a special function register (SFR) to control the Battery Level Detector.

[Description of Bits]

- **ENBL** (bit 0)

The ENBL bit is used to control activation (ON) or deactivation (OFF) of the Battery Level Detector.
The Battery Level Detector is activated (ON) and deactivated (OFF) by setting the ENBL bit to "1" and "0", respectively.

ENBL	Description
0	Deactivates the Battery Level Detector (OFF) (initial value)
1	Activates the Battery Level Detector (ON).

- **BLDF** (bit 1)

The BLDF bit is the judgment result flag of the Battery Level Detector.
The BLDF bit is set to "1" or "0" when the power supply voltage (VDD) is lower than or higher than the threshold voltage selected by LD3 to LD0 bits of BLDCON0 register, respectively.

BLDF	Description
0	Higher than the threshold voltage (initial value)
1	Lower than the threshold voltage

27.3 Description of Operation

27.3.1 Threshold Voltage

The threshold voltage (VCMP) is selected by setting the bits of BLDCON0.
Table 27-1 shows the threshold voltages and the accuracy.

Table 27-1 Threshold Voltages and Accuracy

BLDCON0				Threshold voltage	Accuracy	Temperature
LD3	LD2	LD1	LD0	V_{CMP}	Ta = 25°C	deviation
0	0	0	0	1.35 V	±2.0%	±0.1%/°C
0	0	0	1	1.40 V		
0	0	1	0	1.45 V		
0	0	1	1	1.50 V		
0	1	0	0	1.60 V		
0	1	0	1	1.70 V		
0	1	1	0	1.80 V		
0	1	1	1	1.90 V		
1	0	0	0	2.00 V		
1	0	0	1	2.10 V		
1	0	1	0	2.20 V		
1	0	1	1	2.30 V		
1	1	0	0	2.40 V		
1	1	0	1	2.50 V		
1	1	1	0	2.70 V		
1	1	1	1	2.90 V		

27.3.2 Operation of Battery Level Detector

Activation (ON) and deactivation (OFF) of the Battery Level Detector are controlled by setting the ENBL bit of the Battery Level Detector control register (BLDCON1), and the result of the comparison of the power supply voltage (VDD) to the threshold voltage is output to the BLDF bit of BLDCON1.
When ENBL, the enable control bit of the Battery Level Detector, is set to "1", the detector is activated (ON). When ENBL is set to "0", the detector is deactivated (OFF) and has no supply current.
BLDF indicates the result of comparison. When BLDF bit is set to "1", it indicates the power supply voltage is lower than the threshold voltage. When BLDF bit is set to "0", it indicates the power supply voltage (VDD) is higher than the threshold voltage. The Battery Level Detector requires a settling time. Read BLDF bit 1ms or more after ENBL bit is set to "1".
Figure 27-2 shows an example of the operation timing diagram.

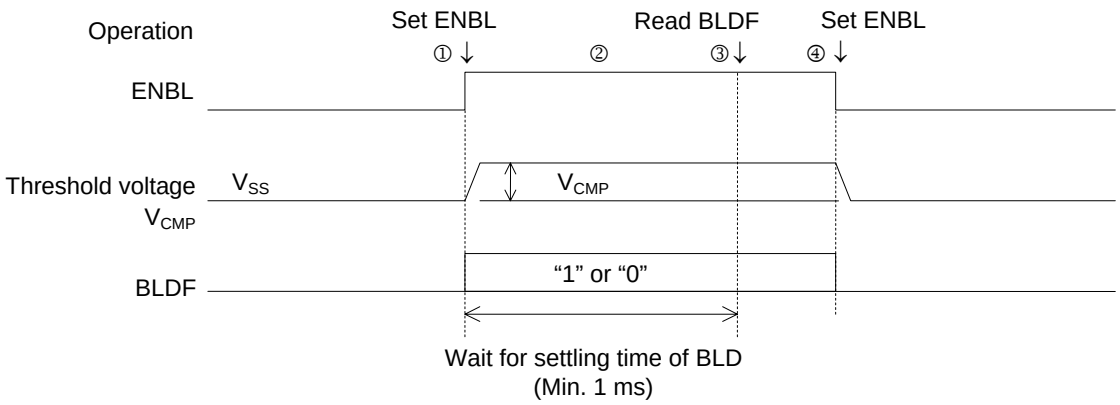


Figure 27-2 Example of Operation Timing Diagram

The operations in Figure 27-2 are described below.

① The Battery Level Detector is activated (ON) by setting the ENBL bit to "1".
② Wait the settling time (min. 1 ms) of the Battery Level Detector.
③ Read BLDF bit.
④ Set ENBL bit to "0".

Note:
Select the threshold voltage (VCMP) when the ENBL bit is "0".

Chapter 28

Power Supply Circuit

28. Power Supply Circuit

28.1 Overview

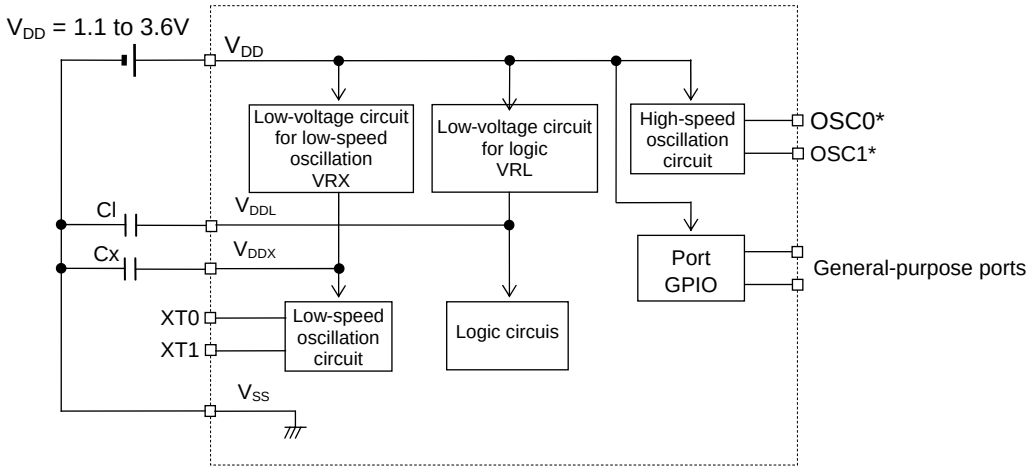
This LSI includes a regulated power supply for the internal logic (VRL) and a regulated power supply for low-speed oscillation (VRX).
The VRL outputs the operating voltage, V_{DDL}, of the internal logic, program memory, RAM, etc.
The VRX outputs the operating voltage, V_{DDX}, for low-speed oscillation.
For the circuit configuration of the power supplies (AVDD, AVSS) for the analog circuits, see Chapter 25, "Successive Approximation Type A/D converter".
For the circuit configuration of the power supplies for LCD (VL1 to VL4), see Chapter 26, "LCD Driver".

28.1.1 Features

- VRL outputs the operating voltage, V_{DDL}, of the internal logic, program memory, RAM, etc.
- VRX outputs the operating voltage, V_{DDX}, for low-speed oscillation.

28.1.2 Configuration

Figure 28-1 shows the configuration of the power supply circuit.



*: Shows the secondary function of the port.

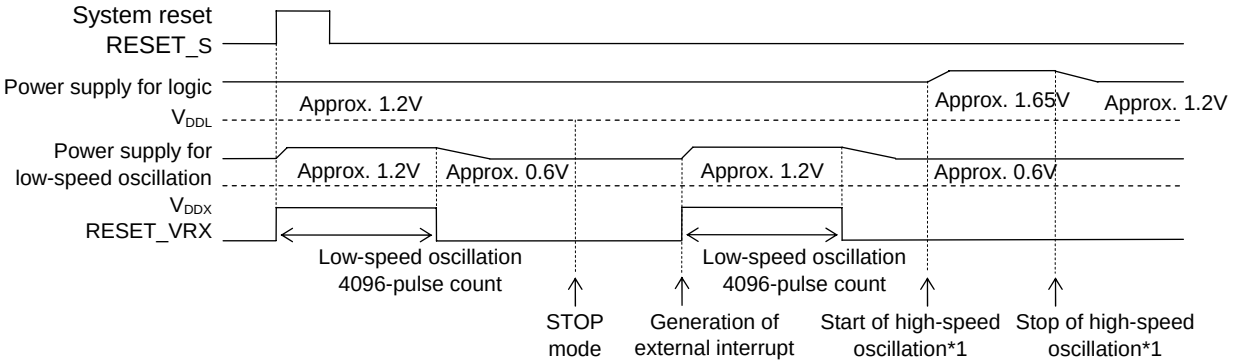
Figure 28-1 Configuration of Power Supply Circuit

28.1.3 List of Pins

Pin name	I/O	Description
V_{DDL}	—	Positive power supply pin for the internal logic circuits
V_{DDX}	—	Positive power supply pin for low-speed oscillation

28.2 Description of Operation

V_{DDL} and V_{DDX} become approx. 1.2 V at a system reset.
V_{DDL} becomes approx. 1.65 V (Typ.) when high-speed oscillation starts in crystal/ceramic oscillation mode or PLL oscillation mode or external clock mode. When high-speed oscillation stops, the voltage becomes about 1.2V (Typ.).
V_{DDX} becomes approx. 0.6 V (Typ.) after 4096 low-speed oscillation clock (XTCLK) pulses are counted after the system reset is released. As a result of release of STOP mode (generation of external interrupt), V_{DDX} becomes approx. 1.2 V(Typ.) and then approx. 0.6 V (Typ.) after 4096 low-speed oscillation clock (XTCLK) pulses are counted.
Figure 28-2 shows the operation waveforms of the power supply circuit.



*1: Crystal/ceramic oscillation, PLL oscillation, External clock input mode (500 kHz CR oscillation not included)

Figure 28-2 Operation Waveforms of Power Supply Circuit

Chapter 29

On-Chip Debug Function

29. On-Chip Debug Function

29.1 Overview

ML610Q421/ML610Q422 has an on-chip debug function allowing Flash memory rewriting.
The on-chip debug emulator (uEASE) is connected to ML610Q421/ML610Q422 to perform the on-chip debug function.

29.2 Method of Connecting to On-Chip Debug Emulator

Figure 29-1 shows connection to the on-chip debug emulator (uEASE).
For on-chip debug emulator, see "uEASE User's Manual".

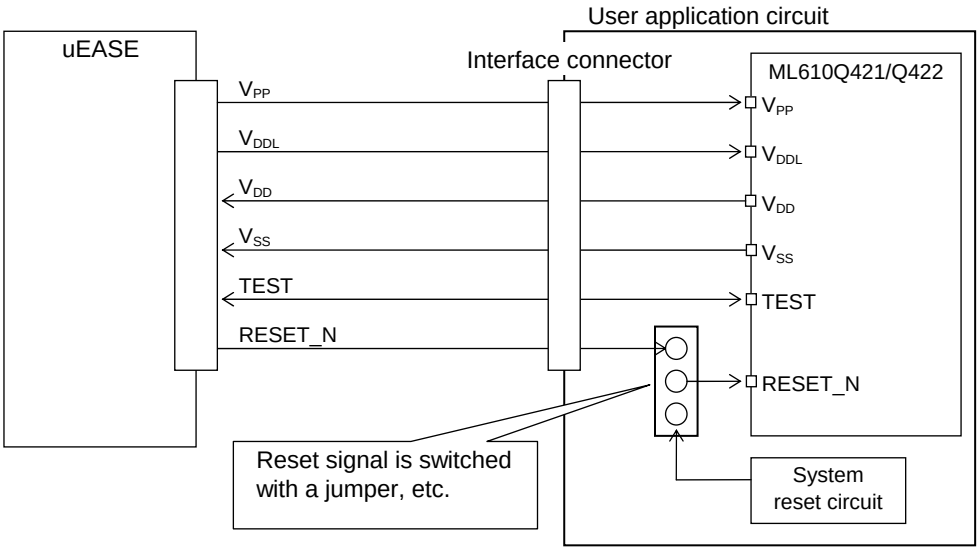


Figure 29-1 Connection to On-chip Debug Emulator (uEASE)

Note:
– Please do not apply LSIs used for debugging to mass production.
– When using the on-chip debug function or the flash rewrite function after mounting of the board, design the board so that the 6 pins (V_{PP}, V_{DD}, V_{DDL}, V_{SS}, RESET_N, and TEST) required for connection to the on-chip debug emulator can be connected.
– "3.0V to 3.6V" has to be supplied to VDD while debugging and writing flash.
– When the system reset circuit is included in the user application circuit, enable switching of the connection in the user application circuit, as shown above. When the system reset circuit is not included in the user application circuit, the RESET_N pin can be connected directy to the RESET_N pin of this LSI.

For details, see "uEASE User's Manual" and "uEASE Target Connection Manual".

29.3 Flash Memory Rewrite Function

Flash memory erase/write can be performed with the the memory mounted on board by using the commands from the on-chip debug emulator (uEASE). For more details on the on-chip debug emulator, see "uEASE User's Manual". Table 29-2 shows the Flash memory rewrite functions.

Table 29-2 Flash Memory Rewrite Functions

Function	Outline
Chip erase	Erase of 16 Kwords (overall area)
Block erase	Erase of 8 Kwords (16 Kbytes)
1-word write	Write of 1 word (2 bytes)
Random read	Read of input address

Table 29-3 shows the conditions and specifications of Flash memory rewrite.

Table 29-3 Specifications of Flash Memory Rewrite

Parameter		Specifications
Rewrite count		80
Operating temperature		0°C to 40°C
Operating voltage	V_{PP}	8 V (Typ.) (Supplied from uEASE)
	V_{DD}	3.0V to 3.6 V
	V_{DDL}	2.7 V (Typ.) (Supplied from uEASE)
Chip-erase time		77 ms (Typ.), 100 ms (Max.)
Block-erase time		77 ms (Typ.), 100 ms (Max.)
1-word (16 bits) write		41 μs (Typ.), 64 μs (Max.)
Overall-word (16K × 16 bits) write		Approx. 0.68s (Typ.), Approx. 1.05s (Max.)

Note:
When performing Flash memory rewrite (erase, write), a voltage within the range from 3.0V to 3.6 V needs to be applied to the power supply voltage V_{DD}.

Appendixes

Appendix A Registers

Contents of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F000H	Data segment register	DSR	—	R/W	8	00H
0F001H	Reset status register	RSTAT	—	R/W	8	Undefined
0F002H	Frequency control register 0	FCON0	FCON	R/W	8/16	33H
0F003H	Frequency control register 1	FCON1		R/W	8	03H
0F008H	Stop code acceptor	STPACP	—	W	8	Undefined
0F009H	Standby control register	SBYCON	—	W	8	00H
0F00AH	Low-speed time base counter divide register	LTBR	—	R/W	8	00H
0F00BH	High-speed time base counter divide register	HTBDR	—	R/W	8	00H
0F00CH	Low-speed time base counter frequency adjustment register L	LTBADJL	LTBADJ	R/W	8/16	00H
0F00DH	Low-speed time base counter frequency adjustment register H	LTBADJH		R/W	8	00H
0F00EH	Watchdog timer control register	WDTCON	—	R/W	8	00H
0F00FH	Watchdog timer mode register	WDTMOD	—	R/W	8	02H
0F011H	Inperrupt permit register 1	IE1	—	R/W	8	00H
0F012H	Inperrupt permit register 2	IE2	—	R/W	8	00H
0F013H	Inperrupt permit register 3	IE3	—	R/W	8	00H
0F014H	Inperrupt permit register 4	IE4	—	R/W	8	00H
0F015H	Inperrupt permit register 5	IE5	—	R/W	8	00H
0F016H	Inperrupt permit register 6	IE6	—	R/W	8	00H
0F017H	Inperrupt permit register 7	IE7	—	R/W	8	00H
0F018H	Inperrupt request register 0	IRQ0	—	R/W	8	00H
0F019H	Inperrupt request register 1	IRQ1	—	R/W	8	00H
0F01AH	Inperrupt request register 2	IRQ2	—	R/W	8	00H
0F01BH	Inperrupt request register 3	IRQ3	—	R/W	8	00H
0F01CH	Inperrupt request register 4	IRQ4	—	R/W	8	00H
0F01DH	Inperrupt request register 5	IRQ5	—	R/W	8	00H
0F01EH	Inperrupt request register 6	IRQ6	—	R/W	8	00H
0F01FH	Inperrupt request register 7	IRQ7	—	R/W	8	00H
0F020H	External interrupt control register 0	EXICON0	—	R/W	8	00H
0F021H	External interrupt control register 1	EXICON1	—	R/W	8	00H
0F022H	External interrupt control register 2	EXICON2	—	R/W	8	00H
0F028H	Block control register 0	BLKCON0	—	R/W	8	00H
0F029H	Block control register 1	BLKCON1	—	R/W	8	00H
0F02AH	Block control register 2	BLKCON2	—	R/W	8	00H
0F02BH	Block control register 3	BLKCON3	—	R/W	8	00H
0F02CH	Block control register 4	BLKCON4	—	R/W	8	00H
0F030H	Timer 0 data register	TM0D	TM0DC	R/W	8/16	0FFH
0F031H	Timer 0 counter register	TM0C		R/W	8	00H
0F032H	Timer 0 control register 0	TM0CON0	TM0CON	R/W	8/16	00H
0F033H	Timer 0 control register 1	TM0CON1		R/W	8	00H
0F034H	Timer 1 data register	TM1D	TM1DC	R/W	8/16	0FFH
0F035H	Timer 1 counter register	TM1C		R/W	8	00H
0F036H	Timer 1 control register 0	TM1CON0	TM1CON	R/W	8/16	00H
0F037H	Timer 1 control register 1	TM1CON1		R/W	8	00H
0F038H	Timer 2 data register	TM2D	TM2DC	R/W	8/16	0FFH

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F039H	Timer 2 counter register	TM2C		R/W	8	00H
0F03AH	Timer control register 0	TM2CON0	TM2CON	R/W	8/16	0A0H
0F03BH	Timer 2 control register 1	TM2CON1		R/W	8	00H
0F03CH	Timer 3 data register	TM3D	TM3DC	R/W	8/16	0FFH
0F03DH	Timer 3 counter register	TM3C		R/W	8	00H
0F03EH	Timer 3 control register 0	TM3CON0	TM3CON	R/W	8/16	00H
0F03FH	Timer 3 control register 1	TM3CON1		R/W	8	00H
0F080H	1kHz timer count register L	T1KCRL	T1KCR	R/W	8/16	00H
0F081H	1kHz timer count register H	T1KCRH		R/W	8	00H
0F082H	1kHz timer control register	T1KCON	—	R/W	8	00H
0F090H	Capture control register	CAPCON	—	R/W	8	00H
0F091H	Capture status register	CAPSTAT	—	R/W	8	00H
0F092H	Capture data register 0	CAPR0	—	R	8	00H
0F093H	Capture data register 1	CAPR1	—	R	8	00H
0F0A0H	PWM0 period register L	PW0PL	PW0P	R/W	8/16	0FFH
0F0A1H	PWM00 period register H	PW0PH		R/W	8	0FFH
0F0A2H	PWM0 duty register L	PW0DL	PW0D	R/W	8/16	00H
0F0A3H	PWM0 duty register H	PW0DH		R/W	8	00H
0F0A4H	PWM0 dounter register L	PW0CL	PW0C	R/W	8/16	00H
0F0A5H	PWM0 dounter register H	PW0CH		R/W	8	00H
0F0A6H	PWM0 control register 0	PW0CON0	PW0CON	R/W	8/16	00H
0F0A7H	PWM0 control register 1	PW0CON1		R/W	8	40H
0F0D0H	Battery Level Detector control register 0	BLDCON0	BLDCON	R/W	8/16	00H
0F0D1H	Battery Level Detector control register 1	BLDCON1		R/W	8	00H
0F0F0H	Bias circuit control register	BIASCON	—	R/W	8	08H
0F0F1H	Display contrast register	DSPCNT	—	R/W	8	00H
0F0F2H	Display mode register 0	DSPMOD0	DSPMOD	R/W	8/16	00H
0F0F3H	Display mode register 1	DSPMOD1		R/W	8	00H
0F0F4H	Display control register	DSPCON	—	R/W	8	00H
0F100H	Display register 00	DSPR00	—	R/W	8	Undefined
0F101H	Display register 01	DSPR01	—	R/W	8	Undefined
0F102H	Display register 02	DSPR02	—	R/W	8	Undefined
0F103H	Display register 03	DSPR03	—	R/W	8	Undefined
0F104H	Display register 04	DSPR04	—	R/W	8	Undefined
0F105H	Display register 05	DSPR05	—	R/W	8	Undefined
0F106H	Display register 06	DSPR06	—	R/W	8	Undefined
0F107H	Display register 07	DSPR07	—	R/W	8	Undefined
0F108H	Display register 08	DSPR08	—	R/W	8	Undefined
0F109H	Display register 09	DSPR09	—	R/W	8	Undefined
0F10AH	Display register 0A	DSPR0A	—	R/W	8	Undefined
0F10BH	Display register 0B	DSPR0B	—	R/W	8	Undefined
0F10CH	Display register 0C	DSPR0C	—	R/W	8	Undefined
0F10DH	Display register 0D	DSPR0D	—	R/W	8	Undefined
0F10EH	Display register 0E	DSPR0E	—	R/W	8	Undefined
0F10FH	Display register 0F	DSPR0F	—	R/W	8	Undefined
0F110H	Display register 10	DSPR10	—	R/W	8	Undefined
0F111H	Display register 11	DSPR11	—	R/W	8	Undefined
0F112H	Display register 12	DSPR12	—	R/W	8	Undefined
0F113H	Display register 13	DSPR13	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F114H	Display register 14	DSPR14	—	R/W	8	Undefined
0F115H	Display register 15	DSPR15	—	R/W	8	Undefined
0F116H	Display register 16	DSPR16	—	R/W	8	Undefined
0F117H	Display register 17	DSPR17	—	R/W	8	Undefined
0F118H	Display register 18	DSPR18	—	R/W	8	Undefined
0F119H	Display register 19	DSPR19	—	R/W	8	Undefined
0F11AH	Display register 1A	DSPR1A	—	R/W	8	Undefined
0F11BH	Display register 1B	DSPR1B	—	R/W	8	Undefined
0F11CH	Display register 1C	DSPR1C	—	R/W	8	Undefined
0F11DH	Display register 1D	DSPR1D	—	R/W	8	Undefined
0F11EH	Display register 1E	DSPR1E	—	R/W	8	Undefined
0F11FH	Display register 1F	DSPR1F	—	R/W	8	Undefined
0F120H	Display register 20	DSPR20	—	R/W	8	Undefined
0F121H	Display register 21	DSPR21	—	R/W	8	Undefined
0F122H	Display register 22	DSPR22	—	R/W	8	Undefined
0F123H	Display register 23	DSPR23	—	R/W	8	Undefined
0F124H	Display register 24	DSPR24	—	R/W	8	Undefined
0F125H	Display register 25	DSPR25	—	R/W	8	Undefined
0F126H	Display register 26	DSPR26	—	R/W	8	Undefined
0F127H	Display register 27	DSPR27	—	R/W	8	Undefined
0F128H	Display register 28	DSPR28	—	R/W	8	Undefined
0F129H	Display register 29	DSPR29	—	R/W	8	Undefined
0F12AH	Display register 2A	DSPR2A	—	R/W	8	Undefined
0F12BH	Display register 2B	DSPR2B	—	R/W	8	Undefined
0F12CH	Display register 2C	DSPR2C	—	R/W	8	Undefined
0F12DH	Display register 2D	DSPR2D	—	R/W	8	Undefined
0F12EH	Display register 2E	DSPR2E	—	R/W	8	Undefined
0F12FH	Display register 2F	DSPR2F	—	R/W	8	Undefined
0F130H	Display register 30	DSPR30	—	R/W	8	Undefined
0F131H	Display register 31	DSPR31	—	R/W	8	Undefined
0F132H	Display register 32	DSPR32	—	R/W	8	Undefined
0F133H	Display register 33	DSPR33	—	R/W	8	Undefined
0F134H	Display register 34	DSPR34	—	R/W	8	Undefined
0F135H	Display register 35	DSPR35	—	R/W	8	Undefined
0F136H	Display register 36	DSPR36	—	R/W	8	Undefined
0F137H	Display register 37	DSPR37	—	R/W	8	Undefined
0F138H	Display register 38	DSPR38	—	R/W	8	Undefined
0F139H	Display register 39	DSPR39	—	R/W	8	Undefined
0F13AH	Display register 3A	DSPR3A	—	R/W	8	Undefined
0F13BH	Display register 3B	DSPR3B	—	R/W	8	Undefined
0F13CH	Display register 3C	DSPR3C	—	R/W	8	Undefined
0F13DH	Display register 3D	DSPR3D	—	R/W	8	Undefined
0F13EH	Display register 3E	DSPR3E	—	R/W	8	Undefined
0F13FH	Display register 3F	DSPR3F	—	R/W	8	Undefined
0F140H	Display register 40	DSPR40	—	R/W	8	Undefined
0F141H	Display register 41	DSPR41	—	R/W	8	Undefined
0F142H	Display register 42	DSPR42	—	R/W	8	Undefined
0F143H	Display register 43	DSPR43	—	R/W	8	Undefined
0F144H	Display register 44	DSPR44	—	R/W	8	Undefined
0F145H	Display register 45	DSPR45	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F146H	Display register 46	DSPR46	—	R/W	8	Undefined
0F147H	Display register 47	DSPR47	—	R/W	8	Undefined
0F148H	Display register 48	DSPR48	—	R/W	8	Undefined
0F149H	Display register 49	DSPR49	—	R/W	8	Undefined
0F14AH	Display register 4A	DSPR4A	—	R/W	8	Undefined
0F14BH	Display register 4B	DSPR4B	—	R/W	8	Undefined
0F14CH	Display register 4C	DSPR4C	—	R/W	8	Undefined
0F14DH	Display register 4D	DSPR4D	—	R/W	8	Undefined
0F14EH	Display register 4E	DSPR4E	—	R/W	8	Undefined
0F14FH	Display register 4F	DSPR4F	—	R/W	8	Undefined
0F150H	Display register 50	DSPR50	—	R/W	8	Undefined
0F151H	Display register 51	DSPR51	—	R/W	8	Undefined
0F152H	Display register 52	DSPR52	—	R/W	8	Undefined
0F153H	Display register 53	DSPR53	—	R/W	8	Undefined
0F154H	Display register 54	DSPR54	—	R/W	8	Undefined
0F155H	Display register 55	DSPR55	—	R/W	8	Undefined
0F156H	Display register 56	DSPR56	—	R/W	8	Undefined
0F157H	Display register 57	DSPR57	—	R/W	8	Undefined
0F158H	Display register 58	DSPR58	—	R/W	8	Undefined
0F159H	Display register 59	DSPR59	—	R/W	8	Undefined
0F15AH	Display register 5A	DSPR5A	—	R/W	8	Undefined
0F15BH	Display register 5B	DSPR5B	—	R/W	8	Undefined
0F15CH	Display register 5C	DSPR5C	—	R/W	8	Undefined
0F15DH	Display register 5D	DSPR5D	—	R/W	8	Undefined
0F15EH	Display register 5E	DSPR5E	—	R/W	8	Undefined
0F15FH	Display register 5F	DSPR5F	—	R/W	8	Undefined
0F160H	Display register 60	DSPR60	—	R/W	8	Undefined
0F161H	Display register 61	DSPR61	—	R/W	8	Undefined
0F162H	Display register 62	DSPR62	—	R/W	8	Undefined
0F163H	Display register 63	DSPR63	—	R/W	8	Undefined
0F164H	Display register 64	DSPR64	—	R/W	8	Undefined
0F165H	Display register 65	DSPR65	—	R/W	8	Undefined
0F166H	Display register 66	DSPR66	—	R/W	8	Undefined
0F167H	Display register 67	DSPR67	—	R/W	8	Undefined
0F168H	Display register 68	DSPR68	—	R/W	8	Undefined
0F169H	Display register 69	DSPR69	—	R/W	8	Undefined
0F16AH	Display register 6A	DSPR6A	—	R/W	8	Undefined
0F16BH	Display register 6B	DSPR6B	—	R/W	8	Undefined
0F16CH	Display register 6C	DSPR6C	—	R/W	8	Undefined
0F16DH	Display register 6D	DSPR6D	—	R/W	8	Undefined
0F16EH	Display register 6E	DSPR6E	—	R/W	8	Undefined
0F16FH	Display register 6F	DSPR6F	—	R/W	8	Undefined
0F170H	Display register 70	DSPR70	—	R/W	8	Undefined
0F171H	Display register 71	DSPR71	—	R/W	8	Undefined
0F200H	NMI data register	NMID	—	R	8	Undefined
0F201H	NMI control register	NMICON	—	R/W	8	00H
0F204H	Port 0 data register	P0D	—	R	8	Undefined
0F206H	Port 0 control register 0	P0CON0	P0CON	R/W	8/16	00H
0F207H	Port 0 control register 1	P0CON1		R/W	8	00H
0F208H	Port 1 data register	P1D	—	R	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F20AH	Port 1 control register 0	P1CON0	P1CON	R/W	8/16	00H
0F20BH	Port 1 control register 1	P1CON1		R/W	8	00H
0F210H	Port 2 data register	P2D	—	R/W	8	00H
0F212H	Port 2 control register 0	P2CON0	P2CON	R/W	8/16	00H
0F213H	Port 2 control register 1	P2CON1		R/W	8	00H
0F214H	Port 2 mode register	P2MOD0	—	R/W	8	00H
0F218H	Port 3 data register	P3D	—	R/W	8	00H
0F219H	Port 3 direction register	P3DIR	—	R/W	8	00H
0F21AH	Port 3 control register 0	P3CON0	P3CON	R/W	8/16	00H
0F21BH	Port 3 control register 1	P3CON1		R/W	8	00H
0F21CH	Port 3 mode register 0	P3MOD0	P3MOD	R/W	8/16	00H
0F21DH	Port 3 mode register 1	P3MOD1		R/W	8	00H
0F220H	Port 4 data register	P4D	—	R/W	8	00H
0F221H	Port 4 direction register	P4DIR	—	R/W	8	00H
0F222H	Port 4 control register 0	P4CON0	P4CON	R/W	8/16	00H
0F223H	Port 4 control register 1	P4CON1		R/W	8	00H
0F224H	Port 4 mode register 0	P4MOD0	P4MOD	R/W	8/16	00H
0F225H	Port 4 mode register 1	P4MOD1		R/W	8	00H
0F250H	Port A data register	PAD	—	R/W	8	00H
0F251H	Port A direction register	PADIR	—	R/W	8	00H
0F252H	Port A control register 0	PACON0	PACON	R/W	8/16	00H
0F253H	Port A control register 1	PACON1		R/W	8	00H
0F280H	Serial port 0 transmit/receive buffer L	SIO0BUFL	SIO0BUF	R/W	8/16	00H
0F281H	Serial port 0 transmit/receive buffer H	SIO0BUFH		R/W	8	00H
0F282H	Serial port 0 control register	SIO0CON	—	R/W	8	00H
0F284H	Serial port 0 mode register 0	SIO0MOD0	SIO0MOD	R/W	8/16	00H
0F285H	Serial port 0 mode register 1	SIO0MOD1		R/W	8	00H
0F290H	UART0 transmit/receive buffer	UA0BUF	—	R/W	8	00H
0F291H	UART0 control register	UA0CON	—	R/W	8	00H
0F292H	UART0 mode register 0	UA0MOD0	UA0MOD	R/W	8/16	00H
0F293H	UART0 mode register 1	UA0MOD1		R/W	8	00H
0F294H	UART0 baud rate register L	UA0BRTL	UA0BRT	R/W	8/16	0FFH
0F295H	UART0 baud rate register H	UA0BRTH		R/W	8	0FH
0F296H	UART0 status register	UA0STAT	—	R/W	8	00H
0F2A0H	I2C bus 0 receive data register	I2C0RD	—	R	8	00H
0F2A1H	I2C bus 0 slave address register	I2C0SA	—	R/W	8	00H
0F2A2H	I2C bus 0 transmit data register	I2C0TD	—	R/W	8	00H
0F2A3H	I2C bus 0 control register	I2C0CON	—	R/W	8	00H
0F2A4H	I2C bus 0 mode register	I2C0MOD	—	R/W	8	00H
0F2A5H	I2C bus 0 status register	I2C0STAT	—	R	8	00H
0F2C0H	Melody 0 control register	MD0CON	—	R/W	8	00H
0F2C1H	Melody 0 tempo code register	MD0TMP	—	R/W	8	00H
0F2C2H	Melody 0 tone scale code register	MD0TON	MD0TL	R/W	8/16	00H
0F2C3H	Melody 0 tone length code register	MD0LEN		R/W	8	00H
0F2D0H	SA-ADC result register 0L	SADR0L	SADR0	R	8/16	00H
0F2D1H	SA-ADC result register 0H	SADR0H		R	8	00H
0F2D2H	SA-ADC result register 1L	SADR1L	SADR1	R	8/16	00H
0F2D3H	SA-ADC result register 1H	SADR1H		R	8	00H
0F2F0H	SA-ADC control register 0	SADCON0	SADCON	R/W	8/16	00H

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2F1H	SA-ADC control register 1	SADCON1		R/W	8	00H
0F2F2H	SA-ADC mode register 0	SADMOD0	—	R/W	8	00H
0F300H	RC-ADC counter A register 0	RADCA0	—	R/W	8	00H
0F301H	RC-ADC counterA register 1	RADCA1	—	R/W	8	00H
0F302H	RC-ADC counterA register 2	RADCA2	—	R/W	8	00H
0F304H	RC-ADC counterB register 0	RADCB0	—	R/W	8	00H
0F305H	RC-ADC counterB register 1	RADCB1	—	R/W	8	00H
0F306H	RC-ADC counterB register 2	RADCB2	—	R/W	8	00H
0F308H	RC-ADC mode register	RADMOD	—	R/W	8	00H
0F309H	RC-ADC control register	RADCON	—	R/W	8	00H
0F400H	Display allocation register A	DS0C0A	—	R/W	8	Undefined
0F401H	Display allocation register A	DS1C0A	—	R/W	8	Undefined
0F402H	Display allocation register A	DS2C0A	—	R/W	8	Undefined
0F403H	Display allocation register A	DS3C0A	—	R/W	8	Undefined
0F404H	Display allocation register A	DS4C0A	—	R/W	8	Undefined
0F405H	Display allocation register A	DS5C0A	—	R/W	8	Undefined
0F406H	Display allocation register A	DS6C0A	—	R/W	8	Undefined
0F407H	Display allocation register A	DS7C0A	—	R/W	8	Undefined
0F408H	Display allocation register A	DS8C0A	—	R/W	8	Undefined
0F409H	Display allocation register A	DS9C0A	—	R/W	8	Undefined
0F40AH	Display allocation register A	DS10C0A	—	R/W	8	Undefined
0F40BH	Display allocation register A	DS11C0A	—	R/W	8	Undefined
0F40CH	Display allocation register A	DS12C0A	—	R/W	8	Undefined
0F40DH	Display allocation register A	DS13C0A	—	R/W	8	Undefined
0F40EH	Display allocation register A	DS14C0A	—	R/W	8	Undefined
0F40FH	Display allocation register A	DS15C0A	—	R/W	8	Undefined
0F410H	Display allocation register A	DS16C0A	—	R/W	8	Undefined
0F411H	Display allocation register A	DS17C0A	—	R/W	8	Undefined
0F412H	Display allocation register A	DS18C0A	—	R/W	8	Undefined
0F413H	Display allocation register A	DS19C0A	—	R/W	8	Undefined
0F414H	Display allocation register A	DS20C0A	—	R/W	8	Undefined
0F415H	Display allocation register A	DS21C0A	—	R/W	8	Undefined
0F416H	Display allocation register A	DS22C0A	—	R/W	8	Undefined
0F417H	Display allocation register A	DS23C0A	—	R/W	8	Undefined
0F418H	Display allocation register A	DS24C0A	—	R/W	8	Undefined
0F419H	Display allocation register A	DS25C0A	—	R/W	8	Undefined
0F41AH	Display allocation register A	DS26C0A	—	R/W	8	Undefined
0F41BH	Display allocation register A	DS27C0A	—	R/W	8	Undefined
0F41CH	Display allocation register A	DS28C0A	—	R/W	8	Undefined
0F41DH	Display allocation register A	DS29C0A	—	R/W	8	Undefined
0F41EH	Display allocation register A	DS30C0A	—	R/W	8	Undefined
0F41FH	Display allocation register A	DS31C0A	—	R/W	8	Undefined
0F420H	Display allocation register A	DS32C0A	—	R/W	8	Undefined
0F421H	Display allocation register A	DS33C0A	—	R/W	8	Undefined
0F422H	Display allocation register A	DS34C0A	—	R/W	8	Undefined
0F423H	Display allocation register A	DS35C0A	—	R/W	8	Undefined
0F424H	Display allocation register A	DS36C0A	—	R/W	8	Undefined
0F425H	Display allocation register A	DS37C0A	—	R/W	8	Undefined
0F426H	Display allocation register A	DS38C0A	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F427H	Display allocation register A	DS39C0A	—	R/W	8	Undefined
0F428H	Display allocation register A	DS40C0A	—	R/W	8	Undefined
0F429H	Display allocation register A	DS41C0A	—	R/W	8	Undefined
0F42AH	Display allocation register A	DS42C0A	—	R/W	8	Undefined
0F42BH	Display allocation register A	DS43C0A	—	R/W	8	Undefined
0F42CH	Display allocation register A	DS44C0A	—	R/W	8	Undefined
0F42DH	Display allocation register A	DS45C0A	—	R/W	8	Undefined
0F42EH	Display allocation register A	DS46C0A	—	R/W	8	Undefined
0F42FH	Display allocation register A	DS47C0A	—	R/W	8	Undefined
0F430H	Display allocation register A	DS48C0A	—	R/W	8	Undefined
0F431H	Display allocation register A	DS49C0A	—	R/W	8	Undefined
0F432H	Display allocation register A	DS50C0A	—	R/W	8	Undefined
0F433H	Display allocation register A	DS51C0A	—	R/W	8	Undefined
0F434H	Display allocation register A	DS52C0A	—	R/W	8	Undefined
0F435H	Display allocation register A	DS53C0A	—	R/W	8	Undefined
0F436H	Display allocation register A	DS54C0A	—	R/W	8	Undefined
0F437H	Display allocation register A	DS55C0A	—	R/W	8	Undefined
0F438H	Display allocation register A	DS56C0A	—	R/W	8	Undefined
0F439H	Display allocation register A	DS57C0A	—	R/W	8	Undefined
0F43AH	Display allocation register A	DS58C0A	—	R/W	8	Undefined
0F43BH	Display allocation register A	DS59C0A	—	R/W	8	Undefined
0F43CH	Display allocation register A	DS60C0A	—	R/W	8	Undefined
0F43DH	Display allocation register A	DS61C0A	—	R/W	8	Undefined
0F43EH	Display allocation register A	DS62C0A	—	R/W	8	Undefined
0F43FH	Display allocation register A	DS63C0A	—	R/W	8	Undefined
0F440H	Display allocation register A	DS0C1A	—	R/W	8	Undefined
0F441H	Display allocation register A	DS1C1A	—	R/W	8	Undefined
0F442H	Display allocation register A	DS2C1A	—	R/W	8	Undefined
0F443H	Display allocation register A	DS3C1A	—	R/W	8	Undefined
0F444H	Display allocation register A	DS4C1A	—	R/W	8	Undefined
0F445H	Display allocation register A	DS5C1A	—	R/W	8	Undefined
0F446H	Display allocation register A	DS6C1A	—	R/W	8	Undefined
0F447H	Display allocation register A	DS7C1A	—	R/W	8	Undefined
0F448H	Display allocation register A	DS8C1A	—	R/W	8	Undefined
0F449H	Display allocation register A	DS9C1A	—	R/W	8	Undefined
0F44AH	Display allocation register A	DS10C1A	—	R/W	8	Undefined
0F44BH	Display allocation register A	DS11C1A	—	R/W	8	Undefined
0F44CH	Display allocation register A	DS12C1A	—	R/W	8	Undefined
0F44DH	Display allocation register A	DS13C1A	—	R/W	8	Undefined
0F44EH	Display allocation register A	DS14C1A	—	R/W	8	Undefined
0F44FH	Display allocation register A	DS15C1A	—	R/W	8	Undefined
0F450H	Display allocation register A	DS16C1A	—	R/W	8	Undefined
0F451H	Display allocation register A	DS17C1A	—	R/W	8	Undefined
0F452H	Display allocation register A	DS18C1A	—	R/W	8	Undefined
0F453H	Display allocation register A	DS19C1A	—	R/W	8	Undefined
0F454H	Display allocation register A	DS20C1A	—	R/W	8	Undefined
0F455H	Display allocation register A	DS21C1A	—	R/W	8	Undefined
0F456H	Display allocation register A	DS22C1A	—	R/W	8	Undefined
0F457H	Display allocation register A	DS23C1A	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F458H	Display allocation register A	DS24C1A	—	R/W	8	Undefined
0F459H	Display allocation register A	DS25C1A	—	R/W	8	Undefined
0F45AH	Display allocation register A	DS26C1A	—	R/W	8	Undefined
0F45BH	Display allocation register A	DS27C1A	—	R/W	8	Undefined
0F45CH	Display allocation register A	DS28C1A	—	R/W	8	Undefined
0F45DH	Display allocation register A	DS29C1A	—	R/W	8	Undefined
0F45EH	Display allocation register A	DS30C1A	—	R/W	8	Undefined
0F45FH	Display allocation register A	DS31C1A	—	R/W	8	Undefined
0F460H	Display allocation register A	DS32C1A	—	R/W	8	Undefined
0F461H	Display allocation register A	DS33C1A	—	R/W	8	Undefined
0F462H	Display allocation register A	DS34C1A	—	R/W	8	Undefined
0F463H	Display allocation register A	DS35C1A	—	R/W	8	Undefined
0F464H	Display allocation register A	DS36C1A	—	R/W	8	Undefined
0F465H	Display allocation register A	DS37C1A	—	R/W	8	Undefined
0F466H	Display allocation register A	DS38C1A	—	R/W	8	Undefined
0F467H	Display allocation register A	DS39C1A	—	R/W	8	Undefined
0F468H	Display allocation register A	DS40C1A	—	R/W	8	Undefined
0F469H	Display allocation register A	DS41C1A	—	R/W	8	Undefined
0F46AH	Display allocation register A	DS42C1A	—	R/W	8	Undefined
0F46BH	Display allocation register A	DS43C1A	—	R/W	8	Undefined
0F46CH	Display allocation register A	DS44C1A	—	R/W	8	Undefined
0F46DH	Display allocation register A	DS45C1A	—	R/W	8	Undefined
0F46EH	Display allocation register A	DS46C1A	—	R/W	8	Undefined
0F46FH	Display allocation register A	DS47C1A	—	R/W	8	Undefined
0F470H	Display allocation register A	DS48C1A	—	R/W	8	Undefined
0F471H	Display allocation register A	DS49C1A	—	R/W	8	Undefined
0F472H	Display allocation register A	DS50C1A	—	R/W	8	Undefined
0F473H	Display allocation register A	DS51C1A	—	R/W	8	Undefined
0F474H	Display allocation register A	DS52C1A	—	R/W	8	Undefined
0F475H	Display allocation register A	DS53C1A	—	R/W	8	Undefined
0F476H	Display allocation register A	DS54C1A	—	R/W	8	Undefined
0F477H	Display allocation register A	DS55C1A	—	R/W	8	Undefined
0F478H	Display allocation register A	DS56C1A	—	R/W	8	Undefined
0F479H	Display allocation register A	DS57C1A	—	R/W	8	Undefined
0F47AH	Display allocation register A	DS58C1A	—	R/W	8	Undefined
0F47BH	Display allocation register A	DS59C1A	—	R/W	8	Undefined
0F47CH	Display allocation register A	DS60C1A	—	R/W	8	Undefined
0F47DH	Display allocation register A	DS61C1A	—	R/W	8	Undefined
0F47EH	Display allocation register A	DS62C1A	—	R/W	8	Undefined
0F47FH	Display allocation register A	DS63C1A	—	R/W	8	Undefined
0F480H	Display allocation register A	DS0C2A	—	R/W	8	Undefined
0F481H	Display allocation register A	DS1C2A	—	R/W	8	Undefined
0F482H	Display allocation register A	DS2C2A	—	R/W	8	Undefined
0F483H	Display allocation register A	DS3C2A	—	R/W	8	Undefined
0F484H	Display allocation register A	DS4C2A	—	R/W	8	Undefined
0F485H	Display allocation register A	DS5C2A	—	R/W	8	Undefined
0F486H	Display allocation register A	DS6C2A	—	R/W	8	Undefined
0F487H	Display allocation register A	DS7C2A	—	R/W	8	Undefined
0F488H	Display allocation register A	DS8C2A	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F489H	Display allocation register A	DS9C2A	—	R/W	8	Undefined
0F48AH	Display allocation register A	DS10C2A	—	R/W	8	Undefined
0F48BH	Display allocation register A	DS11C2A	—	R/W	8	Undefined
0F48CH	Display allocation register A	DS12C2A	—	R/W	8	Undefined
0F48DH	Display allocation register A	DS13C2A	—	R/W	8	Undefined
0F48EH	Display allocation register A	DS14C2A	—	R/W	8	Undefined
0F48FH	Display allocation register A	DS15C2A	—	R/W	8	Undefined
0F490H	Display allocation register A	DS16C2A	—	R/W	8	Undefined
0F491H	Display allocation register A	DS17C2A	—	R/W	8	Undefined
0F492H	Display allocation register A	DS18C2A	—	R/W	8	Undefined
0F493H	Display allocation register A	DS19C2A	—	R/W	8	Undefined
0F494H	Display allocation register A	DS20C2A	—	R/W	8	Undefined
0F495H	Display allocation register A	DS21C2A	—	R/W	8	Undefined
0F496H	Display allocation register A	DS22C2A	—	R/W	8	Undefined
0F497H	Display allocation register A	DS23C2A	—	R/W	8	Undefined
0F498H	Display allocation register A	DS24C2A	—	R/W	8	Undefined
0F499H	Display allocation register A	DS25C2A	—	R/W	8	Undefined
0F49AH	Display allocation register A	DS26C2A	—	R/W	8	Undefined
0F49BH	Display allocation register A	DS27C2A	—	R/W	8	Undefined
0F49CH	Display allocation register A	DS28C2A	—	R/W	8	Undefined
0F49DH	Display allocation register A	DS29C2A	—	R/W	8	Undefined
0F49EH	Display allocation register A	DS30C2A	—	R/W	8	Undefined
0F49FH	Display allocation register A	DS31C2A	—	R/W	8	Undefined
0F4A0H	Display allocation register A	DS32C2A	—	R/W	8	Undefined
0F4A1H	Display allocation register A	DS33C2A	—	R/W	8	Undefined
0F4A2H	Display allocation register A	DS34C2A	—	R/W	8	Undefined
0F4A3H	Display allocation register A	DS35C2A	—	R/W	8	Undefined
0F4A4H	Display allocation register A	DS36C2A	—	R/W	8	Undefined
0F4A5H	Display allocation register A	DS37C2A	—	R/W	8	Undefined
0F4A6H	Display allocation register A	DS38C2A	—	R/W	8	Undefined
0F4A7H	Display allocation register A	DS39C2A	—	R/W	8	Undefined
0F4A8H	Display allocation register A	DS40C2A	—	R/W	8	Undefined
0F4A9H	Display allocation register A	DS41C2A	—	R/W	8	Undefined
0F4AAH	Display allocation register A	DS42C2A	—	R/W	8	Undefined
0F4ABH	Display allocation register A	DS43C2A	—	R/W	8	Undefined
0F4ACH	Display allocation register A	DS44C2A	—	R/W	8	Undefined
0F4ADH	Display allocation register A	DS45C2A	—	R/W	8	Undefined
0F4AEH	Display allocation register A	DS46C2A	—	R/W	8	Undefined
0F4AFH	Display allocation register A	DS47C2A	—	R/W	8	Undefined
0F4B0H	Display allocation register A	DS48C2A	—	R/W	8	Undefined
0F4B1H	Display allocation register A	DS49C2A	—	R/W	8	Undefined
0F4B2H	Display allocation register A	DS50C2A	—	R/W	8	Undefined
0F4B3H	Display allocation register A	DS51C2A	—	R/W	8	Undefined
0F4B4H	Display allocation register A	DS52C2A	—	R/W	8	Undefined
0F4B5H	Display allocation register A	DS53C2A	—	R/W	8	Undefined
0F4B6H	Display allocation register A	DS54C2A	—	R/W	8	Undefined
0F4B7H	Display allocation register A	DS55C2A	—	R/W	8	Undefined
0F4B8H	Display allocation register A	DS56C2A	—	R/W	8	Undefined
0F4B9H	Display allocation register A	DS57C2A	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F4BAH	Display allocation register A	DS58C2A	—	R/W	8	Undefined
0F4BBH	Display allocation register A	DS59C2A	—	R/W	8	Undefined
0F4BCH	Display allocation register A	DS60C2A	—	R/W	8	Undefined
0F4BDH	Display allocation register A	DS61C2A	—	R/W	8	Undefined
0F4BEH	Display allocation register A	DS62C2A	—	R/W	8	Undefined
0F4BFH	Display allocation register A	DS63C2A	—	R/W	8	Undefined
0F4C0H	Display allocation register A	DS0C3A	—	R/W	8	Undefined
0F4C1H	Display allocation register A	DS1C3A	—	R/W	8	Undefined
0F4C2H	Display allocation register A	DS2C3A	—	R/W	8	Undefined
0F4C3H	Display allocation register A	DS3C3A	—	R/W	8	Undefined
0F4C4H	Display allocation register A	DS4C3A	—	R/W	8	Undefined
0F4C5H	Display allocation register A	DS5C3A	—	R/W	8	Undefined
0F4C6H	Display allocation register A	DS6C3A	—	R/W	8	Undefined
0F4C7H	Display allocation register A	DS7C3A	—	R/W	8	Undefined
0F4C8H	Display allocation register A	DS8C3A	—	R/W	8	Undefined
0F4C9H	Display allocation register A	DS9C3A	—	R/W	8	Undefined
0F4CAH	Display allocation register A	DS10C3A	—	R/W	8	Undefined
0F4CBH	Display allocation register A	DS11C3A	—	R/W	8	Undefined
0F4CCH	Display allocation register A	DS12C3A	—	R/W	8	Undefined
0F4CDH	Display allocation register A	DS13C3A	—	R/W	8	Undefined
0F4CEH	Display allocation register A	DS14C3A	—	R/W	8	Undefined
0F4CFH	Display allocation register A	DS15C3A	—	R/W	8	Undefined
0F4D0H	Display allocation register A	DS16C3A	—	R/W	8	Undefined
0F4D1H	Display allocation register A	DS17C3A	—	R/W	8	Undefined
0F4D2H	Display allocation register A	DS18C3A	—	R/W	8	Undefined
0F4D3H	Display allocation register A	DS19C3A	—	R/W	8	Undefined
0F4D4H	Display allocation register A	DS20C3A	—	R/W	8	Undefined
0F4D5H	Display allocation register A	DS21C3A	—	R/W	8	Undefined
0F4D6H	Display allocation register A	DS22C3A	—	R/W	8	Undefined
0F4D7H	Display allocation register A	DS23C3A	—	R/W	8	Undefined
0F4D8H	Display allocation register A	DS24C3A	—	R/W	8	Undefined
0F4D9H	Display allocation register A	DS25C3A	—	R/W	8	Undefined
0F4DAH	Display allocation register A	DS26C3A	—	R/W	8	Undefined
0F4DBH	Display allocation register A	DS27C3A	—	R/W	8	Undefined
0F4DCH	Display allocation register A	DS28C3A	—	R/W	8	Undefined
0F4DDH	Display allocation register A	DS29C3A	—	R/W	8	Undefined
0F4DEH	Display allocation register A	DS30C3A	—	R/W	8	Undefined
0F4DFH	Display allocation register A	DS31C3A	—	R/W	8	Undefined
0F4E0H	Display allocation register A	DS32C3A	—	R/W	8	Undefined
0F4E1H	Display allocation register A	DS33C3A	—	R/W	8	Undefined
0F4E2H	Display allocation register A	DS34C3A	—	R/W	8	Undefined
0F4E3H	Display allocation register A	DS35C3A	—	R/W	8	Undefined
0F4E4H	Display allocation register A	DS36C3A	—	R/W	8	Undefined
0F4E5H	Display allocation register A	DS37C3A	—	R/W	8	Undefined
0F4E6H	Display allocation register A	DS38C3A	—	R/W	8	Undefined
0F4E7H	Display allocation register A	DS39C3A	—	R/W	8	Undefined
0F4E8H	Display allocation register A	DS40C3A	—	R/W	8	Undefined
0F4E9H	Display allocation register A	DS41C3A	—	R/W	8	Undefined
0F4EAH	Display allocation register A	DS42C3A	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F4EBH	Display allocation register A	DS43C3A	—	R/W	8	Undefined
0F4ECH	Display allocation register A	DS44C3A	—	R/W	8	Undefined
0F4EDH	Display allocation register A	DS45C3A	—	R/W	8	Undefined
0F4EEH	Display allocation register A	DS46C3A	—	R/W	8	Undefined
0F4EFH	Display allocation register A	DS47C3A	—	R/W	8	Undefined
0F4F0H	Display allocation register A	DS48C3A	—	R/W	8	Undefined
0F4F1H	Display allocation register A	DS49C3A	—	R/W	8	Undefined
0F4F2H	Display allocation register A	DS50C3A	—	R/W	8	Undefined
0F4F3H	Display allocation register A	DS51C3A	—	R/W	8	Undefined
0F4F4H	Display allocation register A	DS52C3A	—	R/W	8	Undefined
0F4F5H	Display allocation register A	DS53C3A	—	R/W	8	Undefined
0F4F6H	Display allocation register A	DS54C3A	—	R/W	8	Undefined
0F4F7H	Display allocation register A	DS55C3A	—	R/W	8	Undefined
0F4F8H	Display allocation register A	DS56C3A	—	R/W	8	Undefined
0F4F9H	Display allocation register A	DS57C3A	—	R/W	8	Undefined
0F4FAH	Display allocation register A	DS58C3A	—	R/W	8	Undefined
0F4FBH	Display allocation register A	DS59C3A	—	R/W	8	Undefined
0F4FCH	Display allocation register A	DS60C3A	—	R/W	8	Undefined
0F4FDH	Display allocation register A	DS61C3A	—	R/W	8	Undefined
0F4FEH	Display allocation register A	DS62C3A	—	R/W	8	Undefined
0F4FFH	Display allocation register A	DS63C3A	—	R/W	8	Undefined
0F500H	Display allocation register A	DS0C4A	—	R/W	8	Undefined
0F501H	Display allocation register A	DS1C4A	—	R/W	8	Undefined
0F502H	Display allocation register A	DS2C4A	—	R/W	8	Undefined
0F503H	Display allocation register A	DS3C4A	—	R/W	8	Undefined
0F504H	Display allocation register A	DS4C4A	—	R/W	8	Undefined
0F505H	Display allocation register A	DS5C4A	—	R/W	8	Undefined
0F506H	Display allocation register A	DS6C4A	—	R/W	8	Undefined
0F507H	Display allocation register A	DS7C4A	—	R/W	8	Undefined
0F508H	Display allocation register A	DS8C4A	—	R/W	8	Undefined
0F509H	Display allocation register A	DS9C4A	—	R/W	8	Undefined
0F50AH	Display allocation register A	DS10C4A	—	R/W	8	Undefined
0F50BH	Display allocation register A	DS11C4A	—	R/W	8	Undefined
0F50CH	Display allocation register A	DS12C4A	—	R/W	8	Undefined
0F50DH	Display allocation register A	DS13C4A	—	R/W	8	Undefined
0F50EH	Display allocation register A	DS14C4A	—	R/W	8	Undefined
0F50FH	Display allocation register A	DS15C4A	—	R/W	8	Undefined
0F510H	Display allocation register A	DS16C4A	—	R/W	8	Undefined
0F511H	Display allocation register A	DS17C4A	—	R/W	8	Undefined
0F512H	Display allocation register A	DS18C4A	—	R/W	8	Undefined
0F513H	Display allocation register A	DS19C4A	—	R/W	8	Undefined
0F514H	Display allocation register A	DS20C4A	—	R/W	8	Undefined
0F515H	Display allocation register A	DS21C4A	—	R/W	8	Undefined
0F516H	Display allocation register A	DS22C4A	—	R/W	8	Undefined
0F517H	Display allocation register A	DS23C4A	—	R/W	8	Undefined
0F518H	Display allocation register A	DS24C4A	—	R/W	8	Undefined
0F519H	Display allocation register A	DS25C4A	—	R/W	8	Undefined
0F51AH	Display allocation register A	DS26C4A	—	R/W	8	Undefined
0F51BH	Display allocation register A	DS27C4A	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F51CH	Display allocation register A	DS28C4A	—	R/W	8	Undefined
0F51DH	Display allocation register A	DS29C4A	—	R/W	8	Undefined
0F51EH	Display allocation register A	DS30C4A	—	R/W	8	Undefined
0F51FH	Display allocation register A	DS31C4A	—	R/W	8	Undefined
0F520H	Display allocation register A	DS32C4A	—	R/W	8	Undefined
0F521H	Display allocation register A	DS33C4A	—	R/W	8	Undefined
0F522H	Display allocation register A	DS34C4A	—	R/W	8	Undefined
0F523H	Display allocation register A	DS35C4A	—	R/W	8	Undefined
0F524H	Display allocation register A	DS36C4A	—	R/W	8	Undefined
0F525H	Display allocation register A	DS37C4A	—	R/W	8	Undefined
0F526H	Display allocation register A	DS38C4A	—	R/W	8	Undefined
0F527H	Display allocation register A	DS39C4A	—	R/W	8	Undefined
0F528H	Display allocation register A	DS40C4A	—	R/W	8	Undefined
0F529H	Display allocation register A	DS41C4A	—	R/W	8	Undefined
0F52AH	Display allocation register A	DS42C4A	—	R/W	8	Undefined
0F52BH	Display allocation register A	DS43C4A	—	R/W	8	Undefined
0F52CH	Display allocation register A	DS44C4A	—	R/W	8	Undefined
0F52DH	Display allocation register A	DS45C4A	—	R/W	8	Undefined
0F52EH	Display allocation register A	DS46C4A	—	R/W	8	Undefined
0F52FH	Display allocation register A	DS47C4A	—	R/W	8	Undefined
0F530H	Display allocation register A	DS48C4A	—	R/W	8	Undefined
0F531H	Display allocation register A	DS49C4A	—	R/W	8	Undefined
0F532H	Display allocation register A	DS50C4A	—	R/W	8	Undefined
0F533H	Display allocation register A	DS51C4A	—	R/W	8	Undefined
0F534H	Display allocation register A	DS52C4A	—	R/W	8	Undefined
0F535H	Display allocation register A	DS53C4A	—	R/W	8	Undefined
0F536H	Display allocation register A	DS54C4A	—	R/W	8	Undefined
0F537H	Display allocation register A	DS55C4A	—	R/W	8	Undefined
0F538H	Display allocation register A	DS56C4A	—	R/W	8	Undefined
0F539H	Display allocation register A	DS57C4A	—	R/W	8	Undefined
0F53AH	Display allocation register A	DS58C4A	—	R/W	8	Undefined
0F53BH	Display allocation register A	DS59C4A	—	R/W	8	Undefined
0F53CH	Display allocation register A	DS60C4A	—	R/W	8	Undefined
0F53DH	Display allocation register A	DS61C4A	—	R/W	8	Undefined
0F53EH	Display allocation register A	DS62C4A	—	R/W	8	Undefined
0F53FH	Display allocation register A	DS63C4A	—	R/W	8	Undefined
0F540H	Display allocation register A	DS0C5A	—	R/W	8	Undefined
0F541H	Display allocation register A	DS1C5A	—	R/W	8	Undefined
0F542H	Display allocation register A	DS2C5A	—	R/W	8	Undefined
0F543H	Display allocation register A	DS3C5A	—	R/W	8	Undefined
0F544H	Display allocation register A	DS4C5A	—	R/W	8	Undefined
0F545H	Display allocation register A	DS5C5A	—	R/W	8	Undefined
0F546H	Display allocation register A	DS6C5A	—	R/W	8	Undefined
0F547H	Display allocation register A	DS7C5A	—	R/W	8	Undefined
0F548H	Display allocation register A	DS8C5A	—	R/W	8	Undefined
0F549H	Display allocation register A	DS9C5A	—	R/W	8	Undefined
0F54AH	Display allocation register A	DS10C5A	—	R/W	8	Undefined
0F54BH	Display allocation register A	DS11C5A	—	R/W	8	Undefined
0F54CH	Display allocation register A	DS12C5A	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F54DH	Display allocation register A	DS13C5A	—	R/W	8	Undefined
0F54EH	Display allocation register A	DS14C5A	—	R/W	8	Undefined
0F54FH	Display allocation register A	DS15C5A	—	R/W	8	Undefined
0F550H	Display allocation register A	DS16C5A	—	R/W	8	Undefined
0F551H	Display allocation register A	DS17C5A	—	R/W	8	Undefined
0F552H	Display allocation register A	DS18C5A	—	R/W	8	Undefined
0F553H	Display allocation register A	DS19C5A	—	R/W	8	Undefined
0F554H	Display allocation register A	DS20C5A	—	R/W	8	Undefined
0F555H	Display allocation register A	DS21C5A	—	R/W	8	Undefined
0F556H	Display allocation register A	DS22C5A	—	R/W	8	Undefined
0F557H	Display allocation register A	DS23C5A	—	R/W	8	Undefined
0F558H	Display allocation register A	DS24C5A	—	R/W	8	Undefined
0F559H	Display allocation register A	DS25C5A	—	R/W	8	Undefined
0F55AH	Display allocation register A	DS26C5A	—	R/W	8	Undefined
0F55BH	Display allocation register A	DS27C5A	—	R/W	8	Undefined
0F55CH	Display allocation register A	DS28C5A	—	R/W	8	Undefined
0F55DH	Display allocation register A	DS29C5A	—	R/W	8	Undefined
0F55EH	Display allocation register A	DS30C5A	—	R/W	8	Undefined
0F55FH	Display allocation register A	DS31C5A	—	R/W	8	Undefined
0F560H	Display allocation register A	DS32C5A	—	R/W	8	Undefined
0F561H	Display allocation register A	DS33C5A	—	R/W	8	Undefined
0F562H	Display allocation register A	DS34C5A	—	R/W	8	Undefined
0F563H	Display allocation register A	DS35C5A	—	R/W	8	Undefined
0F564H	Display allocation register A	DS36C5A	—	R/W	8	Undefined
0F565H	Display allocation register A	DS37C5A	—	R/W	8	Undefined
0F566H	Display allocation register A	DS38C5A	—	R/W	8	Undefined
0F567H	Display allocation register A	DS39C5A	—	R/W	8	Undefined
0F568H	Display allocation register A	DS40C5A	—	R/W	8	Undefined
0F569H	Display allocation register A	DS41C5A	—	R/W	8	Undefined
0F56AH	Display allocation register A	DS42C5A	—	R/W	8	Undefined
0F56BH	Display allocation register A	DS43C5A	—	R/W	8	Undefined
0F56CH	Display allocation register A	DS44C5A	—	R/W	8	Undefined
0F56DH	Display allocation register A	DS45C5A	—	R/W	8	Undefined
0F56EH	Display allocation register A	DS46C5A	—	R/W	8	Undefined
0F56FH	Display allocation register A	DS47C5A	—	R/W	8	Undefined
0F570H	Display allocation register A	DS48C5A	—	R/W	8	Undefined
0F571H	Display allocation register A	DS49C5A	—	R/W	8	Undefined
0F572H	Display allocation register A	DS50C5A	—	R/W	8	Undefined
0F573H	Display allocation register A	DS51C5A	—	R/W	8	Undefined
0F574H	Display allocation register A	DS52C5A	—	R/W	8	Undefined
0F575H	Display allocation register A	DS53C5A	—	R/W	8	Undefined
0F576H	Display allocation register A	DS54C5A	—	R/W	8	Undefined
0F577H	Display allocation register A	DS55C5A	—	R/W	8	Undefined
0F578H	Display allocation register A	DS56C5A	—	R/W	8	Undefined
0F579H	Display allocation register A	DS57C5A	—	R/W	8	Undefined
0F57AH	Display allocation register A	DS58C5A	—	R/W	8	Undefined
0F57BH	Display allocation register A	DS59C5A	—	R/W	8	Undefined
0F57CH	Display allocation register A	DS60C5A	—	R/W	8	Undefined
0F57DH	Display allocation register A	DS61C5A	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F57EH	Display allocation register A	DS62C5A	—	R/W	8	Undefined
0F57FH	Display allocation register A	DS63C5A	—	R/W	8	Undefined
0F580H	Display allocation register A	DS0C6A	—	R/W	8	Undefined
0F581H	Display allocation register A	DS1C6A	—	R/W	8	Undefined
0F582H	Display allocation register A	DS2C6A	—	R/W	8	Undefined
0F583H	Display allocation register A	DS3C6A	—	R/W	8	Undefined
0F584H	Display allocation register A	DS4C6A	—	R/W	8	Undefined
0F585H	Display allocation register A	DS5C6A	—	R/W	8	Undefined
0F586H	Display allocation register A	DS6C6A	—	R/W	8	Undefined
0F587H	Display allocation register A	DS7C6A	—	R/W	8	Undefined
0F588H	Display allocation register A	DS8C6A	—	R/W	8	Undefined
0F589H	Display allocation register A	DS9C6A	—	R/W	8	Undefined
0F58AH	Display allocation register A	DS10C6A	—	R/W	8	Undefined
0F58BH	Display allocation register A	DS11C6A	—	R/W	8	Undefined
0F58CH	Display allocation register A	DS12C6A	—	R/W	8	Undefined
0F58DH	Display allocation register A	DS13C6A	—	R/W	8	Undefined
0F58EH	Display allocation register A	DS14C6A	—	R/W	8	Undefined
0F58FH	Display allocation register A	DS15C6A	—	R/W	8	Undefined
0F590H	Display allocation register A	DS16C6A	—	R/W	8	Undefined
0F591H	Display allocation register A	DS17C6A	—	R/W	8	Undefined
0F592H	Display allocation register A	DS18C6A	—	R/W	8	Undefined
0F593H	Display allocation register A	DS19C6A	—	R/W	8	Undefined
0F594H	Display allocation register A	DS20C6A	—	R/W	8	Undefined
0F595H	Display allocation register A	DS21C6A	—	R/W	8	Undefined
0F596H	Display allocation register A	DS22C6A	—	R/W	8	Undefined
0F597H	Display allocation register A	DS23C6A	—	R/W	8	Undefined
0F598H	Display allocation register A	DS24C6A	—	R/W	8	Undefined
0F599H	Display allocation register A	DS25C6A	—	R/W	8	Undefined
0F59AH	Display allocation register A	DS26C6A	—	R/W	8	Undefined
0F59BH	Display allocation register A	DS27C6A	—	R/W	8	Undefined
0F59CH	Display allocation register A	DS28C6A	—	R/W	8	Undefined
0F59DH	Display allocation register A	DS29C6A	—	R/W	8	Undefined
0F59EH	Display allocation register A	DS30C6A	—	R/W	8	Undefined
0F59FH	Display allocation register A	DS31C6A	—	R/W	8	Undefined
0F5A0H	Display allocation register A	DS32C6A	—	R/W	8	Undefined
0F5A1H	Display allocation register A	DS33C6A	—	R/W	8	Undefined
0F5A2H	Display allocation register A	DS34C6A	—	R/W	8	Undefined
0F5A3H	Display allocation register A	DS35C6A	—	R/W	8	Undefined
0F5A4H	Display allocation register A	DS36C6A	—	R/W	8	Undefined
0F5A5H	Display allocation register A	DS37C6A	—	R/W	8	Undefined
0F5A6H	Display allocation register A	DS38C6A	—	R/W	8	Undefined
0F5A7H	Display allocation register A	DS39C6A	—	R/W	8	Undefined
0F5A8H	Display allocation register A	DS40C6A	—	R/W	8	Undefined
0F5A9H	Display allocation register A	DS41C6A	—	R/W	8	Undefined
0F5AAH	Display allocation register A	DS42C6A	—	R/W	8	Undefined
0F5ABH	Display allocation register A	DS43C6A	—	R/W	8	Undefined
0F5ACH	Display allocation register A	DS44C6A	—	R/W	8	Undefined
0F5ADH	Display allocation register A	DS45C6A	—	R/W	8	Undefined
0F5AEH	Display allocation register A	DS46C6A	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F5AFH	Display allocation register A	DS47C6A	—	R/W	8	Undefined
0F5B0H	Display allocation register A	DS48C6A	—	R/W	8	Undefined
0F5B1H	Display allocation register A	DS49C6A	—	R/W	8	Undefined
0F5B2H	Display allocation register A	DS50C6A	—	R/W	8	Undefined
0F5B3H	Display allocation register A	DS51C6A	—	R/W	8	Undefined
0F5B4H	Display allocation register A	DS52C6A	—	R/W	8	Undefined
0F5B5H	Display allocation register A	DS53C6A	—	R/W	8	Undefined
0F5B6H	Display allocation register A	DS54C6A	—	R/W	8	Undefined
0F5B7H	Display allocation register A	DS55C6A	—	R/W	8	Undefined
0F5B8H	Display allocation register A	DS56C6A	—	R/W	8	Undefined
0F5B9H	Display allocation register A	DS57C6A	—	R/W	8	Undefined
0F5BAH	Display allocation register A	DS58C6A	—	R/W	8	Undefined
0F5BBH	Display allocation register A	DS59C6A	—	R/W	8	Undefined
0F5BCH	Display allocation register A	DS60C6A	—	R/W	8	Undefined
0F5BDH	Display allocation register A	DS61C6A	—	R/W	8	Undefined
0F5BEH	Display allocation register A	DS62C6A	—	R/W	8	Undefined
0F5BFH	Display allocation register A	DS63C6A	—	R/W	8	Undefined
0F5C0H	Display allocation register A	DS0C7A	—	R/W	8	Undefined
0F5C1H	Display allocation register A	DS1C7A	—	R/W	8	Undefined
0F5C2H	Display allocation register A	DS2C7A	—	R/W	8	Undefined
0F5C3H	Display allocation register A	DS3C7A	—	R/W	8	Undefined
0F5C4H	Display allocation register A	DS4C7A	—	R/W	8	Undefined
0F5C5H	Display allocation register A	DS5C7A	—	R/W	8	Undefined
0F5C6H	Display allocation register A	DS6C7A	—	R/W	8	Undefined
0F5C7H	Display allocation register A	DS7C7A	—	R/W	8	Undefined
0F5C8H	Display allocation register A	DS8C7A	—	R/W	8	Undefined
0F5C9H	Display allocation register A	DS9C7A	—	R/W	8	Undefined
0F5CAH	Display allocation register A	DS10C7A	—	R/W	8	Undefined
0F5CBH	Display allocation register A	DS11C7A	—	R/W	8	Undefined
0F5CCH	Display allocation register A	DS12C7A	—	R/W	8	Undefined
0F5CDH	Display allocation register A	DS13C7A	—	R/W	8	Undefined
0F5CEH	Display allocation register A	DS14C7A	—	R/W	8	Undefined
0F5CFH	Display allocation register A	DS15C7A	—	R/W	8	Undefined
0F5D0H	Display allocation register A	DS16C7A	—	R/W	8	Undefined
0F5D1H	Display allocation register A	DS17C7A	—	R/W	8	Undefined
0F5D2H	Display allocation register A	DS18C7A	—	R/W	8	Undefined
0F5D3H	Display allocation register A	DS19C7A	—	R/W	8	Undefined
0F5D4H	Display allocation register A	DS20C7A	—	R/W	8	Undefined
0F5D5H	Display allocation register A	DS21C7A	—	R/W	8	Undefined
0F5D6H	Display allocation register A	DS22C7A	—	R/W	8	Undefined
0F5D7H	Display allocation register A	DS23C7A	—	R/W	8	Undefined
0F5D8H	Display allocation register A	DS24C7A	—	R/W	8	Undefined
0F5D9H	Display allocation register A	DS25C7A	—	R/W	8	Undefined
0F5DAH	Display allocation register A	DS26C7A	—	R/W	8	Undefined
0F5DBH	Display allocation register A	DS27C7A	—	R/W	8	Undefined
0F5DCH	Display allocation register A	DS28C7A	—	R/W	8	Undefined
0F5DDH	Display allocation register A	DS29C7A	—	R/W	8	Undefined
0F5DEH	Display allocation register A	DS30C7A	—	R/W	8	Undefined
0F5DFH	Display allocation register A	DS31C7A	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F5E0H	Display allocation register A	DS32C7A	—	R/W	8	Undefined
0F5E1H	Display allocation register A	DS33C7A	—	R/W	8	Undefined
0F5E2H	Display allocation register A	DS34C7A	—	R/W	8	Undefined
0F5E3H	Display allocation register A	DS35C7A	—	R/W	8	Undefined
0F5E4H	Display allocation register A	DS36C7A	—	R/W	8	Undefined
0F5E5H	Display allocation register A	DS37C7A	—	R/W	8	Undefined
0F5E6H	Display allocation register A	DS38C7A	—	R/W	8	Undefined
0F5E7H	Display allocation register A	DS39C7A	—	R/W	8	Undefined
0F5E8H	Display allocation register A	DS40C7A	—	R/W	8	Undefined
0F5E9H	Display allocation register A	DS41C7A	—	R/W	8	Undefined
0F5EAH	Display allocation register A	DS42C7A	—	R/W	8	Undefined
0F5EBH	Display allocation register A	DS43C7A	—	R/W	8	Undefined
0F5ECH	Display allocation register A	DS44C7A	—	R/W	8	Undefined
0F5EDH	Display allocation register A	DS45C7A	—	R/W	8	Undefined
0F5EEH	Display allocation register A	DS46C7A	—	R/W	8	Undefined
0F5EFH	Display allocation register A	DS47C7A	—	R/W	8	Undefined
0F5F0H	Display allocation register A	DS48C7A	—	R/W	8	Undefined
0F5F1H	Display allocation register A	DS49C7A	—	R/W	8	Undefined
0F5F2H	Display allocation register A	DS50C7A	—	R/W	8	Undefined
0F5F3H	Display allocation register A	DS51C7A	—	R/W	8	Undefined
0F5F4H	Display allocation register A	DS52C7A	—	R/W	8	Undefined
0F5F5H	Display allocation register A	DS53C7A	—	R/W	8	Undefined
0F5F6H	Display allocation register A	DS54C7A	—	R/W	8	Undefined
0F5F7H	Display allocation register A	DS55C7A	—	R/W	8	Undefined
0F5F8H	Display allocation register A	DS56C7A	—	R/W	8	Undefined
0F5F9H	Display allocation register A	DS57C7A	—	R/W	8	Undefined
0F5FAH	Display allocation register A	DS58C7A	—	R/W	8	Undefined
0F5FBH	Display allocation register A	DS59C7A	—	R/W	8	Undefined
0F5FCH	Display allocation register A	DS60C7A	—	R/W	8	Undefined
0F5FDH	Display allocation register A	DS61C7A	—	R/W	8	Undefined
0F5FEH	Display allocation register A	DS62C7A	—	R/W	8	Undefined
0F5FFH	Display allocation register A	DS63C7A	—	R/W	8	Undefined
0F600H	Display allocation register B	DS0C0B	—	R/W	8	Undefined
0F601H	Display allocation register B	DS1C0B	—	R/W	8	Undefined
0F602H	Display allocation register B	DS2C0B	—	R/W	8	Undefined
0F603H	Display allocation register B	DS3C0B	—	R/W	8	Undefined
0F604H	Display allocation register B	DS4C0B	—	R/W	8	Undefined
0F605H	Display allocation register B	DS5C0B	—	R/W	8	Undefined
0F606H	Display allocation register B	DS6C0B	—	R/W	8	Undefined
0F607H	Display allocation register B	DS7C0B	—	R/W	8	Undefined
0F608H	Display allocation register B	DS8C0B	—	R/W	8	Undefined
0F609H	Display allocation register B	DS9C0B	—	R/W	8	Undefined
0F60AH	Display allocation register B	DS10C0B	—	R/W	8	Undefined
0F60BH	Display allocation register B	DS11C0B	—	R/W	8	Undefined
0F60CH	Display allocation register B	DS12C0B	—	R/W	8	Undefined
0F60DH	Display allocation register B	DS13C0B	—	R/W	8	Undefined
0F60EH	Display allocation register B	DS14C0B	—	R/W	8	Undefined
0F60FH	Display allocation register B	DS15C0B	—	R/W	8	Undefined
0F610H	Display allocation register B	DS16C0B	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F611H	Display allocation register B	DS17C0B	—	R/W	8	Undefined
0F612H	Display allocation register B	DS18C0B	—	R/W	8	Undefined
0F613H	Display allocation register B	DS19C0B	—	R/W	8	Undefined
0F614H	Display allocation register B	DS20C0B	—	R/W	8	Undefined
0F615H	Display allocation register B	DS21C0B	—	R/W	8	Undefined
0F616H	Display allocation register B	DS22C0B	—	R/W	8	Undefined
0F617H	Display allocation register B	DS23C0B	—	R/W	8	Undefined
0F618H	Display allocation register B	DS24C0B	—	R/W	8	Undefined
0F619H	Display allocation register B	DS25C0B	—	R/W	8	Undefined
0F61AH	Display allocation register B	DS26C0B	—	R/W	8	Undefined
0F61BH	Display allocation register B	DS27C0B	—	R/W	8	Undefined
0F61CH	Display allocation register B	DS28C0B	—	R/W	8	Undefined
0F61DH	Display allocation register B	DS29C0B	—	R/W	8	Undefined
0F61EH	Display allocation register B	DS30C0B	—	R/W	8	Undefined
0F61FH	Display allocation register B	DS31C0B	—	R/W	8	Undefined
0F620H	Display allocation register B	DS32C0B	—	R/W	8	Undefined
0F621H	Display allocation register B	DS33C0B	—	R/W	8	Undefined
0F622H	Display allocation register B	DS34C0B	—	R/W	8	Undefined
0F623H	Display allocation register B	DS35C0B	—	R/W	8	Undefined
0F624H	Display allocation register B	DS36C0B	—	R/W	8	Undefined
0F625H	Display allocation register B	DS37C0B	—	R/W	8	Undefined
0F626H	Display allocation register B	DS38C0B	—	R/W	8	Undefined
0F627H	Display allocation register B	DS39C0B	—	R/W	8	Undefined
0F628H	Display allocation register B	DS40C0B	—	R/W	8	Undefined
0F629H	Display allocation register B	DS41C0B	—	R/W	8	Undefined
0F62AH	Display allocation register B	DS42C0B	—	R/W	8	Undefined
0F62BH	Display allocation register B	DS43C0B	—	R/W	8	Undefined
0F62CH	Display allocation register B	DS44C0B	—	R/W	8	Undefined
0F62DH	Display allocation register B	DS45C0B	—	R/W	8	Undefined
0F62EH	Display allocation register B	DS46C0B	—	R/W	8	Undefined
0F62FH	Display allocation register B	DS47C0B	—	R/W	8	Undefined
0F630H	Display allocation register B	DS48C0B	—	R/W	8	Undefined
0F631H	Display allocation register B	DS49C0B	—	R/W	8	Undefined
0F632H	Display allocation register B	DS50C0B	—	R/W	8	Undefined
0F633H	Display allocation register B	DS51C0B	—	R/W	8	Undefined
0F634H	Display allocation register B	DS52C0B	—	R/W	8	Undefined
0F635H	Display allocation register B	DS53C0B	—	R/W	8	Undefined
0F636H	Display allocation register B	DS54C0B	—	R/W	8	Undefined
0F637H	Display allocation register B	DS55C0B	—	R/W	8	Undefined
0F638H	Display allocation register B	DS56C0B	—	R/W	8	Undefined
0F639H	Display allocation register B	DS57C0B	—	R/W	8	Undefined
0F63AH	Display allocation register B	DS58C0B	—	R/W	8	Undefined
0F63BH	Display allocation register B	DS59C0B	—	R/W	8	Undefined
0F63CH	Display allocation register B	DS60C0B	—	R/W	8	Undefined
0F63DH	Display allocation register B	DS61C0B	—	R/W	8	Undefined
0F63EH	Display allocation register B	DS62C0B	—	R/W	8	Undefined
0F63FH	Display allocation register B	DS63C0B	—	R/W	8	Undefined
0F640H	Display allocation register B	DS0C1B	—	R/W	8	Undefined
0F641H	Display allocation register B	DS1C1B	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F642H	Display allocation register B	DS2C1B	—	R/W	8	Undefined
0F643H	Display allocation register B	DS3C1B	—	R/W	8	Undefined
0F644H	Display allocation register B	DS4C1B	—	R/W	8	Undefined
0F645H	Display allocation register B	DS5C1B	—	R/W	8	Undefined
0F646H	Display allocation register B	DS6C1B	—	R/W	8	Undefined
0F647H	Display allocation register B	DS7C1B	—	R/W	8	Undefined
0F648H	Display allocation register B	DS8C1B	—	R/W	8	Undefined
0F649H	Display allocation register B	DS9C1B	—	R/W	8	Undefined
0F64AH	Display allocation register B	DS10C1B	—	R/W	8	Undefined
0F64BH	Display allocation register B	DS11C1B	—	R/W	8	Undefined
0F64CH	Display allocation register B	DS12C1B	—	R/W	8	Undefined
0F64DH	Display allocation register B	DS13C1B	—	R/W	8	Undefined
0F64EH	Display allocation register B	DS14C1B	—	R/W	8	Undefined
0F64FH	Display allocation register B	DS15C1B	—	R/W	8	Undefined
0F650H	Display allocation register B	DS16C1B	—	R/W	8	Undefined
0F651H	Display allocation register B	DS17C1B	—	R/W	8	Undefined
0F652H	Display allocation register B	DS18C1B	—	R/W	8	Undefined
0F653H	Display allocation register B	DS19C1B	—	R/W	8	Undefined
0F654H	Display allocation register B	DS20C1B	—	R/W	8	Undefined
0F655H	Display allocation register B	DS21C1B	—	R/W	8	Undefined
0F656H	Display allocation register B	DS22C1B	—	R/W	8	Undefined
0F657H	Display allocation register B	DS23C1B	—	R/W	8	Undefined
0F658H	Display allocation register B	DS24C1B	—	R/W	8	Undefined
0F659H	Display allocation register B	DS25C1B	—	R/W	8	Undefined
0F65AH	Display allocation register B	DS26C1B	—	R/W	8	Undefined
0F65BH	Display allocation register B	DS27C1B	—	R/W	8	Undefined
0F65CH	Display allocation register B	DS28C1B	—	R/W	8	Undefined
0F65DH	Display allocation register B	DS29C1B	—	R/W	8	Undefined
0F65EH	Display allocation register B	DS30C1B	—	R/W	8	Undefined
0F65FH	Display allocation register B	DS31C1B	—	R/W	8	Undefined
0F660H	Display allocation register B	DS32C1B	—	R/W	8	Undefined
0F661H	Display allocation register B	DS33C1B	—	R/W	8	Undefined
0F662H	Display allocation register B	DS34C1B	—	R/W	8	Undefined
0F663H	Display allocation register B	DS35C1B	—	R/W	8	Undefined
0F664H	Display allocation register B	DS36C1B	—	R/W	8	Undefined
0F665H	Display allocation register B	DS37C1B	—	R/W	8	Undefined
0F666H	Display allocation register B	DS38C1B	—	R/W	8	Undefined
0F667H	Display allocation register B	DS39C1B	—	R/W	8	Undefined
0F668H	Display allocation register B	DS40C1B	—	R/W	8	Undefined
0F669H	Display allocation register B	DS41C1B	—	R/W	8	Undefined
0F66AH	Display allocation register B	DS42C1B	—	R/W	8	Undefined
0F66BH	Display allocation register B	DS43C1B	—	R/W	8	Undefined
0F66CH	Display allocation register B	DS44C1B	—	R/W	8	Undefined
0F66DH	Display allocation register B	DS45C1B	—	R/W	8	Undefined
0F66EH	Display allocation register B	DS46C1B	—	R/W	8	Undefined
0F66FH	Display allocation register B	DS47C1B	—	R/W	8	Undefined
0F670H	Display allocation register B	DS48C1B	—	R/W	8	Undefined
0F671H	Display allocation register B	DS49C1B	—	R/W	8	Undefined
0F672H	Display allocation register B	DS50C1B	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F673H	Display allocation register B	DS51C1B	—	R/W	8	Undefined
0F674H	Display allocation register B	DS52C1B	—	R/W	8	Undefined
0F675H	Display allocation register B	DS53C1B	—	R/W	8	Undefined
0F676H	Display allocation register B	DS54C1B	—	R/W	8	Undefined
0F677H	Display allocation register B	DS55C1B	—	R/W	8	Undefined
0F678H	Display allocation register B	DS56C1B	—	R/W	8	Undefined
0F679H	Display allocation register B	DS57C1B	—	R/W	8	Undefined
0F67AH	Display allocation register B	DS58C1B	—	R/W	8	Undefined
0F67BH	Display allocation register B	DS59C1B	—	R/W	8	Undefined
0F67CH	Display allocation register B	DS60C1B	—	R/W	8	Undefined
0F67DH	Display allocation register B	DS61C1B	—	R/W	8	Undefined
0F67EH	Display allocation register B	DS62C1B	—	R/W	8	Undefined
0F67FH	Display allocation register B	DS63C1B	—	R/W	8	Undefined
0F680H	Display allocation register B	DS0C2B	—	R/W	8	Undefined
0F681H	Display allocation register B	DS1C2B	—	R/W	8	Undefined
0F682H	Display allocation register B	DS2C2B	—	R/W	8	Undefined
0F683H	Display allocation register B	DS3C2B	—	R/W	8	Undefined
0F684H	Display allocation register B	DS4C2B	—	R/W	8	Undefined
0F685H	Display allocation register B	DS5C2B	—	R/W	8	Undefined
0F686H	Display allocation register B	DS6C2B	—	R/W	8	Undefined
0F687H	Display allocation register B	DS7C2B	—	R/W	8	Undefined
0F688H	Display allocation register B	DS8C2B	—	R/W	8	Undefined
0F689H	Display allocation register B	DS9C2B	—	R/W	8	Undefined
0F68AH	Display allocation register B	DS10C2B	—	R/W	8	Undefined
0F68BH	Display allocation register B	DS11C2B	—	R/W	8	Undefined
0F68CH	Display allocation register B	DS12C2B	—	R/W	8	Undefined
0F68DH	Display allocation register B	DS13C2B	—	R/W	8	Undefined
0F68EH	Display allocation register B	DS14C2B	—	R/W	8	Undefined
0F68FH	Display allocation register B	DS15C2B	—	R/W	8	Undefined
0F690H	Display allocation register B	DS16C2B	—	R/W	8	Undefined
0F691H	Display allocation register B	DS17C2B	—	R/W	8	Undefined
0F692H	Display allocation register B	DS18C2B	—	R/W	8	Undefined
0F693H	Display allocation register B	DS19C2B	—	R/W	8	Undefined
0F694H	Display allocation register B	DS20C2B	—	R/W	8	Undefined
0F695H	Display allocation register B	DS21C2B	—	R/W	8	Undefined
0F696H	Display allocation register B	DS22C2B	—	R/W	8	Undefined
0F697H	Display allocation register B	DS23C2B	—	R/W	8	Undefined
0F698H	Display allocation register B	DS24C2B	—	R/W	8	Undefined
0F699H	Display allocation register B	DS25C2B	—	R/W	8	Undefined
0F69AH	Display allocation register B	DS26C2B	—	R/W	8	Undefined
0F69BH	Display allocation register B	DS27C2B	—	R/W	8	Undefined
0F69CH	Display allocation register B	DS28C2B	—	R/W	8	Undefined
0F69DH	Display allocation register B	DS29C2B	—	R/W	8	Undefined
0F69EH	Display allocation register B	DS30C2B	—	R/W	8	Undefined
0F69FH	Display allocation register B	DS31C2B	—	R/W	8	Undefined
0F6A0H	Display allocation register B	DS32C2B	—	R/W	8	Undefined
0F6A1H	Display allocation register B	DS33C2B	—	R/W	8	Undefined
0F6A2H	Display allocation register B	DS34C2B	—	R/W	8	Undefined
0F6A3H	Display allocation register B	DS35C2B	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F6A4H	Display allocation register B	DS36C2B	—	R/W	8	Undefined
0F6A5H	Display allocation register B	DS37C2B	—	R/W	8	Undefined
0F6A6H	Display allocation register B	DS38C2B	—	R/W	8	Undefined
0F6A7H	Display allocation register B	DS39C2B	—	R/W	8	Undefined
0F6A8H	Display allocation register B	DS40C2B	—	R/W	8	Undefined
0F6A9H	Display allocation register B	DS41C2B	—	R/W	8	Undefined
0F6AAH	Display allocation register B	DS42C2B	—	R/W	8	Undefined
0F6ABH	Display allocation register B	DS43C2B	—	R/W	8	Undefined
0F6ACH	Display allocation register B	DS44C2B	—	R/W	8	Undefined
0F6ADH	Display allocation register B	DS45C2B	—	R/W	8	Undefined
0F6AEH	Display allocation register B	DS46C2B	—	R/W	8	Undefined
0F6AFH	Display allocation register B	DS47C2B	—	R/W	8	Undefined
0F6B0H	Display allocation register B	DS48C2B	—	R/W	8	Undefined
0F6B1H	Display allocation register B	DS49C2B	—	R/W	8	Undefined
0F6B2H	Display allocation register B	DS50C2B	—	R/W	8	Undefined
0F6B3H	Display allocation register B	DS51C2B	—	R/W	8	Undefined
0F6B4H	Display allocation register B	DS52C2B	—	R/W	8	Undefined
0F6B5H	Display allocation register B	DS53C2B	—	R/W	8	Undefined
0F6B6H	Display allocation register B	DS54C2B	—	R/W	8	Undefined
0F6B7H	Display allocation register B	DS55C2B	—	R/W	8	Undefined
0F6B8H	Display allocation register B	DS56C2B	—	R/W	8	Undefined
0F6B9H	Display allocation register B	DS57C2B	—	R/W	8	Undefined
0F6BAH	Display allocation register B	DS58C2B	—	R/W	8	Undefined
0F6BBH	Display allocation register B	DS59C2B	—	R/W	8	Undefined
0F6BCH	Display allocation register B	DS60C2B	—	R/W	8	Undefined
0F6BDH	Display allocation register B	DS61C2B	—	R/W	8	Undefined
0F6BEH	Display allocation register B	DS62C2B	—	R/W	8	Undefined
0F6BFH	Display allocation register B	DS63C2B	—	R/W	8	Undefined
0F6C0H	Display allocation register B	DS0C3B	—	R/W	8	Undefined
0F6C1H	Display allocation register B	DS1C3B	—	R/W	8	Undefined
0F6C2H	Display allocation register B	DS2C3B	—	R/W	8	Undefined
0F6C3H	Display allocation register B	DS3C3B	—	R/W	8	Undefined
0F6C4H	Display allocation register B	DS4C3B	—	R/W	8	Undefined
0F6C5H	Display allocation register B	DS5C3B	—	R/W	8	Undefined
0F6C6H	Display allocation register B	DS6C3B	—	R/W	8	Undefined
0F6C7H	Display allocation register B	DS7C3B	—	R/W	8	Undefined
0F6C8H	Display allocation register B	DS8C3B	—	R/W	8	Undefined
0F6C9H	Display allocation register B	DS9C3B	—	R/W	8	Undefined
0F6CAH	Display allocation register B	DS10C3B	—	R/W	8	Undefined
0F6CBH	Display allocation register B	DS11C3B	—	R/W	8	Undefined
0F6CCH	Display allocation register B	DS12C3B	—	R/W	8	Undefined
0F6CDH	Display allocation register B	DS13C3B	—	R/W	8	Undefined
0F6CEH	Display allocation register B	DS14C3B	—	R/W	8	Undefined
0F6CFH	Display allocation register B	DS15C3B	—	R/W	8	Undefined
0F6D0H	Display allocation register B	DS16C3B	—	R/W	8	Undefined
0F6D1H	Display allocation register B	DS17C3B	—	R/W	8	Undefined
0F6D2H	Display allocation register B	DS18C3B	—	R/W	8	Undefined
0F6D3H	Display allocation register B	DS19C3B	—	R/W	8	Undefined
0F6D4H	Display allocation register B	DS20C3B	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F6D5H	Display allocation register B	DS21C3B	—	R/W	8	Undefined
0F6D6H	Display allocation register B	DS22C3B	—	R/W	8	Undefined
0F6D7H	Display allocation register B	DS23C3B	—	R/W	8	Undefined
0F6D8H	Display allocation register B	DS24C3B	—	R/W	8	Undefined
0F6D9H	Display allocation register B	DS25C3B	—	R/W	8	Undefined
0F6DAH	Display allocation register B	DS26C3B	—	R/W	8	Undefined
0F6DBH	Display allocation register B	DS27C3B	—	R/W	8	Undefined
0F6DCH	Display allocation register B	DS28C3B	—	R/W	8	Undefined
0F6DDH	Display allocation register B	DS29C3B	—	R/W	8	Undefined
0F6DEH	Display allocation register B	DS30C3B	—	R/W	8	Undefined
0F6DFH	Display allocation register B	DS31C3B	—	R/W	8	Undefined
0F6E0H	Display allocation register B	DS32C3B	—	R/W	8	Undefined
0F6E1H	Display allocation register B	DS33C3B	—	R/W	8	Undefined
0F6E2H	Display allocation register B	DS34C3B	—	R/W	8	Undefined
0F6E3H	Display allocation register B	DS35C3B	—	R/W	8	Undefined
0F6E4H	Display allocation register B	DS36C3B	—	R/W	8	Undefined
0F6E5H	Display allocation register B	DS37C3B	—	R/W	8	Undefined
0F6E6H	Display allocation register B	DS38C3B	—	R/W	8	Undefined
0F6E7H	Display allocation register B	DS39C3B	—	R/W	8	Undefined
0F6E8H	Display allocation register B	DS40C3B	—	R/W	8	Undefined
0F6E9H	Display allocation register B	DS41C3B	—	R/W	8	Undefined
0F6EAH	Display allocation register B	DS42C3B	—	R/W	8	Undefined
0F6EBH	Display allocation register B	DS43C3B	—	R/W	8	Undefined
0F6ECH	Display allocation register B	DS44C3B	—	R/W	8	Undefined
0F6EDH	Display allocation register B	DS45C3B	—	R/W	8	Undefined
0F6EEH	Display allocation register B	DS46C3B	—	R/W	8	Undefined
0F6EFH	Display allocation register B	DS47C3B	—	R/W	8	Undefined
0F6F0H	Display allocation register B	DS48C3B	—	R/W	8	Undefined
0F6F1H	Display allocation register B	DS49C3B	—	R/W	8	Undefined
0F6F2H	Display allocation register B	DS50C3B	—	R/W	8	Undefined
0F6F3H	Display allocation register B	DS51C3B	—	R/W	8	Undefined
0F6F4H	Display allocation register B	DS52C3B	—	R/W	8	Undefined
0F6F5H	Display allocation register B	DS53C3B	—	R/W	8	Undefined
0F6F6H	Display allocation register B	DS54C3B	—	R/W	8	Undefined
0F6F7H	Display allocation register B	DS55C3B	—	R/W	8	Undefined
0F6F8H	Display allocation register B	DS56C3B	—	R/W	8	Undefined
0F6F9H	Display allocation register B	DS57C3B	—	R/W	8	Undefined
0F6FAH	Display allocation register B	DS58C3B	—	R/W	8	Undefined
0F6FBH	Display allocation register B	DS59C3B	—	R/W	8	Undefined
0F6FCH	Display allocation register B	DS60C3B	—	R/W	8	Undefined
0F6FDH	Display allocation register B	DS61C3B	—	R/W	8	Undefined
0F6FEH	Display allocation register B	DS62C3B	—	R/W	8	Undefined
0F6FFH	Display allocation register B	DS63C3B	—	R/W	8	Undefined
0F700H	Display allocation register B	DS0C4B	—	R/W	8	Undefined
0F701H	Display allocation register B	DS1C4B	—	R/W	8	Undefined
0F702H	Display allocation register B	DS2C4B	—	R/W	8	Undefined
0F703H	Display allocation register B	DS3C4B	—	R/W	8	Undefined
0F704H	Display allocation register B	DS4C4B	—	R/W	8	Undefined
0F705H	Display allocation register B	DS5C4B	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F706H	Display allocation register B	DS6C4B	—	R/W	8	Undefined
0F707H	Display allocation register B	DS7C4B	—	R/W	8	Undefined
0F708H	Display allocation register B	DS8C4B	—	R/W	8	Undefined
0F709H	Display allocation register B	DS9C4B	—	R/W	8	Undefined
0F70AH	Display allocation register B	DS10C4B	—	R/W	8	Undefined
0F70BH	Display allocation register B	DS11C4B	—	R/W	8	Undefined
0F70CH	Display allocation register B	DS12C4B	—	R/W	8	Undefined
0F70DH	Display allocation register B	DS13C4B	—	R/W	8	Undefined
0F70EH	Display allocation register B	DS14C4B	—	R/W	8	Undefined
0F70FH	Display allocation register B	DS15C4B	—	R/W	8	Undefined
0F710H	Display allocation register B	DS16C4B	—	R/W	8	Undefined
0F711H	Display allocation register B	DS17C4B	—	R/W	8	Undefined
0F712H	Display allocation register B	DS18C4B	—	R/W	8	Undefined
0F713H	Display allocation register B	DS19C4B	—	R/W	8	Undefined
0F714H	Display allocation register B	DS20C4B	—	R/W	8	Undefined
0F715H	Display allocation register B	DS21C4B	—	R/W	8	Undefined
0F716H	Display allocation register B	DS22C4B	—	R/W	8	Undefined
0F717H	Display allocation register B	DS23C4B	—	R/W	8	Undefined
0F718H	Display allocation register B	DS24C4B	—	R/W	8	Undefined
0F719H	Display allocation register B	DS25C4B	—	R/W	8	Undefined
0F71AH	Display allocation register B	DS26C4B	—	R/W	8	Undefined
0F71BH	Display allocation register B	DS27C4B	—	R/W	8	Undefined
0F71CH	Display allocation register B	DS28C4B	—	R/W	8	Undefined
0F71DH	Display allocation register B	DS29C4B	—	R/W	8	Undefined
0F71EH	Display allocation register B	DS30C4B	—	R/W	8	Undefined
0F71FH	Display allocation register B	DS31C4B	—	R/W	8	Undefined
0F720H	Display allocation register B	DS32C4B	—	R/W	8	Undefined
0F721H	Display allocation register B	DS33C4B	—	R/W	8	Undefined
0F722H	Display allocation register B	DS34C4B	—	R/W	8	Undefined
0F723H	Display allocation register B	DS35C4B	—	R/W	8	Undefined
0F724H	Display allocation register B	DS36C4B	—	R/W	8	Undefined
0F725H	Display allocation register B	DS37C4B	—	R/W	8	Undefined
0F726H	Display allocation register B	DS38C4B	—	R/W	8	Undefined
0F727H	Display allocation register B	DS39C4B	—	R/W	8	Undefined
0F728H	Display allocation register B	DS40C4B	—	R/W	8	Undefined
0F729H	Display allocation register B	DS41C4B	—	R/W	8	Undefined
0F72AH	Display allocation register B	DS42C4B	—	R/W	8	Undefined
0F72BH	Display allocation register B	DS43C4B	—	R/W	8	Undefined
0F72CH	Display allocation register B	DS44C4B	—	R/W	8	Undefined
0F72DH	Display allocation register B	DS45C4B	—	R/W	8	Undefined
0F72EH	Display allocation register B	DS46C4B	—	R/W	8	Undefined
0F72FH	Display allocation register B	DS47C4B	—	R/W	8	Undefined
0F730H	Display allocation register B	DS48C4B	—	R/W	8	Undefined
0F731H	Display allocation register B	DS49C4B	—	R/W	8	Undefined
0F732H	Display allocation register B	DS50C4B	—	R/W	8	Undefined
0F733H	Display allocation register B	DS51C4B	—	R/W	8	Undefined
0F734H	Display allocation register B	DS52C4B	—	R/W	8	Undefined
0F735H	Display allocation register B	DS53C4B	—	R/W	8	Undefined
0F736H	Display allocation register B	DS54C4B	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F737H	Display allocation register B	DS55C4B	—	R/W	8	Undefined
0F738H	Display allocation register B	DS56C4B	—	R/W	8	Undefined
0F739H	Display allocation register B	DS57C4B	—	R/W	8	Undefined
0F73AH	Display allocation register B	DS58C4B	—	R/W	8	Undefined
0F73BH	Display allocation register B	DS59C4B	—	R/W	8	Undefined
0F73CH	Display allocation register B	DS60C4B	—	R/W	8	Undefined
0F73DH	Display allocation register B	DS61C4B	—	R/W	8	Undefined
0F73EH	Display allocation register B	DS62C4B	—	R/W	8	Undefined
0F73FH	Display allocation register B	DS63C4B	—	R/W	8	Undefined
0F740H	Display allocation register B	DS0C5B	—	R/W	8	Undefined
0F741H	Display allocation register B	DS1C5B	—	R/W	8	Undefined
0F742H	Display allocation register B	DS2C5B	—	R/W	8	Undefined
0F743H	Display allocation register B	DS3C5B	—	R/W	8	Undefined
0F744H	Display allocation register B	DS4C5B	—	R/W	8	Undefined
0F745H	Display allocation register B	DS5C5B	—	R/W	8	Undefined
0F746H	Display allocation register B	DS6C5B	—	R/W	8	Undefined
0F747H	Display allocation register B	DS7C5B	—	R/W	8	Undefined
0F748H	Display allocation register B	DS8C5B	—	R/W	8	Undefined
0F749H	Display allocation register B	DS9C5B	—	R/W	8	Undefined
0F74AH	Display allocation register B	DS10C5B	—	R/W	8	Undefined
0F74BH	Display allocation register B	DS11C5B	—	R/W	8	Undefined
0F74CH	Display allocation register B	DS12C5B	—	R/W	8	Undefined
0F74DH	Display allocation register B	DS13C5B	—	R/W	8	Undefined
0F74EH	Display allocation register B	DS14C5B	—	R/W	8	Undefined
0F74FH	Display allocation register B	DS15C5B	—	R/W	8	Undefined
0F750H	Display allocation register B	DS16C5B	—	R/W	8	Undefined
0F751H	Display allocation register B	DS17C5B	—	R/W	8	Undefined
0F752H	Display allocation register B	DS18C5B	—	R/W	8	Undefined
0F753H	Display allocation register B	DS19C5B	—	R/W	8	Undefined
0F754H	Display allocation register B	DS20C5B	—	R/W	8	Undefined
0F755H	Display allocation register B	DS21C5B	—	R/W	8	Undefined
0F756H	Display allocation register B	DS22C5B	—	R/W	8	Undefined
0F757H	Display allocation register B	DS23C5B	—	R/W	8	Undefined
0F758H	Display allocation register B	DS24C5B	—	R/W	8	Undefined
0F759H	Display allocation register B	DS25C5B	—	R/W	8	Undefined
0F75AH	Display allocation register B	DS26C5B	—	R/W	8	Undefined
0F75BH	Display allocation register B	DS27C5B	—	R/W	8	Undefined
0F75CH	Display allocation register B	DS28C5B	—	R/W	8	Undefined
0F75DH	Display allocation register B	DS29C5B	—	R/W	8	Undefined
0F75EH	Display allocation register B	DS30C5B	—	R/W	8	Undefined
0F75FH	Display allocation register B	DS31C5B	—	R/W	8	Undefined
0F760H	Display allocation register B	DS32C5B	—	R/W	8	Undefined
0F761H	Display allocation register B	DS33C5B	—	R/W	8	Undefined
0F762H	Display allocation register B	DS34C5B	—	R/W	8	Undefined
0F763H	Display allocation register B	DS35C5B	—	R/W	8	Undefined
0F764H	Display allocation register B	DS36C5B	—	R/W	8	Undefined
0F765H	Display allocation register B	DS37C5B	—	R/W	8	Undefined
0F766H	Display allocation register B	DS38C5B	—	R/W	8	Undefined
0F767H	Display allocation register B	DS39C5B	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F768H	Display allocation register B	DS40C5B	—	R/W	8	Undefined
0F769H	Display allocation register B	DS41C5B	—	R/W	8	Undefined
0F76AH	Display allocation register B	DS42C5B	—	R/W	8	Undefined
0F76BH	Display allocation register B	DS43C5B	—	R/W	8	Undefined
0F76CH	Display allocation register B	DS44C5B	—	R/W	8	Undefined
0F76DH	Display allocation register B	DS45C5B	—	R/W	8	Undefined
0F76EH	Display allocation register B	DS46C5B	—	R/W	8	Undefined
0F76FH	Display allocation register B	DS47C5B	—	R/W	8	Undefined
0F770H	Display allocation register B	DS48C5B	—	R/W	8	Undefined
0F771H	Display allocation register B	DS49C5B	—	R/W	8	Undefined
0F772H	Display allocation register B	DS50C5B	—	R/W	8	Undefined
0F773H	Display allocation register B	DS51C5B	—	R/W	8	Undefined
0F774H	Display allocation register B	DS52C5B	—	R/W	8	Undefined
0F775H	Display allocation register B	DS53C5B	—	R/W	8	Undefined
0F776H	Display allocation register B	DS54C5B	—	R/W	8	Undefined
0F777H	Display allocation register B	DS55C5B	—	R/W	8	Undefined
0F778H	Display allocation register B	DS56C5B	—	R/W	8	Undefined
0F779H	Display allocation register B	DS57C5B	—	R/W	8	Undefined
0F77AH	Display allocation register B	DS58C5B	—	R/W	8	Undefined
0F77BH	Display allocation register B	DS59C5B	—	R/W	8	Undefined
0F77CH	Display allocation register B	DS60C5B	—	R/W	8	Undefined
0F77DH	Display allocation register B	DS61C5B	—	R/W	8	Undefined
0F77EH	Display allocation register B	DS62C5B	—	R/W	8	Undefined
0F77FH	Display allocation register B	DS63C5B	—	R/W	8	Undefined
0F780H	Display allocation register B	DS0C6B	—	R/W	8	Undefined
0F781H	Display allocation register B	DS1C6B	—	R/W	8	Undefined
0F782H	Display allocation register B	DS2C6B	—	R/W	8	Undefined
0F783H	Display allocation register B	DS3C6B	—	R/W	8	Undefined
0F784H	Display allocation register B	DS4C6B	—	R/W	8	Undefined
0F785H	Display allocation register B	DS5C6B	—	R/W	8	Undefined
0F786H	Display allocation register B	DS6C6B	—	R/W	8	Undefined
0F787H	Display allocation register B	DS7C6B	—	R/W	8	Undefined
0F788H	Display allocation register B	DS8C6B	—	R/W	8	Undefined
0F789H	Display allocation register B	DS9C6B	—	R/W	8	Undefined
0F78AH	Display allocation register B	DS10C6B	—	R/W	8	Undefined
0F78BH	Display allocation register B	DS11C6B	—	R/W	8	Undefined
0F78CH	Display allocation register B	DS12C6B	—	R/W	8	Undefined
0F78DH	Display allocation register B	DS13C6B	—	R/W	8	Undefined
0F78EH	Display allocation register B	DS14C6B	—	R/W	8	Undefined
0F78FH	Display allocation register B	DS15C6B	—	R/W	8	Undefined
0F790H	Display allocation register B	DS16C6B	—	R/W	8	Undefined
0F791H	Display allocation register B	DS17C6B	—	R/W	8	Undefined
0F792H	Display allocation register B	DS18C6B	—	R/W	8	Undefined
0F793H	Display allocation register B	DS19C6B	—	R/W	8	Undefined
0F794H	Display allocation register B	DS20C6B	—	R/W	8	Undefined
0F795H	Display allocation register B	DS21C6B	—	R/W	8	Undefined
0F796H	Display allocation register B	DS22C6B	—	R/W	8	Undefined
0F797H	Display allocation register B	DS23C6B	—	R/W	8	Undefined
0F798H	Display allocation register B	DS24C6B	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F799H	Display allocation register B	DS25C6B	—	R/W	8	Undefined
0F79AH	Display allocation register B	DS26C6B	—	R/W	8	Undefined
0F79BH	Display allocation register B	DS27C6B	—	R/W	8	Undefined
0F79CH	Display allocation register B	DS28C6B	—	R/W	8	Undefined
0F79DH	Display allocation register B	DS29C6B	—	R/W	8	Undefined
0F79EH	Display allocation register B	DS30C6B	—	R/W	8	Undefined
0F79FH	Display allocation register B	DS31C6B	—	R/W	8	Undefined
0F7A0H	Display allocation register B	DS32C6B	—	R/W	8	Undefined
0F7A1H	Display allocation register B	DS33C6B	—	R/W	8	Undefined
0F7A2H	Display allocation register B	DS34C6B	—	R/W	8	Undefined
0F7A3H	Display allocation register B	DS35C6B	—	R/W	8	Undefined
0F7A4H	Display allocation register B	DS36C6B	—	R/W	8	Undefined
0F7A5H	Display allocation register B	DS37C6B	—	R/W	8	Undefined
0F7A6H	Display allocation register B	DS38C6B	—	R/W	8	Undefined
0F7A7H	Display allocation register B	DS39C6B	—	R/W	8	Undefined
0F7A8H	Display allocation register B	DS40C6B	—	R/W	8	Undefined
0F7A9H	Display allocation register B	DS41C6B	—	R/W	8	Undefined
0F7AAH	Display allocation register B	DS42C6B	—	R/W	8	Undefined
0F7ABH	Display allocation register B	DS43C6B	—	R/W	8	Undefined
0F7ACH	Display allocation register B	DS44C6B	—	R/W	8	Undefined
0F7ADH	Display allocation register B	DS45C6B	—	R/W	8	Undefined
0F7AEH	Display allocation register B	DS46C6B	—	R/W	8	Undefined
0F7AFH	Display allocation register B	DS47C6B	—	R/W	8	Undefined
0F7B0H	Display allocation register B	DS48C6B	—	R/W	8	Undefined
0F7B1H	Display allocation register B	DS49C6B	—	R/W	8	Undefined
0F7B2H	Display allocation register B	DS50C6B	—	R/W	8	Undefined
0F7B3H	Display allocation register B	DS51C6B	—	R/W	8	Undefined
0F7B4H	Display allocation register B	DS52C6B	—	R/W	8	Undefined
0F7B5H	Display allocation register B	DS53C6B	—	R/W	8	Undefined
0F7B6H	Display allocation register B	DS54C6B	—	R/W	8	Undefined
0F7B7H	Display allocation register B	DS55C6B	—	R/W	8	Undefined
0F7B8H	Display allocation register B	DS56C6B	—	R/W	8	Undefined
0F7B9H	Display allocation register B	DS57C6B	—	R/W	8	Undefined
0F7BAH	Display allocation register B	DS58C6B	—	R/W	8	Undefined
0F7BBH	Display allocation register B	DS59C6B	—	R/W	8	Undefined
0F7BCH	Display allocation register B	DS60C6B	—	R/W	8	Undefined
0F7BDH	Display allocation register B	DS61C6B	—	R/W	8	Undefined
0F7BEH	Display allocation register B	DS62C6B	—	R/W	8	Undefined
0F7BFH	Display allocation register B	DS63C6B	—	R/W	8	Undefined
0F7C0H	Display allocation register B	DS0C7B	—	R/W	8	Undefined
0F7C1H	Display allocation register B	DS1C7B	—	R/W	8	Undefined
0F7C2H	Display allocation register B	DS2C7B	—	R/W	8	Undefined
0F7C3H	Display allocation register B	DS3C7B	—	R/W	8	Undefined
0F7C4H	Display allocation register B	DS4C7B	—	R/W	8	Undefined
0F7C5H	Display allocation register B	DS5C7B	—	R/W	8	Undefined
0F7C6H	Display allocation register B	DS6C7B	—	R/W	8	Undefined
0F7C7H	Display allocation register B	DS7C7B	—	R/W	8	Undefined
0F7C8H	Display allocation register B	DS8C7B	—	R/W	8	Undefined
0F7C9H	Display allocation register B	DS9C7B	—	R/W	8	Undefined

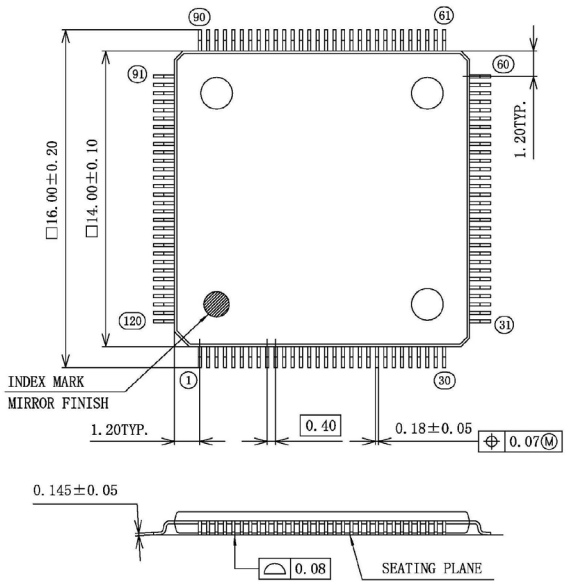
Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F7CAH	Display allocation register B	DS10C7B	—	R/W	8	Undefined
0F7CBH	Display allocation register B	DS11C7B	—	R/W	8	Undefined
0F7CCH	Display allocation register B	DS12C7B	—	R/W	8	Undefined
0F7CDH	Display allocation register B	DS13C7B	—	R/W	8	Undefined
0F7CEH	Display allocation register B	DS14C7B	—	R/W	8	Undefined
0F7CFH	Display allocation register B	DS15C7B	—	R/W	8	Undefined
0F7D0H	Display allocation register B	DS16C7B	—	R/W	8	Undefined
0F7D1H	Display allocation register B	DS17C7B	—	R/W	8	Undefined
0F7D2H	Display allocation register B	DS18C7B	—	R/W	8	Undefined
0F7D3H	Display allocation register B	DS19C7B	—	R/W	8	Undefined
0F7D4H	Display allocation register B	DS20C7B	—	R/W	8	Undefined
0F7D5H	Display allocation register B	DS21C7B	—	R/W	8	Undefined
0F7D6H	Display allocation register B	DS22C7B	—	R/W	8	Undefined
0F7D7H	Display allocation register B	DS23C7B	—	R/W	8	Undefined
0F7D8H	Display allocation register B	DS24C7B	—	R/W	8	Undefined
0F7D9H	Display allocation register B	DS25C7B	—	R/W	8	Undefined
0F7DAH	Display allocation register B	DS26C7B	—	R/W	8	Undefined
0F7DBH	Display allocation register B	DS27C7B	—	R/W	8	Undefined
0F7DCH	Display allocation register B	DS28C7B	—	R/W	8	Undefined
0F7DDH	Display allocation register B	DS29C7B	—	R/W	8	Undefined
0F7DEH	Display allocation register B	DS30C7B	—	R/W	8	Undefined
0F7DFH	Display allocation register B	DS31C7B	—	R/W	8	Undefined
0F7E0H	Display allocation register B	DS32C7B	—	R/W	8	Undefined
0F7E1H	Display allocation register B	DS33C7B	—	R/W	8	Undefined
0F7E2H	Display allocation register B	DS34C7B	—	R/W	8	Undefined
0F7E3H	Display allocation register B	DS35C7B	—	R/W	8	Undefined
0F7E4H	Display allocation register B	DS36C7B	—	R/W	8	Undefined
0F7E5H	Display allocation register B	DS37C7B	—	R/W	8	Undefined
0F7E6H	Display allocation register B	DS38C7B	—	R/W	8	Undefined
0F7E7H	Display allocation register B	DS39C7B	—	R/W	8	Undefined
0F7E8H	Display allocation register B	DS40C7B	—	R/W	8	Undefined
0F7E9H	Display allocation register B	DS41C7B	—	R/W	8	Undefined
0F7EAH	Display allocation register B	DS42C7B	—	R/W	8	Undefined
0F7EBH	Display allocation register B	DS43C7B	—	R/W	8	Undefined
0F7ECH	Display allocation register B	DS44C7B	—	R/W	8	Undefined
0F7EDH	Display allocation register B	DS45C7B	—	R/W	8	Undefined
0F7EEH	Display allocation register B	DS46C7B	—	R/W	8	Undefined
0F7EFH	Display allocation register B	DS47C7B	—	R/W	8	Undefined
0F7F0H	Display allocation register B	DS48C7B	—	R/W	8	Undefined
0F7F1H	Display allocation register B	DS49C7B	—	R/W	8	Undefined
0F7F2H	Display allocation register B	DS50C7B	—	R/W	8	Undefined
0F7F3H	Display allocation register B	DS51C7B	—	R/W	8	Undefined
0F7F4H	Display allocation register B	DS52C7B	—	R/W	8	Undefined
0F7F5H	Display allocation register B	DS53C7B	—	R/W	8	Undefined
0F7F6H	Display allocation register B	DS54C7B	—	R/W	8	Undefined
0F7F7H	Display allocation register B	DS55C7B	—	R/W	8	Undefined
0F7F8H	Display allocation register B	DS56C7B	—	R/W	8	Undefined
0F7F9H	Display allocation register B	DS57C7B	—	R/W	8	Undefined
0F7FAH	Display allocation register B	DS58C7B	—	R/W	8	Undefined

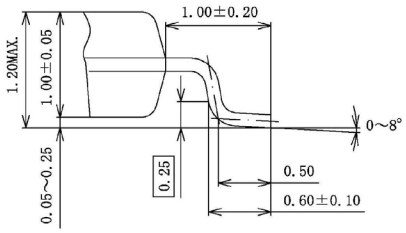
Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F7FBH	Display allocation register B	DS59C7B	—	R/W	8	Undefined
0F7FCH	Display allocation register B	DS60C7B	—	R/W	8	Undefined
0F7FDH	Display allocation register B	DS61C7B	—	R/W	8	Undefined
0F7FEH	Display allocation register B	DS62C7B	—	R/W	8	Undefined
0F7FFH	Display allocation register B	DS63C7B	—	R/W	8	Undefined

Appendix B Package Dimensions

(Unit: mm)

TQFP120-P-1414-0.40-K





Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Plating (≥5μm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	2/Oct. 21, 2009

LAPIS Semiconductor Co.,Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Appendix C Electrical Characteristics

● Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 2	AV_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 3*[1]	V_{PP}	Ta = 25°C	–0.3 to +9.5	V
Power supply voltage 4	V_{DDL}	Ta = 25°C	–0.3 to +3.6	V
Power supply voltage 5	V_{DDX}	Ta = 25°C	–0.3 to +3.6	V
Power supply voltage 6	V_{L1}	Ta = 25°C	–0.3 to +1.75	V
Power supply voltage 7	V_{L2}	Ta = 25°C	–0.3 to +3.5	V
Power supply voltage 8	V_{L3}	Ta = 25°C	–0.3 to +5.25	V
Power supply voltage 9	V_{L4}	Ta = 25°C	–0.3 to +7.0	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port3–A, Ta = 25°C	–12 to +11	mA
Output current 2	I_{OUT2}	Port2, Ta = 25°C	–12 to +20	mA
Power dissipation	PD	Ta = 25°C	1.25	W
Storage temperature	T_{STG}	—	–55 to +150	°C

*[1]: ML610Q421/ML610Q422 only

● Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	ML610Q421, ML610Q422, ML610421,ML610422	−20 to +70	°C
		ML610Q421P, ML610Q422P ML610421P,ML610422P	−40 to +85	
Operating voltage	V_{DD}	—	1.1 to 3.6	V
	AV_{DD}	—	2.2 to 3.6	
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.1 to 3.6V	30k to 36k	Hz
		V_{DD} = 1.3 to 3.6V	30k to 650k	
		V_{DD} = 1.8 to 3.6V	30k to 4.2M	
Low-speed crystal oscillation frequency	f_{XTL}	—	32.768k	Hz
Low-speed crystal oscillation external capacitor	C_{DL}	—	0 to 12	pF
	C_{GL}	—	0 to 12	
High-speed crystal/ceramic oscillation frequency	f_{XTH}	—	4.0M / 4.096M	Hz
High-speed crystal oscillation external capacitor	C_{DH}	—	24	pF
	C_{GH}	—	24	
Capacitor externally connected to V_{DDL} pin	C_{L0}	—	1.0±30%	μF
	C_{L1}	—	0.1±30%	
Capacitor externally connected to V_{DDX} pin	C_X	—	0.1±30%	μF
Capacitors externally connected to $V_{L1, 2, 3, 4}$ pins	$C_{a, b, c, d}$	—	1.0±30%	μF
Capacitors externally connected across C1 and C2 pins and across C3 and C4 pins	C_{12}, C_{34}	—	1.0±30%	μF

● Operating Conditions of Flash Memory (ML610Q421/ML610Q421 only)

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At erase/program	0 to +40	°C
Operating voltage	V_{DD}	At erase/program[*1]	2.75 to 3.6	V
	V_{DDL}	At erase/program[*1]	2.5 to 2.75	
	V_{PP}	At erase/program[*1]	7.7 to 8.3	
Erase/program cycles	C_{EP}	—	80	cycles
Data retention	Y_{DR}	—	10	years

[*1]: In addition the power supply to VDD pin and VPP pin, within the range 2.5V to 2.75V has to be supplied to VDDL pin when programming and eraseing Flash ROM.

● DC Characteristics (1/6)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified) (1/6)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
500kHz RC oscillation frequency	f_{RC}	V_{DD} = 1.3 to 3.6V	Ta = 25°C	Typ. –10%	500	Typ. +10%	kHz	1
			Ta = –20 to +70°C	Typ. –25%	500	Typ. +25%	kHz	
			Ta = –40 to +85°C	Typ. –45%	500	Typ. +45%	kHz	
PLL oscillation frequency*4	f_{PLL}	LSCLK = 32.768kHz V_{DD} = 1.8 to 3.6V		-2.5%	8.192	+2.5%	MHz	
Low-speed crystal oscillation start time*2	T_{XTL}	—		—	0.3	2	s	
500kHz RC oscillation start time	T_{RC}	—		—	50	500	μs	
High-speed crystal oscillation start time*3	T_{XTH}	V_{DD} = 1.8 to 3.6V		—	2	20	ms	
PLL oscillation start time	T_{PLL}	V_{DD} = 1.8 to 3.6V		—	1	10		
Low-speed oscillation stop detect time*1	T_{STOP}	—		0.2	3	20		
Reset pulse width	P_{RST}	—		200	—	—	μs	
Reset noise elimination pulse width	P_{NRST}	—		—	—	0.3		
Power-on reset activation power rise time	T_{POR}	—		—	—	10	ms	

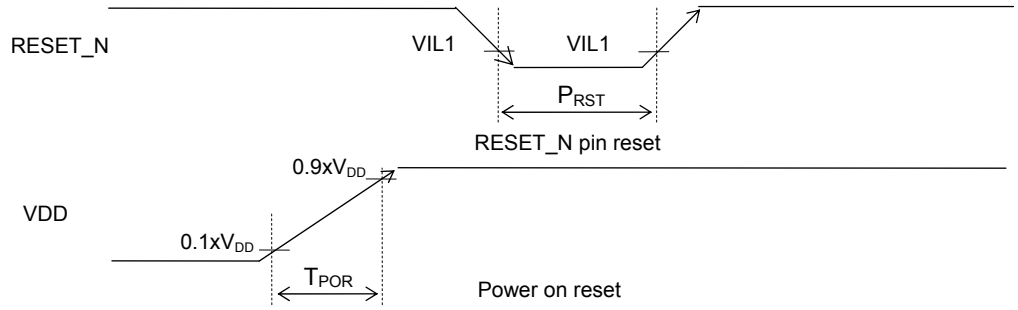
*1: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.

*2 : Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance C_{GL}/C_{DL}=0pF.

*3 : Use 4.096MHz Crystal Oscillator HC49SFWB (Kyocera).

*4 : 1024 clock average.

RESET



● DC Characteristics (2/6)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified) (2/6)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
V_{L1} voltage	V_{L1}	V_{DD} = 3.0V, Tj = 25°C	CN4–0 = 00H	0.89	0.94	0.99	V	1
			CN4–0 = 01H	0.91	0.96	1.01		
			CN4–0 = 02H	0.93	0.98	1.03		
			CN4–0 = 03H	0.95	1.00	1.05		
			CN4–0 = 04H	0.97	1.02	1.07		
			CN4–0 = 05H	0.99	1.04	1.09		
			CN4–0 = 06H	1.01	1.06	1.11		
			CN4–0 = 07H	1.03	1.08	1.13		
			CN4–0 = 08H	1.05	1.10	1.15		
			CN4–0 = 09H	1.07	1.12	1.17		
			CN4–0 = 0AH	1.09	1.14	1.19		
			CN4–0 = 0BH	1.11	1.16	1.21		
			CN4–0 = 0CH	1.13	1.18	1.23		
			CN4–0 = 0DH	1.15	1.20	1.25		
			CN4–0 = 0EH	1.17	1.22	1.27		
			CN4–0 = 0FH	1.19	1.24	1.29		
			CN4–0 = 10H	1.21	1.26	1.31		
			CN4–0 = 11H	1.23	1.28	1.33		
			CN4–0 = 12H	1.25	1.30	1.35		
			CN4–0 = 13H	1.27	1.32	1.37		
			CN4–0 = 14H *1	1.29	1.34	1.39		
			CN4–0 = 15H *1	1.31	1.36	1.41		
			CN4–0 = 16H *1	1.33	1.38	1.43		
			CN4–0 = 17H *1	1.35	1.40	1.45		
			CN4–0 = 18H *1	1.37	1.42	1.47		
			CN4–0 = 19H *1	1.39	1.44	1.49		
			CN4–0 = 1AH *1	1.41	1.46	1.51		
			CN4–0 = 1BH *1	1.43	1.48	1.53		
			CN4–0 = 1CH *1	1.45	1.50	1.55		
			CN4–0 = 1DH *1	1.47	1.52	1.57		
			CN4–0 = 1EH *1	1.49	1.54	1.59		
			CN4–0 = 1FH *1	1.51	1.56	1.61		
V_{L1} temperature deviation	ΔV_{L1}	V_{DD} = 3.0V		—	–1.5	—	mV/°C	
V_{L1} voltage dependency	ΔV_{L1}	V_{DD} = 1.3 to 3.6V		—	5	20	mV/V	
V_{L2} voltage *2	V_{L2}	V_{DD} = 3.0V, Tj = 25°C, 500kΩ load (V_{L4}–V_{SS})		Typ. –10%	V_{L1}×2	Typ. +4%	V	
V_{L3} voltage *2	V_{L3}	V_{DD} = 3.0V, Tj = 25°C, 500kΩ load (V_{L4}–V_{SS})	1/3 bias	Typ. –10%	V_{L1}×2	Typ. +4%		
			1/4 bias		V_{L1}×3			
V_{L4} voltage *2	V_{L4}		1/3 bias	Typ. –10%	V_{L1}×3	Typ. +5%		
			1/4 bias		V_{L1}×4			
LCD bias voltage generation time	T_{BIAS}	—		—	—	600	ms	

*1: When using 1/4 bias, the V_{L1} voltage is set to typ. 1.32 V (same voltage as in CN4–0 = 13H).

*2: Boost clock is 2kHz(initial) for the bias generation. C12=C34=1uF.

● DC Characteristics (3/6)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified) (3/6)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
BLD threshold voltage	V_{BLD}	V_{DD} = 1.35 to 3.6V	LD2–0 = 0H	Typ. –2%	1.35	Typ. +2%	V	1
			LD2–0 = 1H		1.4			
			LD2–0 = 2H		1.45			
			LD2–0 = 3H		1.5			
			LD2–0 = 4H		1.6			
			LD2–0 = 5H		1.7			
			LD2–0 = 6H		1.8			
			LD2–0 = 7H		1.9			
			LD2–0 = 8H		2.0			
			LD2–0 = 9H		2.1			
			LD2–0 = 0AH		2.2			
			LD2–0 = 0BH		2.3			
			LD2–0 = 0CH		2.4			
			LD2–0 = 0DH		2.5			
			LD2–0 = 0EH		2.7			
			LD2–0 = 0FH		2.9			
BLD threshold voltage temperature deviation	ΔV_{BLD}	V_{DD} = 1.35 to 3.6V		—	0.1	—	%/°C	
Supply current 1*6	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	Ta = 25°C	—	0.15	0.50	μA	
			Ta = -20 to +70°C	—	—	2.50		
			Ta = -40 to +85°C	—	—	5.00		
Supply current 2*6	IDD2	CPU: In HALT state (LTBC, WDT: Operating*3*5). High-speed oscillation: Stopped. LCD/BIAS circuits: Stopped.	Ta = 25°C	—	0.5	1.3	μA	
			Ta = -20 to +70°C	—	—	3.5		
			Ta = -40 to +85°C	—	—	6.0		
Supply current 3*6	IDD3	CPU: In 32.768kHz operating state.*1*3 High-speed oscillation: Stopped. LCD/BIAS circuits: Operating.*2	Ta = 25°C	—	5	7	μA	
			Ta = -20 to +70°C	—	—	12		
			Ta = -40 to +85°C	—	—	16		
Supply current 4*6	IDD4	CPU: In 500kHz CR operating state. LCD/BIAS circuits: Operating.*2	Ta = 25°C	—	70	85	μA	
			Ta = -20 to +70°C	—	—	100		
			Ta = -40 to +85°C	—	—	120		
Supply current 5*6	IDD5	CPU: In 4.096MHz operating state.*2*3 PLL: In oscillating state. LCD/BIAS circuits: Operating. *2 V_{DD} = 1.8 to 3.6V	Ta = 25°C	—	0.8	1.0	mA	
			Ta = -20 to +70°C	—	—	1.2		
			Ta = -40 to +85°C	—	—	1.2		

Supply current 6*6	IDD6	CPU: In 4.096MHz operating state.*2 PLL: In oscillating state. *3*4 A/D: In operating state. LCD/BIAS circuits: Operating. *2 V_{DD} = AV_{DD} = 3.0V	Ta = 25°C	—	1.5	1.6	mA	
			Ta = -20 to +70°C	—	—	2.5		
			Ta = -40 to +85°C	—	—	2.5		

*1 : CPU operating rate is 100% (No HALT state).
*2 : All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*3 : Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance C_{GL}/C_{DL}=0pF.
*4 : Use 4.096MHz Crystal Oscillator HC49SFWB (Kyocera).
*5 : Significant bits of BLKCON0~BLKCON4 registers are all "1".
*6 : ML610Q421/ML610Q422 only

● DC Characteristics (4/6) (ML610421/ML610422 only)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified) (4/6)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	Ta = 25°C	—	0.15	0.40	μA	1
			Ta = -20 to +70°C	—	—	2.0		
			Ta = -40 to +85°C	—	—	4.0		
Supply current 2	IDD2	CPU: In HALT state (LTBC, WDT: Operating*3*5). High-speed oscillation: Stopped. LCD/BIAS circuits: Stopped.	Ta = 25°C	—	0.5	1.1	μA	
			Ta = -20 to +70°C	—	—	3.0		
			Ta = -40 to +85°C	—	—	4.5		
Supply current 3	IDD3	CPU: In 32.768kHz operating state.*1*3 High-speed oscillation: Stopped. LCD/BIAS circuits: Operating.*2	Ta = 25°C	—	4	6	μA	
			Ta = -20 to +70°C	—	—	9		
			Ta = -40 to +85°C	—	—	10		
Supply current 4	IDD4	CPU: In 500kHz CR operating state. LCD/BIAS circuits: Operating.*2	Ta = 25°C	—	60	75	μA	
			Ta = -20 to +70°C	—	—	95		
			Ta = -40 to +85°C	—	—	100		
Supply current 5	IDD5	CPU: In 4.096MHz operating state.*2*3 PLL: In oscillating state. LCD/BIAS circuits: Operating. *2 V_{DD} = 1.8 to 3.6V	Ta = 25°C	—	0.6	0.75	mA	
			Ta = -20 to +70°C	—	—	0.85		
			Ta = -40 to +85°C	—	—	0.85		
Supply current 6	IDD6	CPU: In 4.096MHz operating state.*2 PLL: In oscillating state. *3*4 A/D: In operating state. LCD/BIAS circuits: Operating. *2 V_{DD} = AV_{DD} = 3.0V	Ta = 25°C	—	0.8	0.9	mA	
			Ta = -20 to +70°C	—	—	1.0		
			Ta = -40 to +85°C	—	—	1.0		

*1 : CPU operating rate is 100% (No HALT state).

*2 : All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

*3 : Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance C_{GL}/C_{DL}=0pF.

*4 : Use 4.096MHz Crystal Oscillator HC49SFWB (Kyocera).

*5 : Significant bits of BLKCON0~BLKCON4 registers are all "1".

● DC Characteristics (5/6)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified) (5/6)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage 1 (P20–P22/2nd function is selected) (P30–P35) (P40–P47) (PA0–PA7)*1	VOH1	IOH1 = –0.5mA, V_{DD} = 1.8 to 3.6V	V_{DD} –0.5	—	—	V	2
		IOH1 = -0.1mA, V_{DD} = 1.3 to 3.6V	V_{DD} –0.3	—	—		
		IOH1 = -0.03mA, V_{DD} = 1.1 to 3.6V	V_{DD} –0.3	—	—		
	VOL1	IOL1 = +0.5mA, V_{DD} = 1.8 to 3.6V	—	—	0.5		
		IOL1 = +0.1mA, V_{DD} = 1.3 to 3.6V	—	—	0.5		
		IOL1 = +0.03mA, V_{DD} = 1.1 to 3.6V	—	—	0.3		
Output voltage 2 (P20–P22/2nd function is Not selected))	VOH2	IOH1 = –0.5mA, V_{DD} = 1.8 to 3.6V	V_{DD} –0.5	—	—		
		IOH1 = -0.1mA, V_{DD} = 1.3 to 3.6V	V_{DD} –0.3	—	—		
		IOH1 = -0.03mA, V_{DD} = 1.1 to 3.6V	V_{DD} –0.3	—	—		
	VOL2	IOL2 = +5mA, V_{DD} = 1.8 to 3.6V	—	—	0.5		
Output voltage 3 (P40–P41)	VOL3	IOL3 = +3mA, V_{DD} = 2.0 to 3.6V (when I^2C mode is selected)	—	—	0.4		
Output voltage 4 (COM0–7) (COM8-15)*2 (SEG0–49)	VOH4	IOH4 = –0.2mA, VL1=1.2V	V_{L4} –0.2	—	—		
	VOMH4	IOMH4 = +0.2mA, VL1=1.2V	—	—	V_{L3} +0.2		
	VOMH4S	IOMH4S = –0.2mA, VL1=1.2V	V_{L3} –0.2	—	—		
	VOM4	IOM4 = +0.2mA, VL1=1.2V	—	—	V_{L2} +0.2		
	VOM4S	IOM4S = –0.2mA, VL1=1.2V	V_{L2} –0.2	—	—		
	VOML4	IOML4 = +0.2mA, VL1=1.2V	—	—	V_{L1} +0.2		
	VOML4S	IOML4S = –0.2mA, VL1=1.2V	V_{L1} –0.2	—	—		
	VOL4	IOL4 = +0.2mA, VL1=1.2V	—	—	0.2		
Output leakage (P20–P22) (P30–P35) (P40–P47) (PA0–PA7)*1	IOOH	VOH = V_{DD} (in high-impedance state)	—	—	1	µA	3
	IOOL	VOL = V_{SS} (in high-impedance state)	–1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V_{DD}	0	—	1	µA	4
	IIL1	VIL1 = V_{SS}, V_{DD} = 1.8 to 3.6V	–600	–300	–20		
		VIL1 = V_{SS}, V_{DD} = 1.3 to 3.6V	–600	–300	-10		
		VIL1 = V_{SS}, V_{DD} = 1.1 to 3.6V	–600	–300	-2		
Input current 1 (TEST)	IIH1	VIH1 = V_{DD}, V_{DD} = 1.8 to 3.6V	20	300	600		
		VIH1 = V_{DD}, V_{DD} = 1.3 to 3.6V	10	300	600		
		VIH1 = V_{DD}, V_{DD} = 1.1 to 3.6V	2	300	600		
	IIL1	VIL1 = V_{ss}	-1	—	—		

Input current 2 (NMI) (P00–P03) (P10–P11) (P30–P35) (P40–P47) (PA0–PA7)*1	IIH2	VIH2 = V_{DD} (when pulled-down)	V_{DD} = 1.8 to 3.6V	2	30	200	μA	4
			V_{DD} = 1.3 to 3.6V	0.2	30	200		
			V_{DD} = 1.1 to 3.6V	0.01	30	200		
	IIL2	VIL2 = V_{SS} (when pulled-up)	V_{DD} = 1.8 to 3.6V	–200	–30	–2		
			V_{DD} = 1.3 to 3.6V	–200	–30	-0.2		
			V_{DD} = 1.1 to 3.6V	–200	–30	-0.01		
	IIH2Z	VIH2 = V_{DD} (in high-impedance state)		—	—	1		
	IIL2Z	VIL2 = V_{SS} (in high-impedance state)		–1	—	—		

*1: ML610Q421/ML610421 only
*2: ML610Q422/ML610422 only

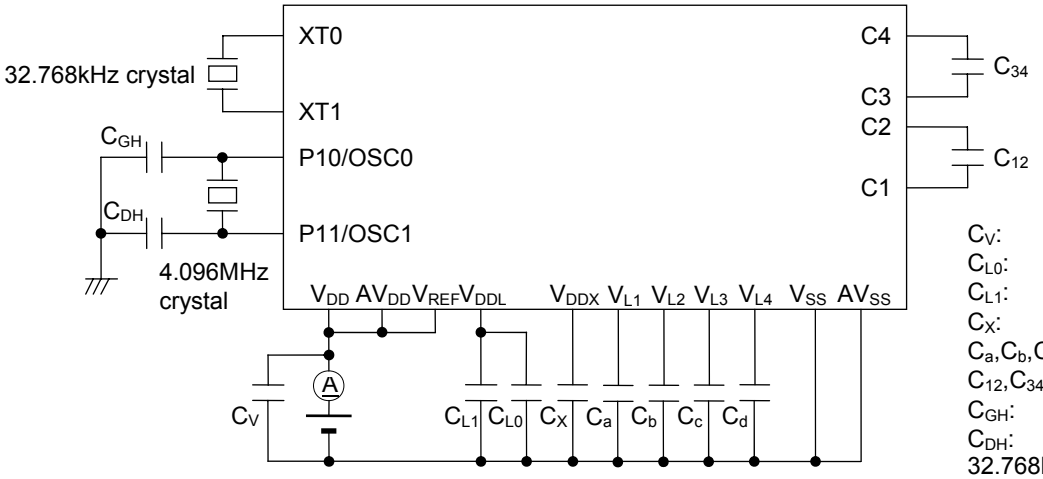
● DC Characteristics (6/6)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P Version, unless otherwise specified) (6/6)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST) (NMI) (P00–P03) (P10–P11) (P31–P35) (P40–P43) (P45–P47) (PA0–PA7)*1	VIH1	V_{DD} = 1.3 to 3.6V	0.7 ×V_{DD}	—	V_{DD}	V	5
		V_{DD} = 1.1 to 3.6V	0.7 ×V_{DD}	—	V_{DD}		
	VIL1	V_{DD} = 1.3 to 3.6V	0	—	0.3 ×V_{DD}		
		V_{DD} = 1.1 to 3.6V	0	—	0.2 ×V_{DD}		
Input voltage 2 (P30, P44)	VIH2	—	0.7 ×V_{DD}	—	V_{DD}		
	VIL2	—	0	—	0.3 ×V_{DD}		
Input pin capacitance (NMI) (P00–P03) (P10–P11) (P30–P35) (P40–P47) (PA0–PA7)*1	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	5	pF	—

*1: ML610Q421/ML610421 only

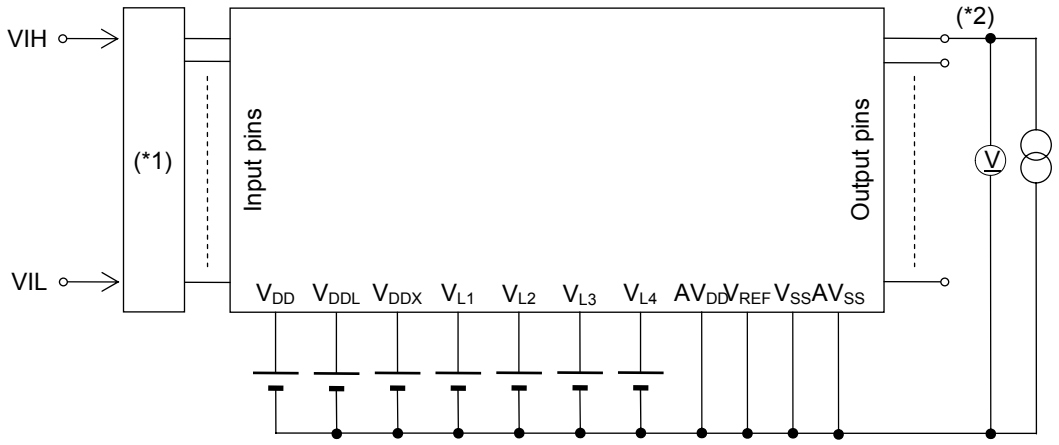
Measuring circuit 1



C_V:	1μF
C_{L0}:	1μF
C_{L1}:	0.1μF
C_X:	0.1μF
C_a,C_b,C_c,C_d:	1μF
C_{12},C_{34}:	1μF
C_{GH}:	24pF
C_{DH}:	24pF

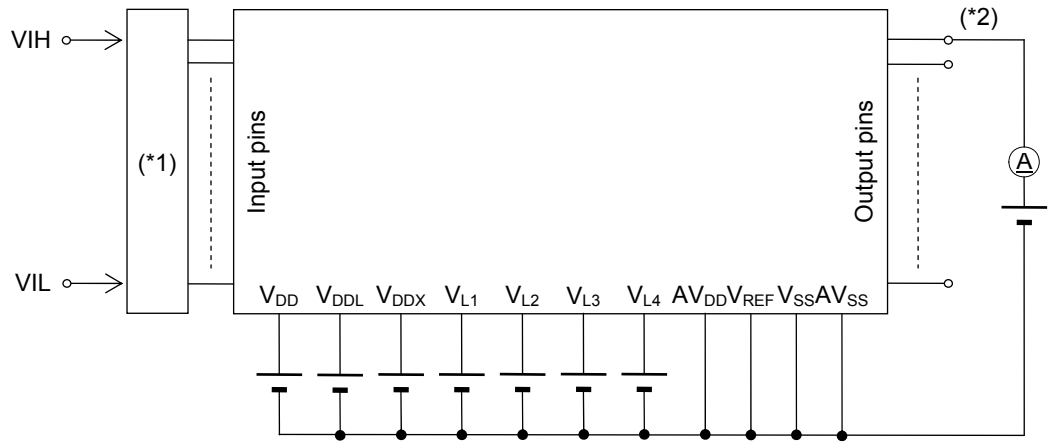
32.768kHz crystal:
C-001R (Epson Toyocom)
4.096MHz crystal:
HC49SFWB (Kyocera)

Measuring circuit 2



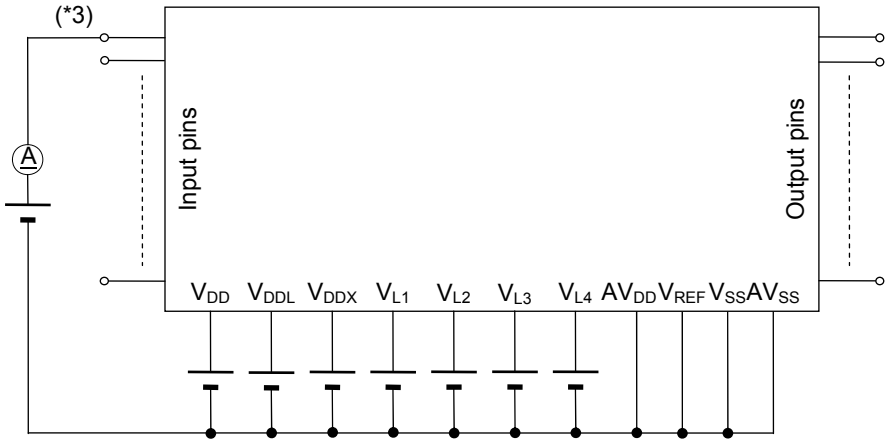
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

Measuring circuit 3



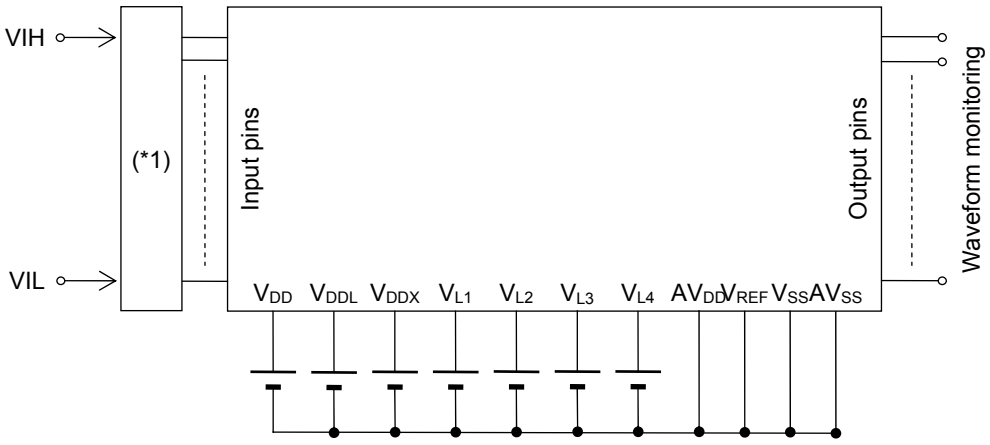
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

Measuring circuit 4



*3: Measured at the specified output pins.

Measuring circuit 5

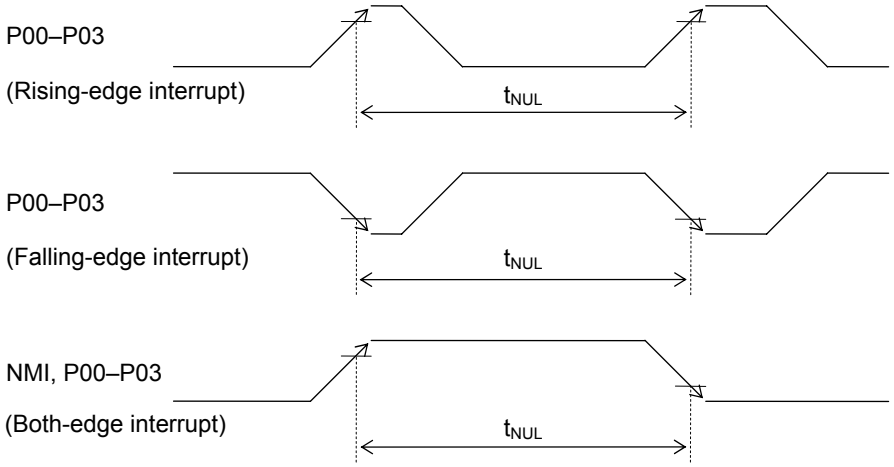


*1: Input logic circuit to determine the specified measuring conditions.

● AC Characteristics (External Interrupt)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = −20 to +70°C, Ta = −40 to +85°C for P Version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	μs

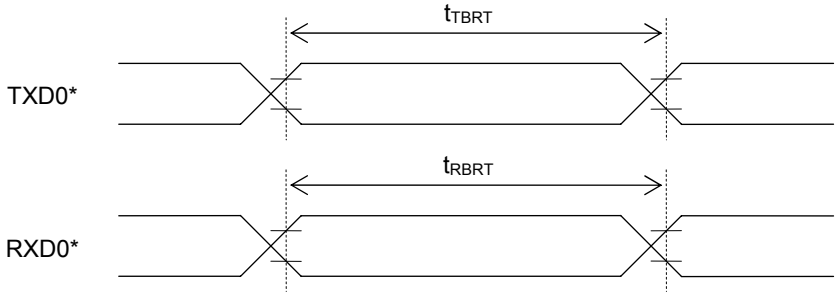


● AC Characteristics (UART)

(V_{DD} = 1.3 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = −20 to +70°C, Ta = −40 to +85°C for P Version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT*[1]	—	s
Receive baud rate	t_{RBRT}	—	BRT*[1] −3%	BRT*[1]	BRT*[1] +3%	s

*[1]: Baud rate period (including the error of the clock frequency selected) set with the UART baud rate register (UA0BRTL,H) and the UART mode register 0 (UA0MOD0).



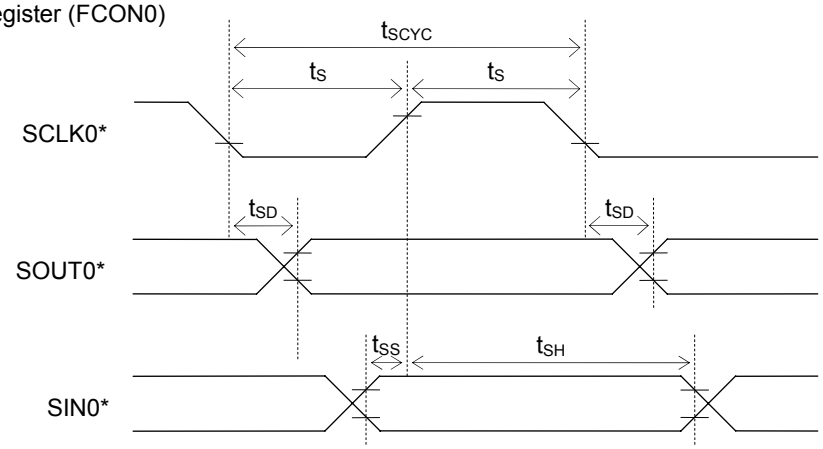
*: Indicates the secondary function of the port.

● AC Characteristics (Synchronous Serial Port)

(V_{DD} = 1.3 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = −20 to +70°C, Ta = −40 to +85°C for P Version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	t_{SCYC}	When RC oscillation is active*2 (V_{DD} = 1.3 to 3.6V)	10	—	—	μs
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	1	—	—	μs
SCLK output cycle (master mode)	t_{SCYC}	—	—	SCLK*1	—	s
SCLK input pulse width (slave mode)	t_{SW}	When RC oscillation is active*2 (V_{DD} = 1.3 to 3.6V)	4	—	—	μs
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	0.4	—	—	μs
SCLK output pulse width (master mode)	t_{SW}	—	SCLK*1 ×0.4	SCLK*1 ×0.5	SCLK*1 ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	When RC oscillation is active*2 (V_{DD} = 1.3 to 3.6V)	—	—	500	ns
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	—	—	240	
SOUT output delay time (master mode)	t_{SD}	When RC oscillation is active*2 (V_{DD} = 1.3 to 3.6V)	—	—	500	ns
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	—	—	240	
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (master mode)	t_{SS}	When RC oscillation is active*2 (V_{DD} = 1.3 to 3.6V)	500	—	—	ns
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	240	—	—	
SIN input hold time	t_{SH}	When RC oscillation is active*2 (V_{DD} = 1.3 to 3.6V)	300	—	—	ns
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	80	—	—	

*1: Clock period selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)
*2: When RC oscillation is selected with OSCM1–0 of the frequency control register (FCON0)
*3: When Crystal/ceramic oscillation, built-in PLL oscillation, or external clock input is selected with OSCM1–0 of the frequency control register (FCON0)



*: Indicates the secondary function of the port.

● AC Characteristics (I^2C Bus Interface: Standard Mode 100kHz)

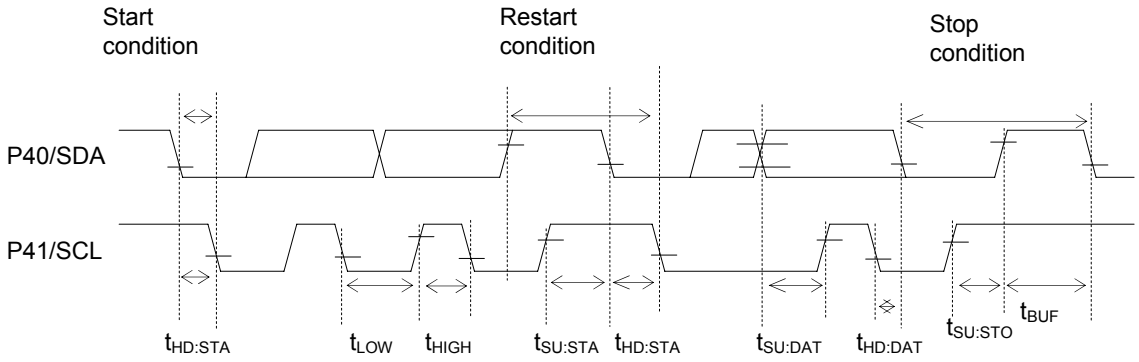
(V_{DD} = 1.8 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P Version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL "L" level time	t_{LOW}	—	4.7	—	—	µs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

● AC Characteristics (I^2C Bus Interface: Fast Mode 400kHz)

(V_{DD} = 1.8 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P Version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL "L" level time	t_{LOW}	—	1.3	—	—	µs
SCL "H" level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs



● AC CHARACTERISTICS (RC Oscillation A/D Converter)

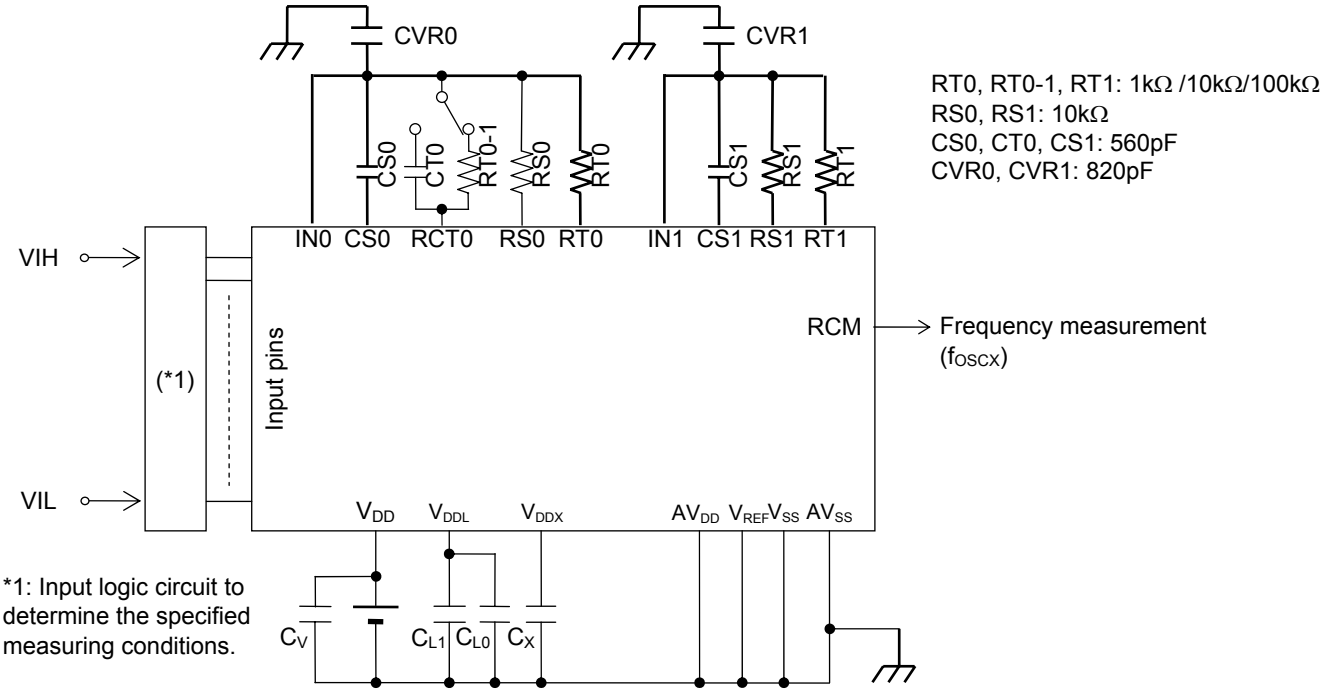
(V_{DD} = 1.3 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P Version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resistors for oscillation	RS0, RS1, RT0, RT0-1,RT1	CS0, CT0, CS1 ≥ 740pF	1	—	—	kΩ
Oscillation frequency VDD = 1.5V	f_{OSC1}	Resistor for oscillation = 1kΩ	209.4	330.6	435.1	kHz
	f_{OSC2}	Resistor for oscillation = 10kΩ	41.29	55.27	64.16	kHz
	f_{OSC3}	Resistor for oscillation = 100kΩ	4.71	5.97	7.06	kHz
RS to RT oscillation frequency ratio *1 VDD = 1.5V	Kf1	RT0, RT0-1, RT1 = 1kHz	5.567	5.982	6.225	—
	Kf2	RT0, RT0-1, RT1 = 10kHz	0.99	1	1.01	—
	Kf3	RT0, RT0-1, RT1 = 100kHz	0.104	0.108	0.118	—
Oscillation frequency VDD = 3.0V	f_{OSC1}	Resistor for oscillation = 1kΩ	407.3	486.7	594.6	kHz
	f_{OSC2}	Resistor for oscillation = 10kΩ	49.76	59.28	72.76	kHz
	f_{OSC3}	Resistor for oscillation = 100kΩ	5.04	5.993	7.04	kHz
RS to RT oscillation frequency ratio *1 VDD = 3.0V	Kf1	RT0, RT0-1, RT1 = 1kHz	8.006	8.210	8.416	—
	Kf2	RT0, RT0-1, RT1 = 10kHz	0.99	1	1.01	—
	Kf3	RT0, RT0-1, RT1 = 100kHz	0.100	0.108	0.115	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(RT0\text{–}CS0\ oscillation)}{f_{OSCx}(RS0\text{–}CS0\ oscillation)},\ \frac{f_{OSCx}(RT0\text{-}1\text{–}CS0\ oscillation)}{f_{OSCx}(RS0\text{–}CS0\ oscillation)},\ \frac{f_{OSCx}(RT1\text{–}CS1\ oscillation)}{f_{OSCx}(RS1\text{–}CS1\ oscillation)}$$

(x = 1, 2, 3)



Note:

- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.

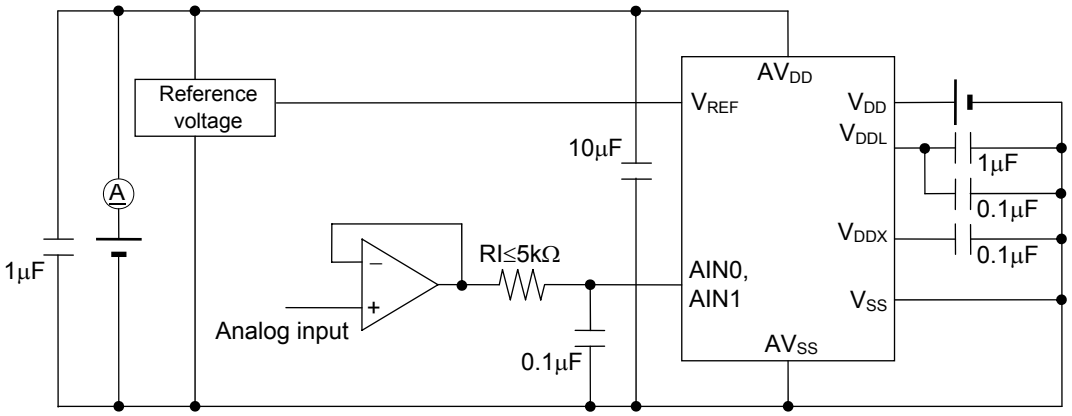
- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have VSS(GND) trace next to the signal.
- Please make wiring to components (capacitor, resisteor and etc.) necessory for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

● Electrical Characteristics of Successive Approximation Type A/D Converter

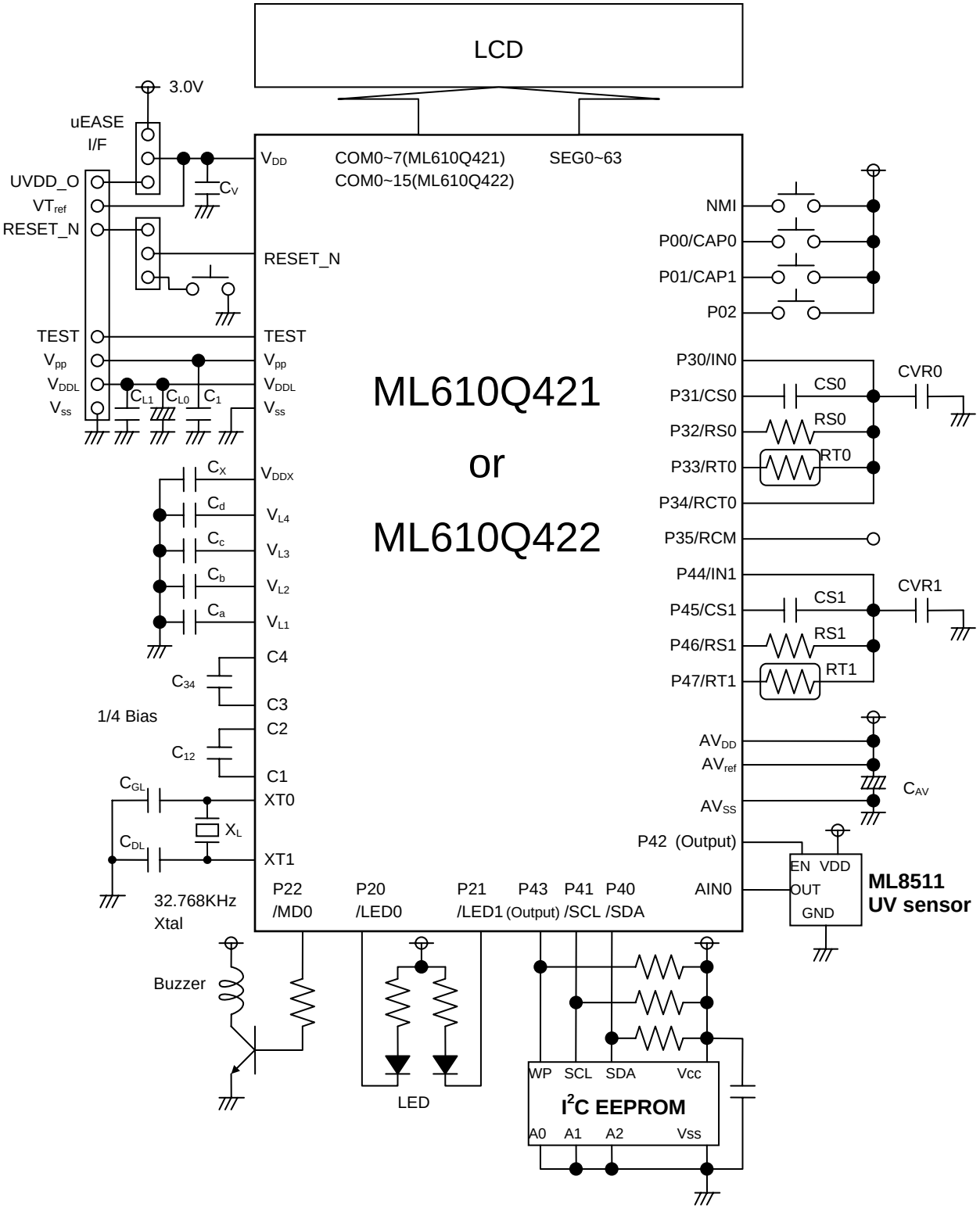
(V_{DD} = 1.8 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P Version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	—	—	—	12	bit
Integral non-linearity error	IDL	2.7V ≤ V_{REF} ≤ 3.6V	–4	—	+4	LSB
		2.2V ≤ V_{REF} ≤ 2.7V	–6	—	+6	
Differential non-linearity error	DNL	2.7V ≤ V_{REF} ≤ 3.6V	–3	—	+3	
		2.2V ≤ V_{REF} ≤ 2.7V	–5	—	+5	
Zero-scale error	V_{OFF}	—	–6	—	+6	
Full-scale error	FSE	—	–6	—	+6	
Reference voltage	V_{REF}	—	2.2	—	AV_{DD}	V
Conversion time	t_{CONV}	SACK = 0 (HSCLK = 375kHz to 625kHz)	—	25	—	ϕ/CH
		SACK = 1 (HSCLK = 1.5MHz to 4.2MHz)	—	112	—	

ϕ: Period of high-speed clock (HSCLK)

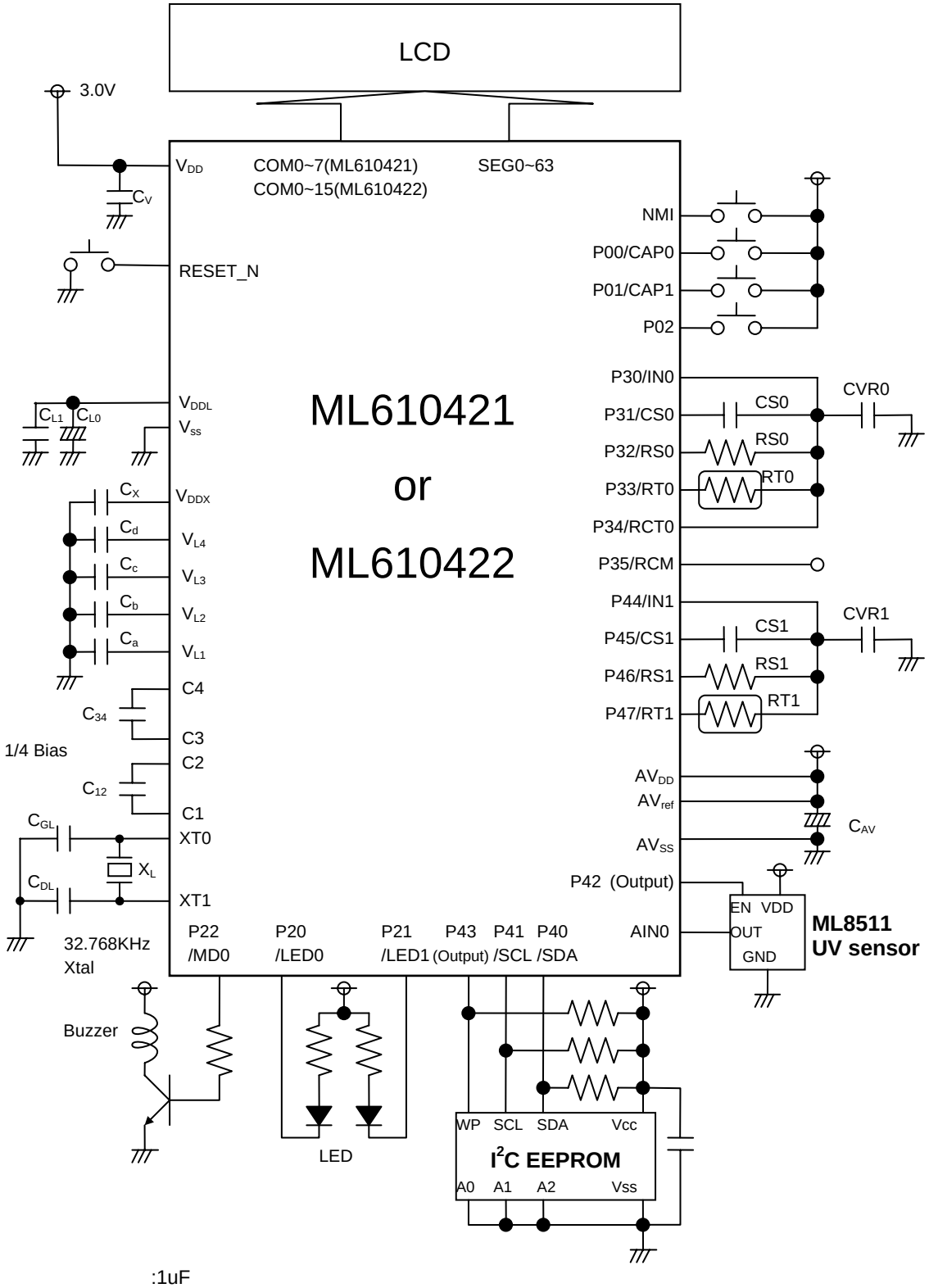


Appendix D Application Circuit Example



C_V	:1uF	C_{L0}	:1uF
C_{L1}	:0.1uF	C_X	:0.1uF
C_1	:1uF	C_{12},C_{34}	:1uF
C_a, C_b, C_c, C_d	:1uF	C_{DL}	: 0 ~ 12pF
C_{GL}	: 0 ~ 12pF	RS0, RS1	: 10 KΩ
C_{AV}	:1uF	CVR0, CVR1	: 820 pF
CS0, CS1	: 560 pF		
RT0, RT1	: Thermistor (103AT/Semitec)		

Figure D-1 Application Circuit Example of ML610Q421/ML610Q422



C_V	:1uF		
C_{L1}	:0.1uF	C_{L0}	:1uF
C_X	:0.1uF		
C_a, C_b, C_c, C_d	:1uF	C_{12},C_{34}	:1uF
C_{GL}	: 0 ~ 12pF	C_{DL}	: 0 ~ 12pF
C_{AV}	:1uF	RS0, RS1	: 10 KΩ
CS0, CS1	: 560 pF	CVR0, CVR1	: 820 pF
RT0, RT1	: Thermistor (103AT/Semitec)		

Figure D-2 Application Circuit Example of ML610421/ML610422

Appendix E Check List

This Check List has notes to prevent commonly-made programming mistakes and frequently overlooked or misunderstood hardware features of the MCU. Check each note listed up chapter by chapter while coding the program or evaluating it using the MCU.

Chapter 1 Overview

[ ] Please confirm how to handle the unused pins(Refer to Section 1.3.4 in the user's manual).

Chapter 2 CPU and Memory

- **Program Memory size**

[ ] 31,744 Byte (0:0000H to 0:7BFFH)

- **Data RAM size**

[ ] 1023 Byte (0:E000H to 0:E3FFH)

- **Unused area**

[ ] Please fill test area 0:7C00H to 0:7DFFH with BRK instruction code "0FFH" (Refer to a startup file "S61042XSW.asm" for programming in the source code).

[ ] For fail safe in your system, please fill unused program memory area (your program code does not use) with BRK instruction code "0FFH". We will fill the area with the code "0FFH" at LAPIS semiconductor's factory programming.

- **Initializing RAM**

[ ] The hardware reset does not initialize RAM. Please initialize RAM by the software.

Chapter 3 Reset

- **Reset activation pulse width**

[ ] Minimum 200us (Refer to Appendix C-2 in the user's manual)

- **Power-on reset occurrence power rising time**

[ ] Maximum 10ms (Refer to Appendix C-2 in the user's manual)

- **Reset status flag**

[ ] No flag is provided that indicates the occurrence of reset by the RESET_N pin (Refer to section 3.2.2. in the user's manual).

- **BRK instruction reset**

[ ] In system reset by the BRK instruction, no special function register (SFR) is initialized either. Therefore initialize the SFRs by your software.

Chapter 4 Standby control / MCU control

- **STOP mode**

[ ] Please note the STPACP is not enabled when both interrupt enable flags and the interrupt request flags are "1" & MIE flag is "0" (Refer to Section 4.2.2~4.2.3. in the user's manual).

[ ] Place two NOP instructions next to the instruction that sets the STP bit to "1"(Refer to Section 4.3.3. in the user's manual).

- **HALT mode**

[ ] Place two NOP instructions next to the instruction that sets the HLT bit to "1"(Refer to Section 4.3.2. in the user's manual).

- **BLKCON registers**

[ ] BLKCON registers enable or disable corresponsive each peripheral (Refer to Section 4.2.4 ~ 4.2.8. in the user's manual).

[ ] When certain bits of block control registers are set to "1", corresponding peripherals are reset (all registers are reset) and operating clocks for the peripherals stop.

[ ] DXTSP bit (bit 4) of BLKCON4 register disables the operation of 32kHz oscillation stop detector in only HALT mode.

Chapter 5 Interrupt

- **Unused interrupt vector table**

[ ] Please define all unused interrupt vector tables for fail safe.

- **Non-maskable interrupt**

[ ] The watchdog timer interrupt (WDTINT) and the NMI interrupt (NMINT) are non-maskable interrupts that do not depend on MIE flag(Refer to Section 5.2.9. and 5.3).

Chapter 6 Clock generation circuit

• Initial System clock

[ ] At power up or system reset, both built-in 500kHz RC oscillation and 32.768kHz crystal oscillation are oscillating, and 1/8 of the 500kHz RC oscillation clock(62.5kHz) is selected as a system clock for CPU.

• PLL oscillation clock

[ ] The PLL oscillation generates 8MHz clock which can be driven to an output pin, however the maximum CPU operating frequency is 4MHz.

• Switching high-speed clock operation mode to low-speed clock operation mode

[ ] When switching the high-speed clock to the low-speed clock after the power up, confirm the low-speed clock is oscillating for sure by checking Q128H bit is "1".

• Switching high-speed clock operation mode to another high-speed clock operation mode

[ ] When switching the high-speed clock mode, the clock must be first switched back to low clock before switching to other high-speed clock (Refer to Section 6.2.2.).

• Port 2nd Function

[ ] Specify the 2nd function for the port 2 when driving a clock to the pin(Refer to Section 6.4 in the user's manual).

[ ] A high-speed crystal/ceramic oscillation or an external clock input mode does not require specifying the 2nd function for the port 1(Refer to Section 18.3.2.)

Chapter 7 TBC (Time Base Counter)

• HTBCLK

[ ] HTBLK goes through the HTBDR register. Set proper valute to the register(Refer to Section 7.2.3. in the user's manual).

• How to read LTBC

[ ] Read consecutively LTBC(Low-speed Time Base Counter) twice until the last data coincides the previous data to prevent reading of uncertain data while counting up the clock (Refer to Section 7.3.1 in the user's manual).

Chapter 10 Timer

• How to read the timer counter registers

[ ] Check notes for reading the timer counter registers while counting up(Refer to Section 10.2.6. ~ 10.2.9. in the user's manual).

Chapter 11 PWM

• Used Pin

[ ] P34(PWM0) pin or P43(PWM0) pin is used.

• How to read the PWM counter registers

[ ] Check notes for reading the PWM counter registers while the PWM is operating(Refer to Section 11.2.4. in the user's manual).

• Port 2nd Function

[ ] Specify the 2nd Function for the port(Refer to Section 11.4 in the user's manual).

Chapter 12 WDT

• Overflow period

Clear WDT during the selected overflow period:

[ ] 125ms, [ ] 500ms, [ ] 2s, [ ] 8s

• WDP

[ ] Check the WDP before writing to the WDTCON and determine writing "5AH" or "0A5H" (Refer to Section 12.2.2. in the user's manual).

Chapter 13 SSIO

- **Used pin**

[ ] P40(SIN0), P41(SCK0) and P42(SOUT0) are used, or P44(SIN0), P45(SCK0) and P46(SOUT0) are used.

- **Port 2nd Function**

[ ] Specify the 2nd Function for the port (Refer to Section 14.4. in the user's manual)

Chapter 14 UART

- **Used pin**

[ ] P02(RXD0) and P43(TXD0) are used, or [ ] P42(RXD0) and P43(TXD0) are used.

[ ] Select the P02 or P42 for RXD0 by specifying U0RSEL bit of UA0MOD0 register.

- **Port 2nd Function**

[ ] Specify the 2nd Function for the port (Refer to Section 14.4. in the user's manual)

Chapter 15 I2C

- **Used pin**

[ ] P40(SDA) pin and P41(SCL) pin used.

- **Port 2nd Function**

[ ] Specify the 2nd Function for the port (Refer to Section 15.4. in the user's manual)

Chapter 16 NMI

- **Handling the pin**

[ ] Don't leave Hi-impedance NMI pin in floating state.

Chapter 17 ~ Chapter 22 Port

- **Handling the pin**

[ ] Don't leave Hi-impedance Input ports in floating state.

- **Port 2nd Function**

[ ] Specify properly PnCON0/1 and PnMOD0/1 registers for each port.

- **Port A**

[ ] ML610Q422/ML610422 does Not have port A.

Chapter 23 Melody / Buzzer

- **Enabling the LSCLK x 2**

[ ] Set ENMLT bit of FCON1 register to "1" to enable the low-speed double clock (LSCLK x 2) before stating the melody or buzzer outputs.

- **Port 2nd Function**

[ ] Specify the 2nd Function for the port (Refer to Section 23.4. in the user's manual)

Chapter 24 RC oscillation type A/D converter

- **Counter register**

[ ] Reading the counter register A or B during the A/D conversion, returns the data written before starting the A/D conversion.

- **Oscillation monitor pin**

[ ] P35/RCM pin is a monitor pin for oscillation clock. The channel 0(P34-P30) and channel 1(P47-P44) share the monitor pin.

[ ] Please use P35/RCM for the evaluation purpose and disable the output while operating in an actual application to minimize the noise.

- **Port 2nd Function**

[ ] Specify the 2nd Function for the port (Refer to Section 24.4. in the user's manual).

[ ] All the Port 3 pins except P35/RCM are configured as pins dedicated to the RC-ADC function during A/D conversion(Refer to Section 24.3.1. in the user's manual).

Chapter 25 Successive Approximation type A/D converter

- **Operating conditions**

[ ] Please confirm the operating voltage and the clock frequency.
V_{DD}=1.8V~3.6V (HSCLK=375KHz~625kHz or 1.5MHz~4.2MHz) , AV_{DD}=2.2V~3.6V

• Others

[ ] Use the A/D converter when the HSCLK is oscillating.

[ ] Do not set SARUN bit of SADCON1 register to "1" on the condition both SACH0 bit and SACH1 bit of SADMOD0 register are "0" (Refer to Section 25.2.7 ~ Section 25.2).

Chapter 26 LCD driver

• Bias

[ ] 1/3 bias or [ ] 1/4 bias

• Duty

[ ] ML610Q421/ML610421: 1/1 ~ 1/8 duty

[ ] ML610Q422/ML610422: 1/1 ~ 1/16 duty

• COM/SEG

[ ] ML610Q421/ML610421: 8COM x 50SEG

[ ] ML610Q422/ML610422: 16COM x 50SEG

• External capacitor

(1/3 bias)

[ ] Ca=1uF(connected to VL1 pin), [ ] Cb=1uF(connected to VL2 pin),

[ ] Cd=1uF(connected to VL4 pin),

[ ] C12=1uF（connected between C1 and C2 pin），[ ] C34=1uF(connected between C3 and C4 pin)

(1/4 bias)

[ ] Ca=1uF(connected to VL1 pin), [ ] Cb=1uF(connected to VL2 pin),

[ ] Cc=1uF(connected to VL3 pin), [ ] Cd=1uF(connected to VL4 pin),

[ ] C12=1uF（connected between C1 and C2 pin），[ ] C34=1uF(connected between C3 and C4 pin)

Chapter 27 BLD (Battery Low Detector)

• Changing the threshold

[ ] Please select the threshold voltage when the BLD circuit is OFF.

Chapter 28 Power circuit

• External capacitor

[ ] CL0=1uF（connected to VDDL pin)， [ ] Cx =0.1uF (connected to VDDX pin）

Chapter 29 On-chip debug (ML610Q421/ML610Q422 only)

[ ] Supply 3.0V ~ 3.6V to VDD pin when programming (erasing and writing) the Flash ROM with LAPIS semiconductor development tool uEASE.

[ ] Please do not apply LSIs being used for debugging to mass production.

[ ] Please validate the ROM code on your production board without LAPIS semiconductor development tool uEASE.

Appendix A SFR (Specific Function Registers)

• Initial data

[ ] Please confirm there are some SFRs have undefined initial value at reset (Refer to Appendix A in the user's manual).

Appendix C Electrical Characteristics

• Operating temperature

[ ] -20'C to +70'C

[ ] -40'C to +85'C

• Operating voltage vs Operating frequency

[ ] Please confirm the operating conditions.

[ ] +1.1V to +3.6V (30kHz to 36kHz: Low-speed crystal oscillation clock operation)

[ ] +1.3V to +3.6V (30kHz to 625kHz: Built-in RC oscillation clock operation)

[ ] +1.8V to +3.6V (30kHz to 4.2MHz: High-speed crystal/ceramic oscillation clock or built-in PLL oscillation clock)

Revision History

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEUL610Q421-01	Jul. 29, 2009	–	–	Formally edition 1.0
FEUL610Q421-02	Mar. 8, 2010	1-13	1-13	Corrected a typo. Pin direction of SOUT0 "I" → "O".
		6-14	6-14	Corrected a typo. LSCLK output pin "P22" → "P20".
		12-1	12-1	Changed description at Feature paragraph in the section 12.1.1.
		12-3	12-3	Changed description in Note.
		12-6	12-6	Changed description about watch dog timer operation (No. ⑧).
		–	12-7	Added the section 12.3.1.
		15-2, 15-7, 15-8, 15-9, 15-13, 15-14	15-2, 15-7, 15-8, 15-9, 15-13, 15-14	Added description that the device does not support arbitration function (multi-master) and clock synchronization (handshake).
		15-8, 15-11, 15-12, 15-13	15-8, 15-11, 15-12, 15-13	Changed a word "restart" to "repeated start".
		23-7	23-7	Added description for reuse the melody after the forced termination.
FEUL610Q421-03	May. 27, 2010	C-5	C-5	*1 conditions are corrected.
FEUL610Q421-04	Dec. 3, 2010	–	–	Add to B version
FEUL610Q421-05	Jun. 1, 2011	—	—	Add to ML610421/ML610422.
		—	1-7	Block diagram of ML610421 is added.
		—	1-8	Block diagram of ML610422 is added.
		—	1-13	Pin layout of ML610421 chip is added.
		—	1-14	Pin layout of ML610422 chip is added.
		—	1-17	Pad coordinates of ML610421 chip is added.
		—	1-18	Pad coordinates of ML610422 chip is added.
		—	1-23	List of ML610421/ML610422 Pins is added.
		3-1	3-1	The written contents of the watch dog timer of 3.1.1 features are changed.
		3-3	3-3	The written contents of the watch dog timer of operation of a 3.3.1 system reset mode are changed.
		20-1 20-10	20-1 20-10	Corrected a typo. CRT0 is corrected to RCT0.
		24-8	24-8	Corrected a typo. CRT0 is corrected to RCT0.
		26-1	26-1	Among the sentence of Chapter 26.1, "LAPIS semiconductor LCD tool only generates table data can be used for the type 3." is corrected, "The programmable display allotment function only generates table data can be used for the type 3."
		付 C-4	付 C-5	Typ value"0" of a BLD threshold voltage temperature deviation is corrected to "0.1."
		—	付 C-7	The consumption current of ML610421/ML610422 is added.

		–	付 D-2	Application circuit example of ML610421/ML620422 is added.