

FDMS015N04B

N-Channel PowerTrench® MOSFET

40 V, 100 A, 1.5 mΩ

Features

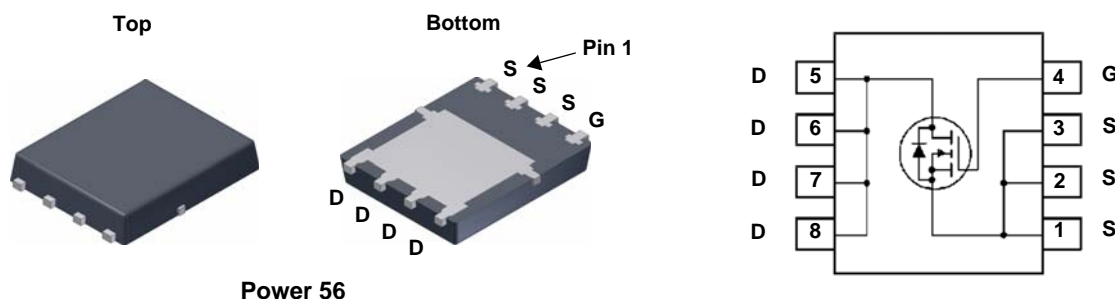
- $R_{DS(on)} = 1.13 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 50 \text{ A}$
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$ and High Efficiency
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies



Power 56

MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted*

Symbol	Parameter	FDMS015N04B	Unit
V_{DSS}	Drain to Source Voltage	40	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	100	A
	- Continuous ($T_C = 25^\circ\text{C}$)		
	- Continuous ($T_A = 25^\circ\text{C}$) (Note 1)	31.3	
I_{DM}	Drain Current	400	A
	- Pulsed (Note 2)		
E_{AS}	Single Pulsed Avalanche Energy	526	mJ
P_D	Power Dissipation	104	W
		($T_C = 25^\circ\text{C}$)	
	($T_A = 25^\circ\text{C}$) (Note 1)	2.5	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDMS015N04B	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 1)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS015N04B	FDMS015N04B	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	40	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	37	-	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 50\text{A}$	-	1.13	1.5	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{V}$, $I_D = 50\text{A}$	-	171	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 20\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	6560	8725	pF
C_{oss}	Output Capacitance		-	2795	3720	pF
C_{rss}	Reverse Transfer Capacitance		-	162	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 20\text{V}$, $V_{GS} = 0\text{V}$	-	3896	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 20\text{V}$, $I_D = 50\text{A}$ $V_{GS} = 0\text{V}$ to 10V	-	91	118	nC
Q_{gs}	Gate to Source Gate Charge		-	26	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	9	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	16	-	nC

(Note 4)

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{V}$, $I_D = 50\text{A}$ $V_{GS} = 10\text{V}$, $R_{GEN} = 4.7\Omega$	-	34	78	ns
t_r	Turn-On Rise Time		-	24	58	ns
$t_{d(off)}$	Turn-Off Delay Time		-	71	152	ns
t_f	Turn-Off Fall Time		-	26	62	ns
ESR	Equivalent Series Resistance	$f = 1\text{MHz}$	-	1.4	-	Ω

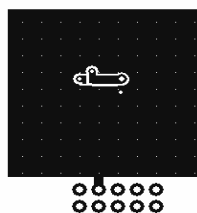
(Note 4)

Drain-Source Diode Characteristics

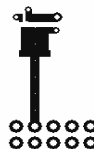
I _S	Maximum Continuous Drain to Source Diode Forward Current	-	-	100	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	400	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _{SD} = 50A		-	-
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _{SD} = 50A		-	78
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100A/μs		-	90
				-	1.3
				-	ns
				-	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50°C/W when mounted on a 1in^2 pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. $L = 3\text{mH}$, $I_{AS} = 18.72\text{A}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

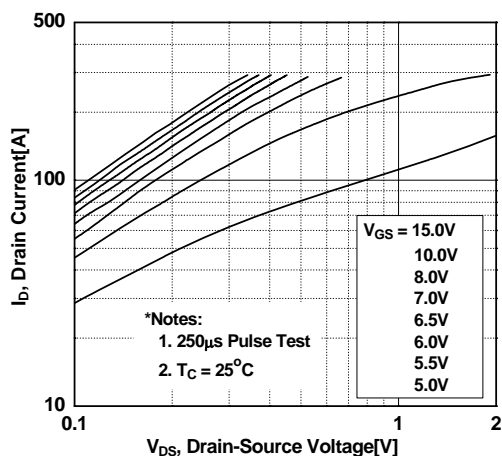


Figure 2. Transfer Characteristics

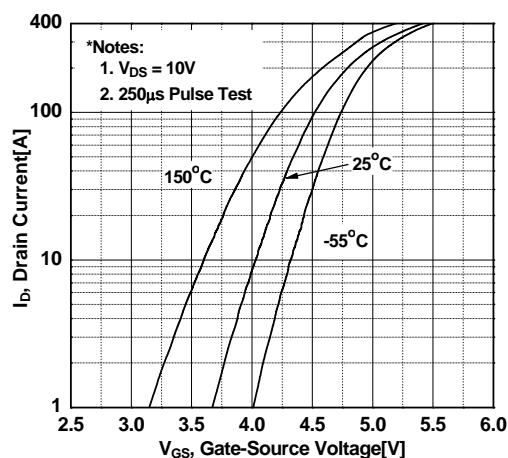


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

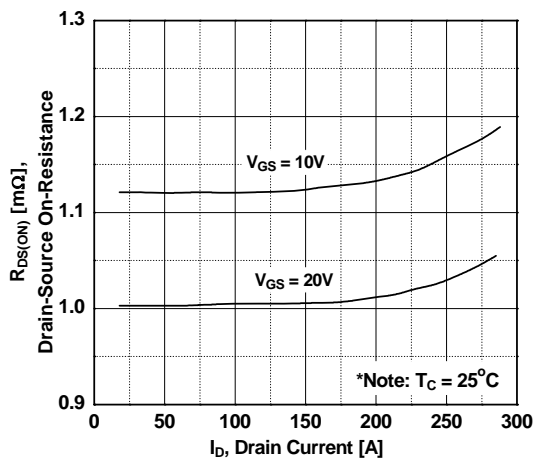


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

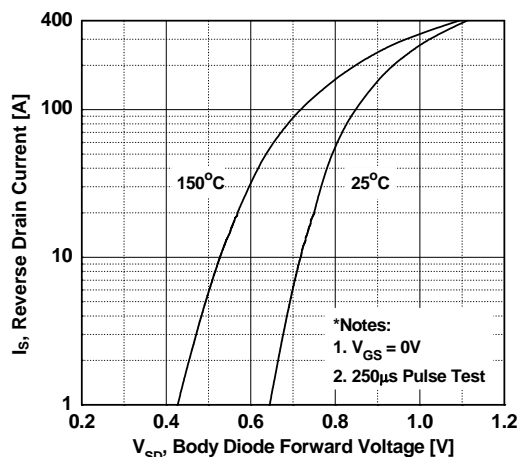


Figure 5. Capacitance Characteristics

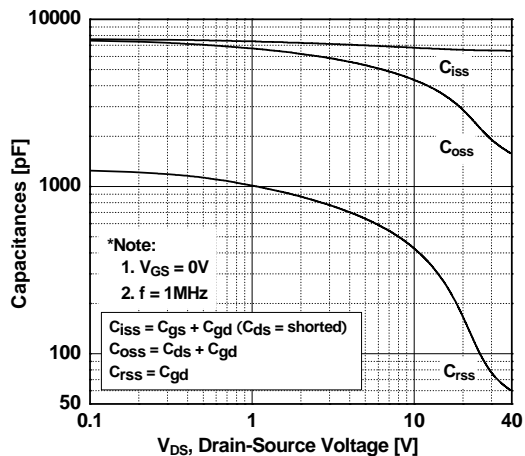
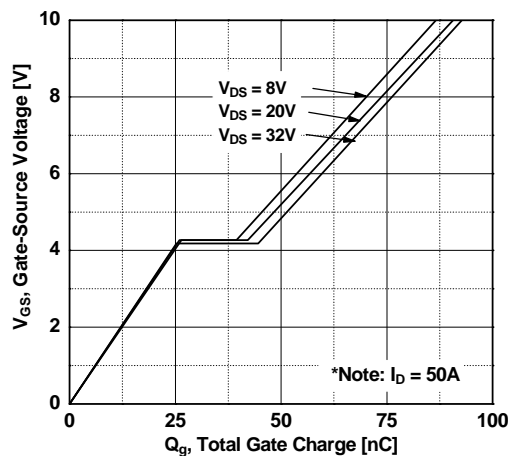


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

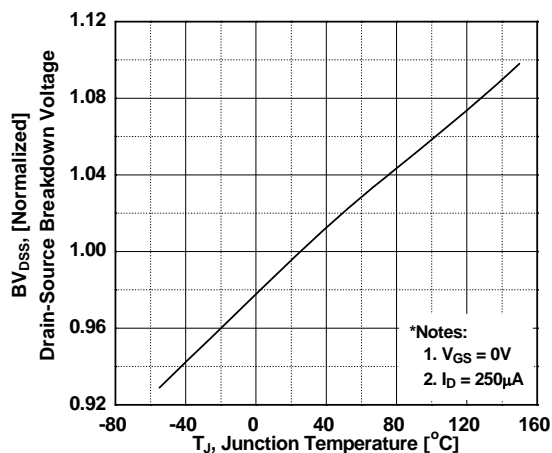


Figure 8. On-Resistance Variation vs. Temperature

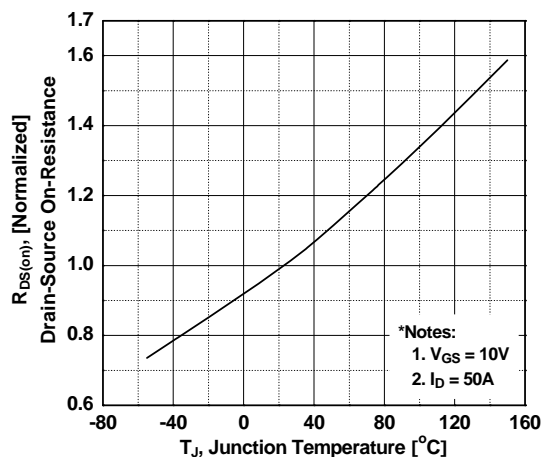


Figure 9. Maximum Safe Operating Area vs. Ambient Temperature

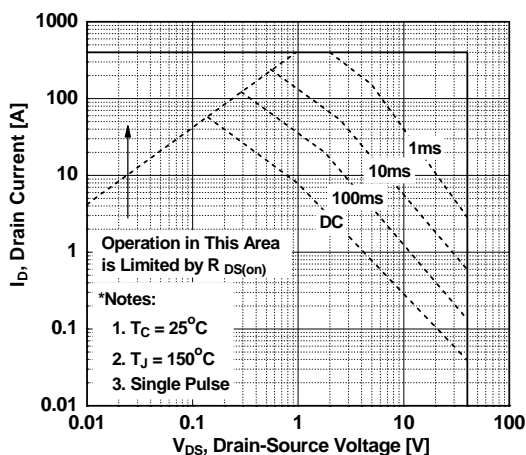


Figure 10. Maximum Drain Current

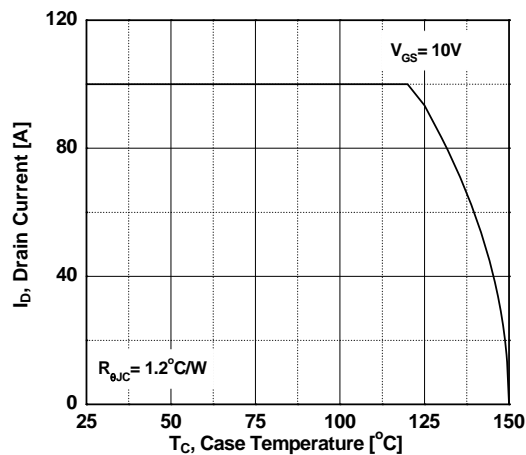


Figure 11. E_oss vs. Drain to Source Voltage

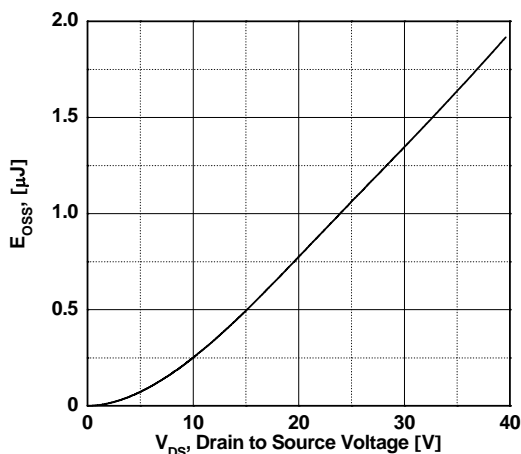
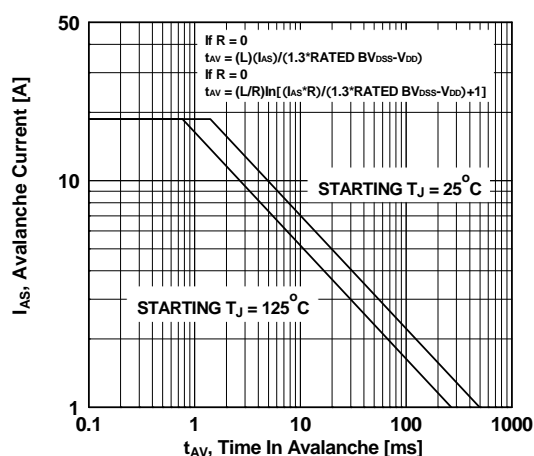
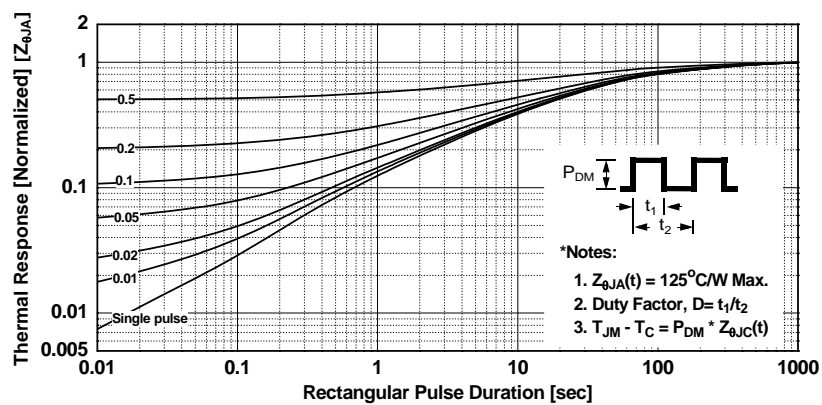


Figure 12. Unclamped Inductive Switching Capability



Typical Performance Characteristics (Continued)

Figure 13. Transient Thermal Response Curve



Gate Charge Test Circuit & Waveform



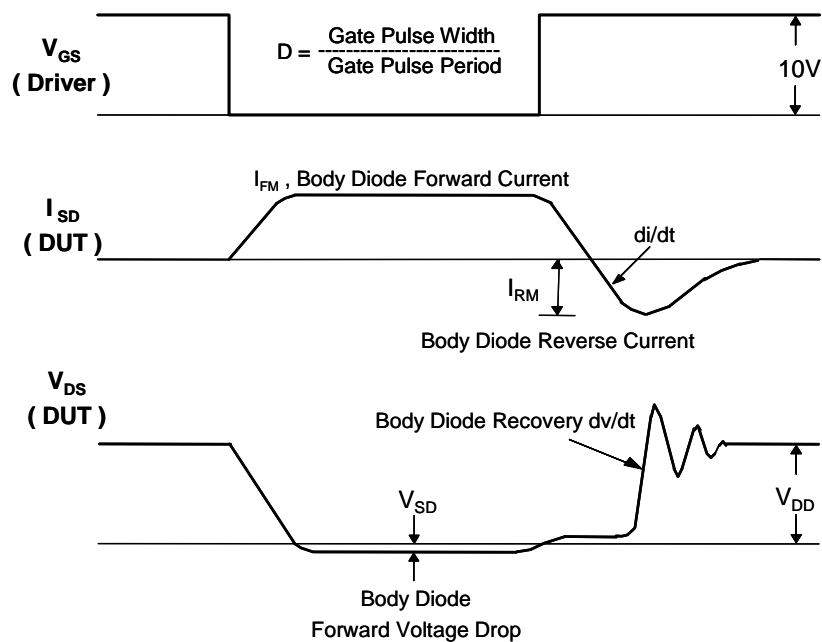
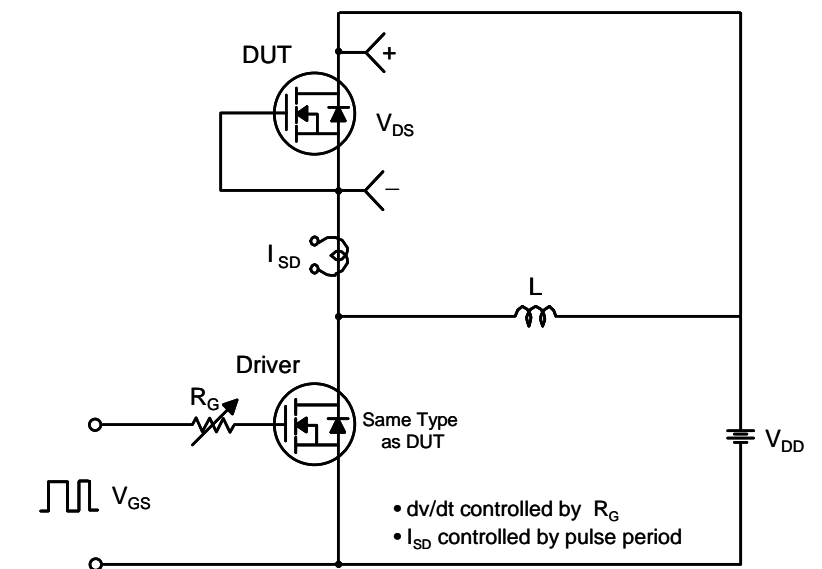
Resistive Switching Test Circuit & Waveforms



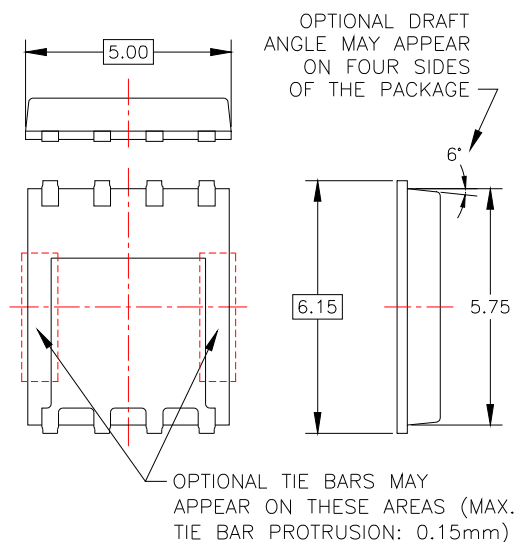
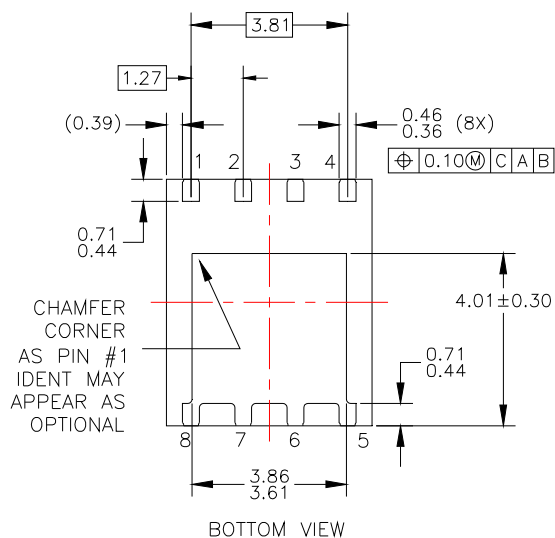
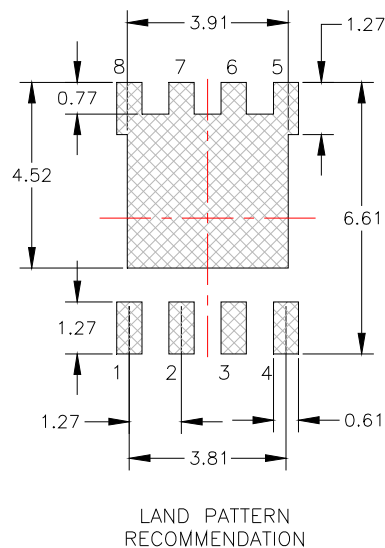
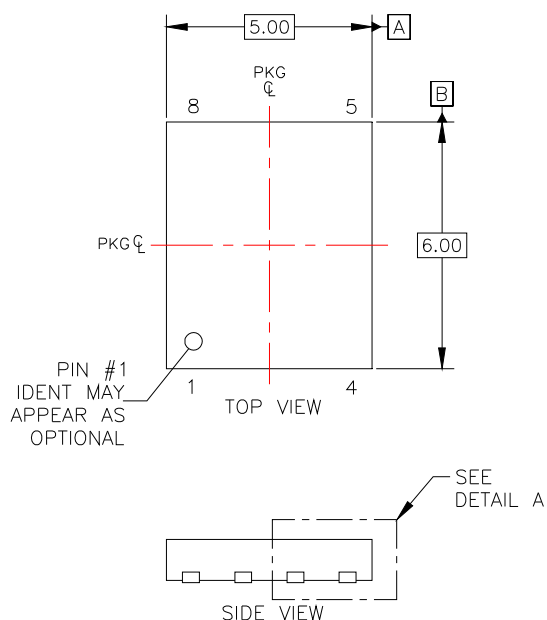
Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms

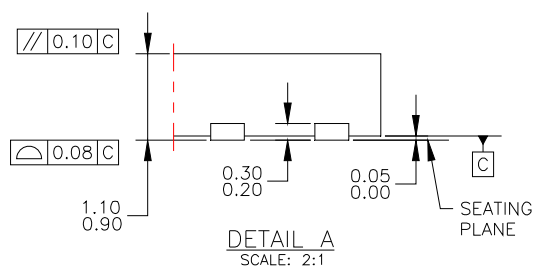


Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN08AREV4




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 AccuPower™
 AX-CAP®
 BitSiC™
 Build it Now™
 CorePLUS™
 CorePOWER™
 CROSSVOL™
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 EcoSPARK®
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SmartMax[™]
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SuperFET[®]
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SuperSOT[™]-6
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 TinyBoost™
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