

FDMC8854

N-Channel Power Trench® MOSFET

30V, 15A, 5.7mΩ

Features

- Max $r_{DS(on)}$ = 5.7mΩ at $V_{GS} = 10V$, $I_D = 15A$
- Max $r_{DS(on)}$ = 7.6mΩ at $V_{GS} = 4.5V$, $I_D = 13A$
- Low Profile - 1mm max in Power 33
- RoHS Compliant

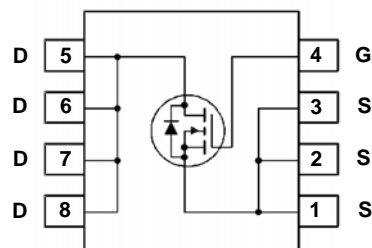
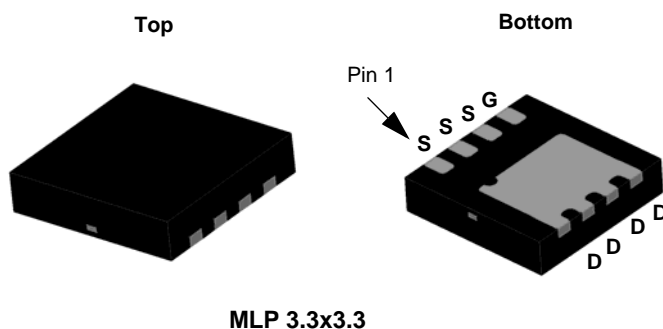


General Description

This N-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced Power Trench process. It has been optimized for power management applications.

Application

- DC - DC Conversion



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	15	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	67	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	15	
	-Pulsed	100	
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	41	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8854	FDMC8854	MLP 3.3x3.3	7"	8mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		21		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$, $V_{GS} = 0\text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 15\text{A}$		4.4	5.7	m Ω
		$V_{GS} = 4.5\text{V}$, $I_D = 13\text{A}$		5.6	7.6	
		$V_{GS} = 10\text{V}$, $I_D = 15\text{A}$, $T_J = 125^\circ\text{C}$		6.6	9.0	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{V}$, $I_D = 15\text{A}$		60		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 10\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$		2560	3405	pF
C_{oss}	Output Capacitance			515	685	pF
C_{rss}	Reverse Transfer Capacitance			290	435	pF
R_g	Gate Resistance	$f = 1\text{MHz}$		1.3		Ω

Switching Characteristics

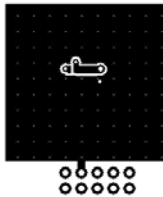
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{V}$, $I_D = 15\text{A}$ $V_{GS} = 10\text{V}$, $R_{GEN} = 6\Omega$		13	23	ns
t_r	Rise Time			5	10	ns
$t_{d(off)}$	Turn-Off Delay Time			31	50	ns
t_f	Fall Time			5	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{DD} = 10\text{V}$, $I_D = 15\text{A}$, $V_{GS} = 10\text{V}$		41	57	nC
Q_{gs}	Gate to Source Gate Charge			7		nC
Q_{gd}	Gate to Drain "Miller" Charge			7		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}$, $I_S = 15\text{A}$ (Note 2)		0.8	1.3	V
t_{rr}	Reverse Recovery Time	$I_F = 15\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$		33	50	ns
Q_{rr}	Reverse Recovery Charge			28	42	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 60°C/W when mounted on a 1in^2 pad of 2 oz copper



b. 135°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty cycle $< 2.0\%$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

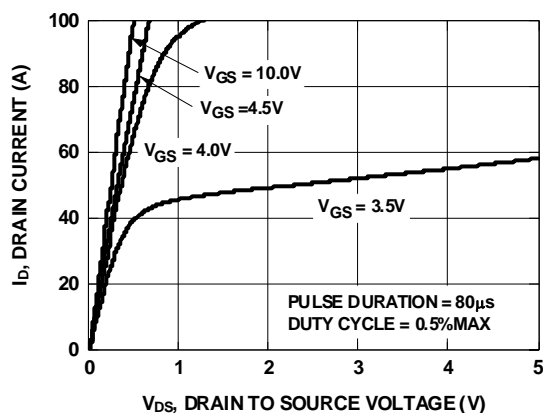


Figure 1. On-Region Characteristics

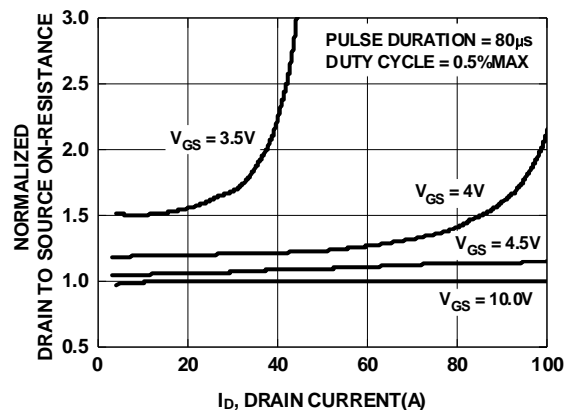


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

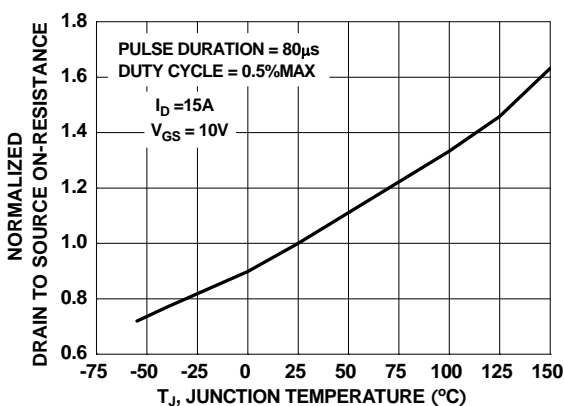


Figure 3. Normalized On-Resistance vs. Junction Temperature

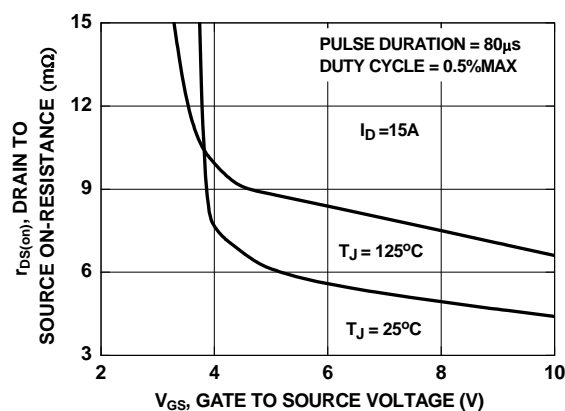


Figure 4. On-Resistance vs. Gate to Source Voltage

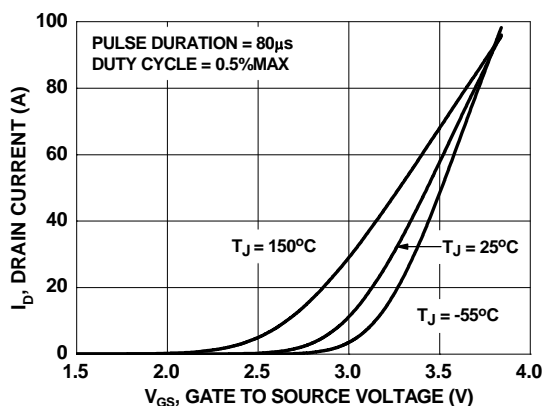


Figure 5. Transfer Characteristics

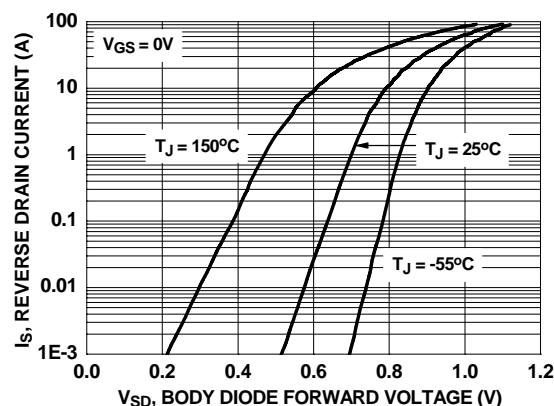


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

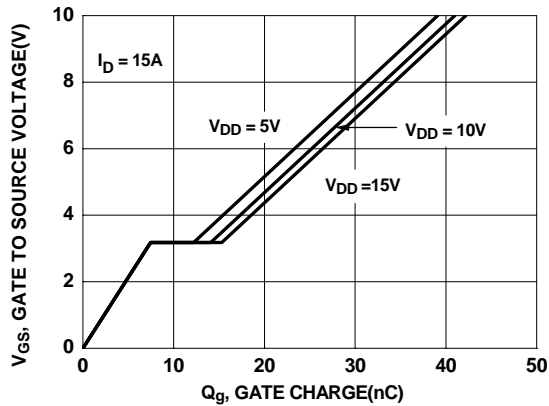


Figure 7. Gate Charge Characteristics

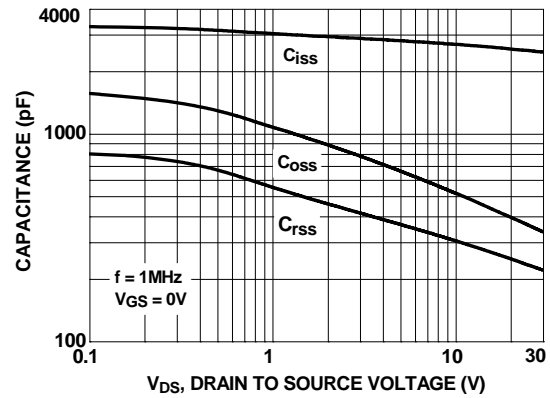


Figure 8. Capacitance vs. Drain to Source Voltage

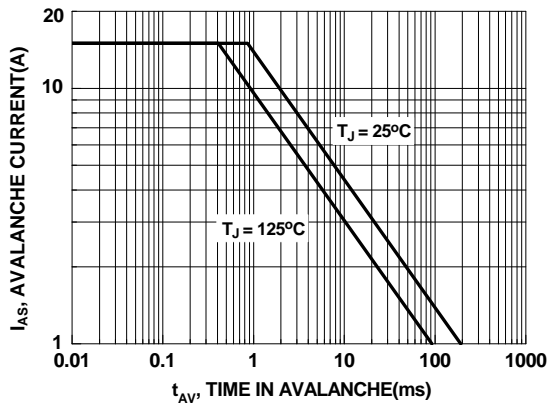


Figure 9. Unclamped Inductive Switching Capability

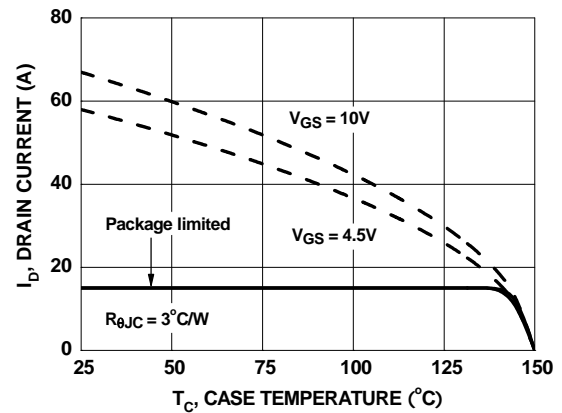


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

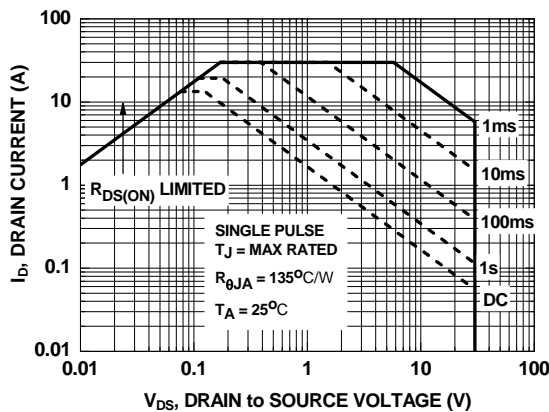


Figure 11. Forward Bias Safe Operating Area

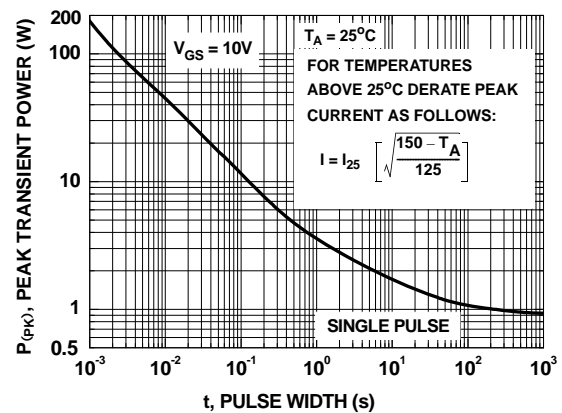


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

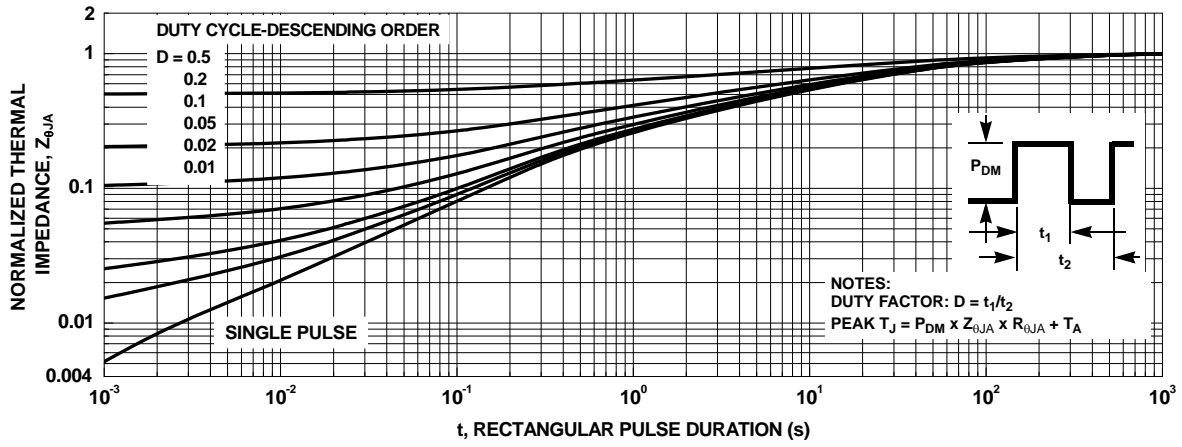
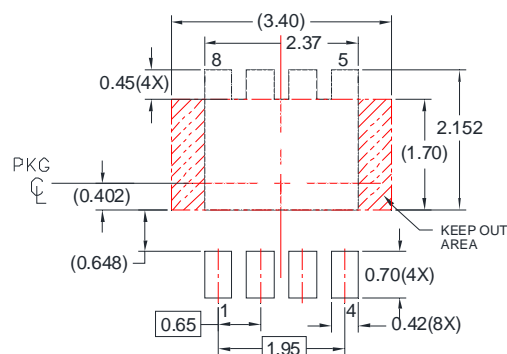
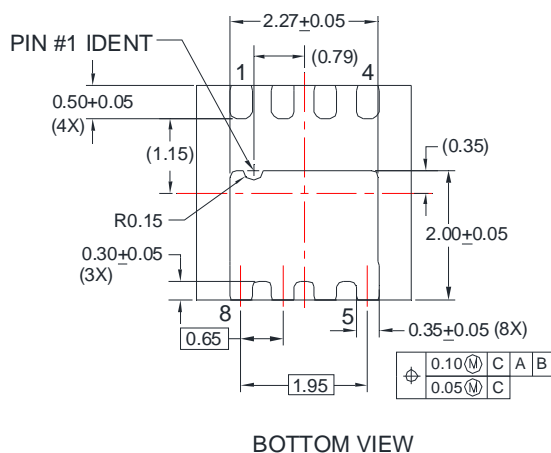
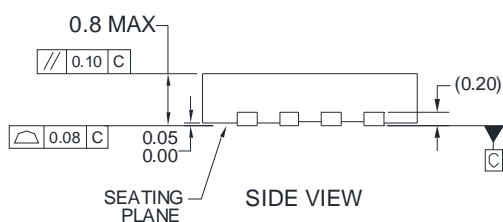
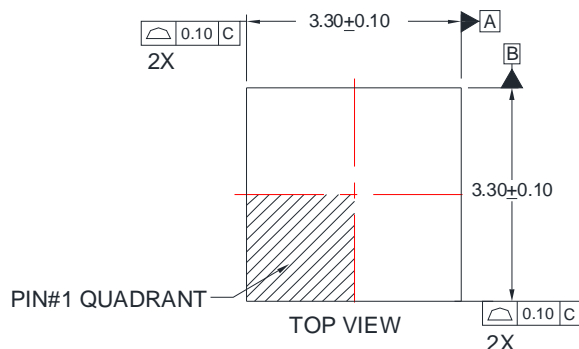


Figure 13. Transient Thermal Response Curve

Dimensional Outline and Pad Layout




NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY
- E. DRAWING FILE NAME : MKT-MLP08Srev2
- F. FAIRCHILD SEMICONDUCTOR







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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I66