

# FDD7N25LZ

## N-Channel UniFET™ MOSFET 250 V, 6.2 A, 550 mΩ

### Features

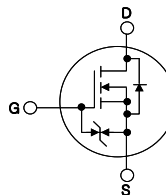
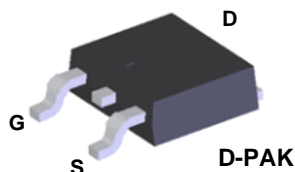
- $R_{DS(on)} = 430 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 3.1 \text{ A}$
- Low Gate Charge (Typ. 12 nC)
- Low  $C_{rss}$  (Typ. 8 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

### Applications

- LCD/LED/PDP TV
- Consumer Appliances
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

### Description

UniFET™ MOSFET is Fairchild Semiconductor®'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted\*

Symbol	Parameter		FDD7N20LZ	Unit
$V_{DSS}$	Drain to Source Voltage		250	V
$V_{GSS}$	Gate to Source Voltage		$\pm 20$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	6.2	A
		- Continuous ( $T_C = 100^\circ\text{C}$ )	3.7	
$I_{DM}$	Drain Current	- Pulsed (Note 1)	25	A
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)		115	mJ
$I_{AR}$	Avalanche Current (Note 1)		5.5	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)		5.6	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		10	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	56	W
		- Derate above $25^\circ\text{C}$	0.45	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FDD7N20LZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	110	

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD7N25LZ	FDD7N25LZ	D-PAK	380mm	16mm	2500

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$ , $T_C = 25^\circ\text{C}$	250	-	-	V
$\Delta BV_{DSS}$ $\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.25	-	$V/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 250\text{V}$ , $V_{GS} = 0\text{V}$ $V_{DS} = 200\text{V}$ , $T_C = 125^\circ\text{C}$	-	-	1 10	$\mu\text{A}$
$I_{GSSF}$	Gate to Body Leakage Current, Forward	$V_{GS} = 20\text{V}$ , $V_{DS} = 0\text{V}$	-	-	10	$\mu\text{A}$
$I_{GSSR}$	Gate to Body Leakage Current, Reverse	$V_{GS} = -20\text{V}$ , $V_{DS} = 0\text{V}$	-	-	-10	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	1.0	-	2.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$ , $I_D = 3.1\text{A}$ $V_{GS} = 5\text{V}$ , $I_D = 3.1\text{A}$	-	0.43 0.45	0.55 0.57	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{V}$ , $I_D = 3.1\text{A}$	-	7	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	480	635	pF
$C_{oss}$	Output Capacitance		-	65	85	pF
$C_{rss}$	Reverse Transfer Capacitance		-	8	12	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 250\text{V}$ , $I_D = 6.2\text{A}$ $V_{GS} = 10\text{V}$ (Note 4)	-	12	16	nC
$Q_{gs}$	Gate to Source Gate Charge		-	1.5	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	4	-	nC

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{V}$ , $I_D = 6.2\text{A}$ $V_{GS} = 10\text{V}$ , $R_G = 25\Omega$ (Note 4)	-	10	30	ns
$t_r$	Turn-On Rise Time		-	15	40	ns
$t_{d(off)}$	Turn-Off Delay Time		-	75	160	ns
$t_f$	Turn-Off Fall Time		-	30	70	ns

### Drain-Source Diode Characteristics

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	5.5	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	20	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 6.2A	-	-	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 6.2A dI <sub>F</sub> /dt = 100A/μs	-	130	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	0.6	-	μC

#### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $L = 6\text{mH}$ ,  $I_{AS} = 6.2\text{A}$ ,  $V_{DD} = 50\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 6.2\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

Figure 1. On-Region Characteristics

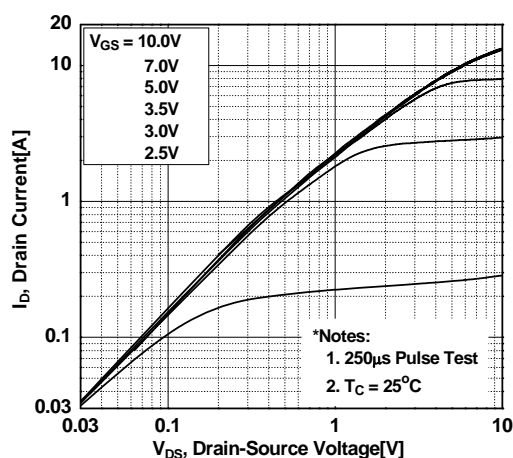


Figure 2. Transfer Characteristics

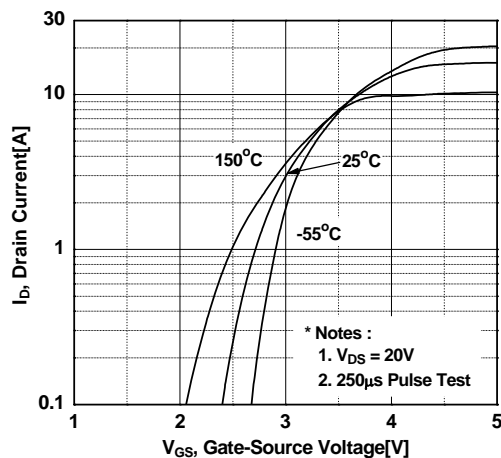


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

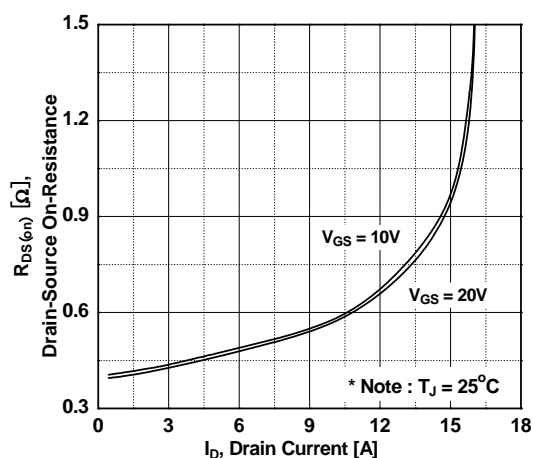


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

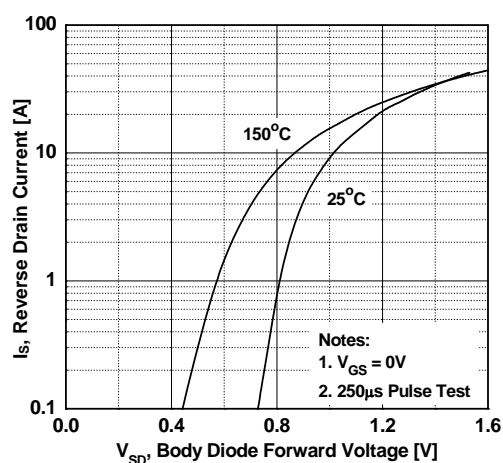


Figure 5. Capacitance Characteristics

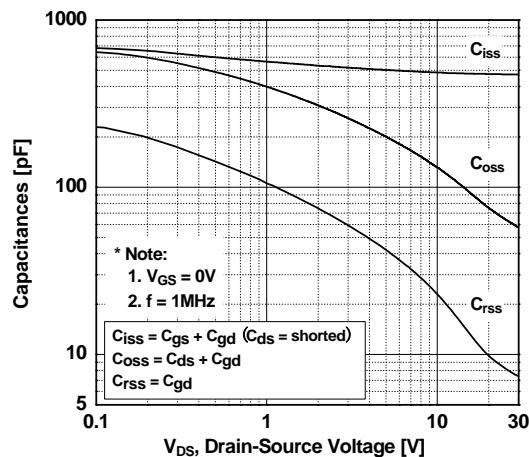
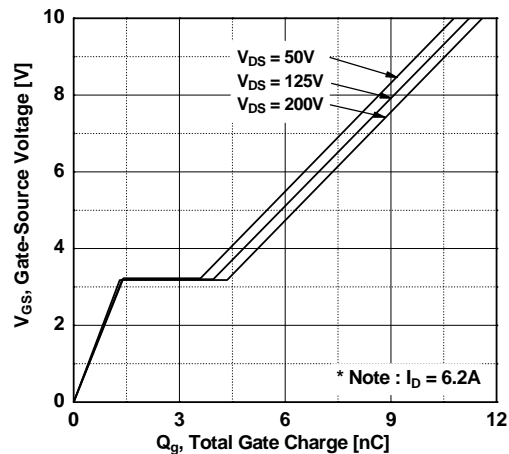
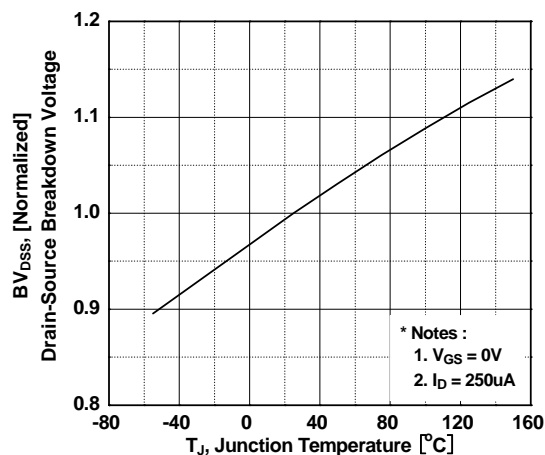


Figure 6. Gate Charge Characteristics

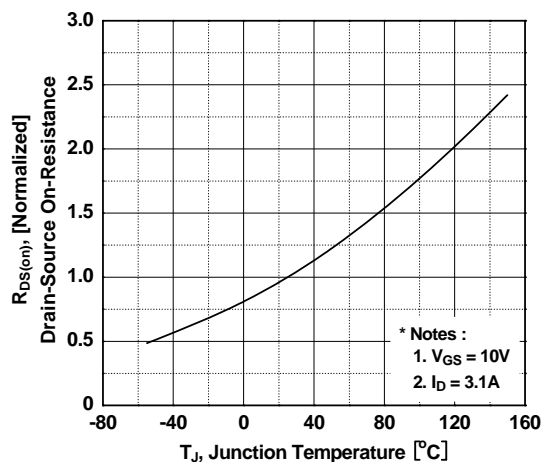


## Typical Performance Characteristics (Continued)

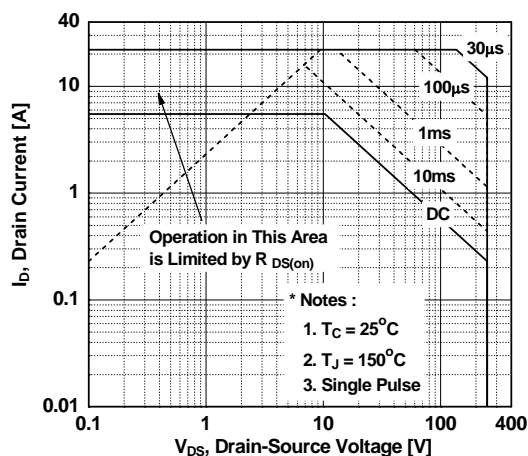
**Figure 7. Breakdown Voltage Variation vs. Temperature**



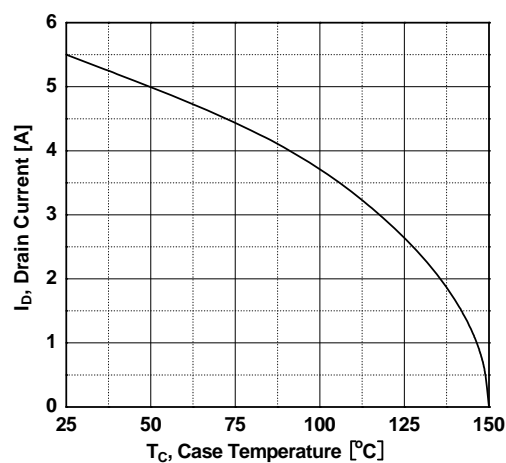
**Figure 8. On-Resistance Variation vs. Temperature**



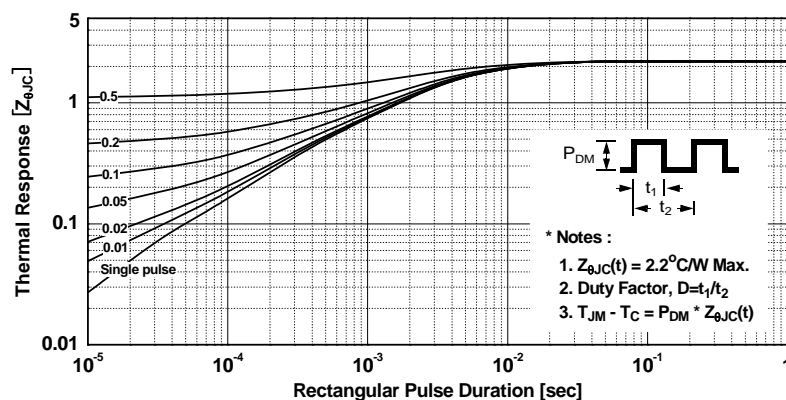
**Figure 9. Maximum Safe Operating Area - FDD7N25LZ**



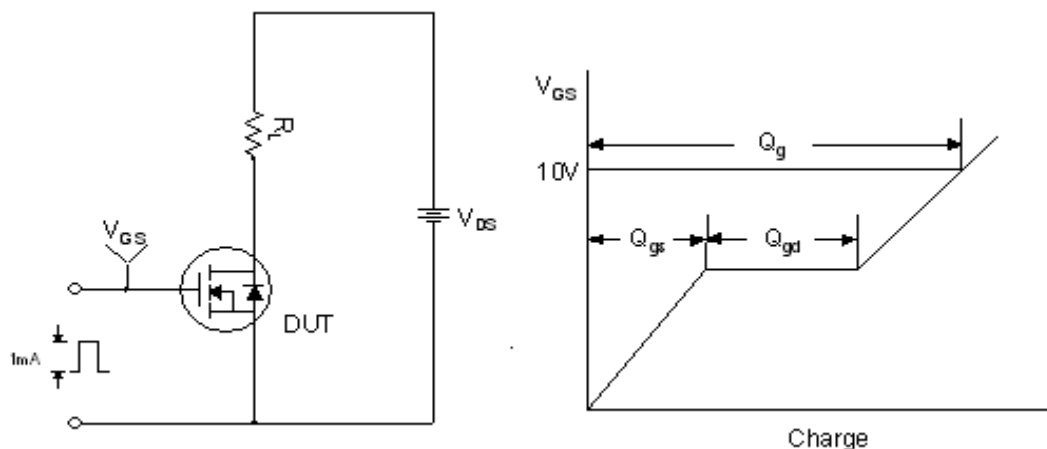
**Figure 10. Maximum Drain Current vs. Case Temperature**



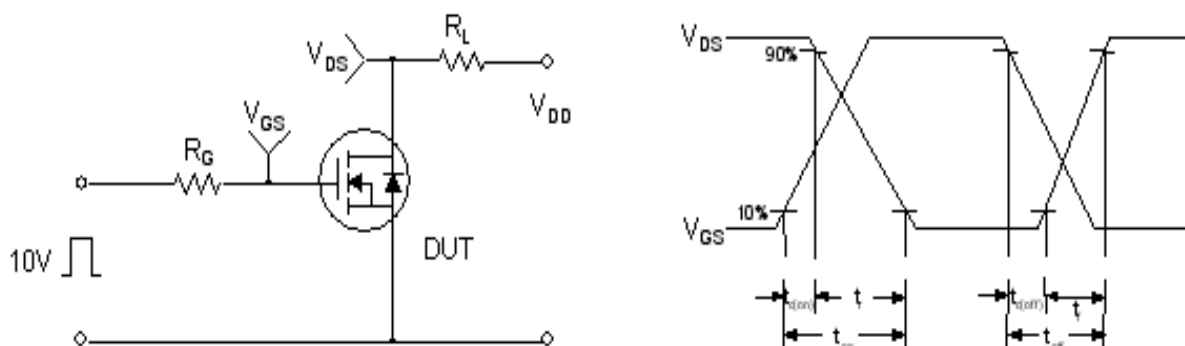
**Figure 11. Transient Thermal Response Curve - FDD7N25LZ**



Gate Charge Test Circuit & Waveform



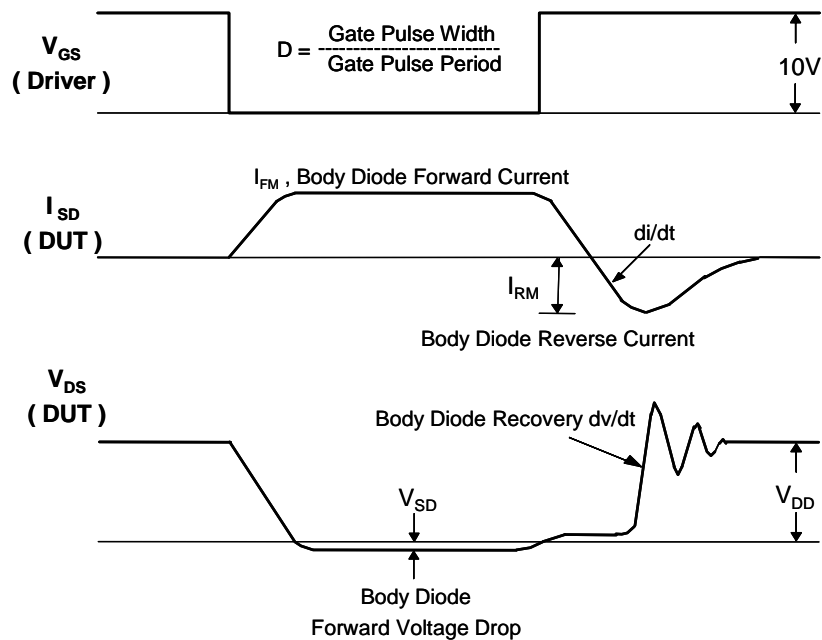
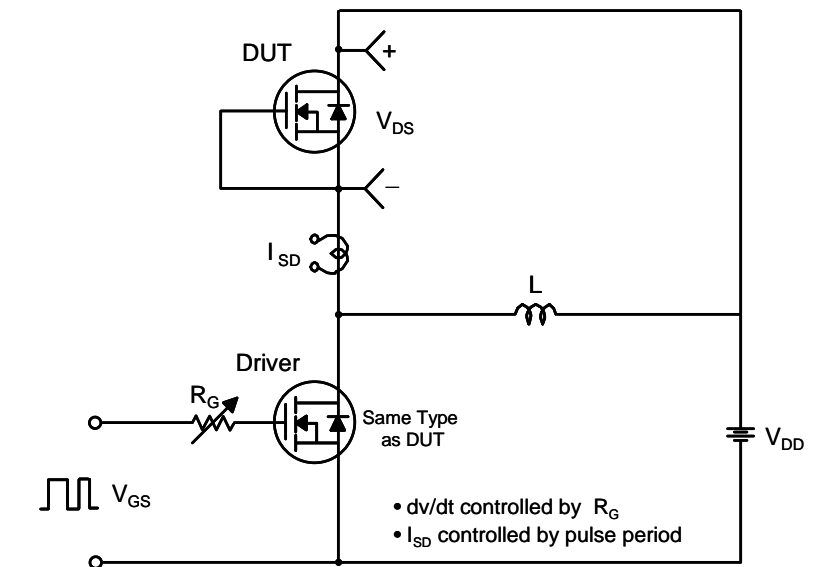
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

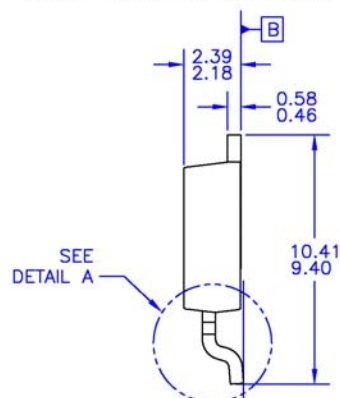
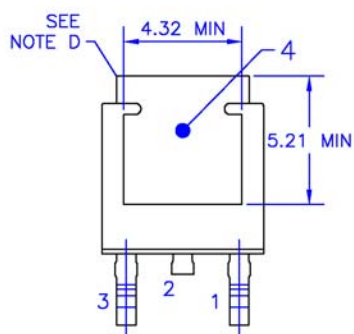
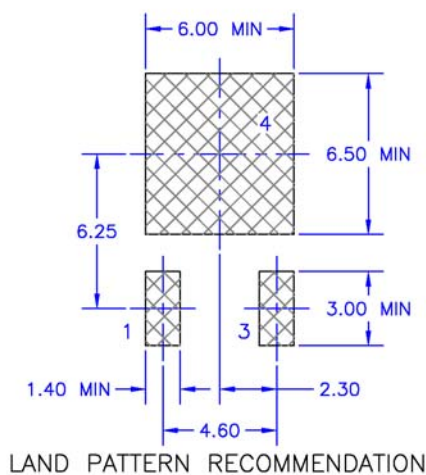
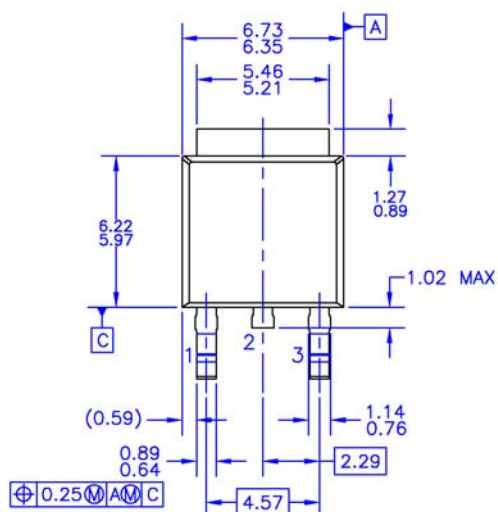


Peak Diode Recovery dv/dt Test Circuit & Waveforms

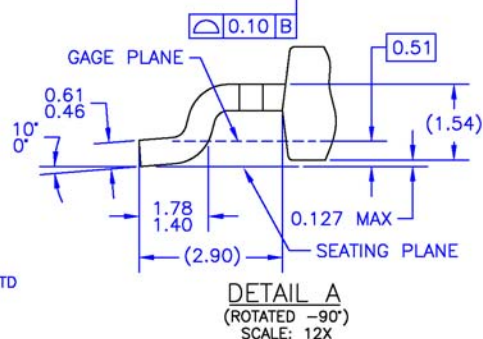


# Mechanical Dimensions

## D-PAK




- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
  - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
  - H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV8




Dimensions in Millimeters


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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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