

March 2013

FDD6N50F

N-Channel UniFETTM FRFET[®] MOSFET 500 V, 5.5 A, 1.15 Ω

Features

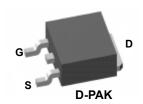
- $R_{DS(on)}$ = 950 m Ω (Typ.) @ V_{GS} = 10 V, I_D = 2.75 A
- Low Gate Charge (Typ. 15nC)
- Low C_{rss} (Typ. 6.3pF)
- 100% Avalanche Tested
- · Improved dv/dt Capability
- · RoHS Compliant

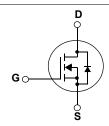
Applications

- LCD/LED/PDP TV
- · Lighting
- · Uninterruptible Power Supply
- · AC-DC Power Supply

Description

UniFETTM MOSFET is Fairchild Semiconductor[®]'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET[®] MOSFET has been enhanced by lifetime control. Its trr is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter			FDD6N50F	Unit
V _{DSS}	Drain to Source Voltage			500	V
V _{GSS}	Gate to Source Voltage			±30	V
1	- Continuous (T _C = 25°C)			5.5	^
^I D	Drain Current	- Continuous (T _C = 100°C)		2.4	Α
I _{DM}	Drain Current	- Pulsed	(Note 1)	22	Α
E _{AS}	Single Pulsed Avalanche E	nergy	(Note 2)	270	mJ
I _{AR}	Avalanche Current		(Note 1)	5.5	Α
E _{AR}	Repetitive Avalanche Energy (Note		(Note 1)	8.9	mJ
dv/dt	Peak Diode Recovery dv/d	lt	(Note 3)	20	V/ns
n	Dawer Dissination	(T _C = 25°C)		89	W
P_{D}	Power Dissipation	- Derate above 25°C		0.71	W/°C
T _J , T _{STG}	Operating and Storage Ter	mperature Range		-55 to +150	°C
TL	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300	°C

Thermal Characteristics

Symbol	Parameter	FDD6N50F	Unit		
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	°C/W		
R _{θJA} Thermal Resistance, Junction to Ambient, Max. 83					
*When mounted on the minimum pad size recommended (PCB Mount)					

Package Marking and Ordering Information T_C = 25°C unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD6N50F	FDD6N50FTM	D-PAK	380mm	16mm	2500

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	eteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A$, $V_{GS} = 0 V$, $T_J = 25 ^{\circ} C$	500	-	-	V
ΔBV _{DSS} / ΔΤ _J	Breakdown Voltage Temperature Coefficient	I _D = 250μA, Referenced to 25°C	-	0.15	-	V/°C
	Zero Gate Voltage Drain Current	V _{DS} = 500V, V _{GS} = 0V	-	-	10	
IDSS	Zero Gate voltage Drain Current	$V_{DS} = 400V, T_C = 125^{\circ}C$	-	-	100	μΑ
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30V, V_{DS} = 0V$	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	3.0	-	5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10V, I_D = 2.75A$	-	0.95	1.15	Ω
9 _{FS}	Forward Transconductance	$V_{DS} = 40V, I_{D} = 2.75A$	-	4.3	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	\\ - 25\\ \\ - 0\\	-	720	960	pF
C _{oss}	Output Capacitance	V _{DS} = 25V, V _{GS} = 0V f = 1MHz		85	115	pF
C _{rss}	Reverse Transfer Capacitance	1 - 11/11/12	-	6.3	9.5	pF
Q _{g(tot)}	Total Gate Charge at 10V		-	15	19.8	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DS} = 400V, I_{D} = 6A$	-	4.4	-	nC
Q _{gd}	Gate to Drain "Miller" Charge	$V_{GS} = 10V$ (Note 4)	1	6.1	-	nC

Switching Characteristics

t _{d(on)}	Turn-On Delay Time			-	17	44	ns
t _r	Turn-On Rise Time	$V_{DD} = 250V, I_{D} = 6A$			28.3	66.6	ns
t _{d(off)}	Turn-Off Delay Time	$R_G = 25\Omega$		-	33.4	76.7	ns
t _f	Turn-Off Fall Time		(Note 4)	-	20.5	51	ns

Drain-Source Diode Characteristics

Is	Maximum Continuous Drain to Source Diode Forward Current		-	-	5.5	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	22	Α
V_{SD}	Drain to Source Diode Forward Voltage $V_{GS} = 0V$, $I_{SD} = 5.5A$		-	-	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _{SD} = 5.5A	-	85	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100A/\mu s$	-	0.15	-	μС

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature 2: L = 16mH, I_{AS} = 5.5A, V_{DD} = 50V, R_{G} = 25 Ω , Starting T_{J} = 25°C 3: $I_{SD} \le$ 5.5A, di/dt \le 200A/ μ s, $V_{DD} \le$ BV $_{DSS}$, Starting T_{J} = 25°C 4: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

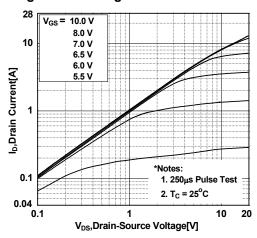


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

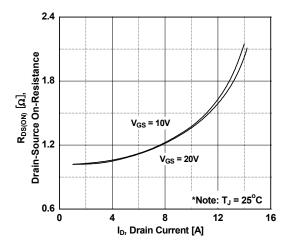


Figure 5. Capacitance Characteristics

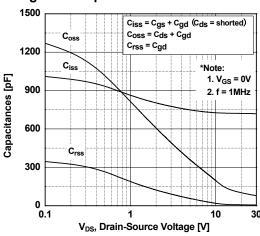


Figure 2. Transfer Characteristics

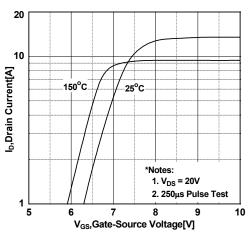


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

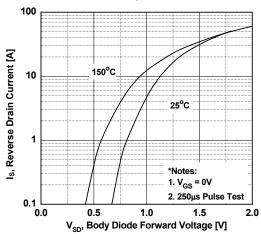
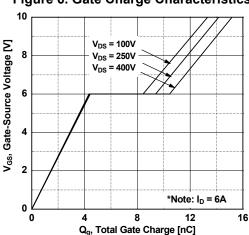


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

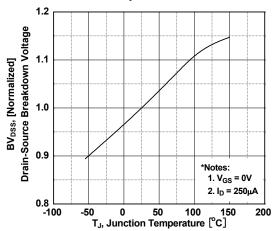


Figure 8. Maximum Safe Operating Area

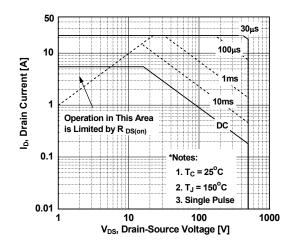


Figure 9. Maximum Drain Current vs. Case Temperature

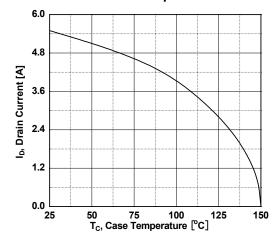
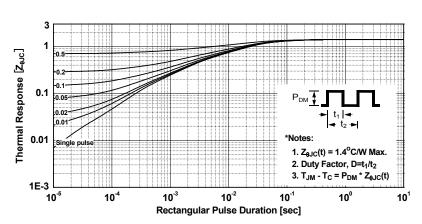
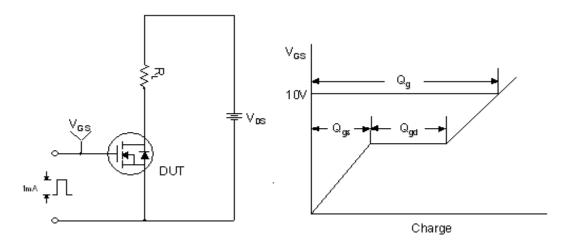


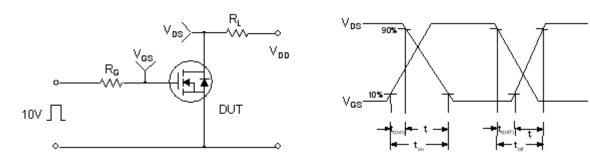
Figure 10. Transient Thermal Response Curve



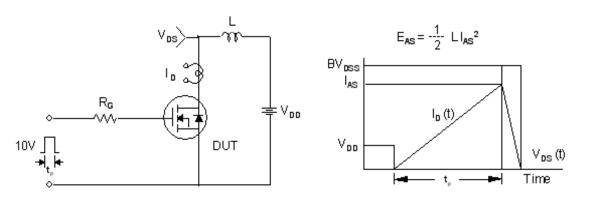
Gate Charge Test Circuit & Waveform



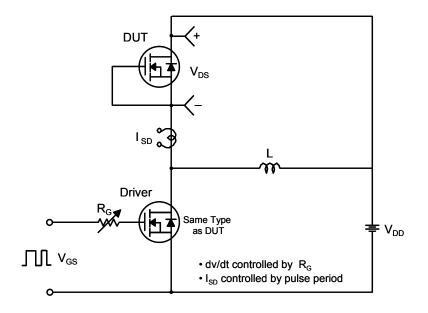
Resistive Switching Test Circuit & Waveforms

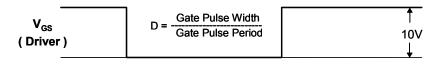


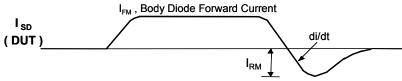
Unclamped Inductive Switching Test Circuit & Waveforms



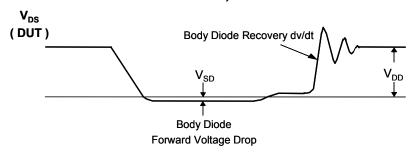
Peak Diode Recovery dv/dt Test Circuit & Waveforms





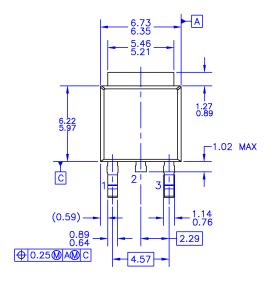


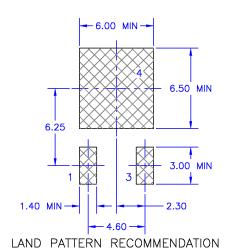
Body Diode Reverse Current

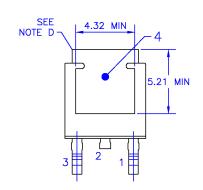


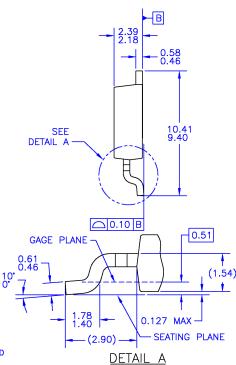
Mechanical Dimensions

D-PAK









(ROTATED -90°) SCALE: 12X

- NOTES: UNLESS OTHERWISE SPECIFIED

 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.

 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONING AND TOLERANCING PER
 ASME Y14.5M-1994.
 D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
 F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
 H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

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Dimensions in Millimeters





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