

March 2013

FDD3N40 / FDU3N40

N-Channel UniFETTM MOSFET 400 V, 2 A, 3.4 Ω

Features

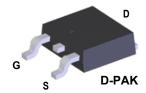
- $R_{DS(on)} = 3.4 \Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = 1 \text{ A}$
- Low Gate Charge (Typ. 4.5 nC)
- Low C_{rss} (Typ. 3.7 pF)
- 100% Avalanche Testes

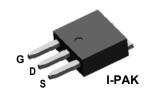
Applications

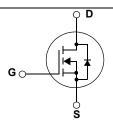
- LED TV
- · Consumer Appliances
- Lighting
- · Uninterruptible Power Supply

Description

UniFETTM MOSFET is Fairchild Semiconductor[®]'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.







Absolute Maximum Ratings

Symbol	Parameter		FDD3N40 / FDU3N40	Unit	
V _{DSS}	Drain-Source Voltag	age		400	V
I _D	Drain Current	- Continuous (T _C = 25°C) - Continuous (T _C = 100°C)		2.0 1.25	A A
I _{DM}	Drain Current	- Pulsed	(Note 1)	8.0	Α
V _{GSS}	Gate-Source voltage		±30	V	
E _{AS}	Single Pulsed Avalanche Energy		(Note 2)	46	mJ
I _{AR}	Avalanche Current		(Note 1)	2	Α
E _{AR}	Repetitive Avalanche Energy		(Note 1)	3	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3		(Note 3)	4.5	V/ns
P_{D}	Power Dissipation	(T _C = 25°C) - Derate above 25°C		30 0.24	W W/°C
T _{J,} T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C	
T _L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		Э,	300	°C

Thermal Characteristics

Symbol	Parameter	FDD3N40 / FDU3N40	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	4.2	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	110	°C/W	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD3N40	FDD3N40TM	D-PAK	380mm	16mm	2500
FDU3N40	FDU3N40TU	I-PAK	-	-	70

Electrical Characteristics $T_C = 25$ °C unless otherwise noted

Symbol	Parameter	Conditions	Min.	Тур.	Max	Unit
Off Charac	teristics					
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	400			V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient $I_D = 250\mu\text{A}$, Referenced to 25°C		-	0.4		V/°C
I _{DSS}	Zero Gate Voltage Drain Current $V_{DS} = 400V, V_{GS} = 0V$ $V_{DS} = 320V, T_{C} = 125^{\circ}C$				1 10	μ Α μ Α
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30V, V _{DS} = 0V	1		100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30V, V _{DS} = 0V	-		-100	nA
On Charac	teristics					I.
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3.0		5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10V, I _D = 1A		2.8	3.4	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 40V, I _D = 1A	-	2		S
Dynamic C	haracteristics			I	-11	
C _{iss}	Input Capacitance	V _{DS} = 25V, V _{GS} = 0V,		173	225	pF
C _{oss}	Output Capacitance	f = 1.0MHz	-	30	40	pF
C _{rss}	Reverse Transfer Capacitance		1	3.7	6	pF
Switching	Characteristics				•	
t _{d(on)}	Turn-On Delay Time	V _{DD} = 200V, I _D = 3A		10	30	ns
t _r	Turn-On Rise Time	$R_{G} = 25\Omega$	-	30	70	ns
t _{d(off)}	Turn-Off Delay Time		-	10	30	ns
t _f	Turn-Off Fall Time	(Note 4)	-	25	60	ns
Qg	Total Gate Charge	V _{DS} = 320V, I _D = 3A	-	4.5	6	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10V		1.2		nC
Q _{gd}	Gate-Drain Charge	(Note 4)	-	2		nC
Drain-Sour	ce Diode Characteristics and Maximur	n Ratings				
I _S	Maximum Continuous Drain-Source Diode Forward Current				2	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current				8	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0V, I _S = 2A			1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _S = 3A		210		ns
Q _{rr}	Reverse Recovery Charge	dl _F /dt =100A/μs		0.75		μС

NOTES

^{1.} Repetitive Rating: Pulse width limited by maximum junction temperature

^{2.} L = 20mH, I_{AS} = 2A, V_{DD} = 50V, R_{G} = 25 Ω , Starting T_{J} = 25 $^{\circ}$ C

^{3.} I_{SD} \leq 2A, di/dt \leq 200A/µs, V_{DD} \leq BV_DSS, Starting T_J = 25°C

^{4.} Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

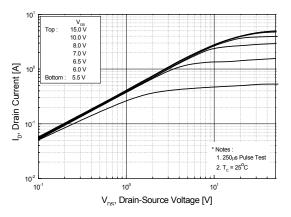


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

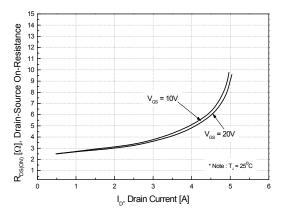


Figure 5. Capacitance Characteristics

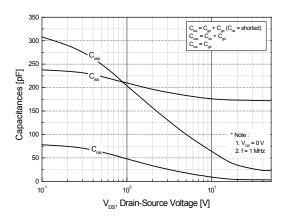


Figure 2. Transfer Characteristics

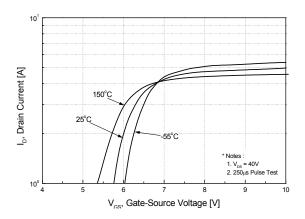


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

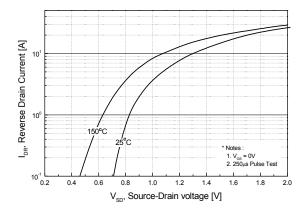
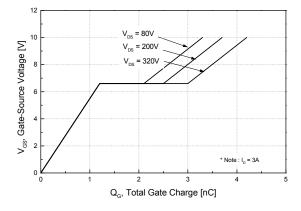


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

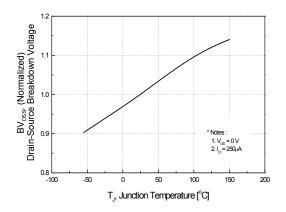


Figure 8. On-Resistance Variation vs. Temperature

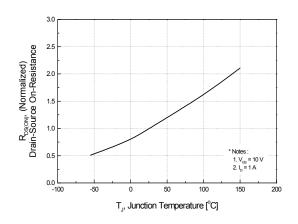


Figure 9. Maximum Safe Operating Area

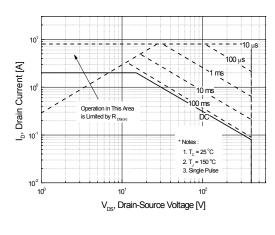


Figure 10. Maximum Drain Current vs. Case Temperature

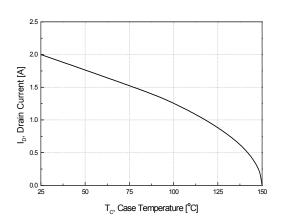
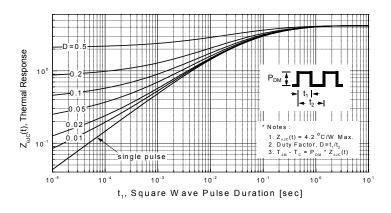
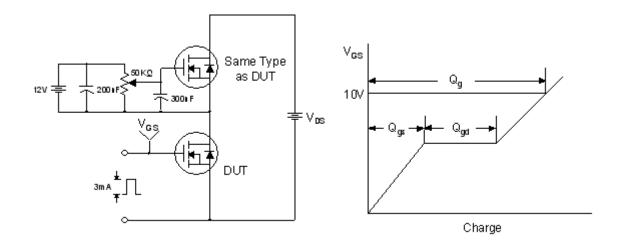


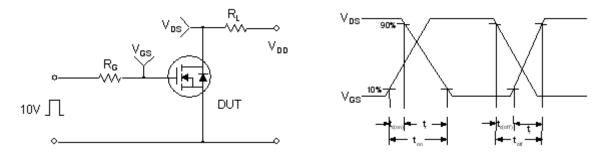
Figure 11. Transient Thermal Response Curve



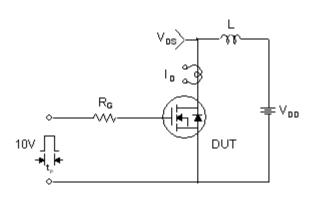
Gate Charge Test Circuit & Waveform

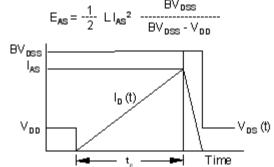


Resistive Switching Test Circuit & Waveforms

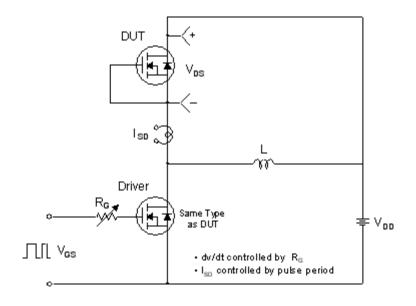


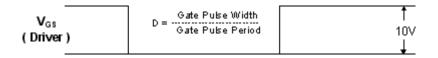
Unclamped Inductive Switching Test Circuit & Waveforms

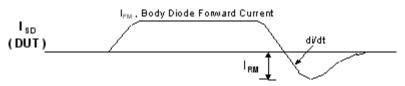




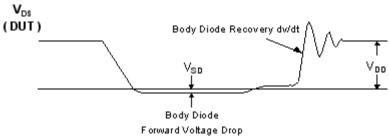
Peak Diode Recovery dv/dt Test Circuit & Waveforms





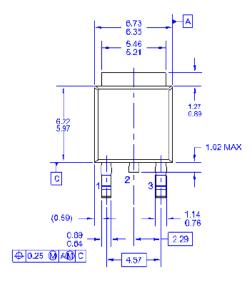


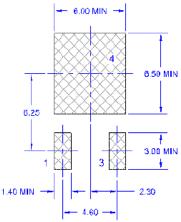
Body Diode Reverse Current



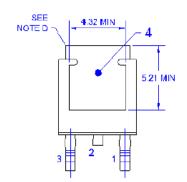
Mechanical Dimensions

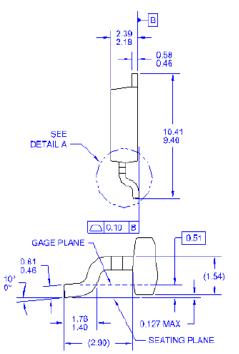
D-PAK





LAND PATTERN RECOMMENDATION





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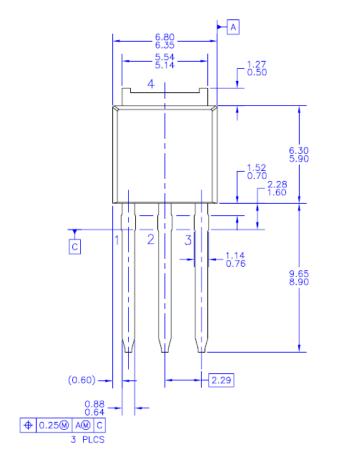
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION, AA.

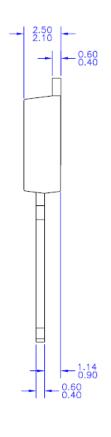
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONING AND FOLERANCING PER ASME YH-3-M-194.
 D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION,
 E) PRESENCE OF TRIMINED CENTER LEAD IS COTIONAL.
 F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, WOLD FLASH AND ITE BAR EX IRUSIONS.
 C) LAND PATTERNIRECOMENDATION 16 BASED ON IPC7951A STD TO220T1003X239-3N,
 H) DRAWING NUMBER AND REVISION: WKT-TO252A03REVB

Dimensions in Millimeters

Mechanical Dimensions

I-PAK







NOTES: UNLESS OTHERWISE SPECIFIED

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 THIS PACKAGE CONFORMS TO JEDEC, TO-251,
 ISSUE C, VARIATION AA, DATED SEP 1988.
 DIMENSIONING AND TOLERANCING PER
 ASME Y14.5M-1994. B)

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