

# FDB024N06

## N-Channel PowerTrench® MOSFET

60 V, 265 A, 2.4 mΩ

### Features

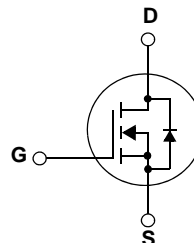
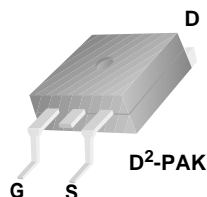
- $R_{DS(on)} = 1.8 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 75 \text{ A}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

### Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

### Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Renewable system



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDB024N06	Unit
$V_{DSS}$	Drain to Source Voltage	60	V
$V_{GSS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	-Continuous ( $T_C = 25^\circ\text{C}$ , Silicon Limited)	265*
		-Continuous ( $T_C = 100^\circ\text{C}$ , Silicon Limited)	190*
		-Continuous ( $T_C = 25^\circ\text{C}$ , Package Limited)	120
$I_{DM}$	Drain Current	- Pulsed (Note 1)	1060
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	2531
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	6.0
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	395
		- Derate above $25^\circ\text{C}$	2.6
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

\*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

### Thermal Characteristics

Symbol	Parameter	FDB024N06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.38	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (1 in <sup>2</sup> pad of 2 oz copper), Max.	40	

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB024N06	FDB024N06	D <sup>2</sup> -PAK	330mm	24mm	800

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	60	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.04	-	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{V}$ , $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 60\text{V}$ , $V_{GS} = 0\text{V}$ , $T_C = 150^\circ\text{C}$	-	-	500	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$ , $I_D = 75\text{A}$	-	1.8	2.4	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}$ , $I_D = 75\text{A}$	-	200	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	11190	14885	pF
$C_{oss}$	Output Capacitance		-	1610	2140	pF
$C_{rss}$	Reverse Transfer Capacitance		-	750	1125	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 48\text{V}$ , $I_D = 75\text{A}$ $V_{GS} = 10\text{V}$ (Note 4)	-	174	226	nC
$Q_{gs}$	Gate to Source Gate Charge		-	54	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	50	-	nC

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{V}$ , $I_D = 75\text{A}$ $V_{GS} = 10\text{V}$ , $R_{GEN} = 25\Omega$ (Note 4)	-	134	278	ns
$t_r$	Turn-On Rise Time		-	324	658	ns
$t_{d(off)}$	Turn-Off Delay Time		-	348	706	ns
$t_f$	Turn-Off Fall Time		-	250	510	ns

### Drain-Source Diode Characteristics

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current	-	-	265	A	
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current	-	-	1060	A	
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 75A	-	-	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 75A	-	69	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> /dt = 100A/μs	-	152	-	nC

#### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $L = 0.9\text{mH}$ ,  $I_{AS} = 75\text{A}$ ,  $V_{DD} = 50\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 75\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

Figure 1. On-Region Characteristics

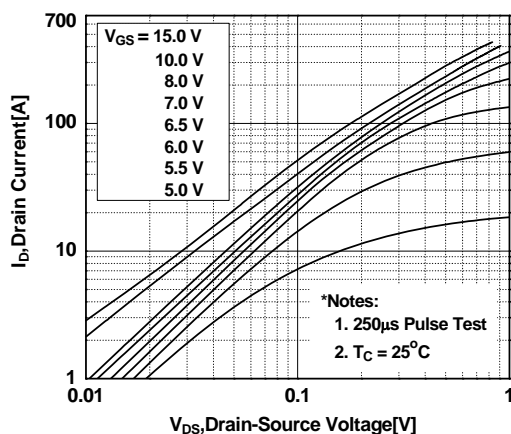


Figure 2. Transfer Characteristics

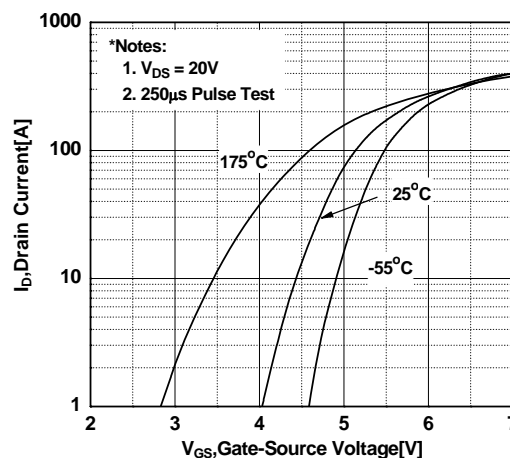


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

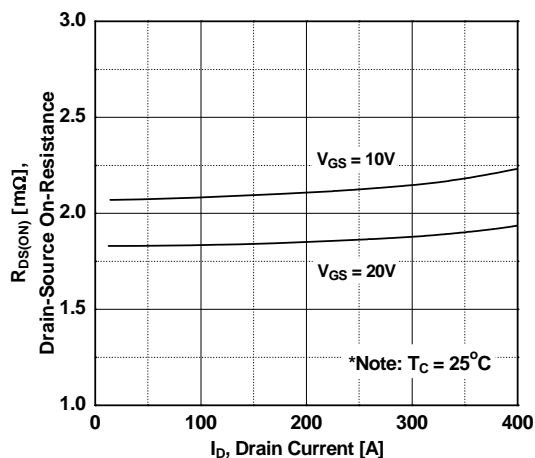


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

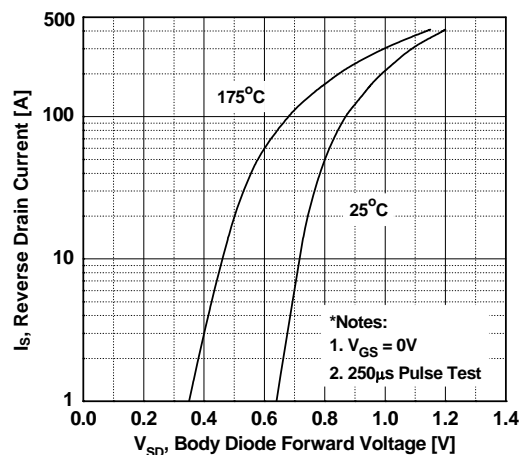


Figure 5. Capacitance Characteristics

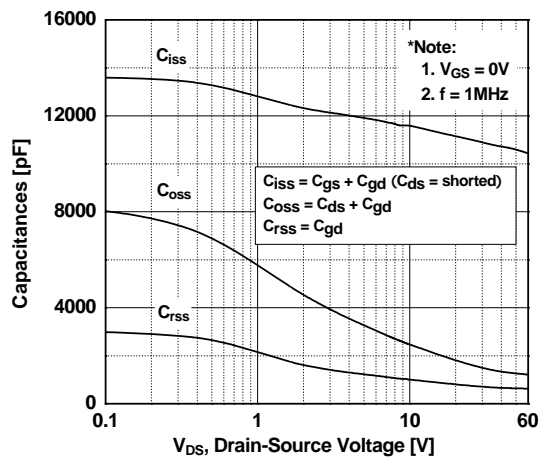
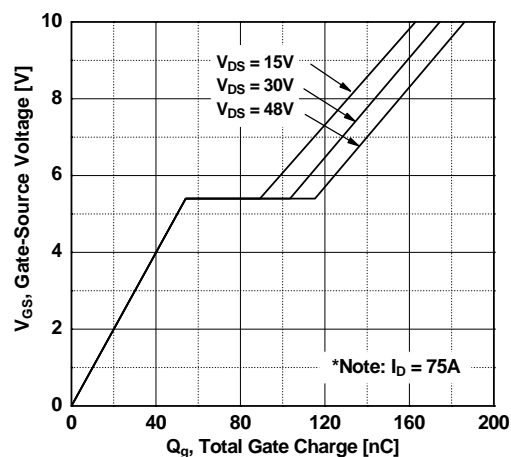
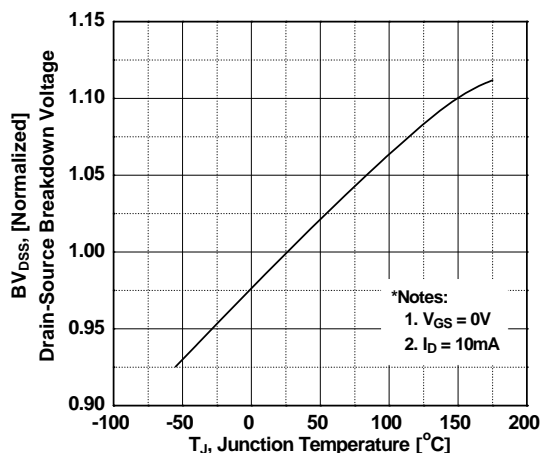


Figure 6. Gate Charge Characteristics

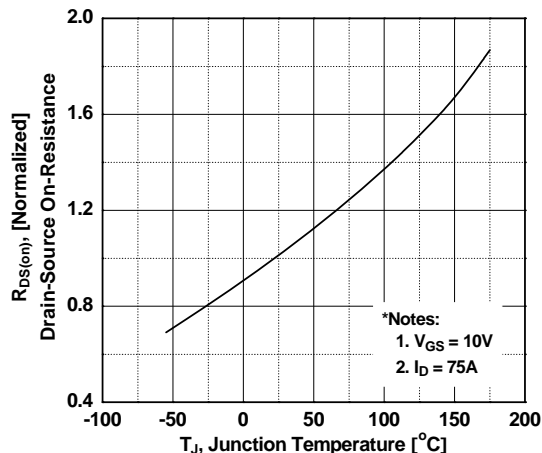


## Typical Performance Characteristics (Continued)

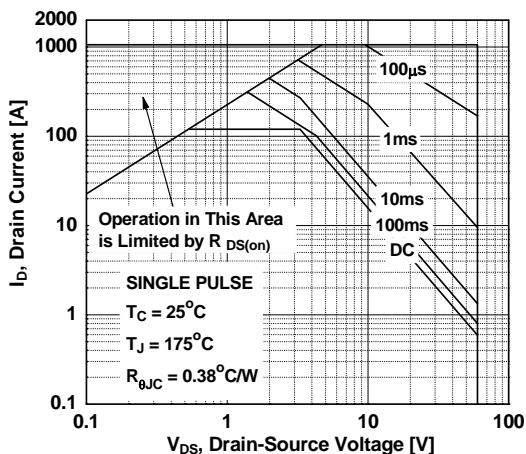
**Figure 7. Breakdown Voltage Variation vs. Temperature**



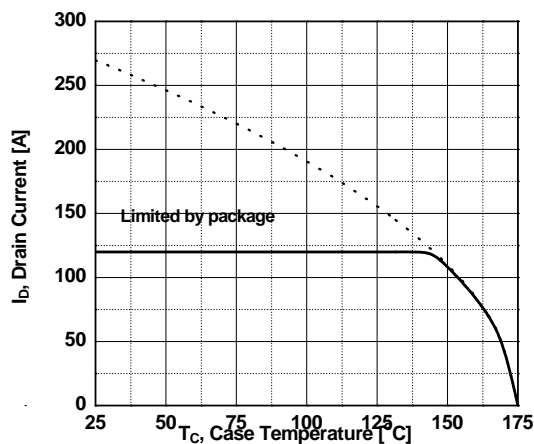
**Figure 8. On-Resistance Variation vs. Temperature**



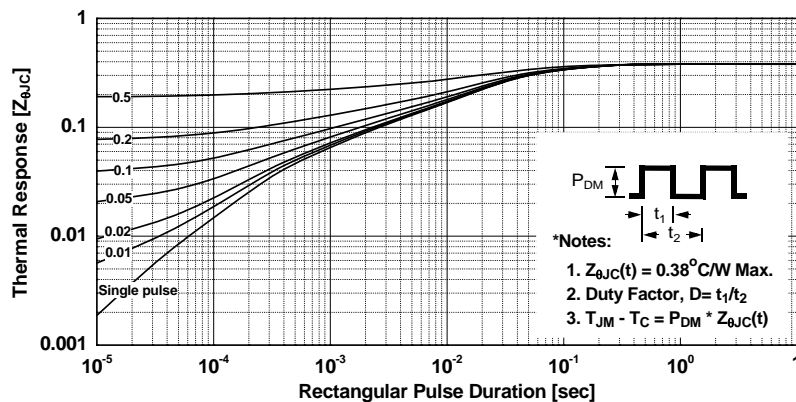
**Figure 9. Maximum Safe Operating Area**



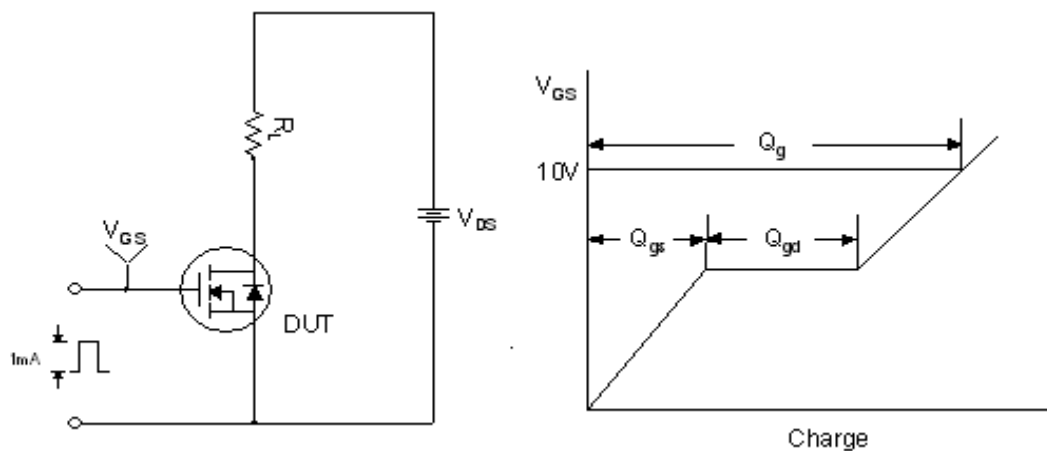
**Figure 10. Maximum Drain Current vs. Case Temperature**



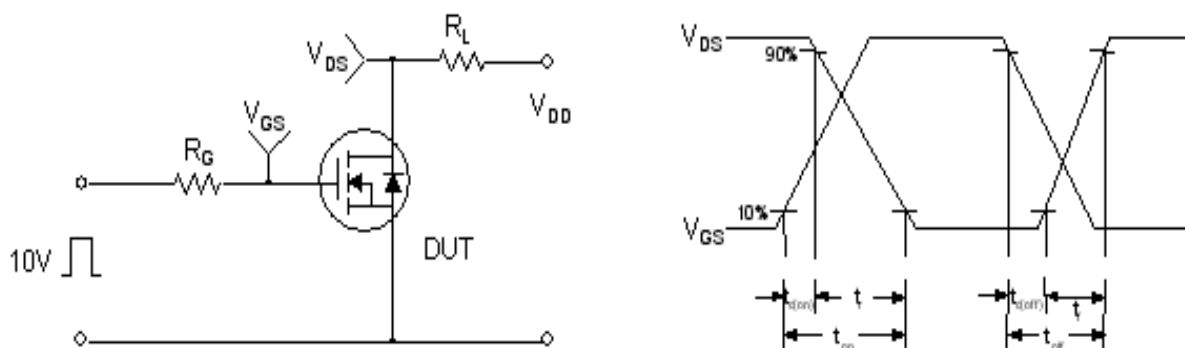
**Figure 11. Transient Thermal Response Curve**



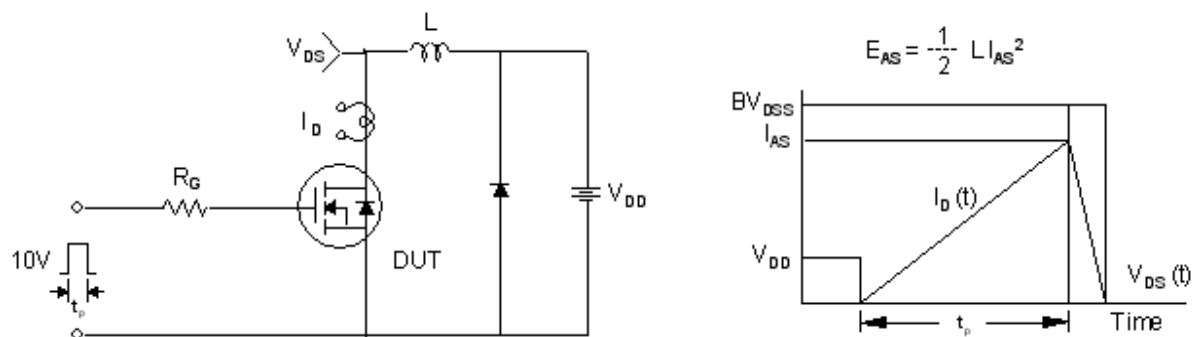
Gate Charge Test Circuit & Waveform



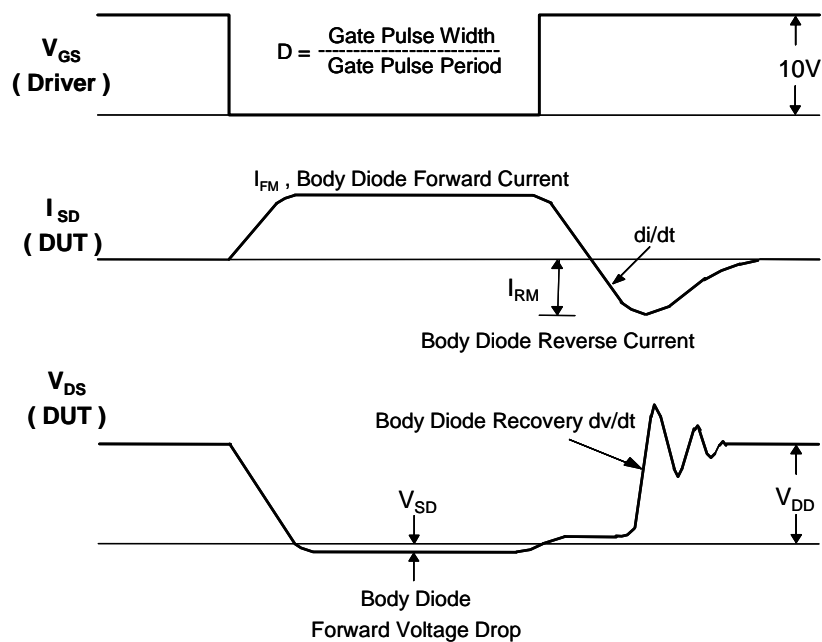
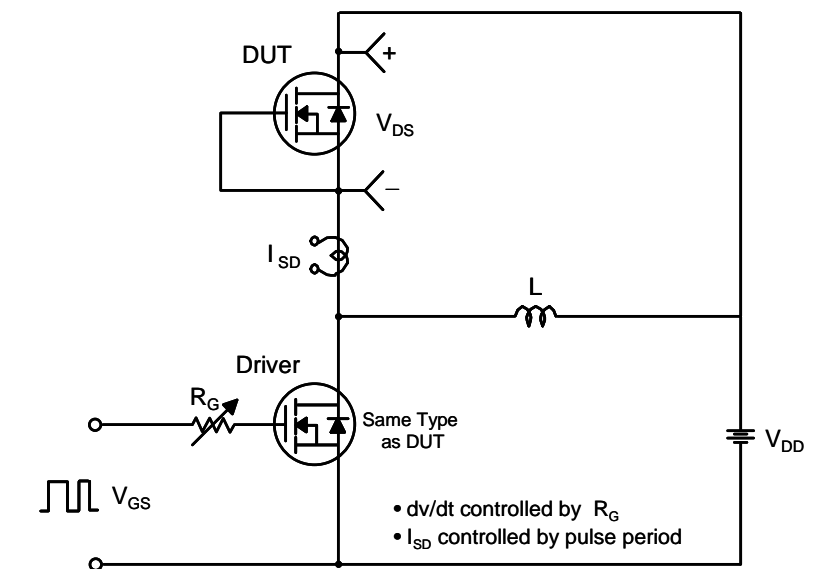
Resistive Switching Test Circuit & Waveforms



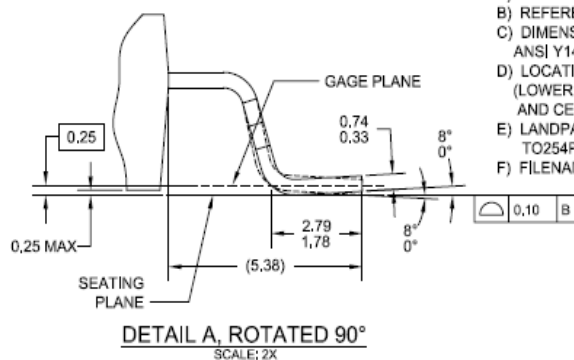
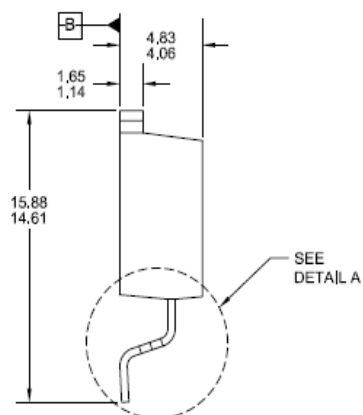
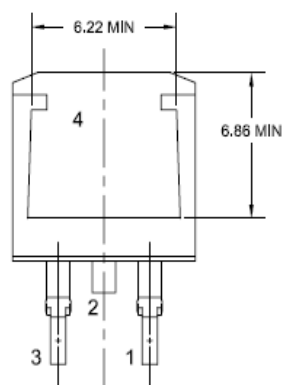
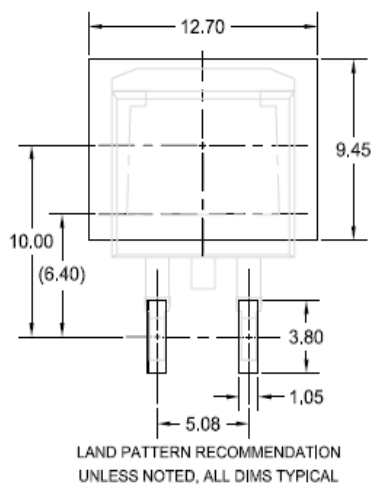
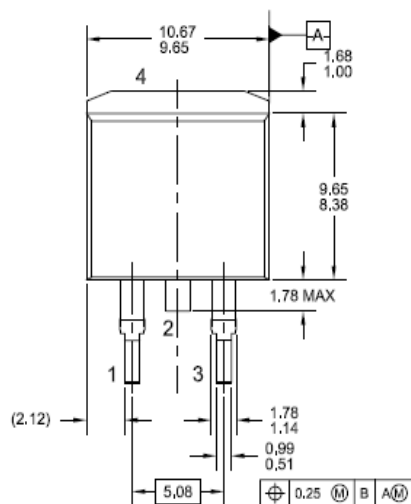
Unclamped Inductive Switching Test Circuit & Waveforms



# Peak Diode Recovery dv/dt Test Circuit & Waveforms



## Mechanical Dimensions

D<sup>2</sup>PAK

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) REFERENCE JEDEC, TO-263, VARIATION AB.
  - C) DIMENSIONING AND TOLERANCING PER  
ANSI Y14.5M - 1994.
  - D) LOCATION OF THE PIN HOLE MAY VARY  
(LOWER LEFT CORNER, LOWER CENTER  
AND CENTER OF THE PACKAGE).
  - E) LANDPATTERN RECOMMENDATION PER IPC  
TO254P1524X482-3N
  - F) FILENAME: TO263A02REV6

### Dimensions in Millimeters

