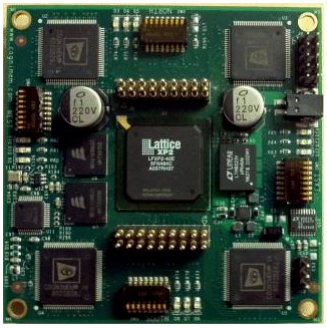
COGNIMEM Technologies, Inc.

CogniBlox-4K

High Performance Pattern Recognition, 3D Stackable Module

CogniBlox is a stackable module allowing the design of versatile, massively parallel pattern recognition architectures for high-performance cognitive computing, sensor fusion, video analytics, and more. It is composed of 4 CM1K chips (4096 neurons), a reconfigurable FPGA, a memory bank, 2 spinal connectors for vertical stacking, and 4 cardinal connectors for communication with other CogniBlox, sensors and devices.



Thanks to the natively hardwired parallel architecture of the CM1K neurons, the CogniBlox boards can be stacked vertically through a "spine" connector, but also connected horizontally to build massively parallel neural networks.

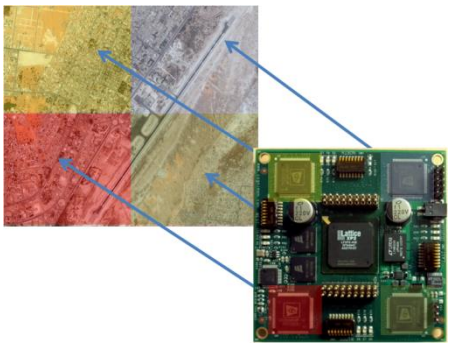
If you need to match one pattern (up to 256 bytes) to 4K, 40K, or more…
CogniBlox will do it in 10 µS per vector consuming 250 mW per 1,000 patterns

CogniBlox for Data Mining

Recognize and classify vectors against large datasets or knowledge bases

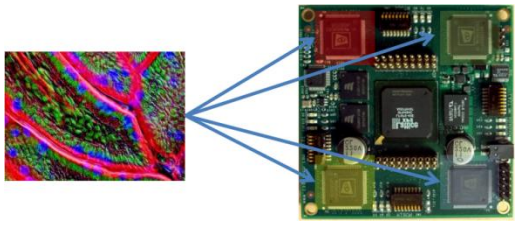
CogniBlox for Video Analytics

Process images N times faster by distributing the recognition to multiple CM1K chips



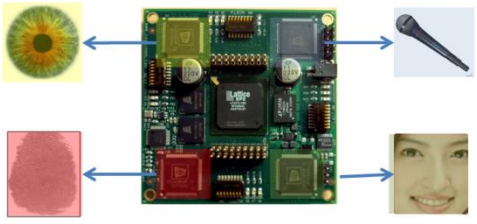
CogniBlox for Complex Recognition

Build robust diagnostics using multiple recognition engine and hypothesis generation

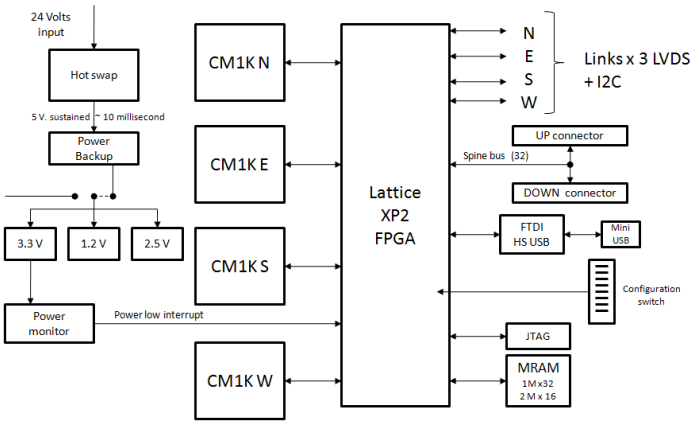


CogniBlox for Sensor Fusion

Multiple sensor inputs (video, sound, accelerometer) for composite recognition



Specifications



- 4 CM1K chips
- Lattice XP2 FPGA with 40,000 gates
- Programmable through a JTAG connector, USB connector or 2 SPI lines
- 2 Mbytes (2M x16bits) MRAM, 35ns access time
- 2 “spinal” spring-loaded 18-pin connectors for vertical stackability of up to 10 CogniBlox modules
- 4 “cardinal” 8-pin push-in connectors for communication with sensors and other devices including another stack of CogniBlox
- Typical interface can be LVSD, I2C, SPI or other. Switch configuration allows for 3 differential pairs and 2 single-ended wires, or, eight single-ended wires
- USB connector to USB high speed 480 Mbit FTDI chip
- JTAG to program and debug the FPGA
- 24V power supply, Hot swap regulator
- During power up/down sequence, the contents of the neurons are saved to, and restored from, MRAM. The power backup time is generous to allow this automatic procedure (< than 5ms)

The Field Programmable Gate Array (FPGA) of the CogniBlox lets you determine if the four CM1K chips will be grouped into single or multiple neural networks (also referred to as a chain of neurons) and how the input data will be dispatched to, and processed by, these various networks. Multiple recognition engines can be programmed in the FPGA and executed independently or with inter-dependencies based on what they recognize, as well as contextual information such as time, location, etc. The programming of the FPGA can go beyond a single CogniBlox board by establishing control and data buses through the “spinal” and “cardinal” connectors of the board. This allows expanding the chains of neurons to thousands and more.

The common denominator of any configuration is for a given chain of neurons (of any size), the recognition of a vector ALWAYS takes only 10 microseconds

Factory Firmware

The FPGA can be programmed using Lattice’s Diamond software which is available as a download from the Lattice website for both Windows and Linux. Once downloaded and installed, it can be used with either a free license or a subscription license.

The default firmware programmed on the FPGA with factory settings implements a simple Register Transfer Level protocol to access the chain of the four CM1K chips.

Ordering Information

Part Number: 901-1001
Options: FPGA firmware for a variety of recognition engines (inquire)

CogniMem Technologies, Inc.
81 Blue Ravine Road, Suite 240, Folsom, CA 95630
916.358-9483 F 916.358.9485