

TOSHIBA Diode Silicon Epitaxial Planar Type

## HN2D03F

### High-Speed Switching Application

- Small package
- Low forward voltage :  $V_F(2) = 0.94 \text{ V (typ.)}$
- Small total capacitance :  $C_T = 2.5 \text{ pF (typ.)}$

### Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

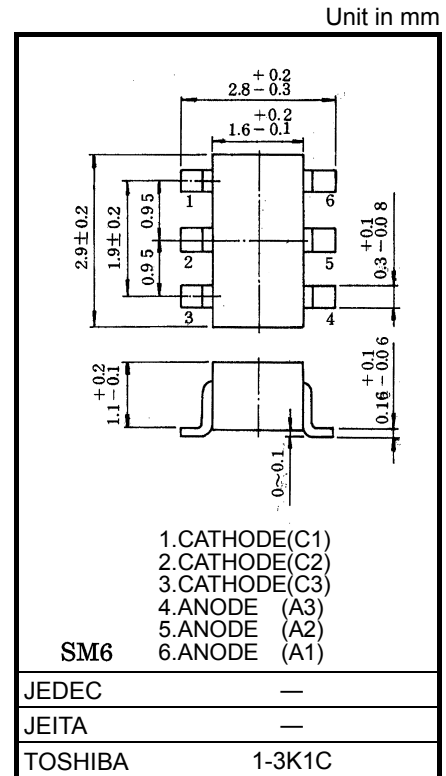
Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse voltage	$V_{RM}$	420	V
Reverse voltage	$V_R$	400	V
Maximum (peak) forward current	$I_{FM}$	300*	mA
Average forward current	$I_O$	100*	mA
Surge current (10ms)	$I_{FSM}$	2*	A
Power dissipation	P	300**	mW
Junction temperature	$T_j$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

\*: Absolute Maximum Ratings per each one of Q1, Q2 or Q3. In case of simultaneous use, the Absolute Maximum Ratings per diode shall be derated to 75%.

\*\*: Total rating

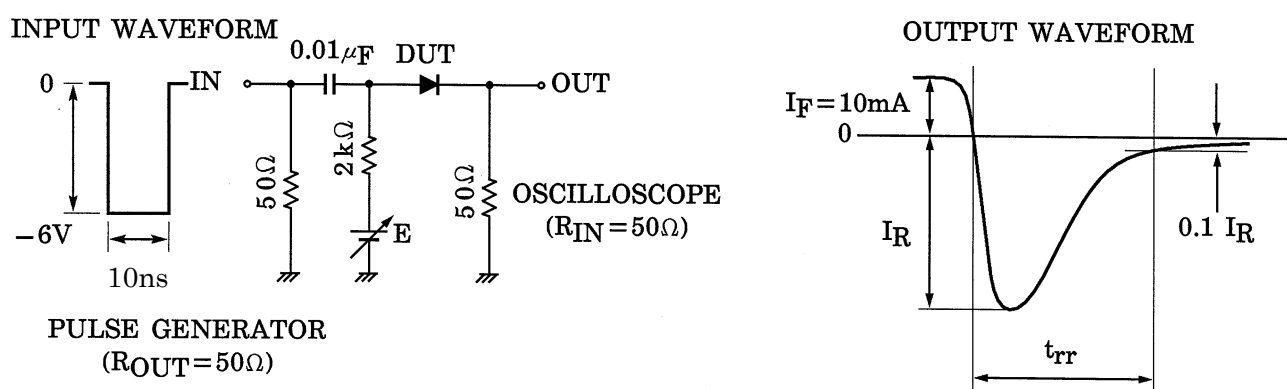


Weight: 15 mg (typ.)

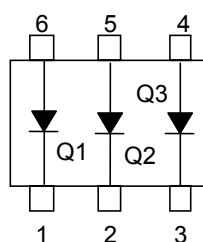
### Electrical Characteristics (Q1, Q2, Q3, Common, $T_a = 25^\circ\text{C}$ )

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_F(1)$	—	$I_F = 10 \text{ mA}$	—	0.8	—	V
	$V_F(2)$	—	$I_F = 100 \text{ mA}$	—	0.94	1.3	
Reverse current	$I_R(1)$	—	$V_R = 300 \text{ V}$	—	—	0.05	$\mu\text{A}$
	$I_R(2)$	—	$V_R = 400 \text{ V}$	—	—	0.1	
Total capacitance	$C_T$	—	$V_R = 0 \text{ V}, f = 1 \text{ MHz}$	—	2.5	—	pF
Reverse recovery time	$t_{rr}$	—	$I_F = 10 \text{ mA}$ (fig.1)	—	0.5	—	$\mu\text{s}$

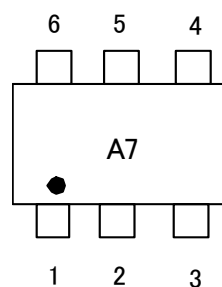
Fig.1 Reverse Recovery Time ( $t_{rr}$ ) Test Circuit

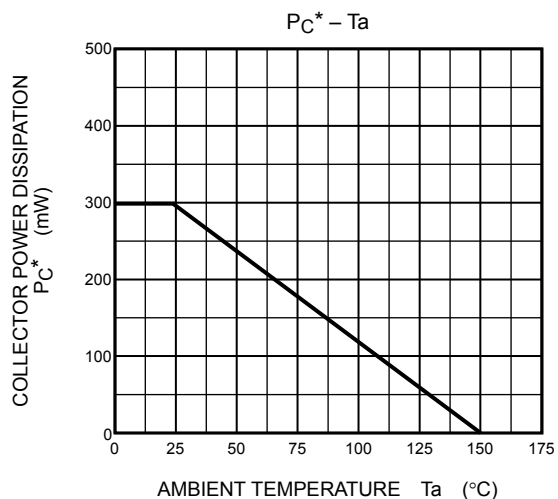
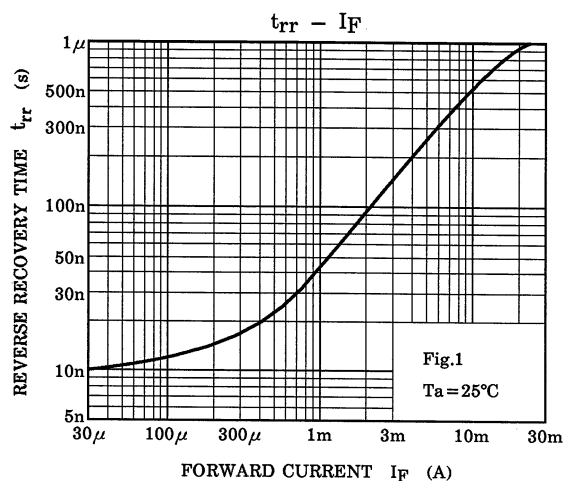
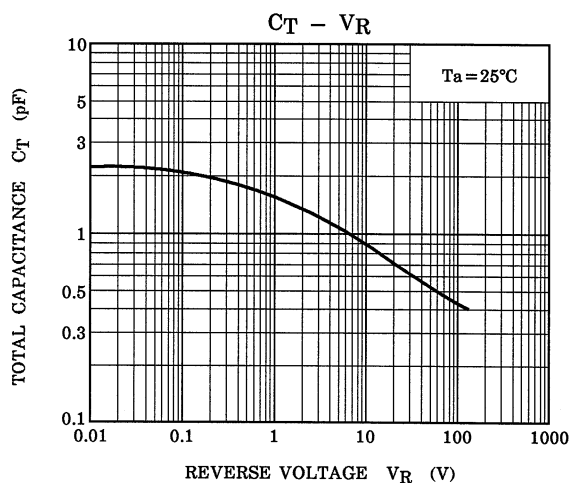
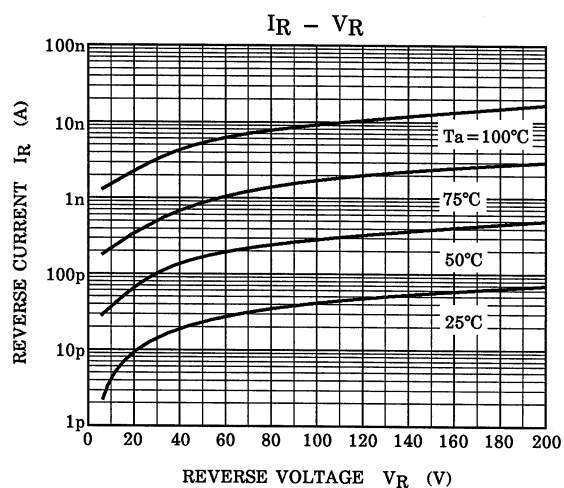
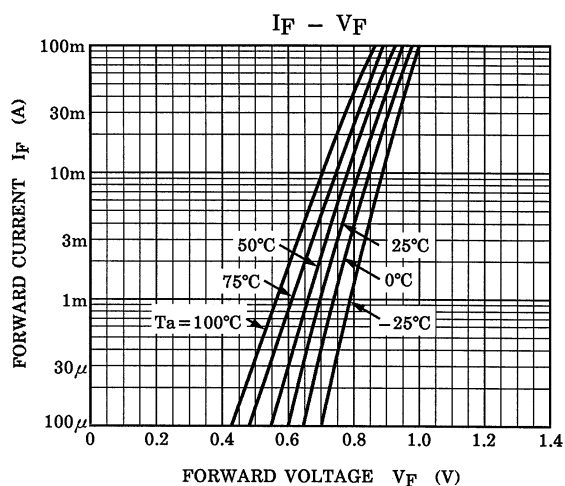


## Pin Assignment (top view)



## Marking





\*Total Rating.

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