Unit: mm

TOSHIBA Diodes for Protecting against ESD Epitaxial Planar Type

# DF3A6.2FU

Product for Use Only as Protection against Electrostatic Discharge (ESD).

- \* This product is for protection against electrostatic discharge (ESD) only and is not intended for any other usage, including without limitation, the constant voltage diode application.
- The mounting of two devices on an ultra-compact package allows the number of parts and the mounting cost to be reduced.

### **Absolute Maximum Ratings (Ta = 25°C)**

Characteristics	Symbol	Rating	Unit
Power dissipation	Р	100	mW
Junction temperature	Tj	125	°C
Storage temperature range	T <sub>stg</sub>	-55~125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

2.1±0.1 1.25±0.1 1.25±0.1 1.25±0.1 1.25±0.1 1.25±0.1 1.25±0.1 1.25±0.1 1.25±0.1

1. CATHODE1

USM 2. CATHODE2 3. ANODE

JEITA — TOSHIBA 1-2P1A

Weight: 0.006 g (typ.)

**JEDEC** 

#### **Electrical Characteristics (Ta = 25°C)**

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Zener voltage	VZ	$I_Z = 5 \text{ mA}$	5.8	6.2	6.6	V
Dynamic impedance	Z <sub>Z</sub>	I <sub>Z</sub> = 5 mA	_	_	30	Ω
Reverse current	I <sub>R</sub>	V <sub>R</sub> = 3 V	_	_	1.0	μА
Terminal capacitance (between Cathode and Anode)	C <sub>T</sub>	V <sub>R</sub> = 0, f = 1 MHz	_	55	_	pF

## **Guaranteed Level of ESD Immunity**

Test Condition	ESD Immunity Level
IEC61000-4-2 (Contact discharge)	± 30 kV

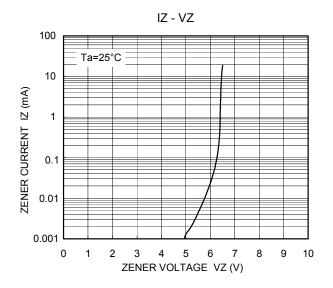
Criterion: No damage to device elements

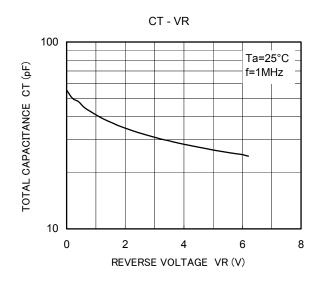
# Marking

# **Equivalent Circuit (top view)**









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