

### STL110N10F7

# N-channel 100 V, 0.005 Ω typ., 21 A, STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet — preliminary data

#### **Features**

Туре	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>TOT</sub>
STL110N10F7	100 V	0.006 Ω (V <sub>GS</sub> = 10 V)	21 A	5 W

- Ultra low on-resistance
- 100% avalanche tested

### **Applications**

Switching applications

### **Description**

This device is an N-channel Power MOSFET developed using the 7<sup>th</sup> generation of STripFET<sup>TM</sup> DeepGATE<sup>TM</sup> technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest  $R_{DS(on)}$  in all packages.

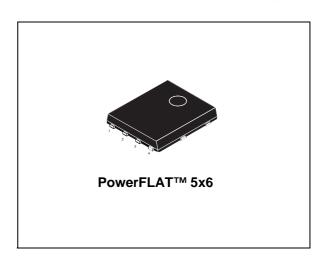


Figure 1. Internal schematic diagram

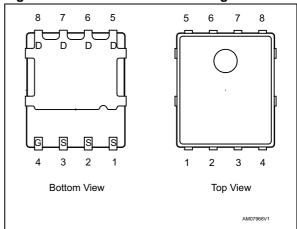


Table 1. Device summary

Order code	Marking	Package	Packaging
STL110N10F7	110N10F7	PowerFLAT™ 5x6	Tape and reel

STL110N10F7 Contents

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STL110N10F7 Electrical ratings

# 1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source voltage	100	V
V <sub>GS</sub>	Gate-source voltage	± 20	V
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 25 °C	110	Α
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 100 °C	77	Α
I <sub>D</sub> <sup>(2)</sup>	Drain current (continuous) at T <sub>C</sub> = 25 °C	21	Α
I <sub>D</sub> <sup>(2)</sup>	Drain current (continuous) at T <sub>C</sub> =100 °C	15	Α
I <sub>DM</sub> <sup>(2)(3)</sup>	Drain current (pulsed)	75	Α
P <sub>TOT</sub> <sup>(1)</sup>	Total dissipation at T <sub>pcb</sub> = 25 °C	5	W
T <sub>J</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	-55 to 175	°C

<sup>1.</sup> This value is rated according to  $R_{\mbox{\scriptsize thj-c.}}$ 

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case	1.13	°C/W
R <sub>thj-pcb</sub> (1)	Thermal resistance junction-pcb	31	°C/W

<sup>1.</sup> When mounted on FR-4 board of 1inch $^2$ , 2oz Cu, t < 10 sec

<sup>2.</sup> This value is rated according to  $R_{thj\text{-pcb.}}$ 

<sup>3.</sup> Pulse width limited by safe operating area.

Electrical characteristics STL110N10F7

# 2 Electrical characteristics

( $T_{CASE}$ =25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage (V <sub>GS</sub> = 0)	I <sub>D</sub> = 250 μA	100			٧
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 100 V V <sub>DS</sub> = 100 V; T <sub>C</sub> =125 °C			1 100	μ <b>Α</b> μ <b>Α</b>
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±20 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2		4	V
R <sub>DS(on)</sub>	Static drain-source on- resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10.5 A		0.005	0.006	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50 \text{ V, f=1 MHz,} $ $V_{GS} = 0$	-	5500 950 30	-	pF pF pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	$V_{DD}$ = 50 V, $I_{D}$ = 21 A $V_{GS}$ =10 V Figure 3	-	60 TBD TBD	1	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> =50 V, I <sub>D</sub> = 10.5 A,		TBD		ns
t <sub>r</sub>	Rise time	$R_{G}$ =4.7 $\Omega$ , $V_{GS}$ = 10 V	_	TBD	_	ns
t <sub>d(off)</sub>	Turn-off delay time	Figure 2		TBD		ns
t <sub>f</sub>	Fall time	r igure z		TBD		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$I_{SD}$	Source-drain current		-		21	Α
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)		-		84	Α
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	I <sub>SD</sub> = 21 A, V <sub>GS</sub> =0	-		TBD	V
t <sub>rr</sub>	Reverse recovery time	I <sub>SD</sub> = 21 A,		TBD		ns
$Q_{rr}$	Reverse recovery charge	di/dt = 80 A/μs,	-	TBD		nC
$I_{RRM}$	Reverse recovery current	V <sub>DD</sub> =80 V, T <sub>j</sub> =150 °C		TBD		Α

<sup>1.</sup> Pulse width limited by safe operating area

<sup>2.</sup> Pulsed: pulse duration=300 $\mu$ s, duty cycle 1.5%

Test circuits STL110N10F7

### 3 Test circuits

Figure 2. Switching times test circuit for resistive load

Figure 3. Gate charge test circuit

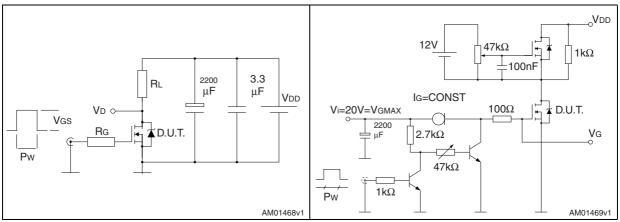


Figure 4. Test circuit for inductive load switching and diode recovery times

Figure 5. Unclamped inductive load test circuit

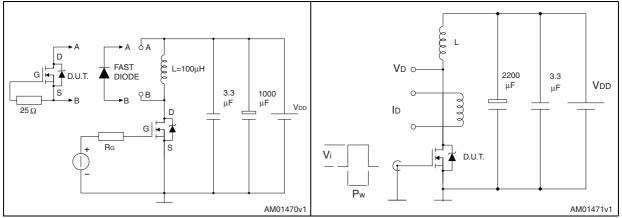
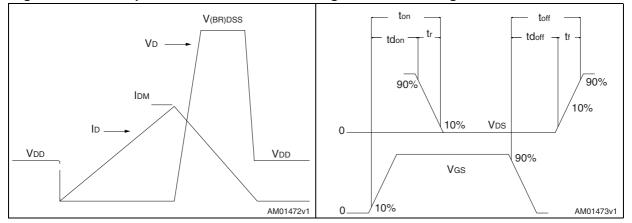


Figure 6. Unclamped inductive waveform

Figure 7. Switching time waveform



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 5x6 type S-C mechanical data

D:		mm	
Dim.	Min.	Тур.	Max.
А	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
е		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35

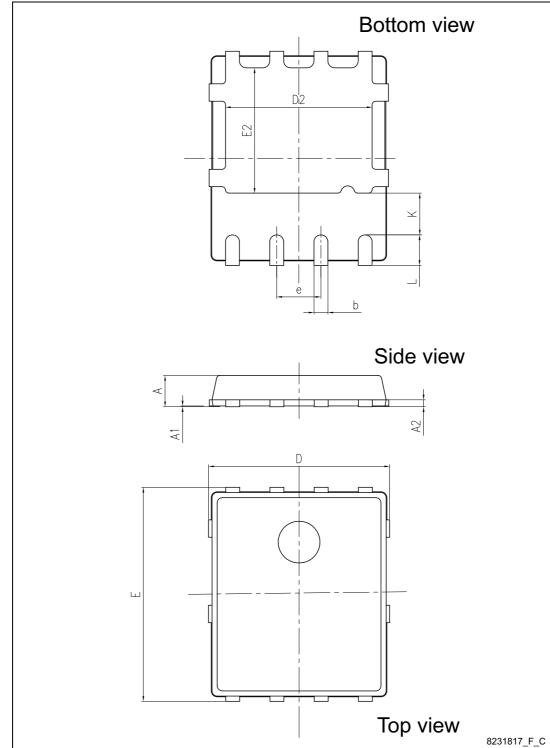


Figure 8. PowerFLAT™ 5x6 type S-C mechanical data

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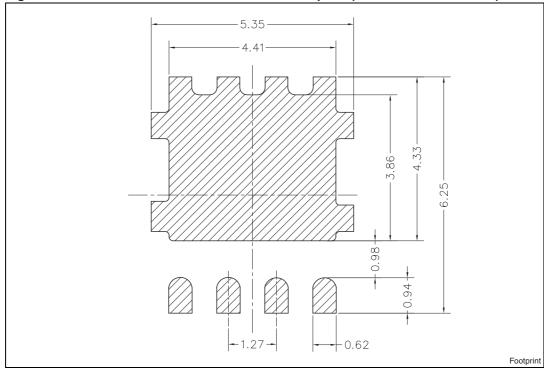


Figure 9. PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)

Revision history STL110N10F7

# 5 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Dec-2012	1	First release.

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